CONSIDERATIONS ON THE DESIGN OF TRANSCEIVERS FOR WIRELESS OPTICAL LANS

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Abstract

This paper discusses practical issues and results on the implementation of low-cost transceivers for several wireless optical LANs, covering most physical layer elements.

Target optical LANs under consideration have bit-rates varying between 1Mbps and 25Mbps, and input photodiode capacitance may vary between 10pF and 50pF. PPM modulation, either in a 4-PPM or 16-PPM format, is typically used in the physical layer.

Differential front-end topologies are presented, both in discrete and integrated (CMOS) implementations, targeting different LANs. Strategies for bandwidth improvement, interference reduction and dynamic range improvement have been used in some of these topologies. These strategies lead to a switched-gain transceiver with a transimpedance gain*bandwidth of 25THzΩ, achieved with a 10pF capacitance photodiode in the input. Both non-sectored and sectored transceivers are discussed. The increased complexity brought about by sectored receivers will be made clear as the design of a signal-to-noise ratio estimator and constraints on power consumption of the basic front-end design are discussed.

Considerations on practical usage of MAP detection confronted with adaptive threshold detection are further presented. Clock recovery issues are also mentioned.

Final comments on practical issues and evolution of these low-cost systems are presented.

Keywords:

Wireless LANs, InfraRed Systems, Transceivers, Sectored Receivers, Front-Ends, PPM Detection, Clock Recovery, Low-Cost Systems

1 Introduction

Wireless optical communication systems have gone through considerable developments in recent years, as optical components have suffered important technologic advances and substantial price decreases. Thus data communications are increasingly using wireless optical systems at higher speeds. These systems are being used as an alternative to cabled media, mainly due to their simpler deployment and reconfiguration.

In wireless optical networks, major hindrance results from the low signal amplitudes that have to be used due to cost, health and power consumption constraints. Furthermore, the non-uniform nature of both the ambient noise and the signal power distribution puts increased demands on the dynamic range of the transceiver circuits. These wireless optical constrains call for new solutions, namely: (i) networks optimized for the usage of low cost optical components, (ii) development of systems with very flexible characteristics of gain and dynamic range, (iii) noise reduction techniques, and (iv) selection of optimal detector structures.

We have been developing wireless optical Local Area Network (LAN) systems pursuing these objectives. This paper documents some of our efforts in implementing practical low-cost transceivers. Section 2 presents the target WLAN (Wireless LAN) characteristics we used as reference for our work and the system reference block we have followed over the last years. Section 3 discusses the emitter radiation diagram used. Section 4 discusses front-ends that we have implemented, both in discrete and integrated format. Section 5 presents some considerations on clock recovery and on the critical issue of code detection. Section 6 discusses recent efforts on the implementation of sectored receivers. Section 7 summarizes some practical constraints related with the implementation of WLAN transceivers. Our conclusions, mostly as directions for future work, are presented in section 8.

Most of the circuit blocks reported here have already been tested in various generations of working prototypes (with varying specifications). More recent work is currently under field test to assess its performance. Nevertheless, our current activity is focused on the cooperative usage of these different circuit blocks to provide efficient WLAN communications.

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2 The Target LAN(s)

2.1 Network Specifications

Our prototype WLANs have gone through several sets of specifications. Nevertheless we have always centred our efforts on diffuse (or multi-spot diffuse) packet networks. Packet format and size have been modified as successive networks were refined. Cell size, transmitted power and bit-rate were the most unstable parameters, as technology developments allowed for better and improved performance networks.

The work here described was developed for systems with varying specifications, with bit-rates between 1Mpbs and 25Mbps and with modulation methods raging from Differential Manchester to Pulse Position Modulation (PPM), both 4-PPM and 16-PPM. Typical cells sizes are around 7×5×3m, and could face either natural or artificial illumination.

The target photodiode (PD) for these systems presents a relatively large junction capacitance, between 8pF and 15pF, depending on the operating point. For increased sensitivity, photodiodes arrays have to be used. Typical systems used 5 to 15 PDs. These PDs have been selected in function of its low cost for a not extremely large junction capacitance. Although diffuse configurations were targeted, the non-uniformity in power distributions created by obstacles still demands for high dynamic range front-ends, able to operate with these low cost PDs.

The packet format used has a structure as follows [ITCOM99a]:

Sync	SFD	DR	DCLA	Length	CRC	MPDU
57-73 slots	*4 slots*	*3 slots*	*32 slots*	*16 bits*	*16 bits*	*Variable*

where Sync is the Synchronisation field, SFD the Start Frame Delimiter, DR the Data Rate (signalises the modulation/bit-rate being transmitted), DCLA is the DC Level Adjustment field (required due to the possibly different DC levels of the packet header and the rest of the packet, which being capacitively couple would cause DC level changes downstream), Length is the packet length, CRC (Cyclic Redundancy Check) the header check, and MPDU is the data packet, with variable size (but limited at most to 4500 bytes).

The specific packet format has been changed over the years. For instance, an EFD (End of Frame Delimiter) has also been used, the CRC field has not been always present, the maximum packet size has been changed, etc... These variations are, however, of minor consequence to the design of the electronic circuits supporting the WLAN, and we will neglect them across this paper.

2.2 Reference System

The basic network assumptions have been stable enough over the last few years for a basic structure to emerge from our implementations, regardless of varying network specifications and improvements in transducer technology. Our reference system is depicted in Fig. 1. It comprises an emitter, a receiver (eventually sectored), and the optical noisy indoor communication channel (a room with artificial lighting).

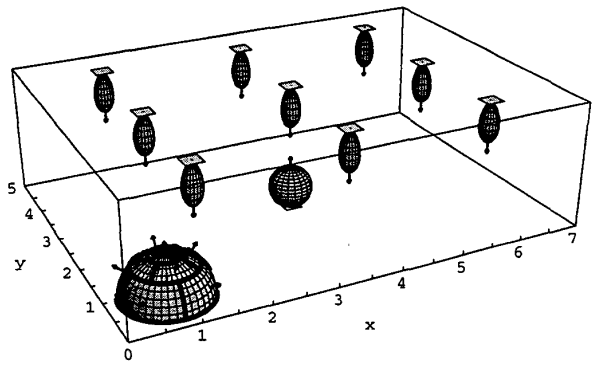

Fig. 1 - Test room (with artificial light sources) and transceiver model (sectored receiver represented).

In this reference model, both the network protocol and the network transceiver are designed in order to achieve an efficient communication system with low complexity and low cost. As technology evolves, the point of equilibrium of these factors has changed, increasing the total bandwidth and the cell size while simultaneously reducing power consumption and transceiver size.

Fig. 2 presents the generic system block diagram of these transceivers. In all these blocks dynamic power control can be applied, to decrease power consumption.

The following functions can be identified in the different communication entities:

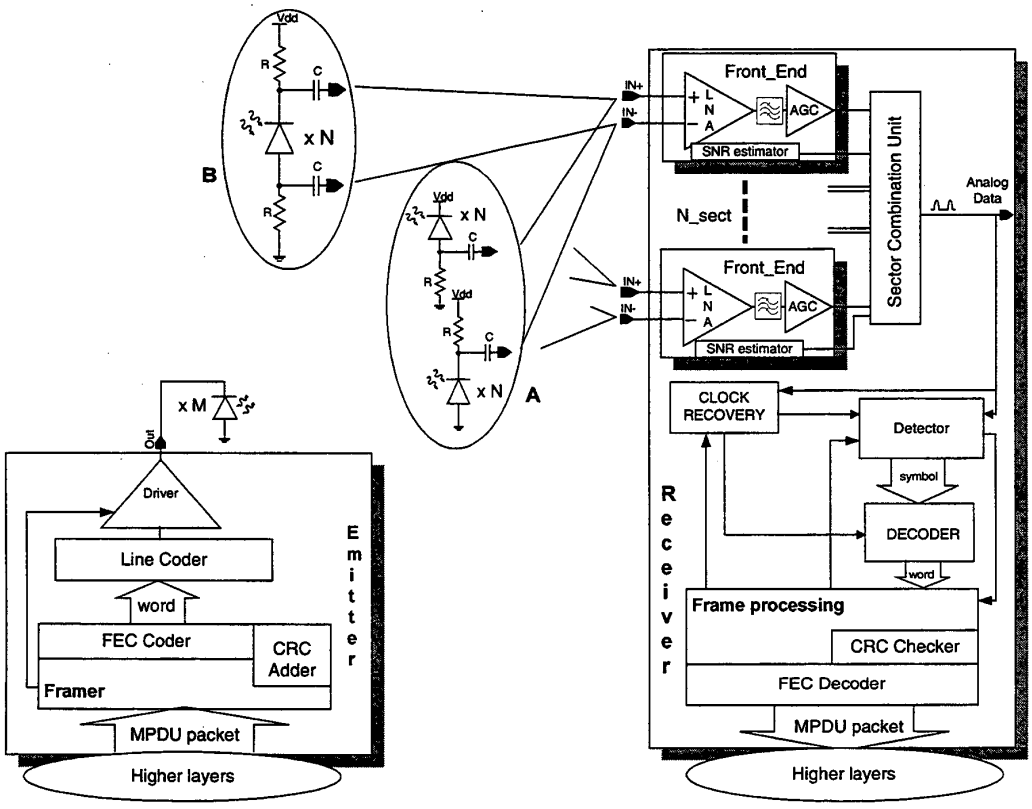

Fig. 2 - System block diagram.

Emitter:

a) Line driver — the unit responsible for the drive of the LED array.
b) Line coding/scrambling — the application of a proper line code chosen for performance, simplicity or power efficiency reasons; additionally the usage of a scrambler may be useful for certain non-limited run-length codes. We have used Non-Return to Zero (NRZ) with scrambling, Differential Manchester and PPM (both 4-PPM and 16-PPM) in different systems.
c) FEC coding — the usage of Forward Error Correction (FEC) methods can improve the Bit Error Rate (BER) performance.
d) Framing operations — the usage of a packet-based network requires this block. It includes the wrap-up of the data with a preamble (and eventually a trailer), and the introduction of an (eventual) CRC field. The packet format has evolved over the years, as discussed in the previous section. We currently adhere to an IEEE 802.11-like format, as shown in section 2.1.
e) System interface — the interface with the remainder of the sender system.

Receiver:

a) Front-end processing — this includes low-noise amplification, the usual current-to-voltage conversion, and an Automatic Gain Control (AGC) amplifier, in order to achieve an analogue signal able to be post-processed. It may also include a filter, in order to improve noise performance. For high performance integrated front-ends, the filter is usually included in the front-end design.
b) SNR estimation — estimates the optical signal-to-noise ratio at the front-end (FE). This estimation may be used either to control the AGC amplifier of the front-end for further combination (in Maximal-Ratio Receivers) or as a signal for the diversity combination unit (in Best Sector Receivers).

c) Sector combination — if several front-ends are used, some form of combination/selection of the different signals is required. This unit will output the "received" analogue signal. If Signal to Noise Ratio (SNR)-dependent AGCs are used in the FE, then some of the functions assigned to this unit may be performed there first. We have used both diversity and non-diversity configurations in our systems.
d) Clock recovery — a clock signal is required for digital detection. This clock is recovered from the analogue received signal. A fast lock on input signal is required.
e) Word detection — the detection of the received word. Three main strategies can be applied: threshold-decision, adaptive threshold decision, and Maximum A-Posteriori (MAP) detection. We tried all three strategies.
f) Word decoding/descrambling - upon detection of the line code word, word decoding will reconstruct the original information.
g) Un-framing — all "packet" information has to be treated (this may imply control signals for the rest of the receiver units), and eventually a CRC check may have to be performed.
h) FEC decoding — if FEC is used in the link, then a proper decoder has to be used (such as a Viterbi decoder).
i) System interface — the interface with the remainder of the receiving system.

In the emitter, the MPDU goes through a unit responsible for frame formatting through the introduction of the several frame fields, including (possible) CRC generation. FEC coding may be applied afterwards, to improve transmission BER. This information is thus applied to a line coder, which converts information words to code symbols, and will finally attack an LED driver.

In the receiver, (possibly several) front-end(s) are driven by low-cost photodiodes. Two types of input connections are possible (see Fig. 2): case A, where a different set of PDs is connected to each FE input; and case B, where the PDs are connected between both FE inputs. If diversity configurations are used, the signals received by these front-ends are delivered to a Selector Combination Unit. This unit will use some sort of SNR estimate per input signal to merge the individual outputs into a single analogue received signal [ITCOM99a, Valadas94]. This signal is delivered to a clock recovery unit (for clock recovery and line code alignment) and to a word detector. A decoder handles this signal, converting the received symbols in information words. Finally this information is passed to the frame-processing unit. This unit performs packet processing (removing all extra fields from the received packet, plus eventual CRC checking and FEC decoding) to finally achieve the transmitted information packet.

This structure allows some possible variants, as has been apparent from the above description. Network complexity (and performance) has increased with successive refinements of these layers. For instance, FEC can be used, but is not essential in the communication system, as some of our preliminary systems showed. Similarly, the usage of diversity receivers (requiring a SNR estimation and a selection combining unit) is not compulsory for achieving a working network, although it improves its efficiency in presence of non-uniform noise.

Therefore, the following sections detailing some of the blocks we have designed should not be interpreted as describing **a single** system. We aim to report on the practical feasibility and relative advantages of several transceiver sub-blocks, if used in a single system. We have used (and some times abandoned, in different degrees of its development) most of these structures and our current aim is the selection of the proper blocks for the implementation of a simple, compact and cost-efficient WLAN.

For simplicity, we will omit the "system interface" units in the next sections. However, these may be quite complex, especially if the network uses a Digital Pulse Interval Modulation (DPIM) based system [Ghassemlooy98]. In DPIM, the relationship between the effective packet size and the number of bits transmitted is not constant, but data-dependent. As a consequence, frequency adaptation (both in the emitter and in the receiver) is required. Therefore, the system requires buffering and off-line processing, instead of real-time, clock dependent processing based in the clock relationships, as shown in [Aguiar98]. By its simpler nature, we will also omit most of the digital design aspects. The bit-rates aimed in our prototypes do not pose special digital design problems - although intelligent power control has to be used throughout the digital sub-blocks.

3 Emitter : Diffuse Configuration

We have designed and used for several years a diffuse radiation configuration [Tavares95a]. This configuration was optimised in order to equalise the optical power distribution over the communication cell. In such optimisation procedure, a square room with 9×9m and with a ceiling height of 3m was considered. The emitter radiation pattern was optimised with a simulation package reported in [Lomba94]. Simulations considered off-the-shelf low-cost LEDs and assumed up to sixteen LEDs. The simulations considered only the first order reflections on the room ceiling, which is a worst-case simulation. In real environments higher order reflections will increase the collected power, despite they may also decrease the power distribution uniformity.

The end result of the optimisation procedure is presented in Fig. 3. With the configuration obtained through the optimisation simulation package, the minimum value of the irradiance within the communication cell was about 57% of

the maximum value achieved. Note that the presence of obstacles may change this power distribution substantially, and thus high dynamic range devices are still required even for this system.

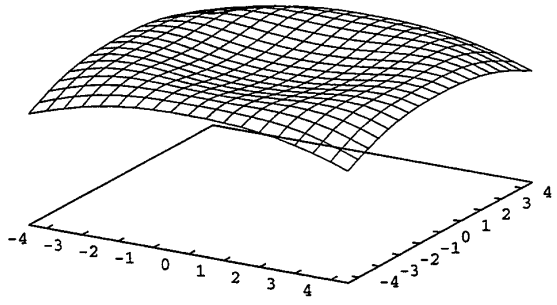

Fig. 3 - Power distribution on reference room

The experimental results achieved with this configuration have been quite satisfactory, once we used pre-equalisation techniques in the LED driver. It has proven to produce a remarkable diffuse radiation pattern in the rooms we usually use for test, even with the presence of normal obstacles (furniture, laboratory equipment, etc...)

4 Front-Ends

A critical element for WLAN performance is the input stage of the Low-Noise Amplifier. For analysing this input stage, a current source with a capacitor in parallel can be used to model the input photodiode. Bias elements will then appear in parallel with the PD model. These elements impact system performance, as they create a band-pass filter at the input of the system.

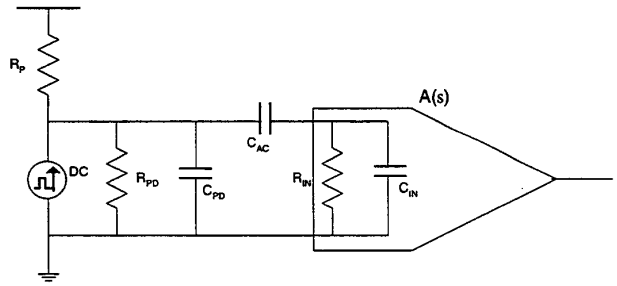

Fig. 4 - Simplified front-end input model.

Fig. 4 shows a typical model for the front-end input, including a simple Low-noise Amplifier (LNA) input model. In this figure, R_P is the bias resistor for the PD, R_{PD} and C_{PD} are the PD resistance and capacitance, R_{IN} and C_{IN} are the front-end input resistance and capacitance (the FE input impedance can be modelled in first approximation by these elements), and C_{acop} is the coupling capacitance. R_P has to be chosen according to the PD being used and the operating point desired.

The transfer function of this system, in terms of input current to the FE, is given by Eq. 1:

$$\frac{V_{out}}{I_{In}} = \frac{C_{AC}}{C_T} \frac{s}{s^2 + s\left(\frac{C_{AC}+C_{PD}}{C_T R_{IN}} + \frac{C_{acop}+C_{IN}}{C_T R_{//}}\right) + \frac{1}{C_T R_{IN} R_{//}}} A_V(s) \qquad (1)$$

where $A_V(s)$ is the amplifier voltage gain, C_T is $C_{AC}C_{IN}+C_{IN}C_{PD}+C_{AC}C_{PD}$ and R// equals the parallel of R_P and R_{PD}. If we neglect the amplifier contribution to the transfer function, the input passive network presents a transfer function with two poles and one zero at the origin: a band-pass filter function, with a low- (f_L) and high- (f_H) cut-off frequencies. Note that the low cut-off frequency may be important for flicker noise reduction.

This expression can be used [Aguiar98b] to discuss the relative merits of the three key types of front-end topologies: high-impedance, low-impedance and transimpedance. Transimpedance amplifiers present the best design trade-off for WLANs, and are thus the most commonly used. Note that even for a transimpedance amplifier, Eq. 1 predicts the

existence of a high-frequency pole dependent on the input capacitance. This is usually the dominant pole in WLANs front-ends.

4.1 Discrete Implementation

A simplified block diagram of a discrete IR receiver is shown in Fig. 5, using the configuration B (Fig. 2). An infrared optical receiver must have the highest possible sensitivity to reduce the required optical power (or in alternative to increase cell size). However, high sensitivity front-ends are very susceptible to Electromagnetic Interference (EMI), which makes the design of the receiver quite a complex issue. To overcome the induced EMI, the receiver was designed with two complementary transimpedance amplifiers. This approach has two effective objectives: i) to use differential circuits in order to reduce the penalty induced by EMI; ii) to increase receiver bandwidth, for the same collected signal, avoiding equalisation. To improve EMI immunity, the layout of the printed circuit board is also carefully designed, with the complementary front-ends similarly implemented.

The IR receiver here referenced [ITCOM99a, ITCOM99b] includes a photodiode array composed by five PIN photodiodes with a global active area of 0.35cm^2. Each photodiode has a junction capacitance of about 12pF. The measured gain of the complementary transimpedance amplifiers was about 154kΩ. The measured bandwidth was about 7MHz, which is large enough for the requirements of a 4Mbps, 4-PPM network. Following each complementary front-end there is a low-pass filter, and these signals were subtracted through a differential amplifier. The measured transimpedance gain of the complete receiver was about 1.2MΩ.

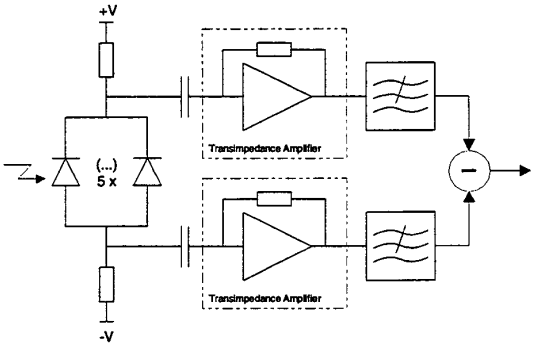

Fig. 5 - Block model of discrete IR front-end.

4.2 Integrated CMOS Front-Ends

We have then developed high-performance monolithic front-ends with two technological constraints: i) target technology should be CMOS, due to its low cost and capabilities of very high integration; and ii) the circuit should be designed to work with these low-cost photodiodes.

These constraints have a direct impact on front-end bandwidth. According to Eq. 1, the input PD capacitance will limit the maximum front-end bandwidth, and CMOS technology places limits on the maximum achievable transconductance gain per device. In practice, both factors imply that a (almost) dominant pole will appear in the circuit, created by the input impedance of the front-end and the parasitic PD capacitance.

We developed several integrated font-ends for baud rates raging from 2Mbps to 50Mbps, assuming both Manchester and 16-PPM modulation (DC levels in these codes are quite different). These front-ends were designed for input photodiodes with junction capacitance ranging from 10pF (for the higher bit-rates) to 100pF. Besides the cut-off frequency imposed by the PD, the intrinsic bandwidth for these front-ends could be controlled externally. Thus we will limit the following discussion to the higher bit-rates, assuming input PDs with junction capacitance of ~10pF. Our design target was once more configuration B (Fig. 2) with the PD placed between both front-end inputs, due to its physical implementation advantages.

High dynamic ranges and low noise were sought for in all designs. These characteristics are required to cope with signal variations (reflection effects, single path illumination or the presence of obstacles can create large signal variations, even when using our "diffuse" configuration) and to optimize cell size. Furthermore signal filtering was done internally in all front-ends.

A single-ended input configuration with a switched gain approach [Cura98] achieved a 10MHz Bandwidth (BW), 48dB[2] dynamic range and 36pA/√Hz noise. This circuit was rapidly evolved into two differential input configurations, in order to avoid electromagnetic interference, but was nevertheless useful for proving the switched gain concept: the large dynamic range possible in WLANs could be handled through a front-end which effectively changed its gain through (internal) discrete steps. This creates a simple structure that can be further optimised if smaller dynamic ranges are possible (achieved through better signal "diffusion", e.g.)

In [Carreiró99], a 56MHz BW, 120kΩ gain differential front-end was implemented. This front-end also implements a switched gain approach, changing the feedback resistors of the LNA to modify the transimpedance gain. The feedback resistor is switched depending on the input signal, in such a way that the system does not reach saturation. Furthermore, the switching system presents hysteresis in order to avoid gain oscillations. As in the discrete case already discussed, two such amplification cells are then connected in a differential configuration, in order to produce a pseudo-differential amplifier. This circuit could potentially achieve large gains, but requires careful compensation along the whole amplification loop.

This circuit was produced in a 5V, 0.8μm, double poly-, n-well CMOS technology. The front-end die size is 1200μm×600μm. Power consumption is 60mW.

In [Vasconcelos99], a "true" differential structure was developed, with low-gain transimpedance blocks as pre-amplifiers, and then post-amplifying the output signal. This structure led to a 400kΩ, 55MHz BW front-end. The input signals can present values between 100nA and 100μA, duty-cycle independent. Output voltage ranges are from 40mV to 800mV.

The implemented circuit comprises three stages: a differential transimpedance amplifier with a switched feedback network, a differential to single-ended voltage amplifier and an output buffer, as shown in Fig. 6. The three stages are DC coupled to avoid baseline shift with signal input. Additionally a control block is added for gain switching purposes.

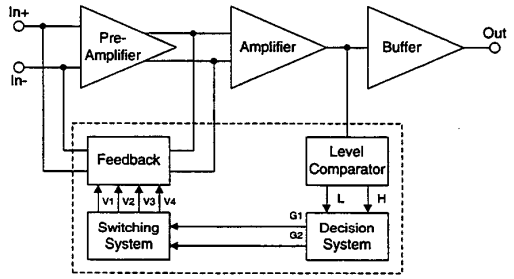

Fig. 6 - Block diagram of a switched gain differential front-end.

The topology used for the transimpedance amplifier is a modified folded cascode configuration [Davidson88, Haralabidis97] where the combination of two branches creates a differential stage. For noise minimisation considerations the transimpedance amplifier also presents an input stage with a large capacitance [Radeka88], once again ideally matched with the PD junction capacitance. Input referred current noise was under 8.2pA/√Hz.

This topology has been seen to be less noisy than the previous circuit, and also not so critically dependent on the compensation parameters. The CMRR value, going from 100dB to 55dB over the entire bandwidth, is high enough to keep electromagnetic interference sufficiently low for the target application.

Nevertheless, this circuit is quite sensitive to DC operating points and requires a pole-zero cancellation at the input for the high gains. If reduced specifications are required (smaller gain and/or bandwidth), both topologies, namely the folded cascode and the starved inverters configurations, can be used without such critical design considerations.

This circuit was produced in a 5V, 0.8μm, double poly, n-well CMOS technology. The die size is 1600×1600μm (including pads). Power consumption is 60mW, of which more than 50% are due to the output buffers.

Fig. 7 confronts these approaches with other design choices. It represents several monolithic CMOS front-ends reported in the literature. Both the front-end bandwidth and the product of its transimpedance gain*bandwidth (Z*BW) are represented in a graph. The Z*BW factor is an easily calculated measure of the quality of the front-end. Note that (with the exception of [Pietruszynski88], which has a large power consumption) values around ~20THzΩ seem to be the state-of-the-art current value, if large dynamic ranges are sought.

[2] We use logarithm units as 10log(A/B) throughout this paper, unless otherwise stated, due to the relationship between optical power and signal current on the PDs.

Neither noise nor dynamic range are represented in Fig. 7, but both can be controlled if high enough Z*BW factors are possible in a given topology. Dynamic ranges of 25-40dB and noise levels of ~10pA/√Hz are reported in several papers. Z*BW values of near 20THzΩ seem to be achievable with present low-cost CMOS technologies, as we have proved. These values may provide a practical rule-of-thumb for WLANs trade-off in terms of achievable bit-rate (for a given BER), cell size and emitter power.

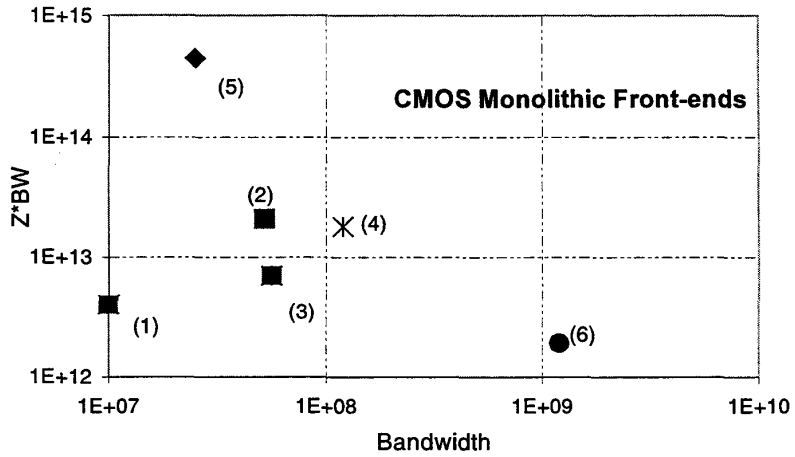

Fig. 7 - Gain*Bandwidth product versus Bandwidth for several monolithic CMOS front-ends.

Front-ends (1-4) were implemented in 0.8μm technologies. Only (1-2) have differential inputs. (1): [Carreir699], (2): [Vasconcelos99], (3): [Cura98], (4): [Steyaert94], (5): [Pietruszynski88], (6): [Toumazou96].

Values for (1-3) were measured with a 10pF input photodiode capacitance. (5) is measured with a 3pF input capacitance. (6) had a 0.25pF input capacitance. The input capacitance is not reported for (4).

Some of the values represented (in particular for (5)) were estimated. No linearity behaviour is known for (5).

5 Receivers

5.1 Clock Recovery

For an integrated system, we have opted by a Phase-Locked Loop (PLL) with a Hogge phase detector. The clock recovery system we are currently using is represented in Fig. 8. The Hogge phase detector is a digital system, avoiding the extra complexity of analogue non-linearity processing in the PLL (see also section 5.2). This phase detector already provides retimed data information, which may be used for word boundary detection and proper MAP detector control.

This clock is divided (in the case of PPM modulation) in order to create the bit and word clocks. These clocks are synchronised in function of the preamble, and of the start of packet detection. Note that other synchronisation approaches (such as [Jungnickel98]) are not practicable, as they require a certain number of words to be received before providing a reliable synchronisation signal: this is impracticable in a packet-based network.

Key design aspects in clock recovery for wireless optical systems, especially with PPM modulation, are the narrow lock range and fast acquisition times required. The clock recovery system implemented uses as Voltage Controlled Oscillator (VCO) an inverter-based ring oscillator. The lock range has been carefully trimmed in order for the system to be able to support parameter variations, and still keep a narrow lock range. This is achieved through separate controls in the ring oscillators' starved inverters. Furthermore, some external control is possible, further decreasing lock time, as some of the starved inverters have an external control point. Nevertheless, a simple start-up circuit has been included for faster lock time, even when no outside control is performed.

We have tested this clock recovery system with several bit-rates, ranging from 6 MHz to 60 MHz, integrated in a receiver. Its performance is clearly adequate inside this range, with peak-to-peak jitter below 20% with random 16-PPM signals, when tested in a receiver with an integrated front-end with 30KΩ gain [Carreir699]. When data signals were directly applied to this clock recovery unit, jitter decreased to values below 15%.

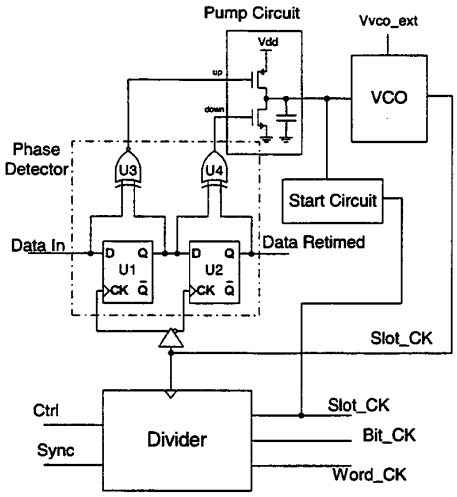

Fig. 8 - PLL with Hogge phase detector

5.2 Symbol Detection

Symbol detection is usually as complex as the complexity of the line code being used. In this section we will focus on PPM detection, as the per-election code for WLANs.

Three main types of symbol detection can be generally used: threshold detection, adaptive threshold detection and maximum-a-posteriori (MAP) detection. Threshold detection is simple to implement, but usually does not provide detection quality for realistic environments. Thus only two types of PPM detection are ordinarily considered in theoretical analysis: adaptive threshold (AT) and MAP — sometimes referred to as maximum likelihood, as PPM word statistics are usually assumed equiprobable. The optimum detection method for PPM, even in the presence of noise (and interference) is a MAP approach [Moreira96, Philips96]. For instance, typical gains of MAP over AT techniques are better than 1.5dB in WLANs without noise; when ambient noise and interference is considered, this gain increases [Moreira96]. This is directly converted into increased WLAN coverage.

Regardless of these considerations, traditional PPM detection is performed by threshold comparison. Simpler approaches use direct threshold detection, while more elaborate ones resort to previous filtering of the signal. Independently of these details, global performance always depends strongly on the way the comparison level is set. Typical approaches for level adjustment range from a manual external adjust (worst performance), going through fixed level comparison [Elmirghani95] and adaptive threshold [Nakamura95]. Improvements in the performance of threshold level systems are normally possible with the introduction of a good quality AGC amplifier before detection. But even with adaptive threshold and AGC circuits, real systems are not able to reach the theoretical limits for AT performance.

Better performances are generally possible with MAP detection. In PPM systems, a MAP detector decides on the symbol received by making a correspondence to the time slot where more energy has been measured. In order to do this, the detector integrates the signal over each slot, and after sampling all the slots in the symbol, decides that the transmitted symbol is the one that corresponds to the time slot with the largest energy value.

The classic approach to this algorithm would lead to the implementation of an analogue peak detector with multiple inputs, one for each slot. Thus, for a M-PPM code, a typical system would require M (integrating) sample-and-hold (S/H) circuits, and M(M-1)/2 two-input comparators; their outputs would be connected to a M-output digital encoder. MAP detection is not usually found in real systems due to the large number of components and the complexity of this approach.

A completely different approach for PPM detection, used in DSP based systems, resorts to analogue-digital (A/D) conversion of the received signal. Each slot is digitally converted as received (by an ADC, analogue-digital converter) and digitally stored in a register; at the end of the PPM symbol, these digital samples are processed in order to determine the received symbol. With a proper ADC, with varying conversion levels, this approach may provide interesting practical results, especially if oversampling and posterior digital processing is done. Major drawbacks are the trade-offs in the A/D converter itself (power consumption vs. silicon size vs. speed) and the digital filtering circuitry required after the conversion. These effectively limit this approach to low bit-rates.

We have developed an alternate analogue-digital architecture that implements a very simple MAP detector [Aguiar97], theoretically providing the same performance as the ideal MAP implementation with much less silicon area and complexity. The MAP detector is schematically represented in Fig. 9 (in the figure, only the lines in bold convey analogue signals). This architecture simply requires a comparator, two S/H circuits, and some digital logic (a register and some control gates) to implement a MAP approach, and thus to achieve the best attainable performance. However, an efficient implementation of this architecture requires the development of a VLSI chip, due to the extremely low signal levels possible in optical systems. Otherwise electromagnetic interference and noise will impair the efficient operation of the circuit.

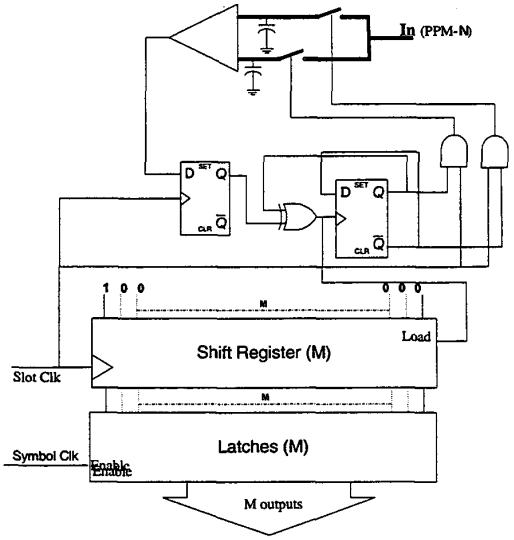

Fig. 9 - Block diagram of analogue/digital MAP detector.

This detector architecture improves on the classic approach by using a differential strategy, a sample is immediately compared with the "largest value found in a slot"; a digital register always keeps track of the slot number this value was detected on. At the end of the symbol, this register holds the decoded PPM word, that is then stored in a latch. At the same time a reset is made to the S/H circuits, restarting the process. The complexity of the classic approach is thus offset by the processing speed of the digital logic and by a more complex mixed analogue-digital design methodology.

We have used this detector in a already mentioned integrated receiver [Carreiró99]. Circuit problems were detected due to the mixing of digital and analogue signals, and to the fact that there are unavoidable connection lines crossing the blocks (due to the architecture itself). Noise is introduced by the clock recovery circuit in the analogue signal and compromises the resolution of the circuit. This problem can be minimised by two sets of measures: i) better power supply noise filtering, and ii) usage of differential circuits in the clock recovery unit.

Table 1 summarises the comparative advantages of several PPM detection methods analysed.

Table 1 - Detector strategies

	Fixed threshold	**Adaptive Threshold**	**DSP**	**MAP (classic)**	**MAP (A/D)**	**MAP (A/D differential)**
A/D	Analogue	Analogue	Digital	Analogue	A/D	A/D
Complexity	Basic	Basic+	High	Medium	Medium	High
Requires integration	No	No	Yes	No	Yes	Yes
Area size	Small	Medium	Large	Large	Medium	Medium+
Power Consumption	Very Low	Low	Large	Large	Low	Medium
Max Bit-Rate	Very High	Very High	Small	Very High	Very High	Very High
Quality	Low	Medium+	High	High	Medium+	High

A further problem related with the usage of MAP detectors is the need for a separate detector for clock recovery. If digital phase detectors are used in the clock recovery system (as discussed in 5.1), then a digital signal has to be delivered to the input of this phase detector. As MAP detection requires the previous synchronisation of the several PPM clocks (otherwise the required digital processing is overly excessive), a different detector is required in the input of such a clock system. In practice this implies that the designer has to implement an adaptive threshold detector as input to these clock recovery system. It is then questionable whether the usage of a MAP detector compensates the extra development effort required for a high-quality detector.

6 Diversity Receivers

Receivers for IR communication systems are usually based on a single optical detector. This is a good configuration in environments where both signal and noise are isotropic. However, in most environments the transmitted signal illuminates the receiver from privileged directions. Also, the ambient light noise emanates from particular directions coinciding with the position of lamps or windows. Moreover, these light sources are frequently in the receiver field-of-view (FOV). These characteristics cause large variations on the SNR, depending on the position, orientation and radiation pattern of both signal and noise sources and on the position, orientation and FOV of the receiver.

To minimise the effects of SNR fluctuations, several receiver techniques were proposed [e.g. Gfeller94, Valadas94, Tang96]. [Gfeller94] suggested an adaptive data rate receiver, where the data rate is continuously adjusted with the purpose of maintaining full network connectivity, trading-off speed and range. [Valadas94] proposed the use of an angle-diversity receiver which was shown to reduce significantly the optical penalty induced by ambient noise [Tavares95b]. More recently, [Tang96] studied the combined use of multi-beam transmitters and angle-diversity receivers, based on a single imaging concentrator coupled with a segmented photodetector, showing also significant optical gains. Angle diversity showed, also, to be very effective in combating multipath dispersion [Lomba95].

An angle-diversity receiver is composed by multiple sectors (optical receivers) with a relatively small FOV. Each sector estimates the SNR of the collected signal. With *Best Sector* receivers only the sector with the best SNR is selected. This contrasts with the case of a *Maximal-Ratio* receiver, where the output signals of all sectors are combined through an adder circuit, and each output signal is proportional to its respective SNR.

A way of implementing a maximal-ratio system is to put the gain of a sector proportional to i/σ^2, where i and σ represent the average signal and noise root mean square (*rms*) values, respectively. This structure of a maximal-ratio angle-diversity receiver is illustrated in Fig. 10. The receiver comprises one front-end, one circuit to estimate the SNR and a variable gain amplifier (VGA) per sector. The output signals of all sectors are combined through an adder circuit.

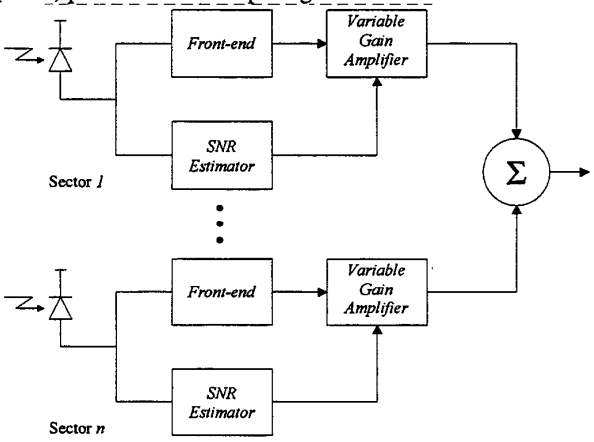

Fig. 10 - Structure of a maximal-ratio diversity receiver.

For a Best Sector receiver, a simpler signal selector would be used, without the need for the VGA (see Fig. 12). The data signal would be selected in function of the best SNR.

6.1 Discrete Implementation (Maximal-Ratio)

The goal of the implemented Maximal-Ratio angle-diversity receiver is to reduce the penalty induced by stationary photocurrent arising from ambient light sources. Our implementation ignores the optical interference produced by artificial light. During the design of the optical sector, it was assumed that the penalty associated with the optical interference could be reduced through the utilisation of an appropriate encoding method, along with adequate electrical and optical filtering [Moreira95, Moreira95b].

In addition to thermal noise, shot noise and optical interference, there is another signal degrading factor (as discussed in section 4.1): EMI. To reduce EMI effects, each sector of the infrared receiver was separated in two complementary low noise transimpedance amplifiers, as discussed before. The design of the optical front-end followed the one presented by [Tavares95a], and was designed to operate at 1Mbps using Manchester line coding. A block diagram of the IR receiver is shown in Fig. 11. Each sector includes two arrays of PIN photodiodes (in this case we have used configuration A (Fig. 2), for simpler front-end design), two differential low-noise transimpedance amplifiers and a differential

amplifier (as discussed in 4.1), but now this is followed by a VGA. The purpose of this VGA is to exhibit an output signal proportional to SNR^2.

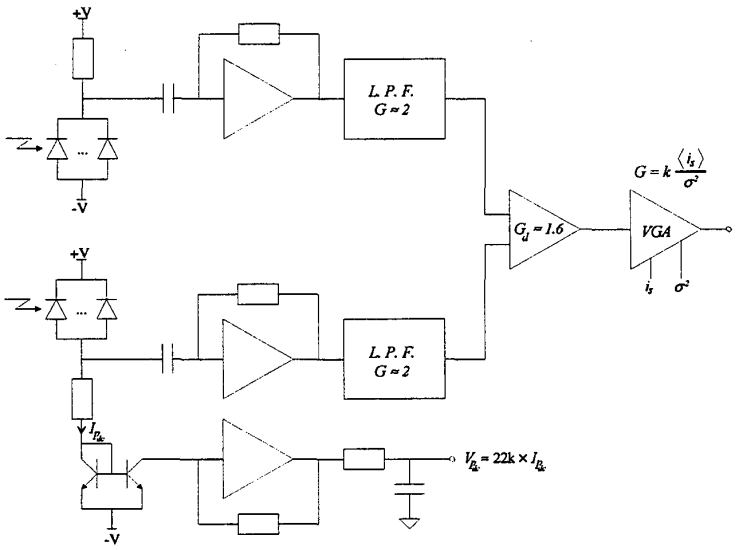

Fig. 11 - Block diagram of one sector.

The gain of each sector in this Maximal-Ratio receiver must be proportional to the relation i/σ^2, and can be described by:

$$G = k\frac{\langle i_S \rangle}{\sigma^2} \tag{2}$$

where $\langle i_s \rangle$ and σ^2 are the average desired signal and the shot noise mean square values referred to the input of the front-end, respectively; k is a scale factor characteristic of the receiver. Thus, the signal amplitude obtained at the output of each sector is proportional to the square of the SNR and can be given by:

$$V_{S_o} = k\left(\frac{\langle i_S \rangle}{\sigma}\right)^2 = k \times (\mathrm{SNR})^2 \tag{3}$$

The variance of the input-referred noise (shot noise), accounting the pulse shaping after the preamplifier, is proportional to the average value of the dc (direct current) photocurrent $I_{P_{DC}}$ and is given by:

$$\sigma^2 = 2qI_2 I_{P_{dc}} B \tag{4}$$

where q is the electronic charge of an electron, B is the bit rate and I_2 is a noise bandwidth factor depending of the transmitter pulse shape and equalised pulse shape only. For our receiver implementation $I_2 \approx 0.56$.

To implement the desired gain it is necessary to evaluate $I_{P_{DC}}$. Since the complementary photodiode arrays are placed near enough, the DC photocurrent induced on both photodiode arrays is almost identical. So, $I_{P_{DC}}$ measurement can be done on one branch of the differential front-end only. Fig. 11 illustrates the evaluation of $I_{P_{DC}}$, which was performed through the inclusion of a current mirror into the photodiode bias circuit.

When designing the VGA it must be taken into account that the optical transmission channel has a large optical range both in terms of signal and noise. These characteristics demand a large dynamic range for the VGA - its gain may need to vary in a large range. Indeed, a series of measurements of PD density presented in [Tavares95a] showed that, in typical well illuminated environments, the DC photocurrent induced in a PIN photodiode could vary between $12\mu A/cm^2$ and $1.2mA/cm^2$. Assuming signal irradiances with an electrical dynamic range of about 40dB, the required dynamic range of the VGA equals 60dB, which is difficult to implement. This problem can be relaxed through the utilisation of a cascade of two VGAs [Tavares95b].

6.2 *Integrated System: Best Sector*

The approaches leading to the implementation of the diversity receiver were quite different in the integrated and the discrete version.

The key difference was related to power consumption and the use of switched gain FEs. The complex structure used for the discrete version would use too much power for integration in a single chip, as the structure illustrated in Fig. 11 would have to be replicated per sector. The situation is furthermore complicated is switched gain front-ends are used.

Thus we implemented an integrated Best-Sector receiver, as presented in Fig. 12. Although the signal selection unit can require some careful design in the case of switched gain front-ends, the real issue is the estimation of the SNR. Note that in the previous case, no real SNR was estimated directly, but the VGAs had gains such that the final output signal was proportional to the sector SNR.

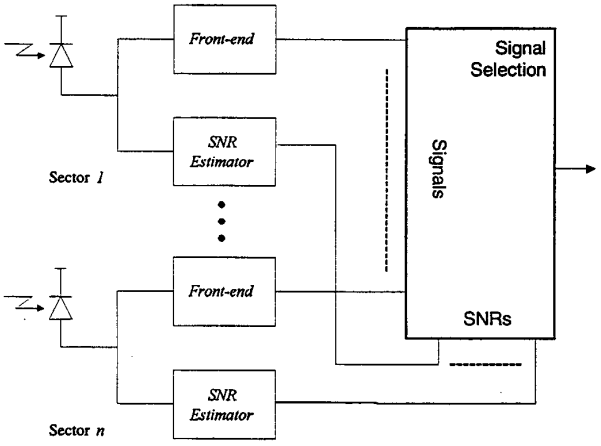

Fig. 12 - Best sector receiver.

In this receiver, a variation of the folded cascoded FE was implemented. Furthermore, we implemented a "true"-SNR estimator through analogue processing. The most complex issue in this implementation is the analogue division required. Several techniques can be used for this task [Alves99], and are summarised in Table 2. Our implementation of the divider circuit follows non-linear feedback theory: analogue division can be achieved through the use of a multiplier placed in the feedback loop of an operational amplifier.

Table 2 - Analogue division techniques

	Pros	Cons
Logarithm conversion	Easy to implement the division	Complex implementation in CMOS of log functions
Translinear circuits	Simple and accurate	Large power consumption, low dynamic range
Current conveyor techniques	Current domain, low noise	Low dynamic range, low design precision
Analogue multiplier and non-linear feedback	Reasonable power, repetitive design	More prone to instability

Fig. 13 represents the schematic of the circuit implemented, after several trade-offs have been analysed [Alves99]. At the heart of this circuit we have three main blocks, two multipliers and one divider. All the periphery circuits presented in Fig. 13 are responsible for signal acquisition and conditioning, biasing and voltage reference. Differential signal paths are used in order to increase noise immunity and also to allow for better rejection of the common-mode components of the signal. In this way it is possible (although probably not desirable) to accommodate both analogue and digital processing units in the same chip. Furthermore, the front-ends for which this circuit was conceived also have differential topologies.

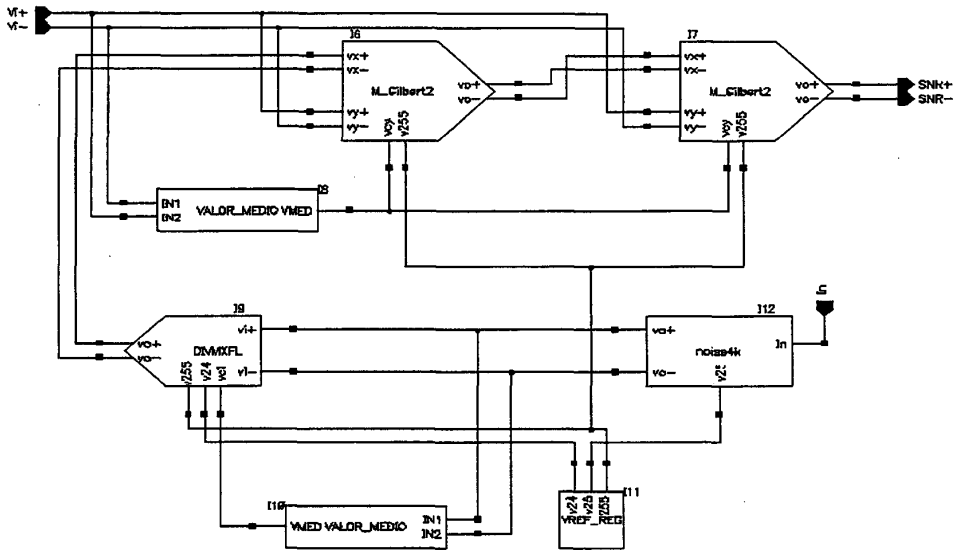

Fig. 13 - SNR estimation block.

The first stage, labelled *noise4k* in the figure, is a simple current to voltage converter, whose principal function is to measure the noise (which is roughly equal to the DC component) in the photodetector. This circuit has also the function of low-pass filtering this noise current (the cut-off frequency is around 2MHz). The acquired noise signal $\sigma^2=2qI_2 I_{p_{DC}}B$, is then fed to the divider circuit, in order to perform the $1/\sigma^2$ function. The next step is the analogue multiplication of this pre-processed noise signal and the output signal of the front-end v_s. Here we assume to have a linear proportionality between the current signal I_s, at the photodetector and this v_s signal (the effects of gain switching are compensated at the signal selection unit). This multiplication is performed twice, in order to obtain v_s^2/σ^2, that is the SNR squared. There are several reasons to measure the SNR squared and not the SNR itself. First, it is not easy to implement square root extraction circuit with the whole dynamic range required for our networks. Second, if this circuit is to be applied to one best sector receiver, it is desirable that it outputs unipolar quantities to simplify the discrimination step.

The blocks labelled *VALOR_MEDIO* are responsible for biasing the multiplier cells. This biasing scheme, based on actual incoming signals, makes the circuit more robust and less dependent on signal levels. Finally the block labelled *VREF_REG* is responsible for all the necessary voltage references in the circuit. We choose to have these references produced inside the chip so that they can be made more accurate. The reference circuit is a simple series regulator, capable of achieve a 22% regulation factor.

Not shown in the figure is the circuit for low-pass filtering the squared SNR result. This filtering step is necessary to provide an average expectation of the optical SNR - its conception is constrained to the type of selection/combining required, the type of signals to handle (PPM, NRZ...), and the type of front-end to be used (fixed gain or switched gain). Note that if non-switched gain front-ends are used, this approach can also be used for a maximal-ratio receiver. The introduction of gain changes in the front-end brings an extra layer of complexity to the system, and thus we decided for the implementation of a simpler Best-Sector receiver.

7 Practical aspects

Cost issues are a key constraint for WLAN wide-deployment. Transceiver cost is a major part on this problem. While some approaches for transceiver design require the implementation of complex lenses (e.g. [Kahn98]), our efforts were centred on electric-related issues. Naturally, better optical approaches should improve on the performance of our networks.

LED prices are already quite low, so the key cost issue is related with the PIN photodiode. Low-cost PDs have small active areas (and thus for large sensitivity systems, several PDs will have to be used) but present reasonably large junction capacitances. This factor places the dominant cost issue on the infra-red transducer and on the transceiver circuitry. As mentioned in section 4, these characteristics of the transducer will limit the relationship between network bandwidth, emitted power and cell size.

All electronic processing has been developed with CMOS technology, both for the analogue and the digital sub-circuits — precisely due to the low cost of this technology. As we have shown, the electronic sub-blocks can implement (given some constraints) baud-rates until 50Mbaud, which makes feasible low-power, low-cost 25Mbps networks with 4-PPM coding.

On the electronic processing discussed, the key constraint was related with the FE characteristics. Its design is inherently complicated by the unwanted characteristics of the input PD junction capacitance. Low noise amplification, with high bandwidth and high gain, would be a hard design problem, even without the PD problems. Additionally, the large dynamic range required, due to the possible power variations inside the rooms, places another design problem to FE design.

Another critical issue in real systems is the impact of EMI in these very high sensitivity front-ends. EMI is pervasive across the whole circuit, from the power supply contacts to the input circuit pins. High common mode rejection ratio circuits are required, placing another extra burden to FE design. Furthermore, extreme care in the differential signal propagation is required. Ideally, the PIN photodiodes should be placed in the same substrate than the LNA. A plastic lens (perhaps metal coated) would be applied above this substrate. This would reduce EMI, but its effects on circuit noise are unknown at this moment.

Nevertheless current low-cost technology seems to be able to achieve noise values in the ~10pA/√Hz range, with products transimpedance gain* bandwidth higher than 20THzΩ. This — together with the above mentioned PD characteristics — imposes a trade-off rule on the network characteristics, in terms of bandwidth and sensitivity. Generically, it seems that this approach may be usable above the 100Mbps value (although probably not with simple diffuse networks, but with more complex approaches, such as multi-spot diffusion), a value usually presented in current simulations as one of the limits for wireless networks.

These bit-rates seem to be achievable only through the resort to diversity receivers. But the sheer size of a sectored receiver precludes its practical implementation in discrete form. Integration is a major consideration for the practical development of WLANs. Thus all the electronics will have to be integrated, eventually in a multi-chip Application Specific Integrated Circuit (ASIC). Diversity brings an increased layer of complexity to WLAN design and prototyping, leading to more complex systems, with higher power consumption.

Our initial approach to WLAN development was oriented towards a single chip receiver. Some of our results [Carreiró99] indicate that this approach, if not unfeasible, involves very complex design issues in terms of the electronics, as we have referenced. We currently are targeting a multi-chip ASIC, with an analogue chip (probably associated with a clock recovery system), and a full digital circuit, covering the whole digital processing required for the network. Note that the usage of a MAP decoder can be questionable, as we have discussed in section 5.2.

From the considerations presented in previous sections, and from our experimental data, a complete diversity receiver would have a power budget with peaks on the order of 4.5W distributed as shown in

Table 3. Note that this value is very dependent on three aspects: i) the network bit-rate, which will require increasingly larger clock frequencies as bit-rates increase; ii) the usage of Complex Programmable Logic Device (CPLD) devices; iii) the power efficiency of the LEDs. Furthermore, notice that this is peak operating power: careful power management would place most of the system in a dormant stage most of the time.

Table 3 - Power budget

		Idle	**Peak power**
Front-end	full-custom	30 mW	30 mW
SNR estimation	full-custom	30 mW	30 mW
Diversity combination	full-custom	<5 mW	<5 mW
Total for N=8 sectors:	full-custom	~480 mW	~480 mW
Clock recovery circuit	full-custom	30-50 mW	30-50 mW
Word Detection	full-custom	~0 mW	< 10 mW
Word Decoding	full-custom	0 mW	5-40 mW
Analogue/digital ASIC	full-custom	~ 500mW	~ 550mW
LEDs (400mW optical)	16 LEDs	~ 0 mW (off)	~ 3 W (sending)
PINs		< 5 mW	< 5 mW
Digital Packet Processing	CPLD	0 mW	~0.3 W
FEC coding/decoding	CPLD	0 mW	~3 W (receiving)
System interface	CPLD	~10 mW	~0.3 W
Grand Total		~500 mW	~4.5 W

The latter issue of CPLD devices is the largest electrical power limitation in the system. It is possible to implement the digital processing in an ASIC [Aguiar98], which will have a much smaller consumption (rough estimates lead to values between 400mW and 800mW). However, the development facilities provided by CPLD technology makes it a technology of choice for prototype implementation. In a final version, an ASIC could be implemented, incorporating all facilities developed in the CPLD. In such a system, power consumption while receiving could be easily reduced to

around 1W, and around 3.5W while sending. Furthermore, idle state dissipation would be in the 0.5W range, as table values seem to indicate. Note that these values are achieved without special low-power design methodologies. Commercial systems could present values below these.

8 Conclusions: Our Quests For The Future

During this document we showed that key blocks for the implementation of wireless IR transceivers can be done with low-cost electronics, and still achieve high-performance results. The convenient choice of network options (such as emitter radiation pattern, FEC and angle diversity), coupled with specially designed hardware, will allow the implementation of simple, low-cost and high performance physical layer for IR networks. Current technology seems to support foreseeable developments in WLANs.

Thus our conclusions are centred in the network we are seeking to implement in the near future.

The network we envisioned is a packet-base, diffuse network, with FEC. Packet structure will have to be carefully considered in order for a low frame error rate to be achieved, and is part of our current work.

The network transceiver will closely follow the diagram of Fig. 2, using sectored receivers. For the same generic transceiver, the relationships between the cell size, transmitted power and bit-rate will be chosen according to the specific application in mind, and few modifications should be required in the basic electronic circuit structures. Our current target is the implementation and trial of a 4Mbps network, over a 5m radius, with 400mW emitter optical power. FE input signals would be in the 100nA-100μA range. However, we expect all the electronics to be immediately adapted to larger bit-rates (10Mbps and 25Mbps) with small increases in transmitter power and/or decreases in cell radius. This would create an environment where the different trade-offs in network design (frame format, transmitted power, bit-rate, cell size, FEC) could be easily evaluated and measured.

Acknowledgements

The work here summarised is the result of several years of development in the field of low-cost WLAN transceivers, where implementation has always tried to follow network evolutions. Many elements have been involved with this work during these years, but a special mention should be done to Adriano Moreira and Cipriano Lomba, in the network aspects, and to Armindo Carreiró, Carla Almeida, Luis Moreira and Rui Antunes, in the implementation questions.

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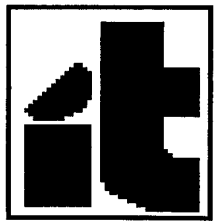
Considerations on the design of transceivers for wireless optical LANs

Rui L. Aguiar, António Tavares, José L. Cura, Eduardo de Vasconcelos, Luis Nero Alves, Rui Valadas, Dinis M. Santos



Overview

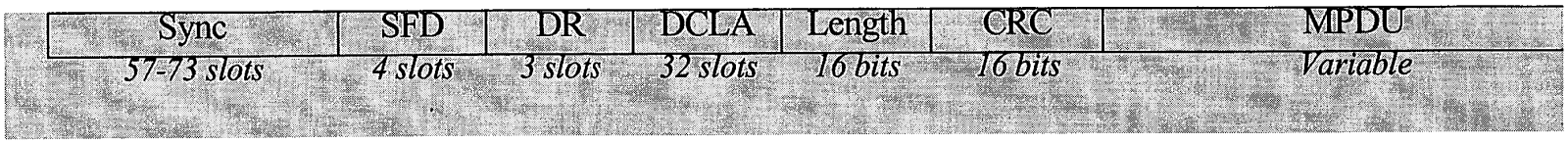
- Introduction: the network(s)
- Front-End Design
- Clock Recovery
- PPM Decoding
- Sectored Receivers
- Overall considerations
- Current Development Targets

Introduction

- **Development of low-cost, high performance WLANs**
- **Electronic circuits (including integration) to support these LANs**
- **Development of a flexible platform to evaluate different HW solutions**

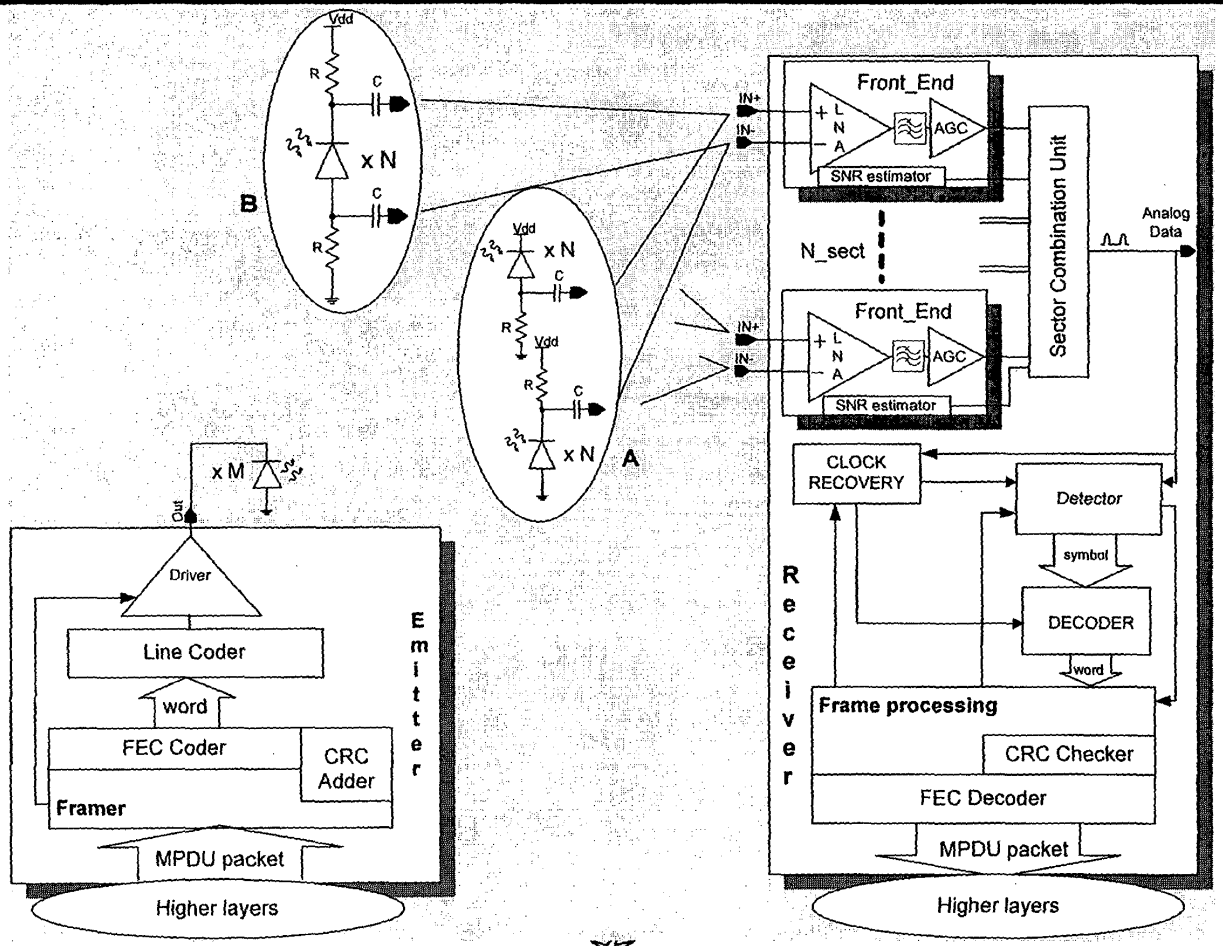
Network Characteristics

- **Diffuse (or MSDC)**
- **Low-Power**
- **Packet based**
- **IEEE 802.11 alike**



  - **Codes: PPM, Manchester, NRZ**
  - **BitRates: 1Mbps-25Mbps**

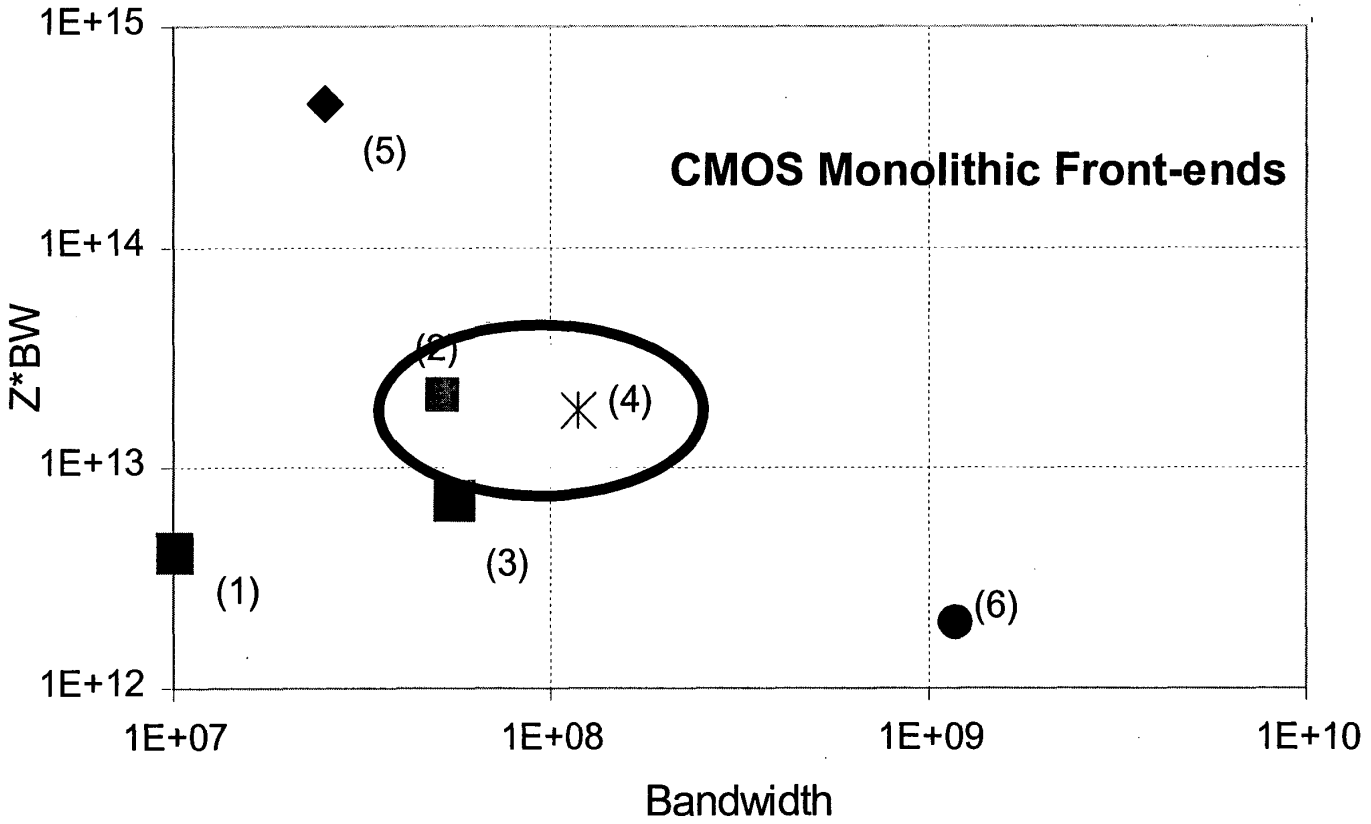
Hardware Development Model



Font-end Design

- Input PD constraints overall performance
- Differential Topology required
- Switched gain approaches provide good architectures
- ~25THzΩ

Font-end Design



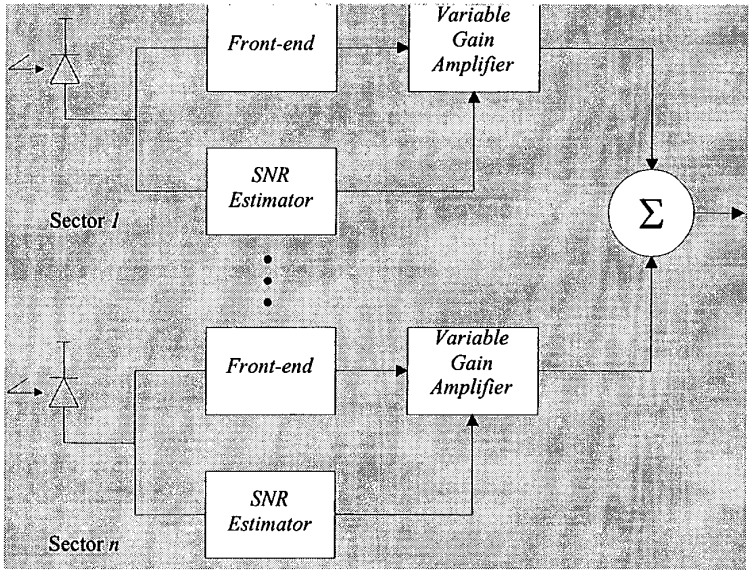
PPM Decoding

	Fixed threshold	Adaptive Threshold	DSP	MAP (classic)	MAP (A/D)	MAP (A/D differential)
A/D	Analogue	Analogue	Digital ✓	Analogue	A/D	A/D
Complexity	Basic ✓	Basic+ ✓	High	Medium	Medium	High
Requires integration	No	No	Yes	No	Yes	Yes
Area size	Small ✓	Medium ✓	Large	Large	Medium ✓	Medium+
Power Consumption	Very Low	Low ✓	Large	Large	Low ✓	Medium
Max Bit-Rate	Very High ✓	Very High ✓	Small	Very High ✓	Very High ✓	Very High ✓
Quality	Low	Medium+ ✓	High ✓	High ✓	Medium+ ✓	High ✓

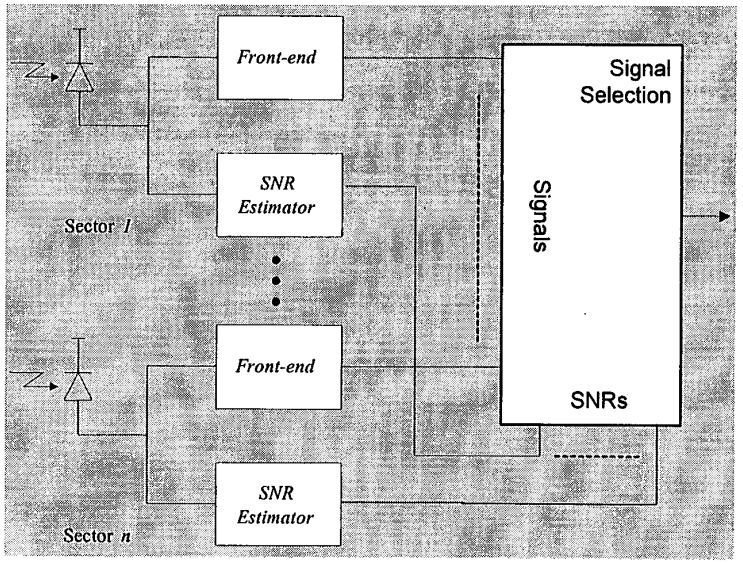
Adaptive threshold seems to be the most practical detection method to implement, specially when it is evaluated with clock recovery considerations

Sectored Receivers

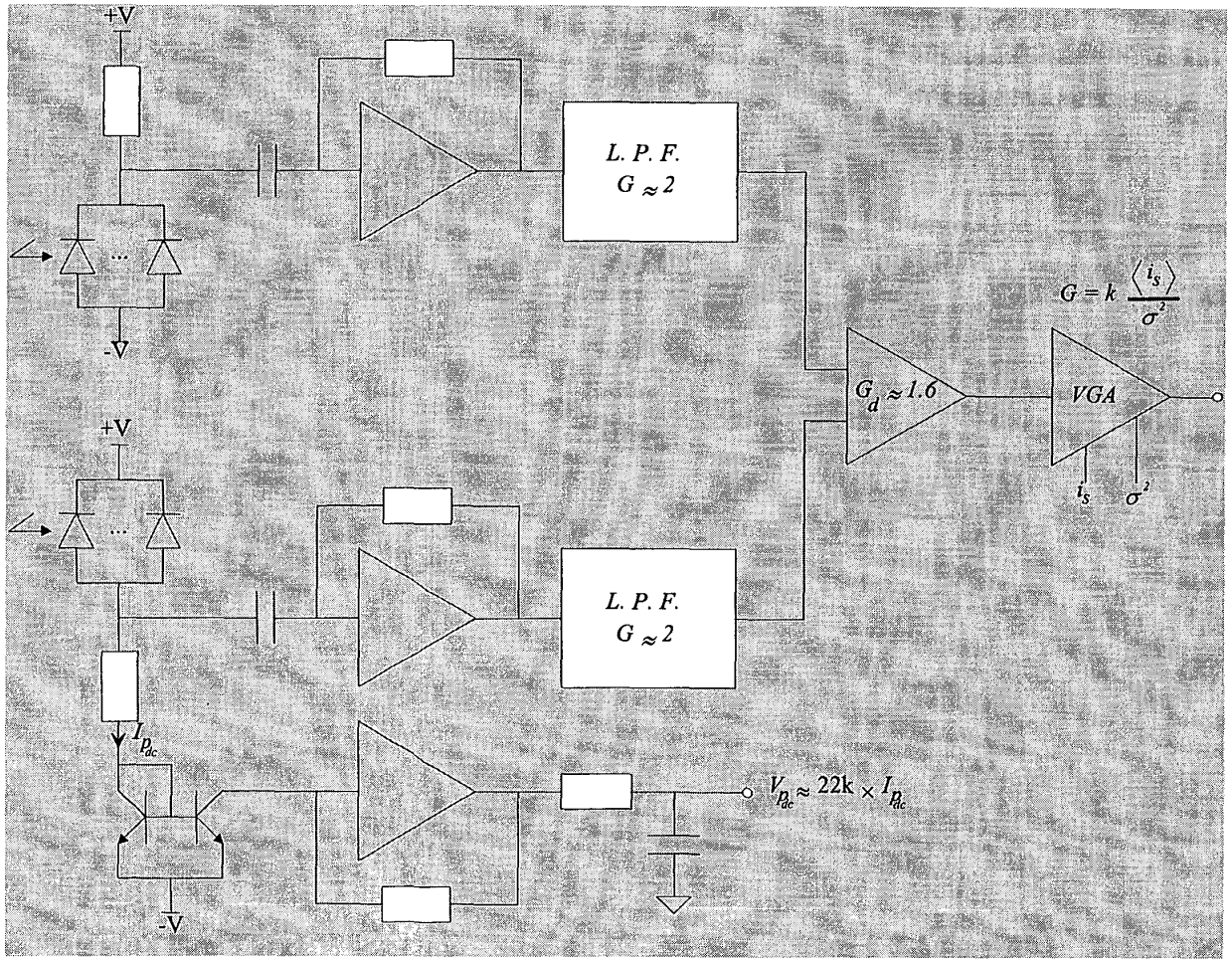
Maximal Ratio



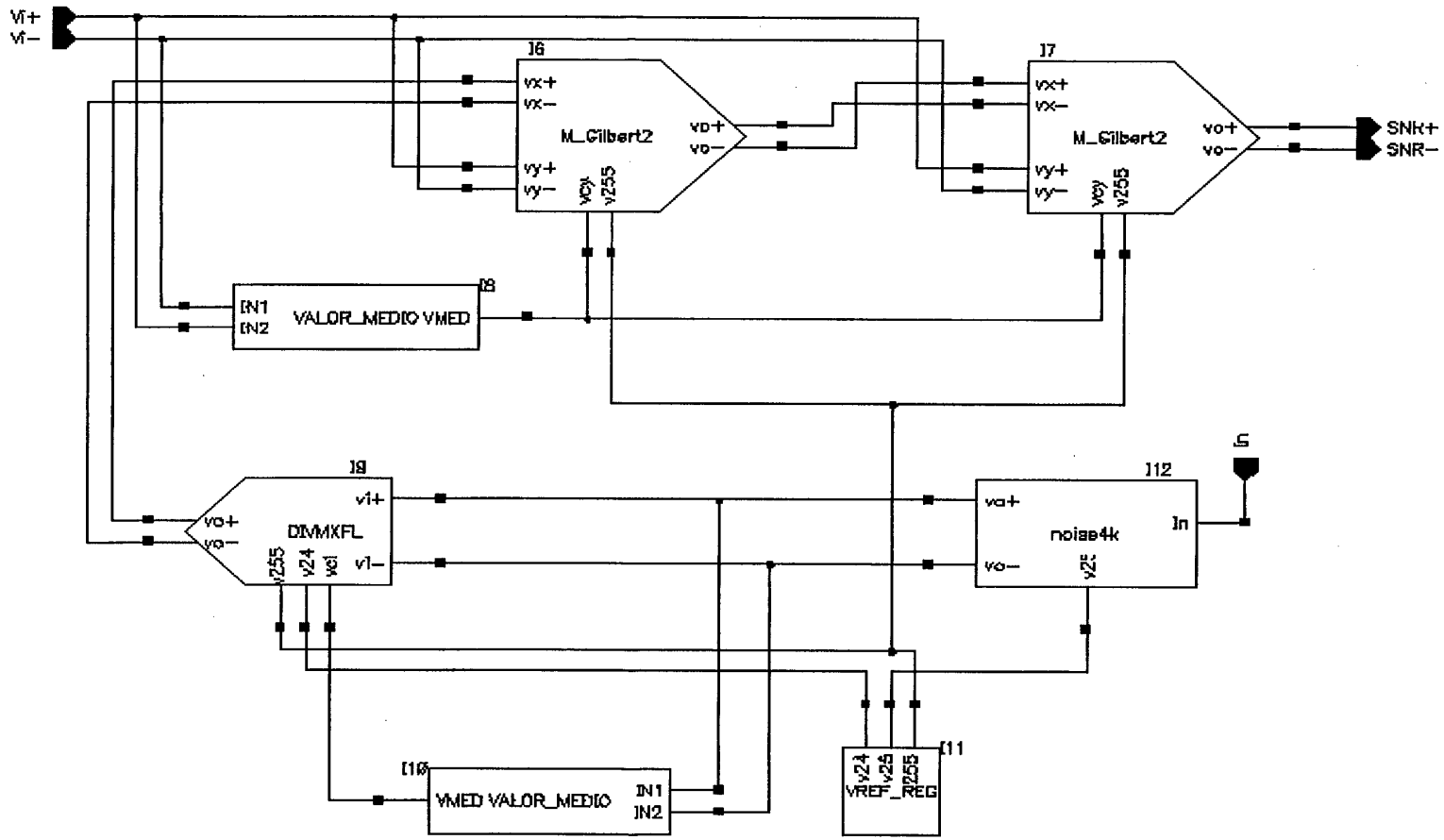
Best Sector



Sectored Receivers: MR



Sectored Receivers: SNR measure



Overall Considerations (I)

- **Major constraints into current development:**
  - **transducer (LED and PINs) characteristics**
  - **integration technology characteristics (CMOS and CPLD)**
  - **power considerations**
  - **high number of sectors**
  - **non-integration of electronics and transducers**

Overall Considerations(II)

- low cost transducers $\Rightarrow$ limitations on bandwidth
- EMI a major problem for high sensitivity systems
- Noise values ~10pA/$\sqrt{Hz}$
- analogue power consumption ~0.5W
- digital power consumption: varies

Current Development Targets

- Development and evaluation of flexible complete system
- Cell sizes around 5m radius
- Optical power < 400 mW
- Low cost integrated system
- Bit rates of 4 Mbps, extending to 10-25 Mbps