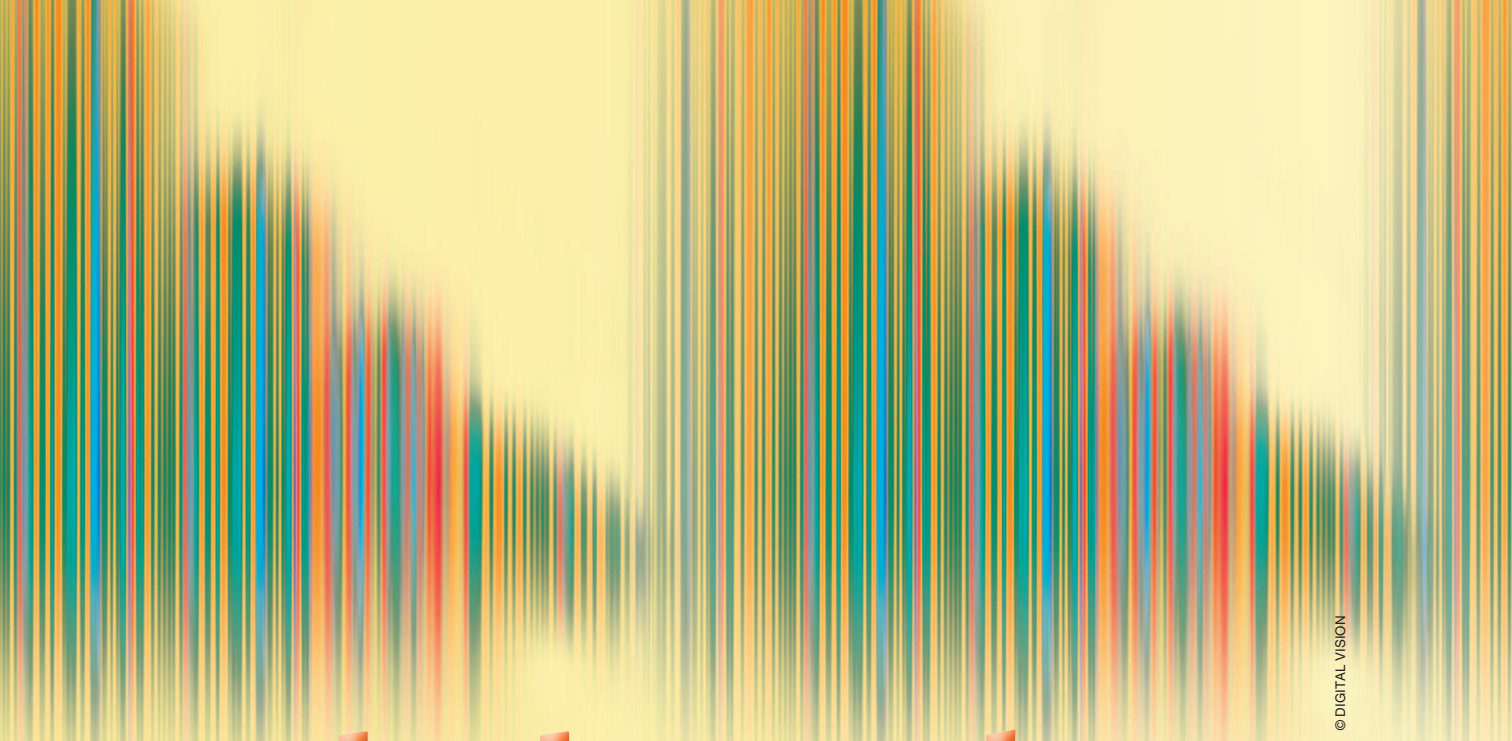

Designing and Testing Software-Defined Radios

Pedro Cruz, Nuno Borges Carvalho, and Kate A. Remley

Software-defined radios (SDRs) will play a key role in future radio configurations because the emergence of new wireless technologies and their integration in a fourth generation of communication standards will necessitate the use of multistandard and multiband radios. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands.

This article reviews the main parts of an SDR to emphasize several possible implementations of both receivers and transmitters. Many of these architectures are actually fairly old techniques that have been recently made practical due to the enormous increase in the capabilities of digital signal processors. We describe solutions for testing and

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The concept of the SDR first appeared with the work of Mitola in 1995.

characterizing these types of devices as well. SDRs typically operate in both the analog and the digital domains, thus mixed-domain instrumentation is necessary to carry out testing.

The concept of the SDR first appeared with the work of Mitola [1] in 1995. In this work, he proposed to create a radio that is fully adaptable by software, enabling the radio to adjust to several communication scenarios automatically. The concept is presented in Figure 1.

SDR front ends consist of the standard subsystems used in most transceivers: modulators and demodulators, frequency converters, power amplifiers (PAs), and low-noise amplifiers (LNAs). However, the modulation and encoding as well as the frequency of operation are determined in software. Such radios typically rely on digital signal processing (DSP) for much of their agility. The SDR is able to adapt itself to the transmission scenario in order to minimize interference to other signals that are present in the air interface. Implementation of such a system requires the ability to scan the spectrum from low to high frequencies using software. This concept has driven many researchers to study cognitive radio (CR) approaches, an idea also proposed by Mitola in [2], where the radio adapts itself to the air interface by optimizing the carrier frequency, modulation, and choice of radio standard to minimize interference and maintain communication in a given scenario.

One of the most promising applications of CR technology is to increase the spectrum occupancy by use of opportunistic radios, where the radio will utilize

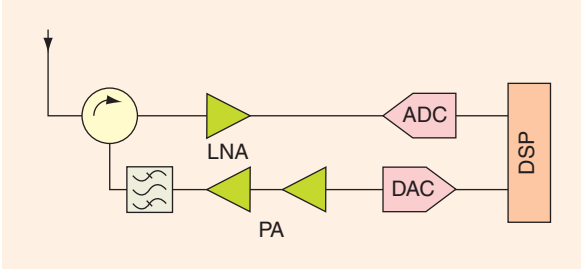

Figure 1. *Common implementation of the software-defined radio concept as described in [1]. A signal incident on the antenna port is routed to a low-noise amplifier (LNA) through a circulator and is then digitized. Demodulation and decoding are accomplished for a number of modulation formats and access schemes using digital signal processing (DSP). The transmission chain is the opposite: baseband signals are generated and up-converted in the DSP module, converted into analog waveforms, amplified, and bandpass filtered before passing through the circulator and antenna. (From [3], used with permission.)*

spectrum that is not being used by other radio systems at a given moment. In order to be able to implement this ideal solution, the radio should see and be aware of the entire spectrum and of the communications being used at a specific time.

The motivation behind the concept of SDR is not only the high flexibility to adapt the front end to simultaneously operate with any modulation, channel bandwidth, or carrier frequency, but also the possible cost savings that using a system based exclusively on digital technology could yield.

In this article, we first give a short overview of several architectures for SDR receiver front ends. Then, several possible architectures for transmitter front ends are described. We discuss methods that can be used to improve amplifier efficiency. Instrumentation currently available in the commercial market that allows the characterization of such types of transceivers is presented in the "Test of Software-Defined Radio Solutions" section. Finally, we summarize this work and identify the more probable solutions from our point of view.

Architectures for Software-Defined Radio Receivers

In this section, several front-end architectures that may be applied to SDR receivers are reviewed. This review is mainly based on [4] and [5].

The first configuration [Figure 2(a)] is the well-known superheterodyne receiver, where the signal received at the antenna is translated to baseband using two down-conversion mixers, bandpass filtered and amplified. The baseband signal is converted to the digital domain where it can be processed. Because of the first mixing process from RF to IF, it is mandatory to use an image-reject filter in front of the mixer. Currently, this architecture is being adopted mostly for higher-RF and millimeter-wave frequency designs [6], [7], such as point-to-point wireless links. In these applications, the solutions discussed in the following are not practical. Actually, superheterodyne receivers have a number of substantial problems when they are applied to SDR applications. Generally, a number of fabrication technologies are used, making full on-chip integration difficult. Also, they are usually designed to a specific channel (in a particular wireless standard). This prevents the expansion of the receiving band for use with signals having various modulation formats and occupied bandwidths. Therefore, the superheterodyne configuration is not attractive for use in SDR receivers due to its complicated expansion for multiband reception.

Another approach is the zero-IF receiver [8], [9], shown in Figure 2(b), which is a simplified version of the superheterodyne architecture. The whole received RF band is selected by a bandpass filter and amplified by an LNA, as in the previous architecture. It is

then directly down converted to dc by a mixer and converted to the digital domain using an analog-to-digital converter (ADC). Compared to the heterodyne architecture, this has a clear reduction in the number of analog components and also allows the use of a filter having much less stringent specifications than the image-reject filter. As a result, this architecture can make use of a high level of integration, making it a common architecture for multiband receivers such as the one described in [9] and for complete transceiver architectures as in [10] and [11]. However, some of these components can be much more difficult to design due to the required performance of each. Also, the direct translation to dc can generate some issues, such as a dc offset [12]. Other issues are related to second-order intermodulation products that are generated around dc, and, since the mixer output is a baseband signal, it can be easily corrupted by the large flicker noise of the mixer [13]. Its advantages make this the most commonly used configuration in radio receivers currently.

A configuration similar to the zero-IF architecture is the low-IF receiver [14], in which the RF signal is mixed down to a nonzero low or moderate IF instead of going directly to dc. In this case, an RF bandpass filter is applied to the incoming signal, which is then amplified. The signal is converted to the digital domain with an ADC of relatively robust performance, which allows the use of DSP for digital filtering for channel-selection and also mitigate in-phase quadrature (I/Q) imbalances in quadrature demodulators. This architecture still allows a high level of integration and does not suffer from the problems of the zero-IF architecture because the desired

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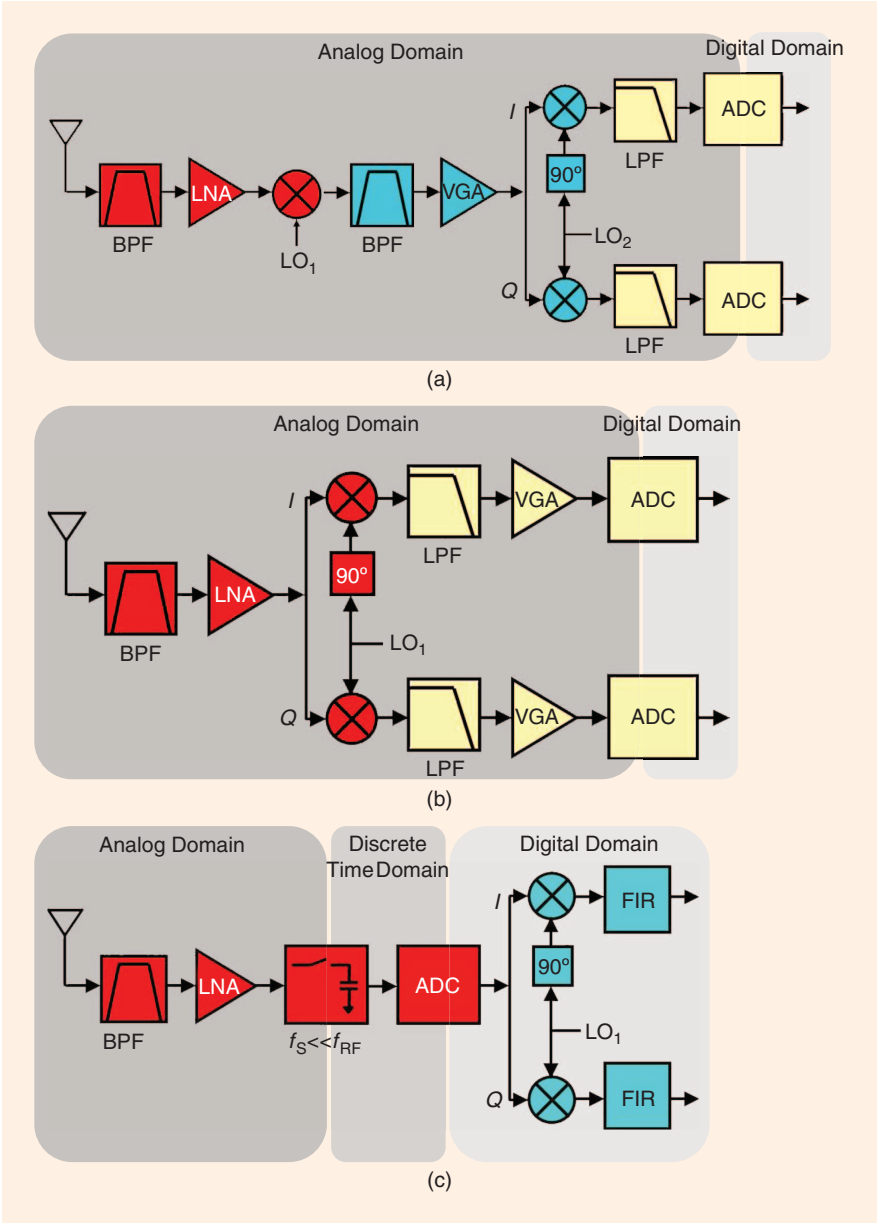

Figure 2. *(a) A superheterodyne receiver architecture where the RF signal is received, filtered, and amplified down-converted to an intermediate frequency where it is again filtered and amplified. Then the signal is converted through a quadrature demodulator to baseband and, in each path (I and Q), filtered, amplified, and converted to the digital domain. (b) A zero-IF architecture in which the RF signal is filtered, amplified, and directly down-converted to baseband by a quadrature demodulator. After that it is filtered, amplified and digitized. (c) A bandpass sampling receiver in which the signal is filtered, amplified, and sampled by a sample-and-hold circuit that is normally a part of the ADC. The signal is mixed-down to the first Nyquist zone, digitized by an ADC, and treated in the digital domain. ADC: analog-to-digital converter, BPF: bandpass filter, FIR: finite impulse response filter, I: in-phase component, LNA: low-noise amplifier, LO: local oscillator, LPF: low-pass filter, Q: quadrature component; VGA: variable gain amplifier.*

signal is not situated around dc. However, in this architecture, the image frequency problem is reintroduced and the ADC power consumption is increased because now a higher conversion rate is required.

Finally, an alternative to the previous solutions is the bandpass sampling receiver [15], [16], Figure 2(c). In this architecture, the received signal is filtered by an RF bandpass filter that can be a tunable filter or a bank of filters. It is amplified using a wideband LNA. The signal is sampled and converted to the digital domain by a high sampling rate ADC and digitally processed. This configuration is based on the fact that all energy from dc to the input analog bandwidth of the sample and hold circuit of the ADC will be folded back to the first Nyquist zone $[0, f_S/2]$ without any mixing down conversion needed. This architecture takes advantage of some properties of sample and hold circuits. As was described in [16], it is possible to pinpoint the resulting intermediate frequency, f_{IF}, based on the relationship

$$\text{if} \quad \text{fix}\left(\frac{f_C}{f_S/2}\right) \quad \text{is} \quad \begin{cases} \text{even}, & f_{IF} = \text{rem}(f_c, f_s) \\ \text{odd}, & f_{IF} = f_s - \text{rem}(f_c, f_s) \end{cases}, \quad (1)$$

where f_C is the carrier frequency, f_S is the sampling frequency, $\text{fix}(a)$is the truncated portion of argument a, and $\text{rem}(a,b)$ is the remainder after division of a by b.

In this case, the RF bandpass signal filtering plays an important role because it must reduce all signal energy (essentially noise) outside the Nyquist zone of the desired frequency band that otherwise would be aliased. If not filtered, the signal energy (noise) outside the desired Nyquist zone is folded back to the first zone together with the desired signal, producing a degradation of the signal-to-noise ratio (SNR). This may be given by

$$SNR = 10*\log_{10}\left(\frac{S}{N_i + (n-1)*N_0}\right), \quad (2)$$

where S represents the desired-signal power, N_i and N_0 are in-band and out-of-band noise, respectively, and n is the number of aliased Nyquist zones.

The advantage of this configuration is that the sampling frequency needed and the subsequent processing rate are proportional to the information bandwidth, rather than to the carrier frequency. This reduces the number of components.

However, some critical requirements exist. For example, the analog input bandwidth of the sample and hold circuit (normally inside the ADC) must include the RF carrier, which is a serious problem, considering the sampling rate of modern ADCs. Clock jitter can also be a problem. Also, RF bandpass filtering is required to avoid overlap of signals.

Other architectures being proposed for use in SDR receivers involve use of direct RF sampling techniques based on discrete-time analog signal processing to receive the signal, such as the ones developed in [17] and [18]. These methods are still in a very immature stage but should be further studied due to their potential efficiency in implementing reconfigurable receivers.

Architectures for Software-Defined Radio Transmitters

The Front End

In this section, we discuss several transmitter architectures that have potential application to SDR systems. As we know, a transmitter is not only the PA but a variety of other circuit components collectively known as the front end. The design of the PA is one of the most challenging aspects of transmitter design, having a high impact on the coverage, the product cost and the power consumption of a wireless system. Here we begin with a consideration of the complete transmitter architecture and, in a following section, discuss the PA as it relates to SDR. This review is mainly based on [19].

The first architecture [Figure 3(a)] is the common superheterodyne transmitter, which is the dual of the superheterodyne receiver presented in Figure 2(a). The signal is created in the digital domain and then converted to the analog domain using simple digital-to-analog converters (DACs). The signal is modulated at an intermediate frequency, where it is amplified and filtered to eliminate harmonics that were generated during modulation. Finally, the signal is up-converted to RF using a local oscillator (LO_2), filtered to remove unwanted image sidebands, amplified by an RF PA and applied to the transmit antenna. The I/Q modulator works at IF, which means hardware components are easier to design than they would be for an RF-based modulator. Finally, the overall gain can be controlled at IF where it is easier to build high-quality variable gain amplifiers. However, such an architecture has a significant number of problems, as in the receiver's case. Therefore, this architecture is mostly adopted for microwave point-to-point wireless links as, for example, in backhaul communications [6], [7] and of course in the above-mentioned field of radio transmitters. The amount of circuitry and low integration level, as well as the required linearity of the PA and the difficulty to implement multimode operation generally prevent the use of superheterodyne transmitters in SDR applications.

Figure 3(b) shows a block diagram of a direct-conversion transmitter [20], [21] that is a simplified

version of the superheterodyne front end. As in the last case, two DACs are used to convert the baseband digital I and Q signals to the analog domain. The low-pass filters that follow eliminate Nyquist images and improve the noise floor. These signals are directly modulated at RF by the use of a high-performance I/Q modulator. After that, the signal is filtered by a bandpass filter centered at the desired output frequency and is amplified by a PA.

In a frequency-agile system, the signal chain must be designed so that carrier frequencies can be synthesized over a defined range that will require a broadband post-modulator or a tunable post-modulator filtering to attenuate out-of-band noise. Thus, due to a phenomenon known as *injection pulling* [22], the strong signal at the output of the PA may couple to the LO_2. As a result, the frequency of the LO_2 can be pulled away from the desired value.

Even though this architecture reduces the amount of circuitry required and easily allows high-level integration, it carries some disadvantages such as possible carrier leakage and phase gain mismatch. Gain control may need to be carried out at RF and this architecture also requires a PA with good linearity. With careful design, these transmitters can be employed in SDR applications, and, with the development of integrated technologies, we have witnessed a fast migration from the superheterodyne architecture to direct-conversion transmitters.

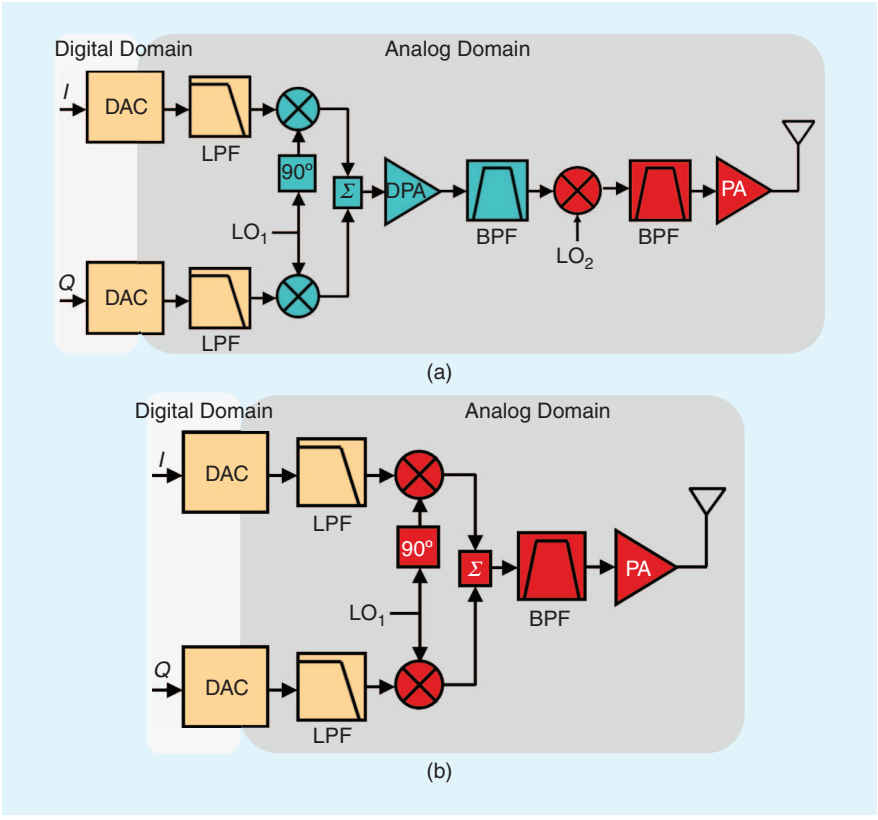

Figure 3. *(a) A superheterodyne transmitter in which the I/Q digital signal is converted to the analog domain, low-pass filtered, and modulated at an intermediate frequency. Then the signal is amplified, filtered, and up-converted to RF where it is filtered again and amplified before being transmitted. (b) A direct conversion architecture where the I/Q digital signal is passed to the analog domain by a DAC, filtered, and then directly modulated at the desired RF frequency. After this, the RF signal is filtered and amplified by a power amplifier. BPF: bandpass filter, DAC: digital-to-analog converter, DPA: driver power amplifier, I: in-phase component, LO: local oscillator, LPF:low-pass filter, PA: power amplifier, Q: quadrature component.*

The Power Amplifier Section

In the previous architectures, the RF PAs (PA block) used are class A, AB, or B, which demonstrate the highest efficiency when operated in the compression region, or are class D, E, and F operated in switching mode [23]. The latter, highly efficient PAs operate in a strongly nonlinear mode. As a result, they can only amplify constant-envelope modulated signals such as those used in the global system for mobile communications (GSM) access format. Modulation types such as quadrature amplitude modulation (QAM) that are used in new access formats such as wideband code division multiple access (W-CDMA) and orthogonal frequency-division multiplexing (OFDM), have high peak-to-average power ratios (PAPRs). The standard way to avoid compression of PAs is to operate them in "back-off" mode, that is, to reduce the input power until the PA is not driven into compression. Unfortunately, this lowers efficiency significantly, especially for high PAPR signals. Several linearization techniques, for example, feedback, feed-forward, or digital predistortion, [23], [24], have been proposed and evaluated, but these are not yet widely used in fully integrated PAs.

The problem of transmitting a high PAPR signal efficiently has been thoroughly investigated over the years. To increase efficiency, a technique proposed some years ago, the Kahn technique [25], is now being studied for use in new transmitter architectures.

Envelope elimination and restoration (EER), proposed by Kahn, is one method to linearize highly nonlinear, highly efficient transmitters. In these systems, the supply voltage of the output RF PA is dynamically

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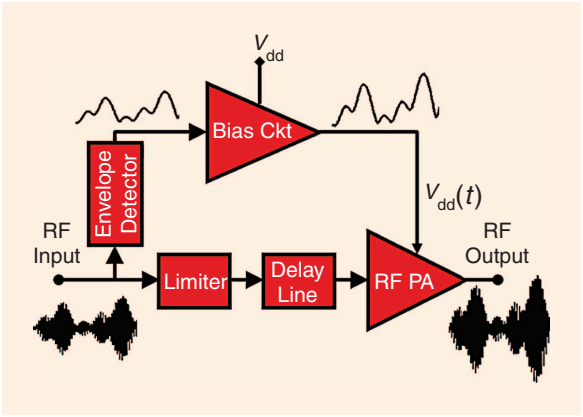

Figure 4. *Block diagram of a Kahn amplifier section in which the RF input signal is split into two branches. One branch is a delayed and constant-envelope RF carrier with phase information (implemented by a limiter and a delay line). The other branch carries the amplitude of the signal envelope to be amplified (Bias Ckt) and then applied to the drain voltage of the RF power amplifier.*

adjusted to restore the amplitude onto a phase-modulated representation of the signal. Figure 4 shows the traditional EER architecture. Although it is a very appealing concept, the actual implementation is very challenging. The challenge arises mainly from the design of a perfect delay line, an accurate limiting stage, an improved bias circuitry that could allow high PAPR and high bandwidths, and the bandwidth that the switched/saturated RF PA should cover to amplify the phase-modulated signal [30].

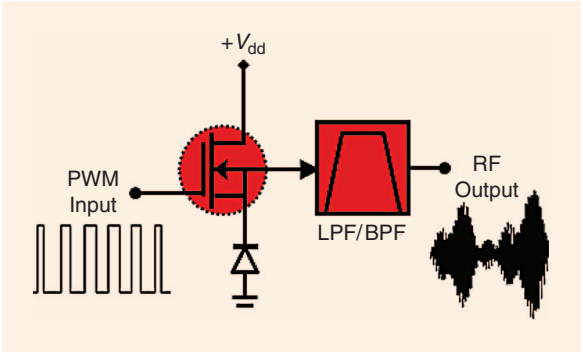

Figure 5. *Simplified circuit of a class-S power amplifier with a digitally generated pulse-width-modulated signal applied at its input. This circuit will generate a baseband signal or an RF signal at the output after the low- or bandpass filtering.*

For these reasons, in modern realizations, with the enormous improvements in DSP capabilities, it has been advantageous to implement the envelope detector, the limiter, and the delay line (time delay) digitally. Such a digital version of an EER transmitter is used in the polar transmitter, which will be explained later.

A visionary solution uses pulse-width modulation to create the so-called all-digital transmitter that will be described next. This all-digital approach is important because of the implementation of novel SDR configurations that will enable cognitive approaches. This approach also enables a low dc power consumption because it allows the use of very-high-efficiency transmitters, such as the class-S PA shown in Figure 5.

Furthermore, as the speed of digital signal processors advances, algorithms in which the DSP provides signals at RF can be envisioned (particularly for switching amplifiers in which the inputs are digital pulse-width modulated signals and the outputs are RF modulated signals) in order to develop the all-digital transmitter.

As shown in Figure 5, the class-S amplifier [26] can be a pure switching amplifier followed by a low-pass filter (to create an envelope signal) or a bandpass filter (to create an RF signal). This amplifier ideally will consume no dc power because the output voltage and the current are equal to zero alternately and, as a result, the efficiency achieved will be 100% in the ideal case. In reality, the class-S amplifier will consume some power in the signal transitions. This is because in real devices, interconnecting components and parasitic capacitance will produce some losses, and finite switching times will occur. The input pulse-width-modulated signal can be generated by a digital signal processor, eliminating the need for a wideband DAC and potentially saving cost.

Unfortunately, if one looks at real-world configurations, it is not possible, yet, to design a high-efficiency class-S amplifier to operate at very high frequencies. Nevertheless, some contributions are appearing in the field [27]. Similar approaches are being tried with sigma-delta modulators [28], [29].

Because of this, switching amplifiers that are being widely used in new configurations are based on envelope elimination and recovery in a polar transmitter configuration [30], [31] in which the envelope information is modulated. As a result, the required bandwidth is much smaller since it is a baseband signal that is being amplified. This allows the use of high-efficiency class-S amplifiers, Figure 6.

If we look at the circuit of Figure 6, the class-S amplifier only amplifies the envelope of the input signal (detected in the digital domain by the digital signal processor, DSP). In this case, the class-S amplifier is only used to vary the bias voltage, $V_{DD}(t)$, of the RF high-power amplifier. In the phase path, a constant-envelope

phase-modulated signal is generated in the DSP and then up-converted to RF and applied to the RF PA. This RF PA is always saturated, providing high efficiency. Nonetheless, the major concern of such schemes is the time alignment between the baseband envelope path and the RF path. This can be compensated in the digital domain by use of DSP.

Other architectures being proposed include amplifier sections based on the Doherty [32], [33] and outphasing [34] techniques. The Doherty scheme combines two PAs (a carrier PA biased in class-B and a peak PA biased in class-C) of equal capacity through quarter-wave-length lines or networks. In modern implementations, DSP can be used to improve the performance of the Doherty amplifier by controlling the drive and bias to the two PAs. For ideal class-B amplifiers the average efficiency can be as high as 70% for high PAPR signals.

The outphasing design, also known as linear amplification using nonlinear components (LINC), produces an amplitude-modulated signal by combining the outputs of two PAs driven with signals of different time-varying phases. Using ideal class-B amplifiers, the average efficiency now can be around 50% for the same large PAPR signals as in the previous case. More details about these designs can be found in [19].

With regard to SDRs, both the Doherty and outphasing techniques can be of high interest for future exploration. This is due to the fact that the improvements in the particular PA section efficiency will lead to higher efficiencies in the entire transmitter. Also, this transmitter architecture holds the promise of operating correctly for several multistandard and multiband signals.

Test of Software-Defined Radio Solutions

After introducing candidate architectures for both receivers and transmitters used in SDR front ends, we next address another important theme: the test and measurement of SDR systems. Key to this discussion is the concept of a mixed-domain measurement technique, because the SDR system always has one input in the analog domain and the other in the digital logic domain. In the SDR concept, the main idea is to push the ADC/DAC as close as possible to the antenna, as shown in Figure 1. As a result, fewer signals will exist in the analog domain, and the measurement of digital signals takes on a level of importance not found in traditional analog-RF system characterization.

For ideal class-B amplifiers the average efficiency can be as high as 70% for high PAPR signals.

Hardware

The instrumentation industry [35]–[37] has developed various instruments suitable for SDR characterization, such as mixed-signal oscilloscopes that are capable of operating in the analog and digital domains at same time. This allows time synchronization of both analog and digital signals in a single instrument. However, mixed-signal oscilloscopes only provide asynchronous sampling. This means that, like a traditional sampling oscilloscope, the mixed-signal oscilloscope uses its internal clock to sample data. As discussed in [38] and [39], when testing SDR devices (including ADCs), the correct evaluation of phase and amplitude transfer functions requires coherent sampling between the input, output, and clock signals. If these signals are asynchronously sampled, then spectral leakage may occur that can completely degrade any amplitude and phase information from the SDR. The spectral leakage arises due to the fact that when performing the necessary Fourier transform (DFT or FFT), the two signals do not share a common time domain grid, and thus they become uncorrelated to each other.

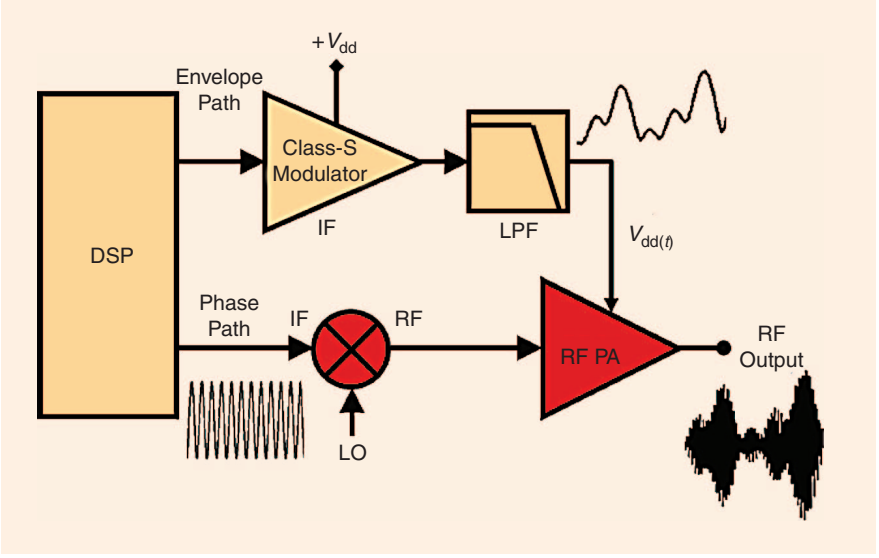

Figure 6. *Block diagram of a polar transmitter. The signal is generated by a DSP and divided into envelope amplitude and constant-envelope phase-modulated components. The pulse-width-modulated envelope signal is amplified by a class-S modulator, then low-pass filtered to produce the analog signal envelope and supplied to the bias of the RF power amplifier. The constant-envelope phase-modulated component is up-converted to RF with a mixer and amplified by the RF power amplifier.*

In a frequency-agile system, the signal chain must be designed so that carrier frequencies can be synthesized over a defined range.

Other potential problems with the mixed-signal oscilloscope include, for instance, the memory size necessary to obtain a behavioral model. Because these instruments normally use very high sampling rates, a huge number of points is required to be able to capture the slow/medium symbol rates of commonly used modulated signals. Thus, these types of instruments are not able to characterize a complete SDR front end in its entirety.

Other approaches also proposed by the instrumentation industry combine several instruments, including logic analyzers, oscilloscopes, vector signal analyzers, or real-time signal analyzers [40]–[42]. For testing an SDR transmitter configuration, these instruments can be used in an arrangement similar to the one shown in Figure 7. With the use of reference signals, trigger signals, and markers, one can acquire synchronized measurements between digital and analog domains and between time and frequency domains. Typical measurements that may be used to evaluate the transmission or reception chains in SDRs with these systems are the progression of error vector magnitude (EVM) and adjacent-channel power ratio (ACPR) throughout the signal chain.

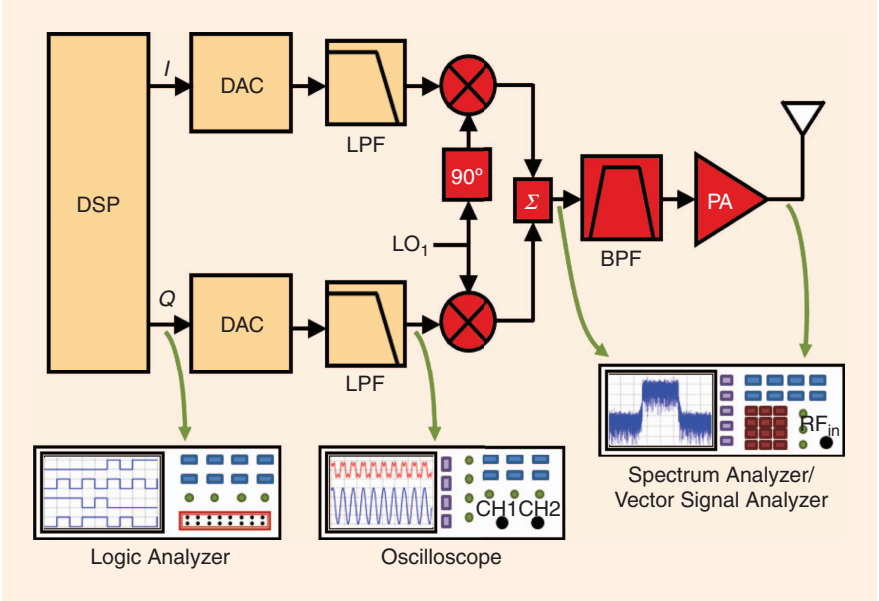

Figure 7. *Instrumentation employed in testing a software defined radio transmitter where several instruments are combined. A logic analyzer acquires the digital logic bits at the output of the digital signal processing (DSP) section, an oscilloscope analyzes the analog signal after the digital-to-analog conversion (DAC) and low-pass filter (LPF) reconstruction, and a spectrum analyzer or a vector signal analyzer obtains the analog RF signal right after the quadrature modulator or also after amplification.*

In [39], the authors discussed the issues of signal timing and synchronization requirements and proposed some solutions, for example, embedding a trigger signal in the test excitation. Some important problems still have to be addressed, such as a calibration procedure for mixed-signal instrumentation. The analog channel in a mixed-signal instrument should ideally measure the reflection coefficient at the input port. Directional couplers should be used to provide a wave-based, impedance-mismatch-corrected characterization of the RF signals incident on the device under test (DUT). With this information, it would be possible to relate the analog input with the digital output in order to find a transfer function or even the complete behavioral model for the SDR system. It is possible to construct such instrumentation using off-the-shelf components and algorithms, for example, the mismatch-correction algorithms discussed in [43]. However, a complete measurement set-up is not currently available commercially.

With this mixed-signal instrumentation, it will be possible to measure figures of merit that are native to analog front ends but also figures of merit that are native to digital communication signals.

Figures of Merit

One common technique to assess the overall performance of a digitally based radio is the bit error rate (BER) test. This test measures the quality of the signal transmission and reception in terms of erroneous data bits over the total bits sent. However, it is a rather limited test because it does not provide much information on the sources of bit errors.

However, if an arrangement similar to the one shown in Figure 7 is used for testing an SDR system, signals in the different domains are acquired simultaneously by the different instruments. This enables the test engineer to pinpoint the possible sources of imperfections throughout the entire signal chain.

In this regard, a second commonly used figure of merit is EVM, which provides insight into potential transmitter and receiver problems [40], [42] because the effects of both magnitude and phase errors on each of the digitally transmitted symbols are measured. EVM essentially measures the overall signal-to-noise-and-distortion ratio, quantifying

signal impairments due to nonlinear distortion, as well as system noise. Contrary to other figures of merit, EVM evaluates the impact on the signal quality in terms of the real transmitted symbols.

A metric that is typically used in transmitter testing quantifies the amount of spectral regrowth in the adjacent channels. Adjacent channel power ratio [ACPR, sometimes called adjacent channel level ratio (ACLR)], is often specified using out-of-band masks that define the maximum allowable transmitted power in an adjacent channel. ACPR usually arises from spectral regrowth due to nonlinear distortion.

ACPR can also be applied to the alternate channels (the channels adjacent to those adjacent to the bandpass signal). ACPR provides a functional test to assess the performance of the entire radio network, because it allows an engineer to evaluate the interference that the nonlinearities in the radio system will impose on other close-by channels.

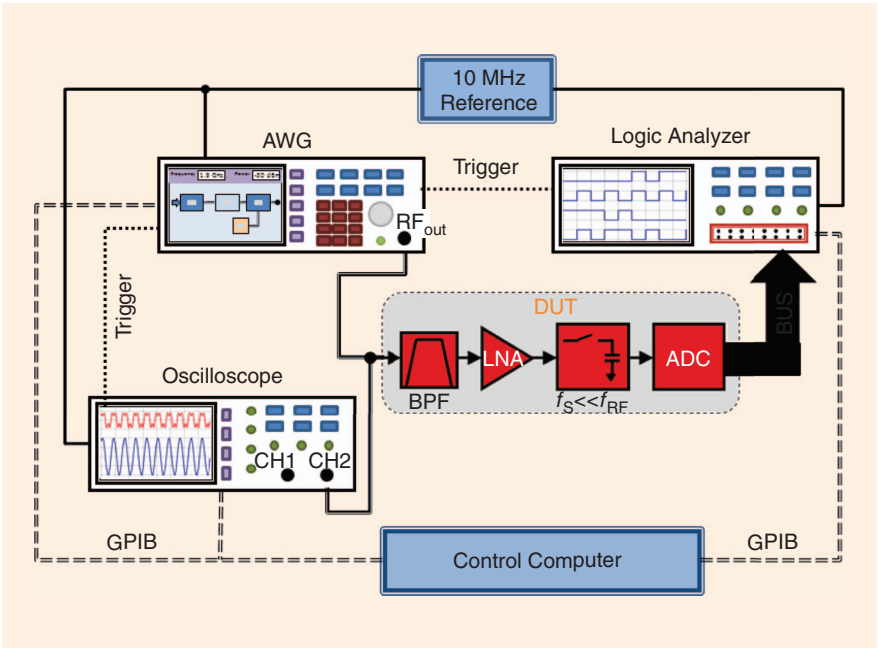

Figure 8. *Laboratory implementation of the instrumentation proposed in [39] for testing SDR front ends. The device under test (DUT) is excited by an arbitrary waveform generator, and an oscilloscope is used to sample the analog signal input to the DUT. A logic analyzer is used to sample the DUT's digital output signal. Reference and trigger signals synchronize the input and output measurements. The instrumentation is controlled by a computer using general purpose interface bus (GPIB) connections.*

For SDR test, as with many radio architectures, the excitation signal to be used during test will affect measured performance of the radio system. The effect of the test signal on radio performance is normally examined through the inherent statistics of the excitation, either using the probability density function (PDF) or the complementary cumulative distribution function (CCDF). The signal's PAPR value is also often used as a figure of merit [44]–[48].

These figures of merit, common to both traditional radio systems and SDRs, are discussed and explained in more detail in "Metrics for Wireless System Test." In the following example, we illustrate the mixed-domain methods that must be used to measure these figures of merit in SDR systems.

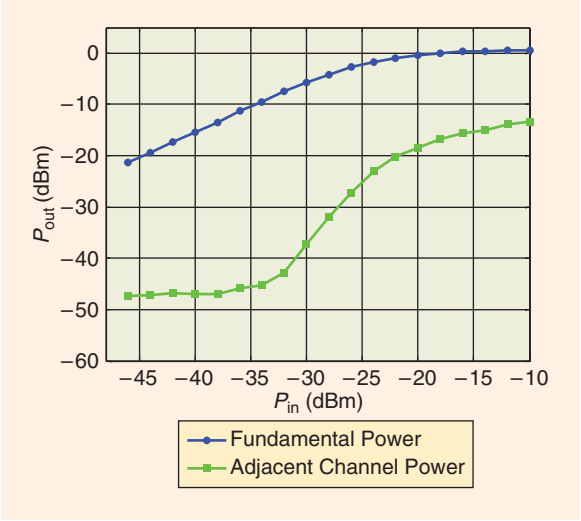

Figure 9. *Measured results at the output of the SDR front end with WiMAX excitation.*

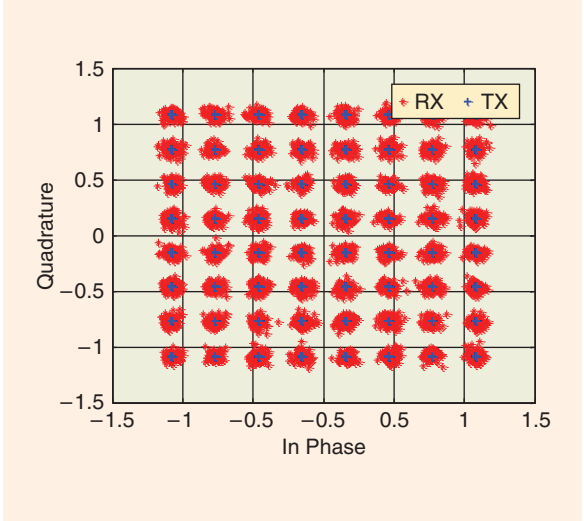

Figure 10. *Constellation diagram comparing the input and output WiMAX signals using 64-QAM modulation.*

Metrics for Wireless System Test

Here we will give a brief description of several figures of merit that were identified throughout the article.

Probability Density Function

In probability theory, a probability density function (PDF) is a function that represents the probability that a random variable X will take on a value less than the number x. Normally, the PDF is determined after a large number of measurements have been performed, which determine the likelihood of all possible values of x. It is a nonnegative function with unit area

$$\text{pdf}(x) = P[a < X \leq b] = \int_a^b f(x)dx, \tag{S1}$$

where a and b represent the limits wherein the probability of X will be assessed.

Complementary Cumulative Distribution Function

The complementary cumulative distribution function (CCDF) curve is closely related to the PDF because it is obtained by means of CCDF = 1 − CDF. The CDF is the cumulative distribution function that is obtained directly from the PDF's statistics as

$$\text{cdf}(x) = \int_{-\infty}^{a} \text{pdf}(x)dx. \tag{S2}$$

A CCDF curve shows how much time a signal spends at or above a certain power level. It is normally expressed in decibels above the average power.

Peak-to-Average Power Ratio

Peak-to-average power ratio (PAPR) is a relationship between the maximum value of the peak power and the average power of a given signal and is a measure of great interest in wireless communications. The evaluation of the impact of PAPR on communications systems is mainly made through the analysis of CCDF curves, where we define a certain percentage in the CCDF curve to pinpoint the PAPR value

$$\text{PAPR} = \frac{\max\limits_{0 \leq n \leq \text{NT}} |x(t)|^2}{\frac{1}{\text{NT}}\int_0^{\text{NT}} |x(t)|^2 dt}, \tag{S3}$$

where NT represents the total number of samples (time interval) that will be considered to determine the PAPR value.

Adjacent Channel Power Ratio

Adjacent channel power ratio (ACPR) is a measure of the amount of distortion that a wireless system generates in the adjacent-frequency channel relative to the power in the main channel. It is usually defined as the ratio of the average power in the adjacent-frequency channel (or offset channel) to the average power in the transmitted-frequency channel as

$$\text{ACPR}_{up} = \frac{\int_{F_1}^{F_2} S(w)\,dw}{\int_{U_1}^{U_2} S(w)\,dw}, \tag{S4}$$

where F_1 and F_2 represent the boundaries of the frequency spectrum, $S(w)$, of the fundamental signal, and U_1 and U_2 are the boundaries of the frequency spectrum of the upper-adjacent channel.

There are two ways of measuring ACPR, as defined in wireless standards, one that considers the ratio between the entire fundamental channel over the entire adjacent channel. The second approach (more popular because it is easier to measure) is to find the ratio of the output power either across the entire main band or in a smaller bandwidth around the center of carrier to the power in the adjacent channel with the same smaller bandwidth.

Bit Error Rate

Bit error rate (BER) represents the ratio of the number of erroneous data bits received to the total number of data bits transmitted. BER is normally given as a percentage, where 0% represents the case where no erroneous bits were detected at the receiver

$$\text{BER} = \frac{N^{\text{o}}\,\text{Erroneous Bits}}{\text{Total Bits Sent}}. \tag{S5}$$

This measurement can be performed in the digital domain by a software function implemented by the test engineer, but also using well-known BER testers that input a known data stream into the transmitter input and compare it with the data bits coming from the receiver's output.

Error Vector Magnitude

Error vector magnitude (EVM) is a measure of modulation and demodulation accuracy, as well as channel impairments. It may be used to quantify the performance of a digital radio transmitter or receiver. A signal sent by a transmitter or received by a receiver will suffer from various imperfections in both the hardware and software implementations that will cause the k modulated-signal constellation points, $Z_c(k)$, to deviate from their ideal locations, $S(k)$. Informally, EVM is a measure of how far the points are from the ideal locations, where, for N transmitted symbols, we have

$$\text{EVM} = \sqrt{\frac{1}{N}\sum_{k=1}^{N} |Z_c(k) - S(k)|^2}. \tag{S6}$$

Measurement Example

To illustrate the measurement of an SDR receiver, we used a mixed-domain measurement set-up such as the one presented in [39] (similar to that presented in Figure 7), as shown in Figure 8. The arbitrary waveform generator simulated the transmitted digitally modulated RF signal, and the receiver was simulated using the components shown in the block diagram. This DUT was excited with a single-user WiMAX signal in frequency-division-duplex mode with a bandwidth of 3 MHz and a modulation type of 64 QAM (3/4) [49].

Figure 9 presents the measured results at the output of the SDR receiver using the logic analyzer. This figure shows the total power averaged over the excitation band of frequencies and the total power in the upper adjacent channel arising from nonlinear distortion. This figure illustrates the mixed-mode nature of SDR testing: The analog output figure of merit ACPR has been reconstructed from the digital output and analog input signals.

We have also evaluated the performance of the DUT at a given input power in terms of EVM. The received digital WiMAX signal was demodulated and corrected in terms of gain and phase delay, and the constellation diagram shown in Figure 10 was obtained. An EVM value of approximately 5.05% was obtained in this particular measurement.

The characterization of the SDR components was only possible due to the fact that we have used a mixed-mode instrument, which allows the simultaneous characterization of the analog and digital waveforms.

Summary and Conclusions

In this article, we have presented a review of both receivers and transmitters that may be used in SDR front ends. We discussed advantages and disadvantages of each. As we saw, a well-designed architecture for a multiband multimode receiver should optimally share available hardware resources and make use of tunable and software-programmable devices. Not every receiver architecture has this feature. In that sense, in our opinion, the SDR receiver front-end will be based either on the zero/low-IF architecture or on the bandpass sampling design when it is more mature.

For the transmitter, the EER technique and its adaptations are promising choices for use in SDR applications because their efficiency is largely independent of PAPR. Thus, they may be readily applied to multistandard and multiband operation [50]. Such SDR and CR transmitter architectures will require not only highly efficient PAs but also wideband PAs [51]. The SDR community is moving from analog to digital approaches for signal transmission, and, thus, the demand for increased switching speed in RF PAs is becoming more evident and more stringent, leading in the future to class-S-based transmitters.

A well-designed architecture for a multiband multimode receiver should optimally share available hardware resources and make use of tunable and software-programmable devices.

Concerning the measurement instrumentation used to characterize SDR systems, we illustrated why mixed-domain instrumentation is essential for characterization of SDRs. We described why some improvements will have to be made in order to develop a synchronous instrument that will characterize SDR front ends rapidly, automatically, and with impedance-mismatch correction. Such an instrument would ideally provide information such as EVM for different types of modulation and adjacent channel power ratio for different technologies and would be able to test multistandard multiband radio configurations. We anticipate seeing these types of instruments on the market as SDR technology becomes more mature.

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