IMS2013 STUDENT DESIGN COMPETITION WINNER
Software-Defined Radio and Digital Signal Processing

An Agile Digital Radio System for UHF White Spaces

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In recent years, we have experienced an impressive spread of mobile communications as well as the emergence of new communication protocols. This lead to an overutilization of some spectrum bands, while the utilization of other bands is sometimes minimal or insignificant. The exploration of the white spaces concept, which represents the unused portions of the spectrum, mainly due to the shutdown of analog TV transmissions, has arisen as a solution for spectrum reuse. Currently, the electromagnetic spectrum is statically allocated, associating each technology to a particular frequency band, which leads to an inefficient use of the spectrum. Thus, it would be advantageous to change the way the electromagnetic spectrum is accessed, adopting a dynamic access paradigm—dynamic spectrum access (DSA). However, for this to be possible, in addition to regulatory changes, it is necessary that the radio physical layer becomes flexible and adaptable, enabling the efficient configuration of various parameters such as transmit frequency and power, modulation, and bandwidth, among others. The well-known concepts or paradigms of software defined radio (SDR) and cognitive radio (CR) are precisely the key to meeting these requirements. Based on these concepts, it will be possible to build a smart, adaptable, efficient, self-aware, and self-learning radio that could easily implement the DSA paradigm [1].

In this way, the main goal of the IEEE Microwave Theory and Techniques Society (MTT-S) 2013 International Microwave Symposium (IMS2013) SDR and Digital Signal Processing (DSP) Student Design Competition is to encourage training and research in SDR and DSP areas. The main criteria for judging are the innovation and success of reaching the goals that the participating teams set in any of the above areas. In this context, the system that was submitted to this contest by the Aveiro team consists of the design and implementation of a field-programmable gate array (FPGA)-based digital radio system for ultrahigh-frequency (UHF) white spaces. The operating frequencies, performance, and features of modern FPGAs make feasible the implementation of digital fully FPGA integrated transceivers with the required physical layer flexibility for CR systems targeting the white spaces frequency bands. This system should be flexible on the carrier frequency and the bandwidth of the transmitted signal. The transmission component of the system is composed of an FPGA-based all-digital transmitter, whose concept is essentially a transmitter where the data path is fully digital from the baseband to the radio-frequency (RF) stage. The receiver is based on a bandpass sampling

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approach, sampling the signal directly at the RF stage using a frequency lower than the Nyquist one. Both architectures are a close approach to the ideal SDR concept. In this project, the modulation used in the RF transmission is on-off keying (OOK), and the frequency band is within 432–434 MHz. This article presents the architecture and the implementation aspects of the system and discusses the obtained results using parameters such as bit error rate (BER) and FPGA occupation statistics.

Transmitter Architecture: All-Digital Transmitter

Traditional analog transmitters perform the RF upconversion stage by multiplying the desired signal by a sinusoidal carrier (e.g., the homodyne transmitter). In an all-digital transmitter, the data path is entirely digital up to the RF stage, which provides high flexibility.

The main architecture of an all-digital transmitter was introduced by Ghannouchi in [2] and is illustrated in Figure 1(a). The digital shaping modulation (DSM) blocks, which can be Sigma-Delta ($\Sigma - \Delta$) or pulse width modulation (PWM), receive the baseband in-phase/quadrature (I/Q) components of the desired signal to be transmitted, converting an n-bit signal representation into a 1-bit output signal. These modulation components are used to make the signal suitable for the RF upconversion process. After the modulation stage, the three digital multiplexers are responsible to modulate the 1-bit baseband signals by a square wave. The set of multiplexers will directly up convert the baseband signal to RF without passing through an intermediate frequency (IF) stage, similarly to a conventional homodyne transmitter. Nevertheless, since a square wave is being used, odd harmonics of the carrier frequency will be generated too. The filter before the antenna has the function to remove the harmonics and convert the digital signal to their analog counterpart, making the signal more suitable to be transmitted by the antenna [2], [3]. The power amplifier (PA) before the filter should be a switching-mode PA (SMPA) for increased efficiency. If a conventional (nonswitched) amplifier is used, it has to be placed after the filter with a subsequent energy-efficiency reduction.

This multiplexer-based architecture has some limitations related to its cost and tight synchronization requirements between the input data of the multiplexer and its selection signal.

It is possible to build an integrated all-digital transmitter using modern FPGA devices, which provide high logic capacity, allow efficient parallelism exploitation, and have dedicated blocks to provide special functions like DSP operations. Besides that, some FPGAs have embedded serializers, called multigigabit transceivers (MGTs), that can be used to generate an RF signal at the FPGA output. Therefore, FPGAs have a really important role in SDR, allowing the implementation of all-digital transmitters, providing them a great flexibility. In Figure 1(b), the architecture of an FPGA-based all-digital transmitter, proposed by Silva et al. in [3] and [4], is presented, solving the limitations of the previous architectures. It is possible to see that the multiplexers were replaced by two blocks [Figure 1(b)]. The first block (interconnection network) is responsible for building a parallel word (W) which have all components of signal v_i, v_q, v_i' and v_q', i.e., complementary versions of v_i and v_q, respectively) replicated by the digital up-conversion factor $N = f_c/f_s$ (where f_c is the desired carrier frequency and f_s is the sampling frequency of the base band signal). The second block is a serializer that puts the parallel word on the output at a bit rate of $4f_c$, which consequently will generate an RF carrier centered at f_c. The serializer is clocked at a frequency f_o that should ensure the bit rate at its output. The filter and PA have the same functions as previously described [3], [4].

With this kind of transmitters it is also possible to use other modulation types like amplitude shift keying (ASK)/OOK or frequency shift-keying (FSK). These modulations are less efficient than I/Q modulations, however, they allow transceivers with lower complexity as adequate to connections with low bit rates. OOK modulation simply puts "on" and "off" the carrier when it is to transmit a one or a zero, respectively. Thus, to transmit a one, it is necessary to serialize an alternate set of ones and zeros with a $2f_c$ bit rate to consequently have the carrier at f_c, which will be ready for transmission after passing through a filter. To transmit a zero, since it is represented with the carrier absence, it is necessary to serialize a set of zeros. In the FSK case, two frequencies are used, one for zero and one for one, respectively. So it is necessary two produce two OOK structures for zero and one transmission.

Receiver Architecture: Band-Pass Sampling Receiver

Typically, radio transceiver architectures perform at least one down-conversion in the analog domain using a mixer and only after that the signal is sampled and quantized by an analog-to-digital converter (ADC). Due to the increased processing capacity and the improvements in DSP techniques, it is possible to move the ADC toward the antenna in an effort to achieve the ideal SDR receiver [5].

The bandpass sampling receiver architecture is a possible approach to achieve a near-ideal SDR receiver. Before presenting it, it is important to remember the sampling process and the Nyquist theorem. This theorem refers to sampling a signal at frequency f_s, where the signal must be frequency limited by $f_s/2$, or, in other words, when sampling a signal whose maximum frequency is f_{max}, the sampling frequency must be $f_s \geq 2f_{max}$. If these conditions are not complied with there will be aliasing and the original signal will be corrupted. In Figure 2(a), two signals to be sampled are represented. The gray signal is frequency limited by $f_s/2$, and the sampled signal is represented in Figure 2(b). It is possible to see that the signal was replicated to the other Nyquist zones because the sampling process introduces a period of f_s in the

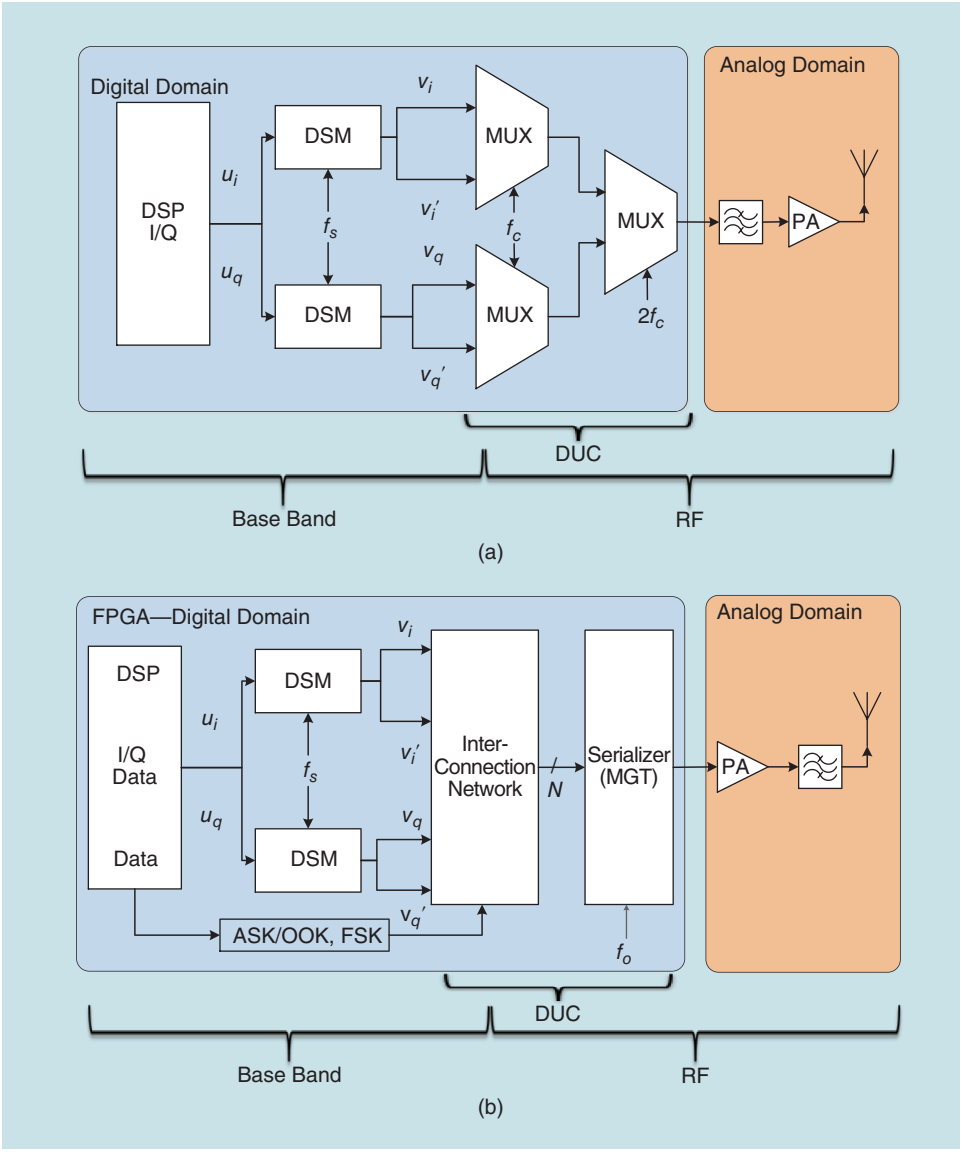

Figure 1. *(a) An all-digital transmitter concept diagram. (b) An FPGA-based all-digital transmitter block diagram. DUC: digital up-conversion [3].*

spectrum of the sampled signal. The red signal is in the third Nyquist zone, i.e., its frequency is greater than the sampling frequency. After the sampling process, this signal is also replicated to the other Nyquist zones, including the first one. So, it is possible to take advantage of the periodicity imposed by the sampling process to down-convert a signal whose frequency is greater than the sampling frequency. The frequency of the replicated signal into the first Nyquist zone (f_{fold}) is given by

$$\text{If } a \text{ is} \begin{cases} \text{even} \Rightarrow f_{fold} = f_c - 0.5af_s \\ \text{odd} \Rightarrow f_{fold} = 0.5(1+a)f_s - f_c, \end{cases} \quad (1)$$

where f_c is the carrier frequency, f_s is the sampling frequency, and a is $INT(2f_c/f_s)$, where INT represents the truncated portion of argument a [6], [7]. However, there are important aspects that need to be considered to correctly apply this technique. First, the signal bandwidth must be smaller than half of the sampling frequency ($f_s/2$). Second, the signal must be filtered before being sampled by confining it to the Nyquist zone of interest in order to avoid aliasing. Another final aspect is related to the Nyquist zone number ($a+1$). As seen in Figure 2, if the signal spectrum falls into an even Nyquist zone, its spectrum is reversed in the first Nyquist zone and digital correction needs to be applied, while if in an odd Nyquist zone, the spectrum is not reversed.

Since the concept has already been explained, Figure 3 presents the architecture of a bandpass sampling receiver. Following Figure 3, it is possible to see that after the antenna there is a bandpass filter, whose function is to limit the signal frequency to the desired Nyquist zone. This is a very important element, otherwise there might be aliasing in the sampling process. After the filter, there is a low noise amplifier (LNA) that amplifies the signal reducing the overall noise floor. Then, there is the ADC that will sample and quantize the signal at a frequency lower then the RF signal. Finally, in the digital domain, a digital signal processor will demodulate and process the received signal. Thus, it is possible to implement a receiver with an architecture fairly close to the SDR ideal concept.

This type of receiver, which samples directly the RF signal, must have an ADC whose clock signal should present a very low jitter, otherwise the ADC signal-to-noise ratio (SNR) will be degraded. The concept of jitter can be defined as the deviation of significant moments that a given signal has in relation to its ideal location in the time domain. The jitter effect in the ADC SNR is given by

$$\text{SNR}_{\text{jitter}} = 20 \times \log_{10}\left(\frac{1}{2\pi.f.t_j}\right), \quad (2)$$

where f is the carrier frequency and t_j is the aperture jitter time of the ADC clock signal [6]. Using (2), it is possible to conclude that the SNR_{jitter} gets degraded with the increasing of the aperture jitter time (t_j) and the carrier frequency (f) [6].

Transmitter Implementation

The proposed scheme presented in the competition was based on an audio transmitter for easier demonstration of the system operation.

Figure 4 presents a block diagram representation of the implemented transmitter. It is possible to see that the diagram starts with the audio sampling and consequently storing the samples in a memory. After that, a block called Framer will read the memory and build a transmission frame. This transmission frame is composed of a header and a payload. The header is composed of two fixed bytes, which are useful in the receiver for synchronization purposes. The payload is made from 128 bytes of audio samples. After composing the transmission frame, the block Framer serializes the frame bit by bit to the multiplexer selection line $-Tx$ bit (Figure 4). Thus, to transmit a one, the multiplexer puts in its output a parallel word (W) composed by an alternate set of ones and zeros. Then the MGT will serialize the parallel word W at a bit rate of $2f_c$ to consequently have the carrier at f_c. To transmit a zero, the MUX puts in its output a parallel word made only from zeros, corresponding to the carrier absence. As already mentioned, the RF analog section is composed of a bandpass filter that has the function to remove the harmonic frequencies of the generated square wave, making the signal suitable to be transmitted by the antenna after passing through the PA.

To implement the digital component of the system, a XUPV5 development board manufactured by Xilinx was used. This development board contains an FPGA Virtex 5, which has enough logic capacity to implement the digital component of the system, contains audio inputs/outputs, and also contains SMA connectors for the MGT where the RF output is generated.

It is intended for the system to be flexible in terms of transmission bit rate and frequency. Concerning the transmission frequency, this is done by varying the MGT clock signal that consequently will produce a variation in the bit rate at the serializer output, which changes the carrier frequency. With the existing clock signals in the XUPV5 board, it is possible to generate four different carriers at 432, 433.3, 433.8, and 434.2 MHz. The transmission bit rate is varied, changing the rate of the multiplexer selection line $-Tx$ bit. The block Framer is synchronous with the block serializer using the signal user clock. This signal is a submultiple of the carrier frequency, and the

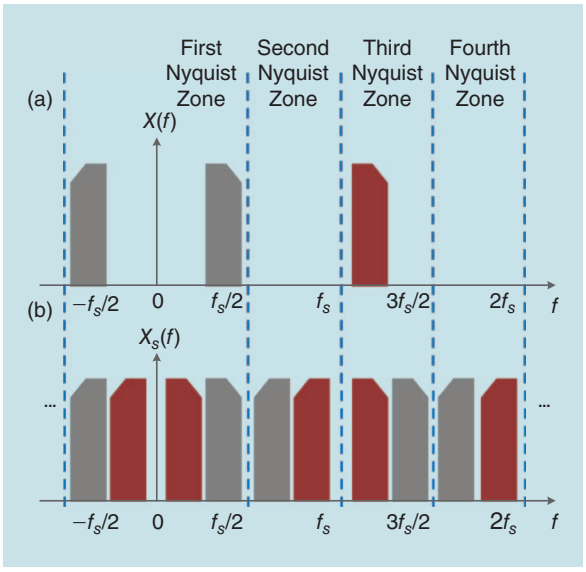

Figure 2. *Frequency domain representation of the sampling process. (a) Signal to be sampled. (b) Sampled signal.*

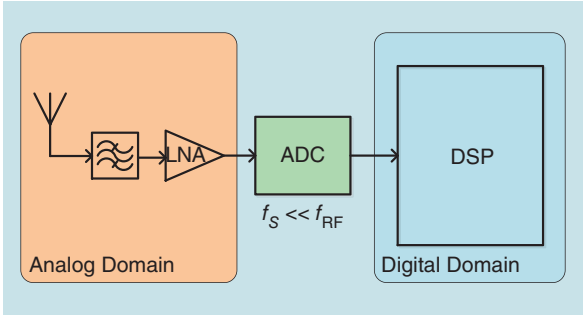

Figure 3. *Bandpass sampling receiver architecture [6], [7].*

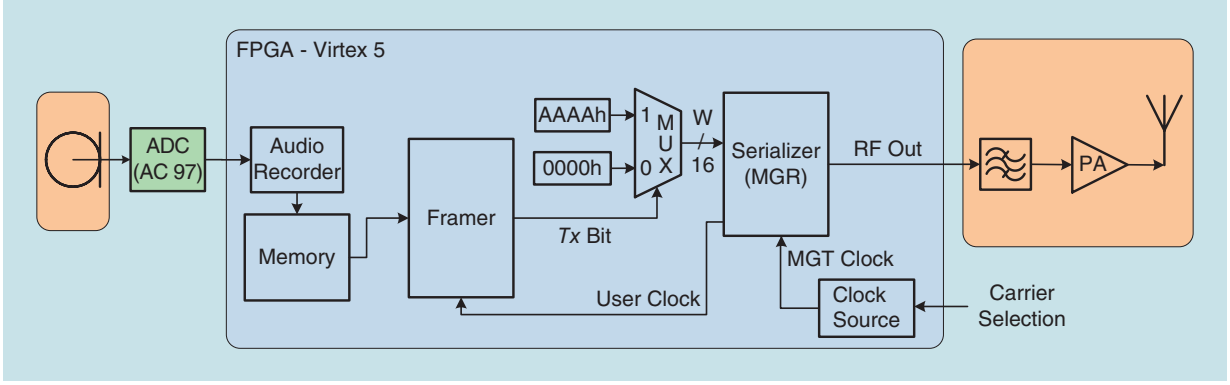

Figure 4. *A block diagram of the implemented transmitter.*

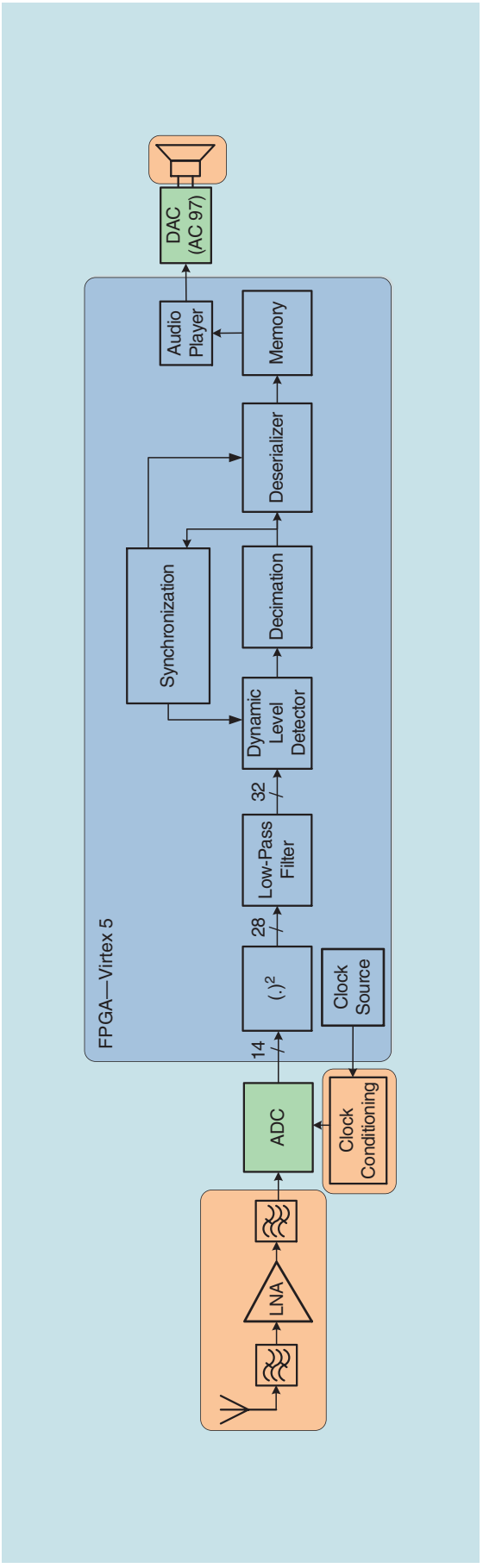

Figure 5. *A block diagram of the implemented receiver.*

Framer block uses it to make a counter that defines the transmission bit rate.

Receiver Implementation

Figure 5 presents the block diagram of the entire receiver architecture. Starting with the analog component that is more complex than it was for the transmitter, it is possible to see that, after the antenna, there is a bandpass filter. As already mentioned, the bandpass filter limits the signal to the Nyquist zone of interest. After the filter, there is an LNA to increase the signal power with low values of added noise, another filter to attenuate some possible distortion, and, finally, the ADC. The used ADC has 14 bits and has a sampler working at 40 MHz, which imposes that the RF signal is sampled at the 21th Nyquist zone. The clock signal given to the ADC comes from the FPGA. This signal passes through a block called "clock conditioning" to filter and amplify the signal before going to the ADC.

After sampling, in the digital domain, an envelope detector made by a squarer and a low-pass filter is implemented. In the low-pass filter output, there is an envelope that is represented in 32 bits. Thus, to recover the transmitted signal, it is necessary to convert this envelope into a one-bit square wave, and it is also necessary to reduce its bit rate. This function is done by the group operation of the block dynamic level detector, decimation, and synchronization. The block dynamic level detector converts the envelope to a square wave, applying a dynamic threshold that allows the radios to be separated by different distances. The block decimation reduces the sample rate to the baseband rate of the signal. Then, the block synchronization analyzes the decimation block output, looking for the frame's header. When it finds the header, this block acknowledges the dynamic level detector block. The block deserializer also receives the acknowledgement, knowing that it can start saving the data into a memory. Finally, the block audio player is responsible for reading the received data from the memory and sending the data to reproduction to the AC 97 codec digital to analog converter (DAC).

Measurement Results

Figure 6 presents a photo of the developed system. As has already been stated, the system is flexible regarding the carrier frequency, in this case, four frequencies are available for transmission: 432, 433.3, 433.8, and 434.2 MHz. Concerning the transmission bit rate, the system is also flexible, as it is possible to choose any bit rate. However, the BER will increase with the bit rate, as is illustrated in Figure 7. This increasing bit rate is related to the decreasing of the time period when the carrier is on, being more difficult to detect its presence.

The digital component of the system was implemented with a low occupation of the FPGA logic resources (lookup tables and flip-flops), 1 and 2% in the transmitter and receiver, respectively.

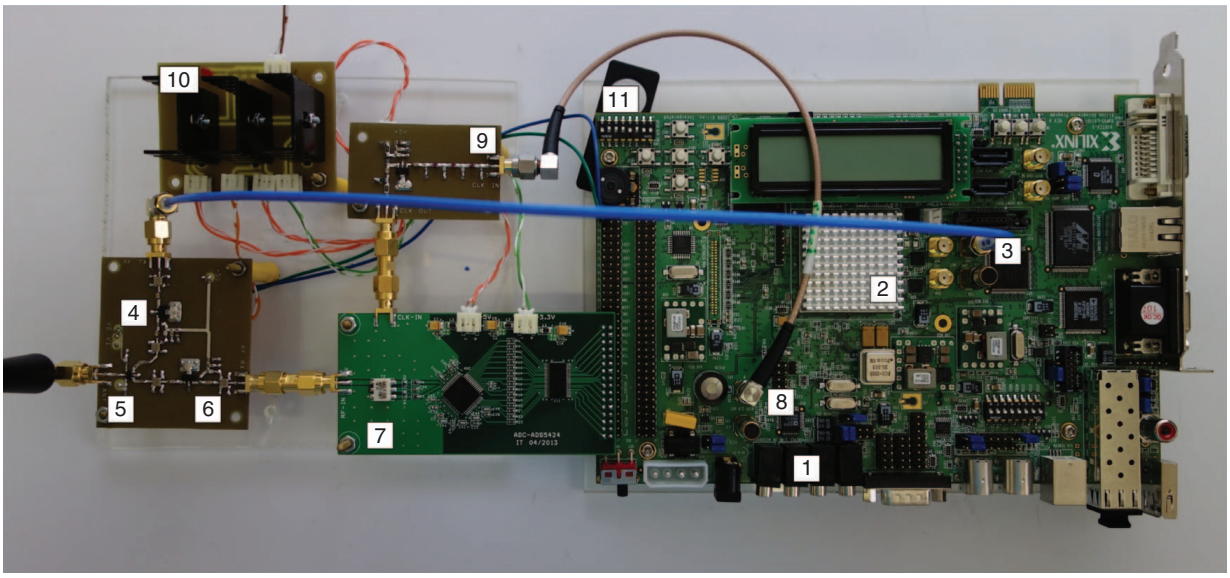

Figure 6. *The system prototype. 1: The audio in/out, 2: virtex 5 FPGA, 3: RF output, 4: PA, 5: antenna, 6: LNA, 7: ADC board, 8: ADC clock source, 9: ADC clock conditioning board, 10: power sources, and 11: carrier selection.*

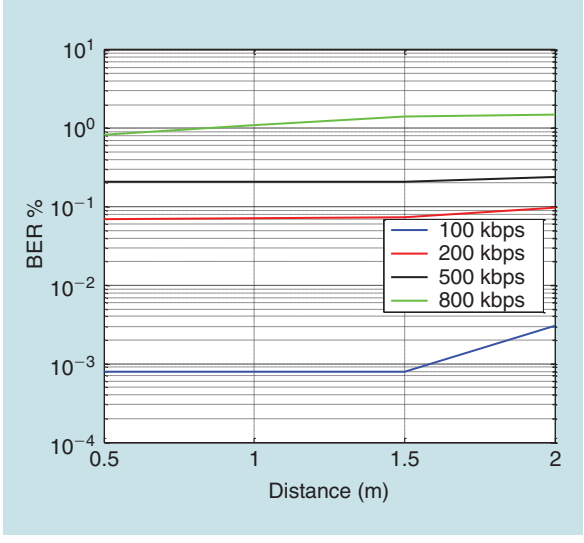

Figure 7. *The system BER as a function of distance and transmission bit rate.*

Another aspect that has been achieved is related to the interoperability between the implemented transmitter and a commercial transceiver using the same modulation and frequency.

Conclusion and Future Work

In this article, an agile digital radio system for UHF white spaces was presented. This system implements SDR architectures, which are very close to the ideal concept and is flexible in terms of the carrier frequency and transmission bit rate. The system was implemented in an FPGA with low occupation of logic resources, which highlights its importance and feasibility of SDR, allowing its integration on moderate capacity devices and the integration with upper network layers functionalities.

For future work, it would be important to add more modulation schemes giving the system one more degree of flexibility. Another important aspect is the use of an external programmable clock generator that could be used to generate a carrier frequency with more flexibility, more precision, and lower jitter.

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