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Design Of A Power Amplifier Based On Si-LDMOS For WiMAX At 3.5GHz

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Abstract

The aim of this thesis work was to design a power amplifier for WiMAX applications at 3.5GHz based on cheap Si-LDMOS technology and to analyze the behavior of the design regarding nonlinear distortions and memory effects.

A MW6S004NT1 Si-LDMOS RF high power transistor, from Freescale, with an ADS MET model was used in the process. This transistor is specified for Class A-AB base station applications with frequencies up to 2GHz. However, we will investigate the capability of using it at WiMAX frequency.

The first step in the work consisted of designing a highly linear Class A power amplifier which achieves the highest output power, efficiency and gain. Load-pull analysis and Pout-PAE optimizations were used in the ADS simulations. The implemented design showed a different behavior than the ADS one, with mismatch problem at the output, a shifted DC bias and a high self heating. After adjustments, the PA showed an acceptable gain of 6 dB, but the achieved output power and efficiency were limited in value for base station use.
The main reasons behind this behavior were the non ideality of the used ADS model, the big size of the transistor and the internal feedback in the package which, at the work frequency, caused a positive feedback in the performance, and a high mismatch certainly at the output.

The next step consisted on redesigning the PA using ADS, despite the non ideality of the model. Several adjustments have been added to the matching and bias networks of this design to improve his performance. The implemented design showed an improved gain of 10.5 dB near the P1dB compression point; however the achieved output power and efficiency at that point were much lower.

The final step in this work consisted of analyzing the behavior of the first design regarding nonlinearity and memory effects for different classes of operation. ADS simulations and measured results were used in the process.
The design showed a low performance regarding intermodulation distortions for class A. However by changing the bias to a class AB operation, the intermodulation distortion rejection was in the range of 39 dBc which is a good value regarding the WiMAX standards (32 dBc). Regarding the memory, the design showed low memory effects or a memoryless behavior with a maximum effect of 1.3 dB.

Despite the output mismatch problem, this cheap transistor has shown a good power performance comparable with the GaAs technology. Extracting the S-parameters and improving the ADS model will be an interesting future work in order to achieve a matched design with better power performance.

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Glossary of Acronyms

ACPR: Adjacent Channel Power Ratio
ADS: Agilent EEsof Advanced Design System
AM: Amplitude Modulation
AN: Accessories Networks
BER: Bit Error Rate
BN: Bias Network
BPSK: Binary Phase Shift Keying.
BS: Base Station
CMOS: Complementary Metal-Oxide Semiconductor
CAD: Computer Aided Design
DSL: Digital Subscriber Line
DSP: Digital Signal Processing
EVM: Error Vector Magnitude
FET: Field Effect Transistor
GaAs: Gallium Arsenide
HB1Tone: Harmonic Balance 1Tone
HB2Tones: Harmonic Balance 2Tones
HFDD: Half Duplex Frequency Division Duplexing
IEEE: Institute of Electrical and Electronics Engineers
IP3: Third Order Intercept Point
IMN: Input Matching Network
IMR: Carrier to Intermodulation Ratio
LAN: Local Area Network
LNA: Low Noise Amplifier
MAC: Medium Access Control
MAG: Maximum Available Gain
MAN: Metropolitan Area Network
MET: Motorola's Electro Thermal
MOS: Metal Oxide Semi-conductor
NLOS: Non-Line Of Sight

OC-x: Optical Carrier Level
OFDMA: Orthogonal Frequency Division Multiple Access
OMN: Output Matching Network
PAE: Power Added Efficiency
PDA: Personal Digital Assistant
PHY: Physical Layer
QAM: Quadrature Amplitude Modulation
QPSK: quadrature phase shift keying
RF: Radio Frequency
Ropt: Optimal Resistance
Si-LDMOS: Silicon Laterally Diffused MOSFET
SNDR : Signal to Noise plus Distorsion Ratio
SSB: Single Side Band
Tx/Ex: Transmit/Exchange
WiMAX: Worldwide Interoperability Microwave Access
WLAN: Wireless Local Area Network
WMAN: Wireless Metropolitan Area Network
WPAN: Wireless Personal Area Network
WWAN: Wireless Wide Area Network

Chapter1. Introduction

1.1 Background

Progress and technology are of the basis of the human life; however, what advantages will they present if they are not accessible at reasonable cost. Solving this issue is the aim of scientists.
Today, we are experiencing the power of DSP techniques through many wireless radio frequency (RF) communication applications. Wireless Wide Area Networks (WWANs), Wireless Metropolitan Area Network (WMANs) or WiMax, Wireless Local Area Networks (WLANs), and Wireless Personal Area Networks (WPANs) all employ sophisticated communication techniques. Some of these techniques include complex modulation schemes, powerful new error-correcting codes, decoding algorithms to combat the effects of channel fading, and so on.

Until recently, WiMAX systems have used technology processes such as Gallium-Arsenide (GaAs) to obtain the performance needed from the RF circuits. Although these technologies provide the functional performance required by radios today, they do not support the cost/scalability business model.

But as the MOS technology is being developed, certainly with CMOS and LDMOS, more research is currently investigating the use of these technologies in radio frequency systems, such in power amplifiers, for frequencies upper than 2GHz, certainly as they present acceptable cost.

The higher switching speeds that result from the smaller geometries being developed in MOS are enabling the design of analog circuits at very high frequencies, within a limit, with very good gain and linearity. It is this new frontier where Intel Labs is focusing research on the design of analog RF circuitry, which utilizes the CMOS or LDMOS technology.
Analog solutions implemented in Si-LDMOS will achieve high performance, functionality, and bandwidth while maintaining low cost, high quality, and robust architecture across the wireless market.

In fact, Silicon Laterally Diffused MOSFET (LDMOS) transistor is widely used in mobile base stations at 0.9 and 1.8(1.9) GHz due to its high power performance and linearity. The high RF output power is due to the new design for a higher DC breakdown voltage of typically 70-75V.

1.2 Objective

High efficiency and good linearity are among the very important characteristics of a base station power amplifier used in majority of the modern applications such as WiMAX.
Both characteristics have always been conflicting requirements which demand innovative power amplifier design techniques. Maintaining the high efficiency attained, over a wide range of the power amplifier operation, and achieving a high output power level are an added requirements in these applications making power amplifier design a challenging task.
Spectrum is expensive, and newer technologies demand transmission of maximum amount of data using the minimum amount of spectrum. This requires sophisticated modulation techniques, such as quadrature phase shift keying (QPSK), leading to wide, dynamic signals that require

linear amplification. Although linear amplification is achievable, it always comes at the expense of efficiency.

Till now power amplifiers have been designed to fulfil the demands of WiMAX system, usually using Gallium-Arsenide (GaAs), but it comes at the expense of the cost. To solve this issue, current researches are investigating the possibility of using cheaper technologies such as Si-LDMOS.

In the light of the above, it is desirable to evaluate the capability and design a power amplifier based on a Si-LDMOS transistor at 3.5 GHz relying on the WiMAX specifications.

1.3 Report Outline

This report has three major goals: first, to provide the reader with an introduction on the principles of power amplifier designs; second, to design and simulate a power amplifier based on a Si-LDMOS transistor at 3.5 GHz relying on the WiMAX specifications; and finally to study the behaviour and power performance of the implemented design regarding bias, class changes and memory effects.
The thesis report is organized as follows:

Chapter 2 gives an introduction to WiMAX system. It describes its properties and presents its specifications for power amplifier design.

Chapter 3 gives a brief introduction to Si-LDMOS technology. It describes its characteristics and its advantages over other technologies.

Chapter 4 is a theoretical chapter; it is divided into three parts. The first one describes the operation classes used in amplifier designs. The second describes deeply the properties of power amplifiers. The last part deals with bias and matching networks used when designing power amplifiers.

Chapter 5 describes the steps used in designing the power amplifier and presents all the simulations done in ADS in order to optimize the design and to study his performance.

Chapter 6 is an industrial chapter; it is divided in two parts. The first one deals with the manufactured design and gives a brief overview of his results. The second part presents all the changes made to the design in order to adjust it for better performance and studies its measured power performance.

Chapter 7 describes all the steps used in order to design a second power amplifier to achieve a better power performance. It presents all the steps and simulations done in ADS to achieve that design. Finally it describes the results obtained from the implemented design.

Chapter 8 is a research chapter; it is divided in two parts. The first one describes the new operation's class definition used. Also it gives simulation and measured results of these classes. The second one gives a deep explanation of memory effects in a power amplifier system. Also it gives simulations and measured results of these effects.

Chapter 9 is a conclusion chapter that provide a brief overview of the achieved results and give a general idea for a future work to be investigated.

Chapter2. WiMAX

2.1 Introduction to WiMAX

Worldwide Interoperability Microwave Access, WiMAX, also known as IEEE 802.16, is a wireless digital communication system that is intended for wireless metropolitan-area network technology that provides interoperable broadband wireless connectivity to fixed, portable and nomadic users. It provides up to 50-kilometers of service area for fixed station, 5-15 Km for mobile station, allowing users to get broadband connectivity without the need of direct line-of-sight to the base station, and provides total data rates up to 70 Mbps enough bandwidth to simultaneously support hundreds of businesses and homes with a single base station.

In fact, the term WiMAX has become synonymous with the IEEE 802.16 Wireless Metropolitan Area Network (MAN) air interface standard [1]. In its original release the 802.16 standard addressed applications in licensed bands in the 10 to 66 GHz frequency range. Subsequent amendments have extended the 802.16 air interface standard to cover non-line of sight (NLOS) applications in licensed and unlicensed bands from 2 to 11 GHz bands, or WiMAX. This is an enormous spectrum range; however the practical market considerations dedicated that the 3.5GHz spectrum will be the first to enjoy WiMAX products, than it will be followed in the future by the 2.5 and 5.8 GHz spectrums. The WiMAX-compliant systems will provide a cost-effective broadband access to users at home, in the office, in areas under-served by wire-line DSL and cable services and even to users on the pause or on the move equipped with portable devices like laptops, PDAs and smart-phones.

2.2 WiMAX Properties

2.2.1 WiMAX Air Interface

WiMAX is a worldwide certification addressing interoperability across IEEE 802.16 standards-based products [1]-[3]-[4]-[5]-[6]. The IEEE 802.16 addresses two usage models:

- Fixed
- Portable

Fixed model
The fixed access model was introduced in the IEEE 802.16-2004 standards. It is a fixed model because it uses a mounted antenna at the user's site. It is a wireless solution for fixed broadband Internet access that provides an interoperable, carrier-class solution for the last mile. This wireless technology presents an efficient replacement to the cable modem, digital subscriber lines (DSL), transmit/exchange (Tx/Ex) circuits and optical carrier level (OC-x) circuits.
The modulation technique used in WiMAX systems and optimized for non-line-of-sight transmission is OFDM which will optimize the wireless data services. In the WiMAX air interface, the basic OFDM symbols are based on a 256 point, bandwidths that range from 1.25 MHz to 20 MHz, and carrier frequencies up to 11 GHz.
As with other OFDM systems, a portion of these 256 subcarriers are set aside (unused) for guard bands and the centre frequency subcarrier is not used because it is easily susceptible to RF

carrier feed through. In WiMAX, only 200 subcarriers are actually used. These 200 carriers are allocated as 192 carriers for data and 8 carriers as pilots. The pilot carriers are always BPSK modulated and the data carriers are BPSK, QPSK, 16 QAM or 64 QAM with multiple code rates and envelope types (constant or varying depending on the pulse shape of the signal).

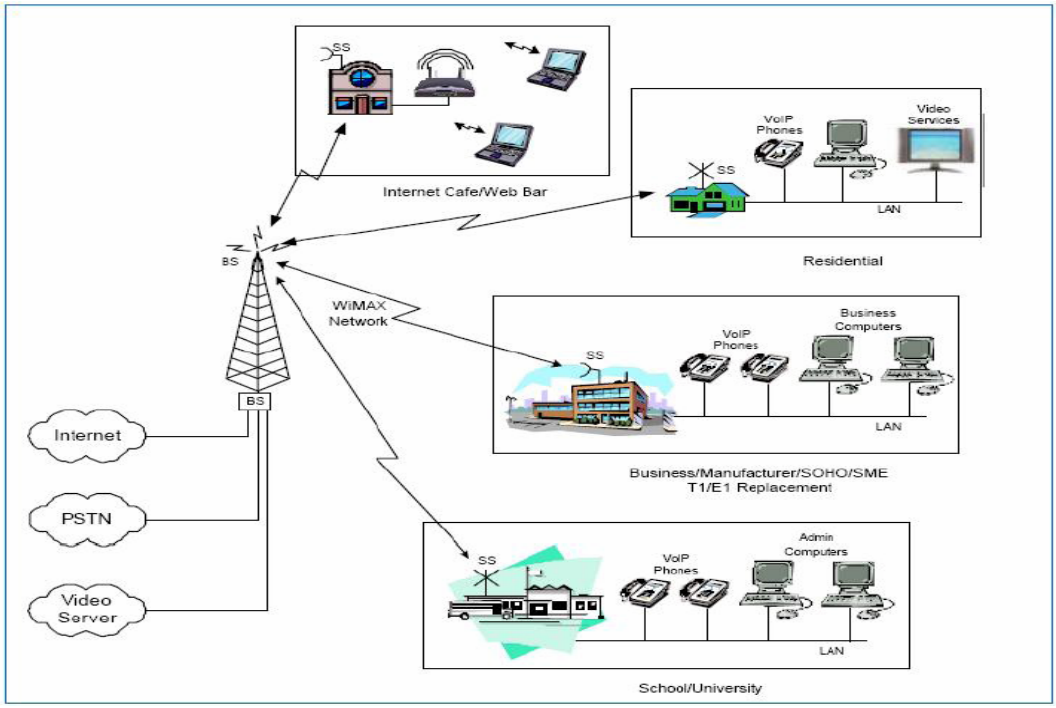


Figure 2.1: WiMAX network topology [2].

Portable model

The IEEE 802.16e standard is an enhancement of the 802.16- 2004 base specification and targets the mobile market by allowing mobile clients with adapters to connect directly to the WiMAX network. The 802.16e standard uses Orthogonal Frequency Division Multiple Access (OFDMA), which is similar to OFDM in that it divides the carriers into multiple subcarriers. OFDMA, however, goes a step further by grouping multiple subcarriers into sub-channels. In fact, a single user might transmit using all of the sub-channels within the carrier space, or multiple users might transmit with each using a portion of the total number of sub-channels simultaneously.

The OFDMA technology supports multiple modulation schemes depending open the users range from the cell. User at closer range will receive signals across more sub-channels at, for example, 64 QAM, whereas a user at greater range would receive signal across fewer sub-channels (with higher gain or power per channel) using a lower bandwidth QPSK technique for example.

WiMAX have improved the last-mile delivery in several key aspects:

- Multi-path interference
- Delay spread

Multi-path interference and delay spread improve performance in situations where there is no direct line-of-sight (NLOS) path between the base station and the user station.

In fact, the system can be configured to use any bandwidth from 1.25 MHz to 20 MHz and regardless of the bandwidth; the symbols always contain 200 carriers. For narrow bandwidth systems, this implies the subcarriers are very closely spaced, which provides a relatively long symbol period (symbol period is defined as 1 / subcarrier spacing). These closely spaced

subcarriers and long symbols help overcome channel impairments such as multipath. This long symbol period is a key differentiator between WiMAX systems and wireless LAN systems (relatively short symbols), which provides WiMAX with significant advantages for long distances and non-line of-sight applications.
However, these narrow subcarriers, which are equivalent to larger symbol periods, will implement the use of more sophisticated technique in the analogue RF circuits to prevent the interference between the narrow adjacent channels.

2.2.2 Flexible Channel Bandwidth

As the distance between a subscriber and the base station (or AP) increases, or as the subscriber starts to move by walking or driving in a car, it becomes more of a challenge for that subscriber to transmit successfully back to the base station at a given power level. For power-sensitive platforms such as laptop computers or handheld devices, it's often not possible for them to transmit to the base station over long distances if the channel bandwidth is wide. The 802.11 channel bandwidth is fixed at 20 MHz. In contrast, applications modelled on third-generation principles limit channel bandwidth to about 1.5 MHz to provide longer range.
The IEEE 802.16-2004 and IEEE 802.16e standards have flexible channel bandwidths between 1.25 and 20 MHz, (20-25 MHz for USA, 28 MHz for EU), to facilitate transmission over longer ranges and to different types of subscriber platforms.
In fact, the 802.16-2004 standards keep more users connected by virtue of its flexible channel widths and adaptive modulation. Because it uses channels narrower than the fixed 20 MHz channels used in 802.11, the 802.16-2004 standards can serve lower data-rate subscribers without wasting bandwidth. When subscribers encounter noisy conditions or low signal strength, the adaptive modulation scheme keeps them connected when they might otherwise be dropped.

2.2.3 Benefits and Challenges

The WiMAX standard relies upon a grant-request access protocol that doesn't allow data collisions and, therefore, uses the available bandwidth more efficiently. No collisions mean any loss of bandwidth due to data retransmission. All communication is coordinated by the base station. Other characteristics of the WiMAX standards include:

• Higher quality of service— The WiMAX standard enables Wireless Internet Service Providers (WISPs) to ensure good QoS for customers that require it and to tailor service levels to meet different customer requirements. For example, it can guarantee high bandwidth to business customers or low latency for voice and video applications, while providing only best-effort and lower-cost service to residential Internet surfers.

• Full support for WMAN service—The WiMAX standard was designed to provide WMAN service. Hence, it is able to support more users and deliver faster data rates at longer distances.

• Robust carrier-class operation—The standard was designed for carrier-class operation. As more users join, they must share the aggregate bandwidth and their individual throughput decreases linearly. The decrease, however, is much less dramatic than what is experienced under 802.11.
This capability is termed "efficient multiple access."

•Smart antenna support—Smart antennas are being used to increase the spectral density (that is, the number of bits that can be communicated over a given channel in a given time) and to

increase the signal–to–noise ratio for WiMAX. Because of performance and technology, WiMAX standards support several adaptive smart antenna types, including:
-Receive spatial diversity antennas
-Simple diversity antennas
-Beam-steering antennas
-Beam-forming antennas

The most significant challenge is that WiMAX is a new technology with emerging support, so the future research will focus on the way to make this technology available to subscribers at high performance and a reasonable cost.

2.3 Power amplifier for WiMax

One of the most important parameters in a RF system is the power amplifier [7]. In fact, at the transmitter side in a base station, a power amplifier is established to improve the signal power and allow farther distance transmission within some limits.
The growth in wireless communications and radar applications has put greater demand on the performance of power amplifiers (PAs). In the recent years, lower microwave frequency, from 800 MHz to 2.5 GHz, has dominated the commercial wireless market. Figure 2.2 shows only some of the main applications in this frequency band.

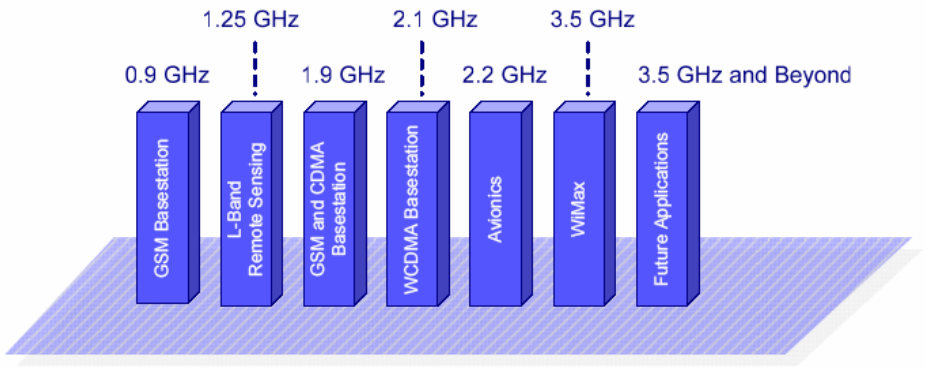


Figure 2.2 Applications of power amplifiers in low microwave frequency [7].

The rapid growth in device technologies and processing technologies presents new opportunities to power amplifier designers. In today's technology, a commercially available package of a push-pull pair of two transistors can output over 200 W at 2 GHz for base station applications. Newer applications, such as WiMax, are also emerging and high power amplifiers are needed in the hundred watt level beyond 2.5 GHz. This opens up possibilities to achieve wireless communications for longer range, better quality and cheaper cost.

Wideband digital modulation, used in WiMax systems, requires a high degree of linearity certainly when using varying envelope modulation. However, linearity implies higher power consumption and lower efficiency. For WiMAX, a power amplifier can work at 4 to 5% efficiency for about a 6 dB backoff from output P1dB. Such a backoff results in about a 2.5% Error Vector Magnitude (EVM) or 32 dBc of Signal to Noise plus Distortion (SNDR). With a class AB Power Amplifier (PA) the efficiencies can run as high as 15 to 18% with similar EVM numbers. Output powers for WiMAX system are not specified exactly, they vary with the system applications, with the modulation type, with the radius and conditions of the covered area. IEEE Standards 802.16-2004 present a wide explanation and specification for different power limits (an average value of a BS WiMAX PA is »29 dBm).

Another important parameter in PA is settling time. When a PA is switched on from cold the power level will overshoot (or undershoot), then settle out. This settling time can be as poor as 100s of msec to get within 0.1 dB of the final value. For OFDM symbols [7], the RX has to estimate the power of a tone from the beginning of a frame to the end of a frame. If there is a droop of power from the beginning to the end of >0.1 dB across the frame, the BER for 64 Quadrature Amplitude Modulation (QAM) will increase. The primary cause for this power droop is that the bias circuits and the output power Field Effect Transistor (FET) are at thermally different points. Since this phenomenon is thermal the effect can last 100s of msec.

To mitigate power drop the bias circuits have to be placed as close to the output FETs as possible so they see the same temperature. In some cases the PA may have to be turned on ahead of the TX cycle to allow the PA to stabilize and remove some of the droop. This implies having a trigger signal based on when data are to be transmitted. Having the MAC and PHY realize this trigger is not a simple matter. The budget of 100 usec for HFDD is taken up by the synthesizer settling and any PA turn-on issues. A possible solution is to design the PA so that the PA settling is <5 usec.

Finally, power amplifiers must present a cost/scalability business model. In fact PAs must provide the functional performance required by the sophisticated communication techniques, such as complex modulation schemes, powerful new error-correcting codes, decoding algorithms to combat the effects of channel fading, and so on, and at the same time they should be available to the market at a reasonable cost.

As the RF challenges mount so do the costs of the Radio. For WiMAX to be successful, the cost versus performance equation has to be balanced carefully.
Until recently, WiMax applications have used technology processes such as Gallium-Arsenide (GaAs) to obtain the performance needed by the power amplifier. The major disadvantage of these transistors is their expensive cost.
To solve this issue, deep investigations are taking their way in studying the use of the Si-LDMOS technology in designing such PAs, due to their cheap cost and good performance in a certain frequency range.

Chapter3. Si-LDMOS Transistor

3.1 Si-Lateral Diffused MOSFET (Si-LDMOS)

In our days, the LDMOS transistor has been increasingly used for RF power amplification in wireless telecommunication systems. The LDMOS devices exhibit some interesting properties such as, better linearity and a negative temperature coefficient. It is therefore today the dominating device in base station amplifiers for mobile telephone systems. The supply voltage for these applications is usually in the region 26-28 V. Some features of LDMOS transistors are described below [8]:

-For high drain current, the LDMOS have high input impedance, and a low negative temperature coefficient.

-LDMOS presents a good thermally stability.

-LDMOS devices have low intermodulation distortion (IMD).

-In addition, LDMOS has a high power gain due to quite low source inductance and low feedback capacitance.

However, this technology presents some disadvantages. One of them is the sensitivity of the gate to electrostatic charges. Second, at higher temperature the output power is reduced due to decreasing of transconductance; and also the size of the die which is big and may introduce some design's and implementation's problems.

In the following, we will present briefly the structure and properties of a Si-LDMOS transistor.

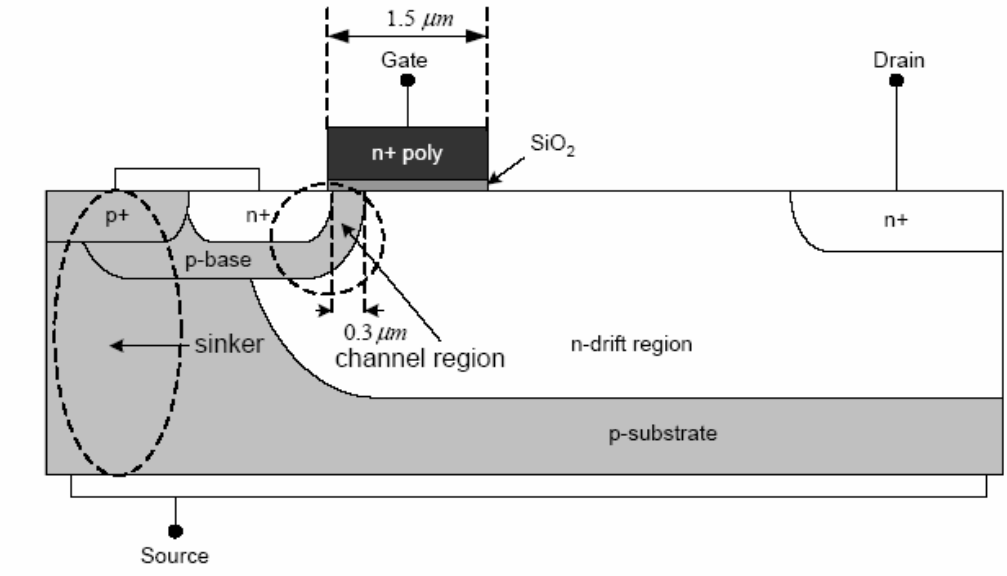


Figure 3.1 LDMOS structure [9].

3.2 LDMOS features

The general structure of a Si-LDMOS transistor is shown in Figure 3.1. The drift region consists of a n-well diffusion in an epitaxial p-substrate. In the n-well the buried p-layer and the surface n-layer are placed between the highly doped drain contact and the polysilicon gate. The buried p-layer is connected to ground outside of the active area. The channel region is formed by lateral diffusion of a p-base implantation. The polysilicon gate length is 1.5 μm and the channel length is measured to 0.3 μm [9].
The LDMOS is a transformed low power MOSFET transistor. The LDMOS structure present several features which improve his RF and power properties from a low power MOSFET transistors. The LDMOS has a low doped and quite long n-drift region, which enhances the depletion region (Figure 3.1). The beneficial result of that is the improvement of the breakdown voltage which can reach 110V. On the other hand the consequence of that is a higher on-state drain resistance, which degrades RF performance. So the approach is a trade-off between the breakdown voltage and speed.
The short channel of LDMOS is created by the lateral diffusion of a p-type implantation (p-base in Figure 3.1), which enhances his RF performance. The sinker principle is widely used for lateral power devices; its advantage is to decrease the number of contacts that makes LDMOS easier to integrate. The bulk–source connection eliminates the extra surface bond wires which reduce the source inductance, and so improve the RF performance.

3.3 RF properties of Si-LDMOS

In a Si-LDMOS transistor, the length of the channel region determines the properties of the system at high frequency. In fact, the shorter channel length improves the linearity since the transistor always works in velocity saturation. In high frequency operation, telecommunication applications such as WiMax, GaAs based HEMT and MESFET are used due its higher saturation velocity compared to Si.
Currently an interest is growing towards Si-LDMOS technology in communication area due to its cost/scalability business model. Since Si is a developed material, the structure of LDMOS gives an excellent high power characteristics, linearity, power gain and offers a wide range of frequency in the order of GHz. The recent investigation shows an improvement in RF characteristics of Si-LDMOS, which surpass BJT and even approaches to SiC-MESFET performance.

For this reason, in the following chapters we will study and design a power amplifier based on Si-LDMOS, operating at 3.5GHz specific for WiMax applications.

Chapter4. Power Amplifier

In this chapter we will describe the theory behind power amplifier designs in depth. First we will investigate the operation classes of amplifiers, certainly class A, AB, B and C. Then the properties of power amplifiers are discussed, certainly the output power, efficiency, gain, linearity and stability.
Finally, we will explain the steps that should be followed to design a class A power amplifier, especially the bias network and the input-output matching network.

4.1 Operation classes

Choosing the bias point of an RF Power Amplifier can determine the level of performance ultimately possible with that PA. In certain applications, it may be desirable to have the transistor conducting for only a certain portion of the input signal. The comparison of PA bias approaches evaluate the trade-offs for: Output Power, Efficiency, Linearity, or other parameters for different applications.
In order to operate a transistor for a certain class, the gate and drain DC voltages have to be biased carefully to certain operation point (quiescent point or Q-point), regarding the desired class. The reason is that the choice of q-point greatly influences the linearity, power handling and efficiency. In addition, as can be seen further, the choice of optimal q-point is limited by a safety region which prevent the transistor from being heated badly and damaged. Details on operation classes can be found in [10]-[11].
Figure 4.1 shows typical classes that are chosen according to specific requirements.

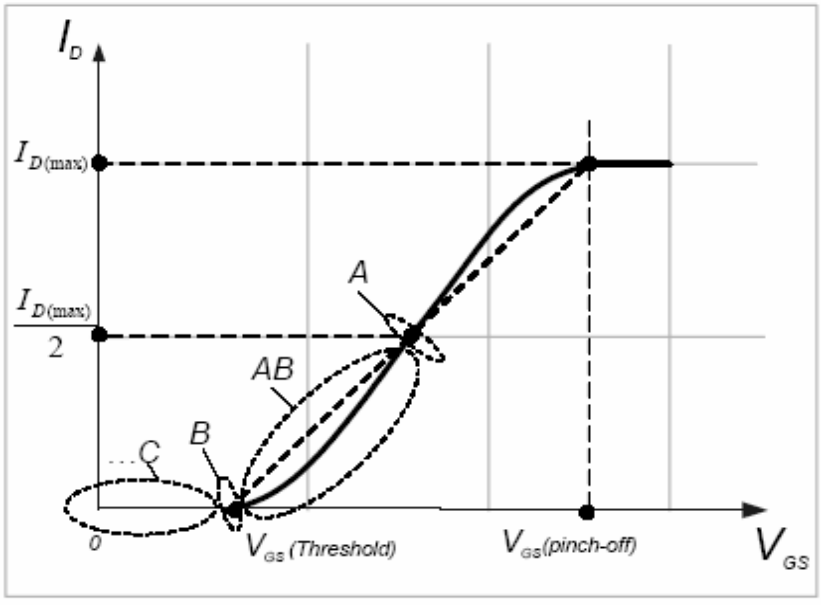


Figure 4.1 Classes of power amplifier [10].

4.1.1 Class A

The most simplistic way to distinguish the amplifiers classes is the conduction angle. Class-A amplifiers have a conduction angle of $\theta_C=2\pi$; Class-AB amplifiers have a conduction angle of $\pi<$

$\theta_C<2\pi$; Class-B amplifiers have a conduction angle of π; Class-C amplifiers have a conduction angle of $\theta_C<\pi$. Figure 4.2 shows the voltage and waveforms of a Class-A amplifier. Class-A PA is the most linear of all amplifier types, where linearity means simply how closely the output signal of the amplifier resembles the input signal. In fact, linear amplification is required when the signal contains AM – Amplitude Modulation or a combination of both, Amplitude and Phase Modulation (SSB, TV video carriers, QPSK, QAM, OFDM). However, the biggest drawback of the Class-A amplifier is the ideal maximum efficiency of 50%. This efficiency number, in practice, is reduced significantly to about 35%.

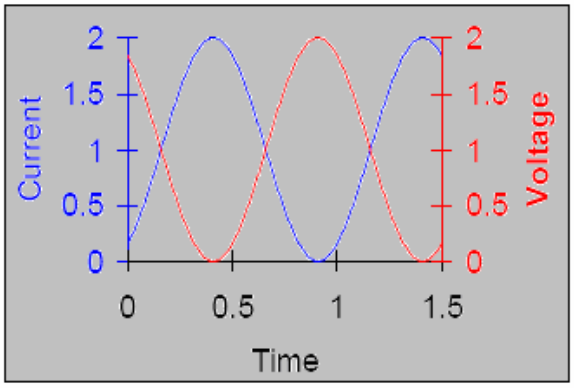


Figure 4.2 Class-A voltage and current waveforms [10].

Class A amplifiers are not suitable for high power amplifier due to their high power dissipation which is well beyond the heat-handling capability of a common-source transistor package.
In today's technology, the use of Class-A amplifiers is only popular at high microwave frequency beyond 5 GHz up to millimetre-wave territory. The advantage of the Class-A amplifier at higher frequency range is that it requires considerably less drive power and has higher gain than other classes of power amplifiers. Since at higher frequency, the power gain is usually the limiting factor in PA design, Class-A is much more suitable.

4.1.2 Class AB

The voltage and the current waveforms of a Class-AB amplifier are shown in Figure 4.3. Since the gate bias level is reduced from Class-A amplifier, the current clipping occurs.
Although current clipping generates harmonics and nonlinear effects, Class-AB amplifiers are popular candidates in power amplifiers designs. In fact, the transistor response of class-AB is wider than for class-B due to the operation point, and its power efficiency is higher than for class-A. So class-AB is shown as a compromise between linearity and efficiency. Many base station-PA designers use Class-A amplifiers as a starting point, and apply harmonic control techniques to improve the efficiency by changing the bias network and moving to Class-AB.

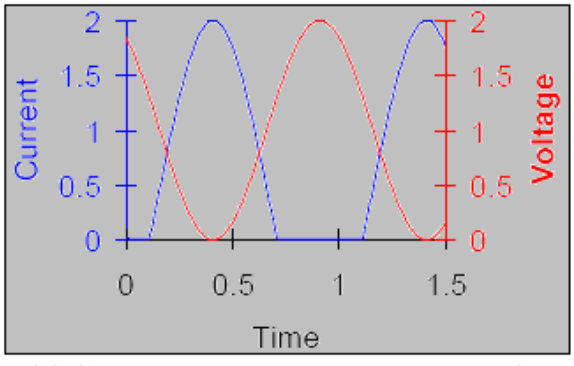


Figure 4.3 Class-AB voltage and current waveforms [10].

4.1.3 Class B

The operation point in a class-B amplifier has to be selected at the threshold voltage to achieve high power efficiency. However, due to the fact that the conduction angle is half the one in class-A, the linear characteristics drastically decrease. The ideal maximum drain efficiency of a Class-B amplifier is 78.5%, which is significantly higher than the Class-A amplifier. Practically, high-power Class-B amplifier can achieve a drain efficiency of 60%. We can easily see that class-B power amplifier dissipate less power than class-A.

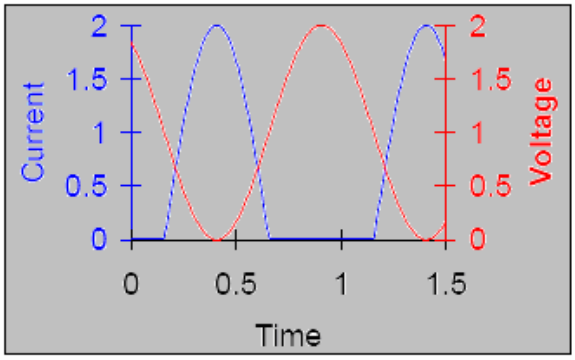


Figure 4.4 Class-B voltage and current waveforms [10].

4.1.4 Class C

Class-C amplifiers are high-efficiency amplifiers, with an ideal efficiency of 100%. However, there are several problems for Class-C implementation. The first drawback of this amplifier is the efficiency comes at the expense of the power gain. In fact, in the classic definition of Class-C amplifier, the output power approaches to zero, as the efficiency approaches to 100%. At microwave frequency, this approach is typically not desired, since high power gain is difficult to obtain. The second drawback is that the amplifier is highly nonlinear, so it can be used only in applications that can tolerate a high degree of nonlinearity, or it has to be used with linearization techniques.

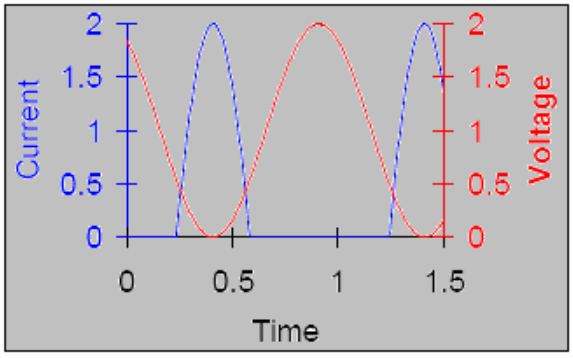


Figure 4.5 Class-C voltage and current waveforms [10].

There are also a number of very high efficiency non-linear amplifiers with reduced conduction angle such as D, E, and F etc. They are not to be further considered in this work due to their very poor linear characteristics, which are outside purview of this work.

4.2 Power Amplifier Properties

The most important parameters that must be considered when designing power amplifiers are listed below:

-Power (dBm or Watts)
-Efficiency (%)
-Gain (dB)
-Linearity
-Stability

These parameters are discussed deeply in [10]-[12].

4.2.1 Power

In RF-microwave circuits, power has two understandings: the power available from the source and the power transferred to or dissipated in the load. Available power is the maximum power accessible from the source. The maximum available power is obtained from the source if the input impedance of the transistor is conjugate matched to the source impedance ($Z_{in} = Z_s^*$). Therefore, for maximum available power as a function of frequency can be expressed as:

$$P_{av}(w) = \frac{1}{8}\frac{|V_s(w)|^2}{\mathrm{Re}\{Z_s(w)\}}, \quad \text{where} \tag{4.1}$$

V_s (w) is the peak value of the sinusoidal voltage applied on input and Re $\{Z_s$ (w)$\}$ is the real part of the source impedance.

The power dissipated in or transferred to the load is expressed by:

$$P_d(w) = \frac{1}{2}\frac{|V_L(w)|^2}{\mathrm{Re}\{Z_L(w)\}}, \text{ where} \tag{4.2}$$

V_L (w) is the peak value of the sinusoidal output voltage and Re $\{Z_L$ (w)$\}$ is the real part of the load impedance.

4.2.2 Efficiency

Efficiency is one of the most important parameters in power amplifier design. It represents the part of the dc power that is converted to RF power. The most commonly definitions used in power amplifier designs for the efficiency are: drain efficiency and power added efficiency.
Drain efficiency is the ratio of the RF-output power to the dc input power.

$$\eta = \frac{P_{OUT}}{P_{dc}}, \text{ where} \tag{4.3}$$

P_{OUT} is fundamental output power at the 1dB compression point P_1, expressed by $P_{OUT}=1/2V_{dc}I_1$
P_{dc} is DC power consumption: $P_{dc} = V_{dc}I_{dc}$.

Power-added efficiency (PAE), however, takes the power of the input signal into account and can be expressed by:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{dc}} \quad (4.4)$$

PAE is generally used for analyzing PA performance when the gain is low. This parameter is particularly important from power-consumption and power dissipation point of view. It is usually quantified in percentages. For example, for a class-A amplifier the transistor conducts during the whole wave period with an efficiency of 50%. It means that more than 50% of the energy dissipates as heat. It is not an acceptable condition for many telecommunication applications due to heating and battery lifetime issues.

4.2.3 Gain

In microwave designs, the gain is represented by different definitions. Its most representative definition is the transducer power gain. It is the ratio between the power delivered to the load and the power available from the source. Transducer gain can be expressed by:

$$G = \frac{P_L}{P_S}, \text{ where} \quad (4.5)$$

P_S is the RF input power and P_L is the RF output power. The typical value of the transducer gain for a RF power amplifier is 10-19 dB (assumed one-stage structure).

The gain can also be represented by the maximum available gain (MAG). It is the ratio between the power available from the output of the transistor and the power available from the source. The maximum value is occurred when the input of the PA is conjugate-matched to the source.
MAG can be defined only if the transistor unconditionally stable. It is useful to evaluate the MAG versus swept frequency. It gives the maximum frequency of oscillation (fmax), which shows the frequency when MAG reaches magnitude of 1 (0 dB). For the same reason, the current gain is evaluated versus frequency. The current gain is the short-circuit output current gain, which is a function of the swept gate voltage and the swept frequency. The value of the frequency, when the current gain drops to the magnitude of 1 (0dB), is called cut-off frequency (fT).

4.2.4 Linearity

The RF power amplifiers are inherently non-linear and are the main contributors for distortion products in a transceiver chain. Power amplifiers effect the utilization of the spectrum through nonlinear performance. Non-linearity is typically caused due to the compression behaviour of the power amplifier, which occurs when the RF transistor operates in its saturation region due to a certain high input level. Usually non-linearity is attributed to gain compression and harmonic distortions resulting in imperfect reproduction of the amplified signal. It is characterized by various techniques depending upon specific modulation and application. Some of the widely used figures for quantifying linearity are the:

- 1 dB compression point
- Third order intermodulation distortion
- Third order intercept point (IP3)

Deep investigation of power amplifier linearity can be found in [13].

4.2.4.1 1 dB Compression point (P_{1dB})

Non-linear response appears in a power amplifier when the output is driven to a point closer to saturation. As the input level approaches this saturation point, the amplifier gain falls off, or compresses. The output 1 dB compression point can be expressed as the output level at which the gain compresses by 1 dB from its linear value. The gain corresponding to the 1 dB compression point is referred to as G_{1dB} and is computed as $G_{1dB} = G_0\text{-}1dB$, where G_0 is the small-signal gain (or $10\log|S_{21}|^2$). $P_{out,1dB}$ at the 1 dB compression point can be expressed in dBm if it is related to the corresponding input power $P_{in,1dB}$ as:

$$P_{out,1dB}(dBm)=G_{1dB}(dB)+P_{in,1dB}(dBm)=G_0\text{-}1dB+P_{in,1dB}(dBm) \quad (4.6)$$

Figure 4.6 shows the relationship between the input and output power of a typical power amplifier.

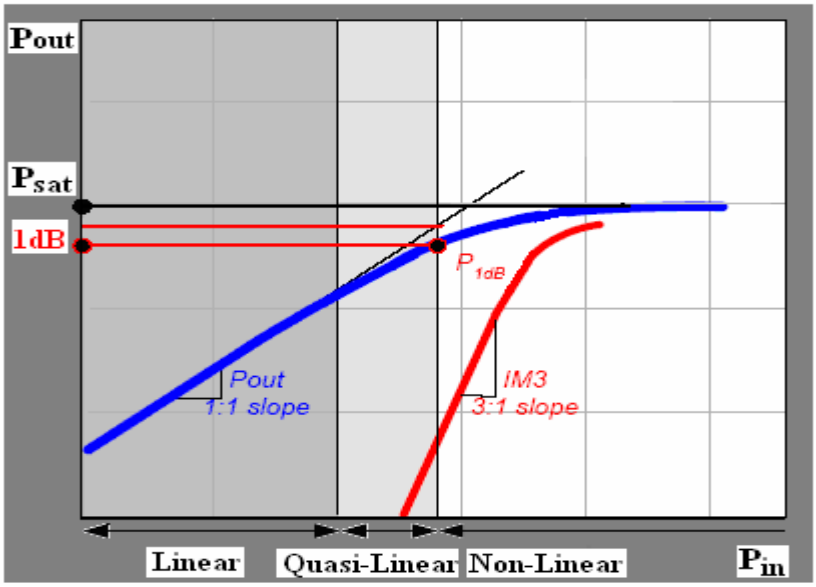


Figure 4.6 Pout vs. Pin, 1dB compression point.

4.2.4.2 Intermodulation Distortion

Intermodulation Distortion is a phenomenon of generation of undesirable mixing products, which distort the fundamental tones and gives rise to intermodulation products. The third order intermodulation products have the maximum effect on the signal, as they are the closest to the fundamental tone. The unwanted spectral components, such as the harmonics, can be filtered out. But the filtering does not work with the third order intermodulation products, as they are too close to the fundamental tone. Figure 4.7 shows the frequency domain representation of the intermodulation distortion caused due to a two-tone signal. Intermodulation products higher than third order, the odd harmonics (fifth, seventh) are important to consider when Pout exceeds the 1dB compression point.

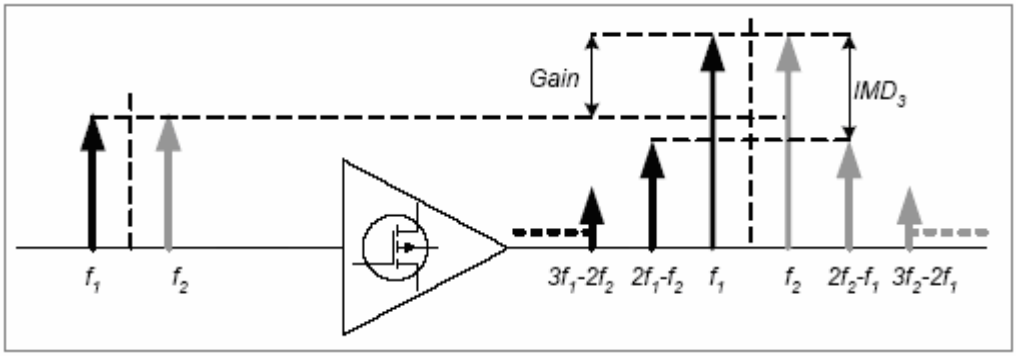


Figure 4.7 Two tone intermodulation distortion.

4.2.4.3 Third order Intercept point

IP3 is defined as the point where the linear extension of the third order intermodulation distortion component intersects the linear extension of the input vs. output line. Figure 4.8 represents the third order intercept point (IP3) in a plot of input power versus the output power. This parameter plays a major role in the analysis of device performance, because higher the IP3, lower is the distortion at higher power levels

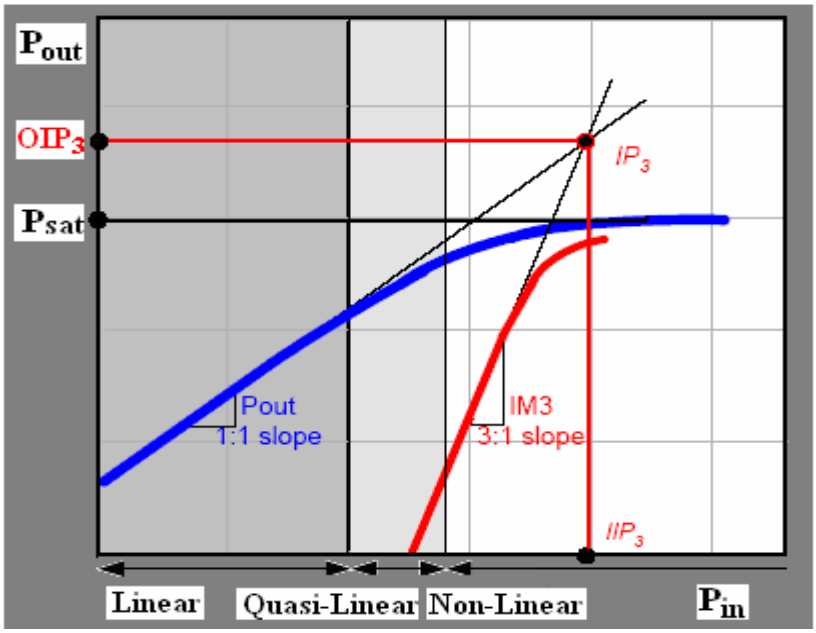


Figure 4.8 Third order interception point.

4.2.5 Stability

Stability is a practical problem frequently encountered in the design of linear PA. Linear, class-A amplifiers are actually more susceptible to oscillation due to their high gain. Instability can be subdivided into two distinct categories: Low-frequency oscillation and in-band instability. In-band instability is avoided by designing the gain to meet the criteria for unconditional stability; i.e., the Rollet *k* factor must be greater than unity for both in-band and out-of-band frequencies. Meeting this criterion usually requires sacrificing some gain through the use of absorptive elements. Large RF power devices typically have very high transconductance, and this can produce low-frequency instability unless great care is taken to terminate both the input and output at low frequencies with impedances for unconditional stability. Because of large

separation from the RF band, this is usually a simple matter requiring a few resistors and capacitors.
The main reason behind unstable behaviour of the active device is a reverse feedback from output to input. Several factors are used in estimating the stability in class-A, AB amplifier. The Rollet's conditions are based on the two-port S-parameters matrix expressed as:

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| \tag{4.7}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} S_{21}|} \tag{4.8}$$

For unconditional stability: k > 1 and |Δ| <1, otherwise the stability has to be taken into account. One of the graphical representations of stability is the stability circles. It is a useful tool to avoid the unstable area when designing the matching networks with a Smith chart. However, it should be noticed that many amplifier could be stable at small signal and start to oscillate at large signal due to the variation of the output impedance (S22) with the output power.
The solution to Instability:

1. Avoid the instability region when matching.
2. Reduce the stage gain to stay within the maximum stable gain range.
3. Reduce the input and output impedance by resistive damping.
4. Change the bias conditions (only for class-A, -AB).
5. Choose a different device.

4.3 Bias and Matching networks

This part of the chapter investigates the general steps that should be followed to design the bias network and the input-output matching network.
The design of a power amplifier comprises several blocks for adjusting conditions to achieve a proper operation of the transistor in accordance to the requirements. The block diagram, Figure 4.9, represents a typical circuit considered in the design process. It consists on a Bias Network (BN), Input Matching Network (IMN), Output Matching Network (OMN), Accessories Networks (AN) and the input and output ports that are assumed to be 50 Ohm.
Bias and matching networks are investigated in [10]-[13].

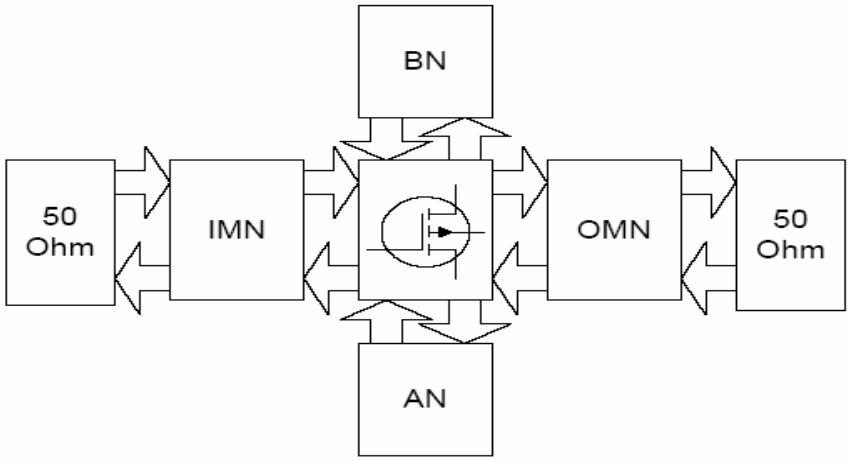


Figure 4.9 Block diagram of an amplifier.

4.3.1 Bias network

The bias network is an important part of the power amplifier design. In fact, the BN control the operation class of the transistor and at the same time it prevents the RF signal from leaking to the DC source and prevents the DC signal from leaking to the RF trajectory.
The BN of a high power amplifier differ from the normal amplifier by the fact that it is non-resistive. The main reason behind that choice is that high power amplifier consumes high current, so to prevent additional heating in the system, non-resistive bias network is used.

Usually, BN consists on blocks of capacitance and inductance whose objective is to work as DC Feed-RF Block in the DC track, and as DC Block-RF Feed in the RF track. Their values depend on the frequency range the power amplifier is supposed to work in. Also the BN shows a importance in long term memory effect and system distortion.

4.3.2 Input/Output matching networks

In power amplifier designs, to achieve high accuracy and maximum power transmission, a matching network is required on the input and output to minimize the reflection (standing waves) problems. Matching networks are passive, consisting of microstriplines, inductors, capacitors and resistors. Input and output matching networks transform the input and output impedance of the transistor to the source and load impedance (usually 50 Ohm).
In the current design, microstriplines will be used in the matching networks.

There are three types of matching principles:

1) **Conjugate matching**

Conjugate match or gain match is a method used in amplifier design, usually LNA, to achieve the maximum output gain. In conjugate matching, the IMN and OMN are adjusted to transfer source/load impedance (50 Ohm) toward device input/output impedance. By this method, theoretically, it is possible to achieve the maximum power gain and the minimum losses due to standing waves.
The conjugate matching is based on small signal S-parameter analysis. It is not effective for power amplifier, because the input signal cannot be treated as a small-signal, and so a power match is usually used (note that conjugate matching can be used for the input matching circuit in class A amplifiers).

2) Load-line matching

The general idea is based on load-line optimal resistance matching (R_{opt}), which provides highest output power. Therefore the OMN must translate the value R_{opt} of the device to load impedance (50 Ohm). The final formula to find Ropt is expressed as:

$R_{opt}= (V_{ds}-V_{knee})/I_{max}$, where

V_{ds} is the supply voltage, V_{knee} is the point where the current reaches saturation region when V_{gs} is constant and I_{max} is the maximum or saturation current. The design of input-matching network is similar to conjugate matching. The theoretical result of loadline-matching design generally is 0.5-3 dB higher in 1dB compression point than the conjugate matching.

Another approach in Load-line matching is the Cripps method which permits the construction of a series of (g_L, r_L) plots for a correspondent array of desired output powers which can be used as a good estimates of output power load contours [10].

3) Matching based on Load Pull analysis

Load pull analysis technique is based on searching the optimal load impedance which a trade-off between efficiency and output power. The method is implemented in different CAD tools. For example, in Agilent EEsof ADS 2005a on the graph window, the output impedances are plotted on the Smith chart, and each load value lead to certain values of gain and output power. The Power and efficiency contours are generated empirically by connecting various loads to the amplifier and by measuring the gain and output power at each value of the load impedance. The implemented Load Pull simulation in Agilent EEsof ADS is utilized in the current work.

Finally, the existence of accessories networks (AN) is mentioned. They are different methods and facilities to improve stability and linearity characteristics of the amplifier. This design considers a model without any accessories networks.

Chapter5. Design and Simulation

This chapter presents the design and simulations of a class A power amplifier based on Si-LDMOS performed using Agilent EEsof ADS simulator. First of all, the Si-LDMOS model utilized in the design from Freescale is described. Then we will describe deeply all the steps followed in the design regarding the features of the system, simulation and evaluation.

5.1 Device under Simulation

The model used in the current design is the Motorola's Electro Thermal (MET) Si-LDMOS MW6S004NT1 model. It is a new model from Freescale; his detailed description has not been published; however a good explanation regarding his characteristics will be given in this section.

The MET LDMOS model of the used transistor is not available as a library in Agilent EEsof ADS, it has been offered privately from Freescale for the current research.
However, a general description of Motorola's MET models will be given, than specific parameters of the used model involving in the design, are presented.
The Motorola's models are commercialised and their library, in Agilent EEsof ADS, include the whole row of LDMOS devices that has been recently developed and produced. The equivalent circuit of empirical large-signal MET LDMOS model is shown in Figure 5.1.

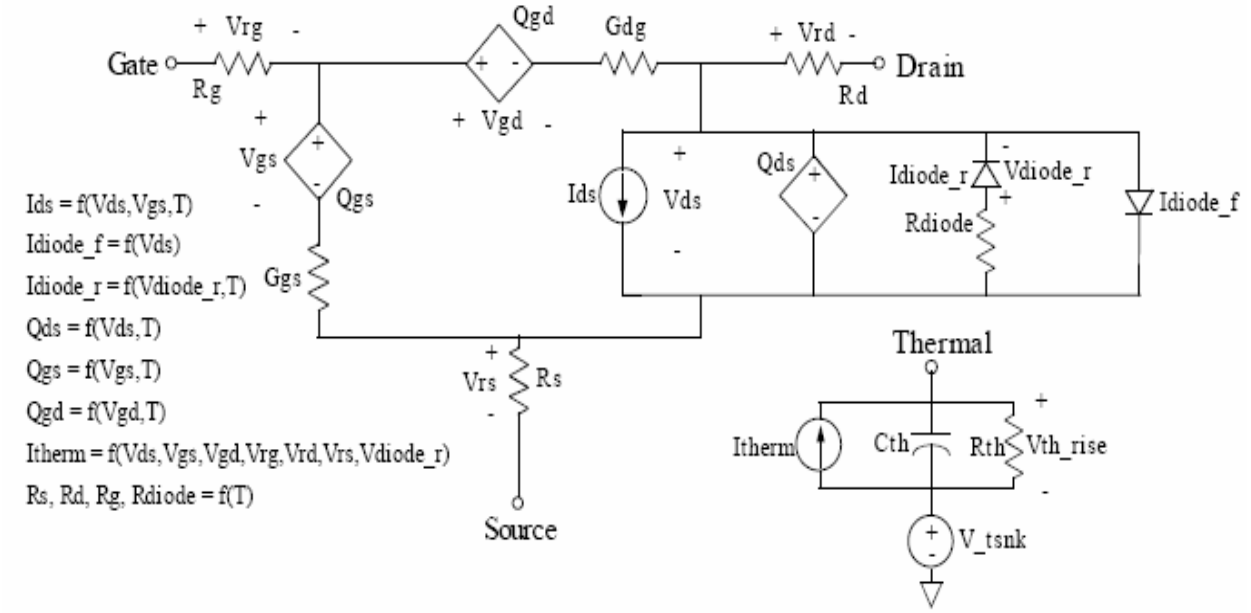


Figure 5.1 Large signal Equivalent Circuit of the MET LDMOS model [14].

Based on this topology, the model has a voltage and temperature dependent nonlinear current source. There are also a forward diode, as a function of voltage, and a reverse diode, as a function of temperature and voltage. The model also has nonlinear capacitances, which are dependent from the appropriate voltages and temperature. There are two internal gate conductances and temperature dependent parasitic resistances. The thermal sub-circuit calculates the instantaneous rise in temperature, where Itherm is total instantaneous power dissipated in the transistor, Rth is the thermal resistance, Cth is the thermal capacitance and Vtsnk is a voltage source that represents the heat sink temperature of the system.

Regarding the MW6S004NT1, it is designed for class A or class AB base station applications with frequency up till 2GHz. Suitable for analog and digital modulation and multicarrier amplifier applications.
Typical output power is 4 Watts, 33% PAE and Vds =28V.
Some specific parameters are listed in Table 5.1.

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5,+68	Vdc
Gate-Source Voltage	V_{GS}	-0.5,+12	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	^{o}C
Operating Junction Temperature	T_j	150	^{o}C
Characteristics	Symbol	Value(1,2)	Unit
Thermal Resistance, Junction to case Case Temperature 76^{o}C, 4W PEP, Tow-Tone Case Temperature 79^{o}C, 4W CW	R_{OJC}	 8.8 8.5	^{o}C/W

Table 5.1 MW6S004NT1 properties

5.2 Design and ADS-simulations

Designing a power amplifier consist on different steps. First of all a DC simulation must be done to find the optimal bias and bias network for the system. Then a small signal S-parameters simulation is done to find the value of the S-parameters and to evaluate the stability of the model with in the used frequency and bias range. After that the Input and Output matching network are designed using load pull simulation (which gave the best results). Finally the whole system is optimized to achieve better output power, efficiency and gain.

5.2.1 DC analysis

The first step of design in the current work is to estimate the I-V characteristic. The results of these simulations decide about the first draft version of bias points. The I-V curves help to see, for example, the operation region of a transistor, the maximum drain currents, threshold voltage, knee region, safety region, etc.

Before building up the circuit, the maximum allowed DC power dissipation must be found.
From Table 5.1, we notice that the Operating Junction Temperature is 150 ^{o}C and the Thermal Resistance, Junction to case is 8.5 ^{o}C/W for a Case Temperature 79^{o}C, 4W CW.

Based on the above, we find:

$$P_{d\max} = \frac{(Tj - Tc)}{R_{JC}} = \frac{(150 - 79)}{8.5} = 8.353 Watts \qquad (5.1)$$

The above result will limits the choice of the bias level to ensure a secure operation region for the transistor and to prevent it form self heat destruction.

The built up circuit is shown in Figure 5.2.

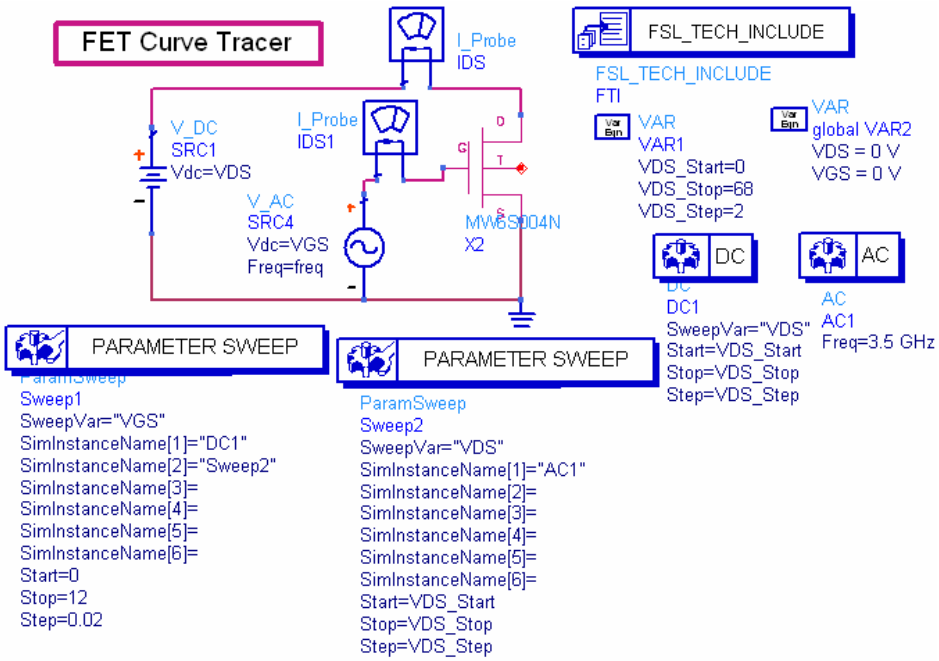


Figure 5.2 I-V curve simulations

It has only bias networks with two DC voltage sources. The sources of the gate and the drain voltages are swept:

V_{gs} = [0-12] V and V_{ds}= [0-68] V.

The results of the I-V simulation are shown in Figure 5.3.

From this simulation we notice that the drain current, for a gate voltage higher than 5V, increase rapidly and the breakdown voltage of the transistor will be lower than 68V, and might reach 30V.
The maximum allowed drain voltage is chosen to be 56V. In fact, the typical V_{ds} is approximated to 28V, given by Freescale for Si-LDMOS operation, and as the quiescent point should have a voltage of $V_Q = \frac{V_{BR} + V_K}{2}$, than V_{BR} is approximated to 56V.
Now, to find the safe operation bias, the saturation drain current I_{dss} will be fixed to 568.9mA in a way to obtain the load line in the safety region. The main reason behind that choice is to choose a 'class A' bias in the safety region. So setting V_{DS}= 56V and P_{dmax}= 8.353 lead to a safe bias of:

V_{ds}=28V, V_{gs}=3.02 V, I_{ds}=0.2969 A, V_{Knee}=2V, V_{th}=2.5V.

The main problem when choosing the bias consisted on the low safety region of the transistor. Figure5.4 show the low safety region compared to the whole bias region. Due to that, and as shown in the following sections, the performance of the system will be limited.
Also we should mention that this DC simulation gave values for the optimal load, the efficiency and the output power. These values are not going to be taken into consideration due to the non-idealistic of the DC simulation.

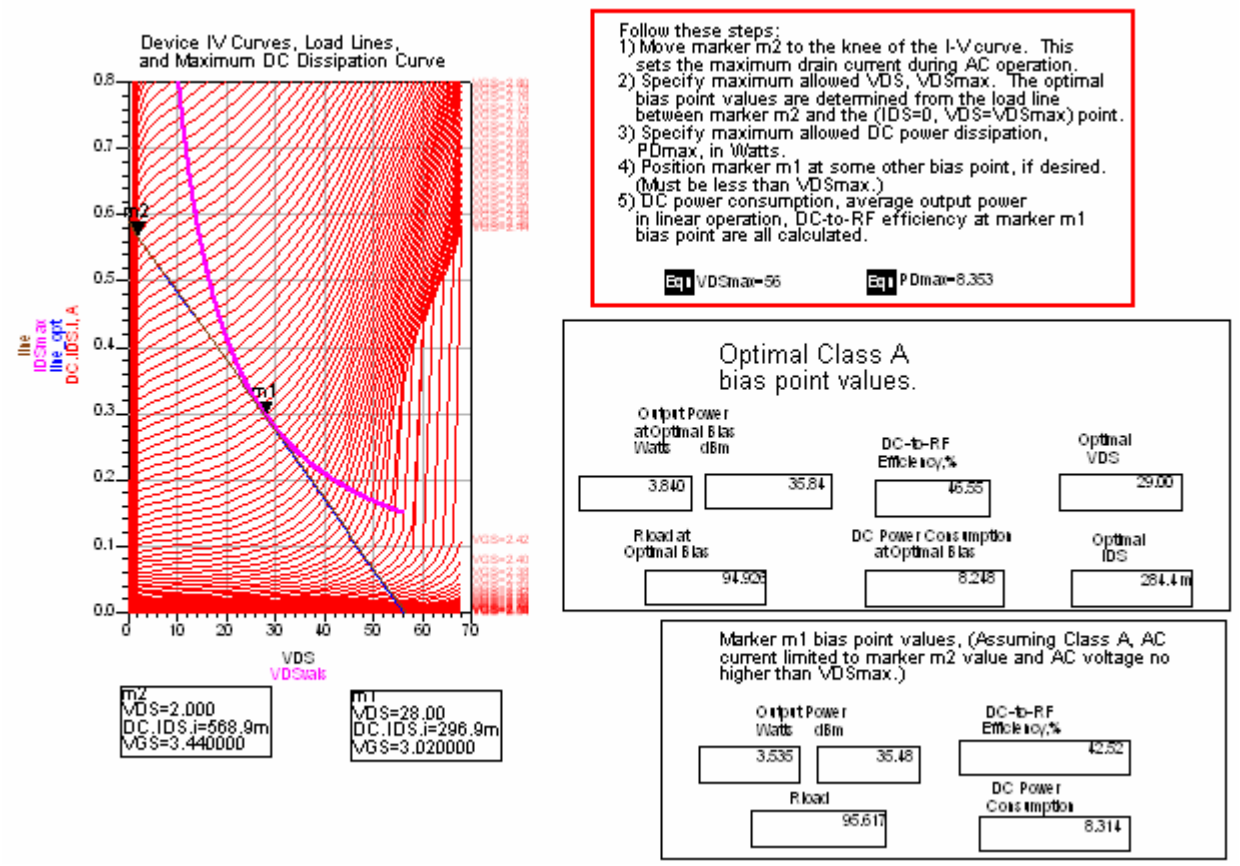


Figure 5.3 I-V curves

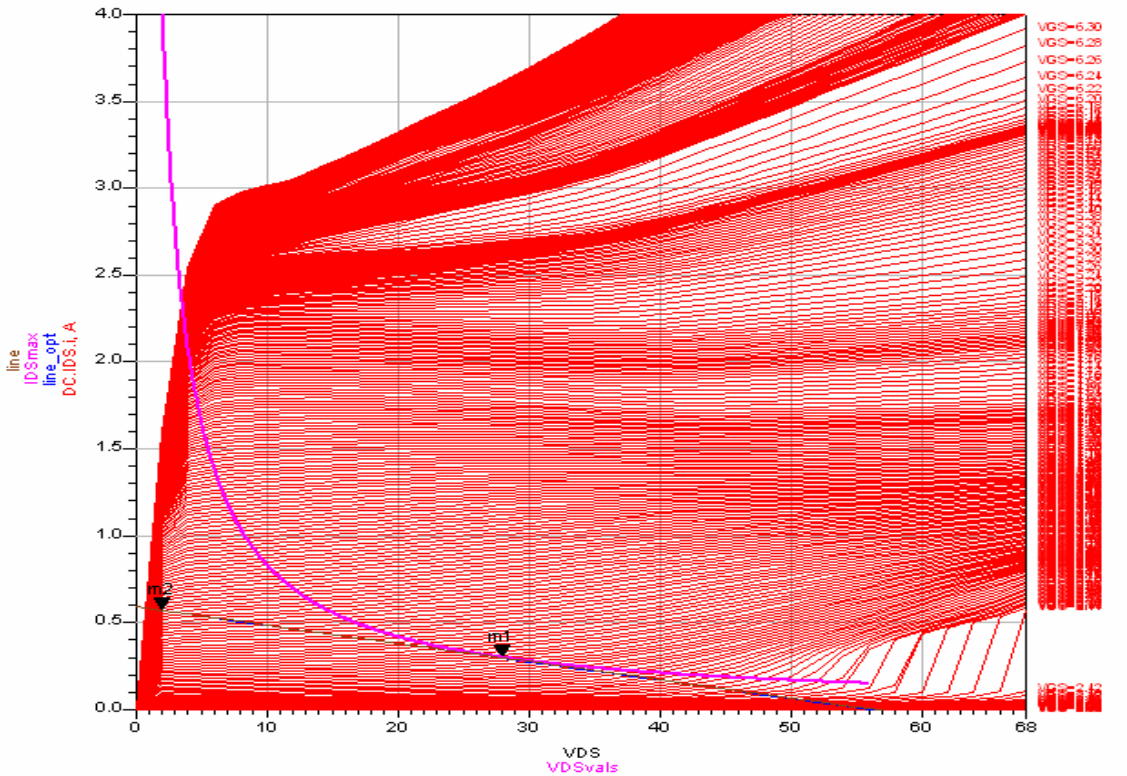


Figure 5.4 Safety region

After finding the bias voltage, the next step is to find the bias network. For that a passive bias will be used to reduce the memory in the system, it consists on a block of capacitors and inductors. These blocks will behave as a DC feed-RF block in the DC trajectory, and as DC

block-RF feed in the RF trajectory. Their values are chosen regarding the range of frequency the system is supposed to work in, 3.5GHz.
The system including the bias network is shown in Figure 5.5.

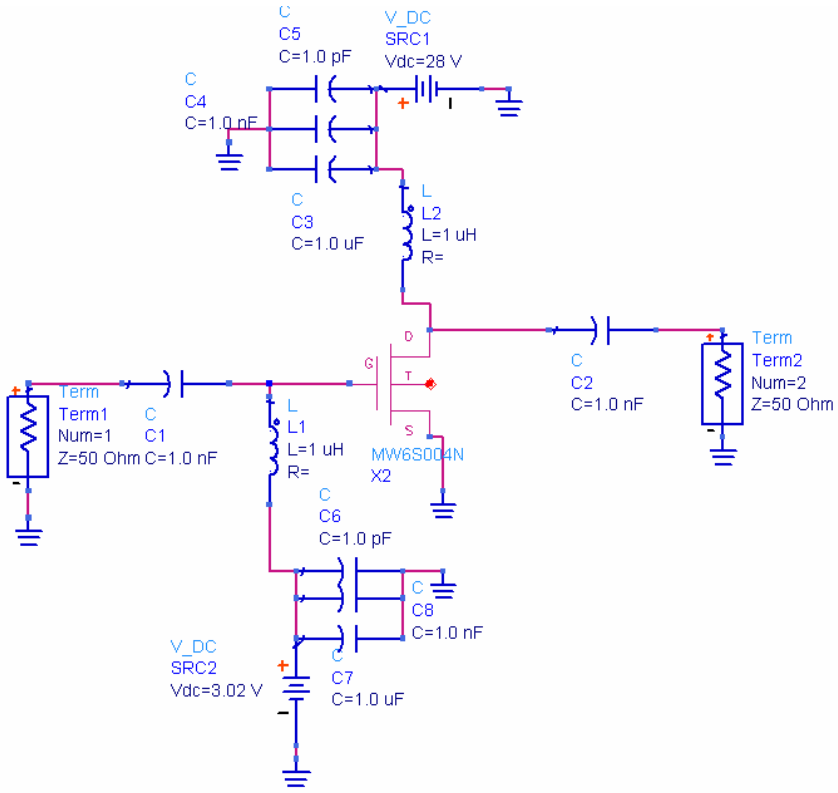


Figure 5.5 Bias network

C1 and C2 have the value of 1 ηF, which will behave as short circuit for RF frequencies and as open circuit for DC.
L1 and L2 = 1μH; C3, C7 = 1μF; C4, C8 =1 ηF; C5, C6=1ρF. These two blocks will behave as short circuit for DC and as open circuit for RF frequencies.
In the following sections, this bias network will be adjusted and optimized for better performance.

5.2.2 Small-signal (S-parameter) simulations

The small-signal S-parameter simulation is implemented in the design to find the value of the S-parameters and the stability region of the biased transistor. In fact, as class A amplifiers present the highest linearity between the other types, and despite the fact that we are designing a high power amplifier, the S-parameters are still usable certainly in designing the input matching network.

Figure 5.6 shows the build up circuit for the S-parameter simulation. We should mention that the build up circuit include the bias network to present a more realistic results.

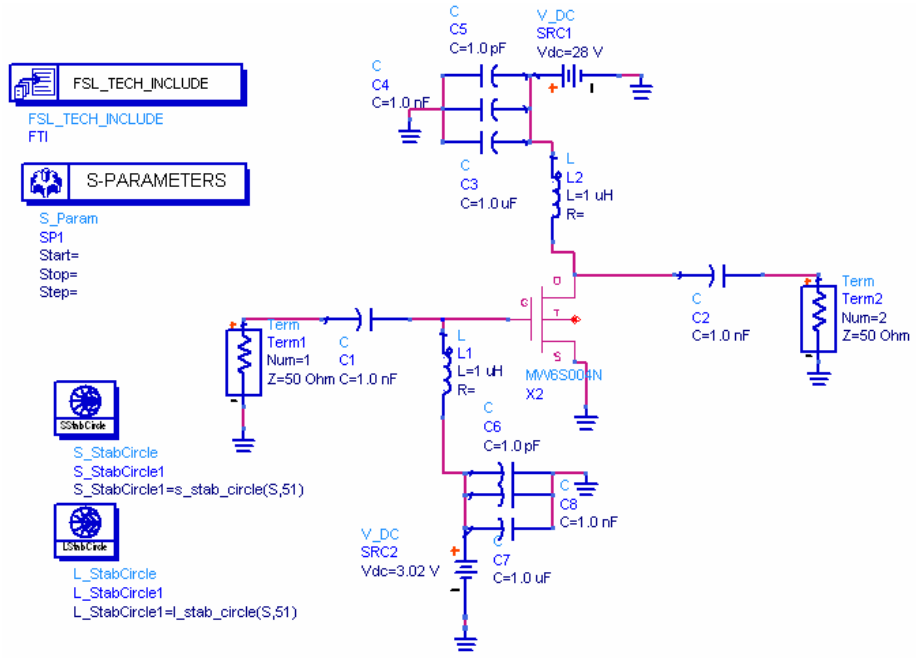


Figure 5.6 S-parameters simulation

The results of the simulation are shown in Figure 5.7. We notice that the system is conditionally stable, so care should be taken when designing the input and output matching networks. Also we notice that the transistor present a gain of 3 dB, which might help us in the design.

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
3.500 GHz	0.924 / 107.103	0.027 / 3.649	1.420 / -89.681	0.775 / 90.096

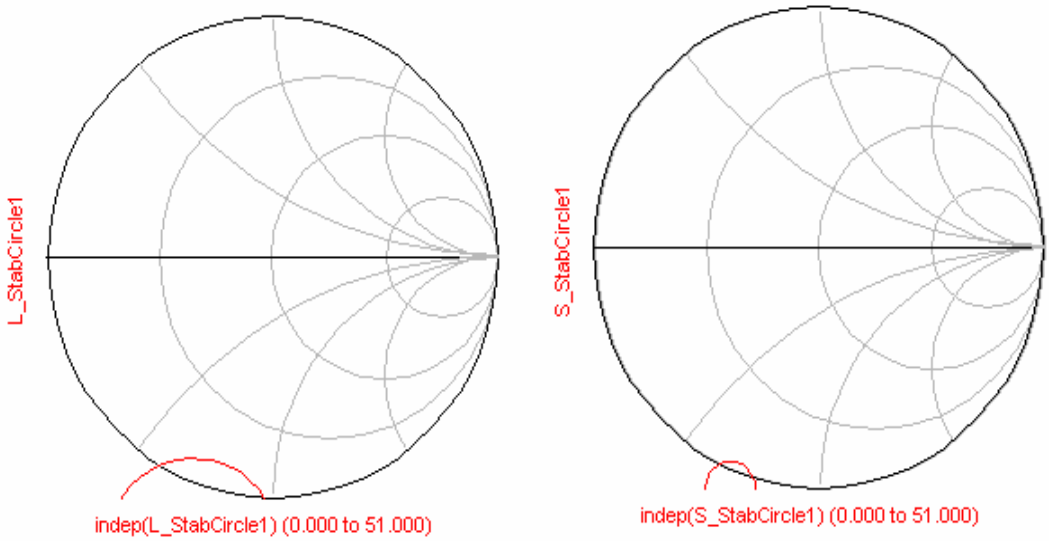


Figure 5.7 S-parameters and stability

5.2.3 Design of matching networks (IMN, OMN)

5.2.3.1 Load pull simulation

Load pull simulation is utilized to find the optimal load value that will maximize the output power and the efficiency, or achieve a compromise between both of them.

This analysis utilizes the built-in ADS load-pull circuit simulator. Different values of load impedance are applied to find out the optimum one, which meets the required value of gain, output power and efficiency. The derived value of the optimum load impedance is going to be utilized to design the OMN.
Before running the simulation, some parameters have to be set.

RFfreq=3500MHz, Vhigh=28V, Vlow=3.02V, dB_Gain_Comp=1, P=20dBm and Zo=50Ω.
The value of the input power, 20dBm is found approximately as the output power range is 4W with an approximate gain of 16dB.
These parameters will allow finding the optimal load at the 1dB compression point at which the performance of the design will be evaluated.
The load pull circuit is shown is Figure 5.8.

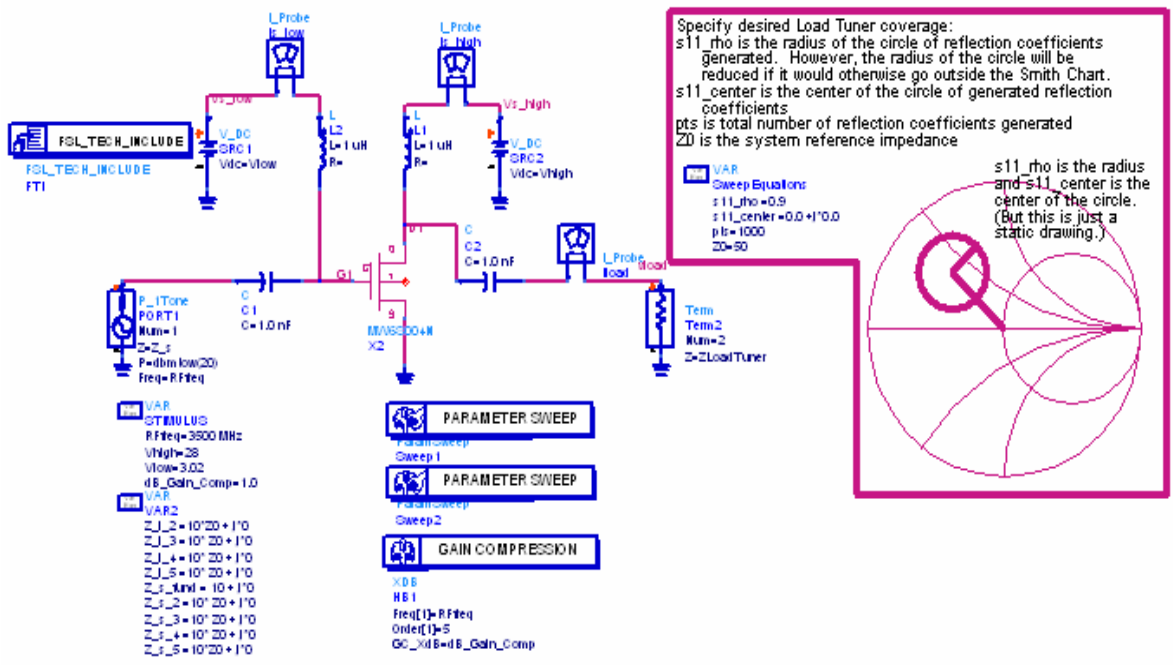


Figure 5.8 Load pull simulation

The results of the simulation are shown in Figure 5.9. The load pull simulation gave an optimal output power of 36.6dBm, PAE of 17.46%. So the optimal load that will compromise between these two values is Z_L=8.081-j*57.971 Ω. This value will give a PAE of 16.31% and a 36.6 dBm.
Although Load pull simulation is one of the best method to calculate the load, the following section will show us that the results are some how different.

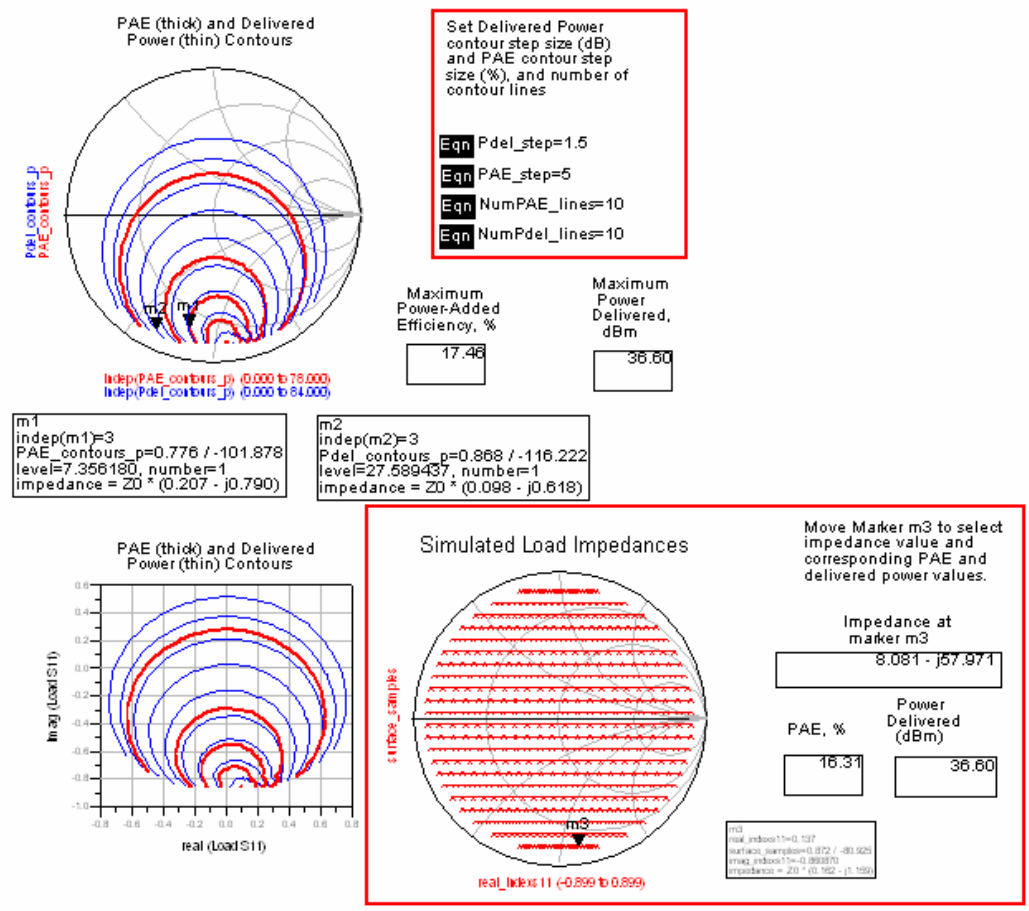


Figure 5.9 Load pull results

5.2.3.2 Output matching network-Input matching network designs

Having the load value, and using a 50 Ω system reference, the load reflection coefficient is found by the following:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{8.081 - j*57.971 - 50}{8.081 - j*57.971 + 50} = 0.871 < -80.92^0 \qquad (5.2)$$

In the load plan, using the smith chart (of 50Ω), we get $Y_{L/50}$ and than we use open-circuited shunt stub. We move first toward load so we will intercept the g=1 circle into two points, we measure and find the length of the series line. Then as we are using the open stub, we move from the open side of the admittance smith chart, toward generator, to the jX of the intersection points; we get the length of the open stubs.
We find for the two solutions:

$$\begin{matrix} d_1 = 0.3195\lambda \\ L_1 = 0.2975\lambda \end{matrix} \quad \text{And} \quad \begin{matrix} d_2 = 0.4055\lambda \\ L_2 = 0.204\lambda \end{matrix}$$

The matching network of the load side is shown in Figure 5.10

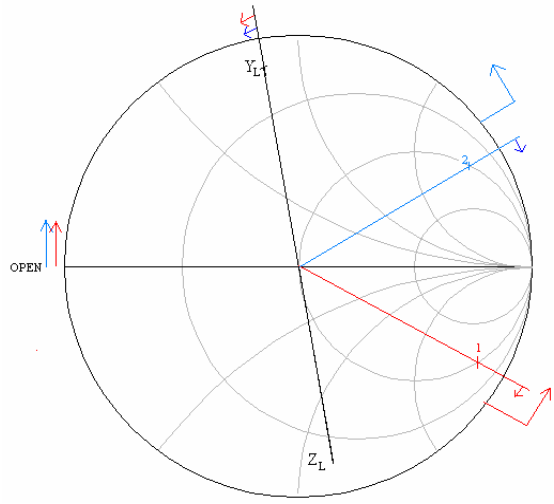


Figure 5.10 Matching network for the load

For the input (Source) section, we choose $\Gamma_S = \Gamma_{IN}^*$ so that we will have maximum power transmitted to the transistor.

$$\text{Or} \quad \Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = 0.906 < 112.844^0 \Rightarrow \Gamma_S = \Gamma_{IN}^* = 0.906 < -112.844^0 \qquad (5.3)$$

In the source plan, using the smith chart (of $50\,\Omega$), we get $Y_{S/50}$ and than we use open-circuited shunt stub. We move first toward load so we will intercept the g=1 circle into two points, we measure and find the length of the series line. Then as we are using the open stub, we move from the open side of the admittance smith chart, toward generator, to the jX of the intersection points; we get the length of the open stubs.
We find for the two solutions:

$$\begin{aligned} d_1 &= 0.373\lambda \\ L_1 &= 0.286\lambda \end{aligned} \quad \text{And} \quad \begin{aligned} d_2 &= 0.44\lambda \\ L_2 &= 0.214\lambda \end{aligned}$$

The matching network of the source side is shown in Figure 5.11

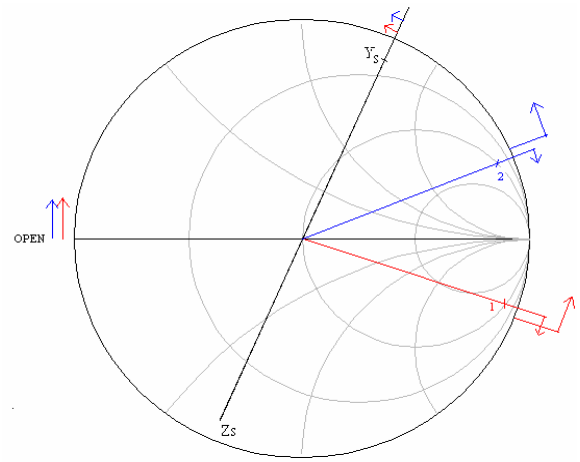


Figure 5.11 Matching network for the source

From the smith chart we see that both coefficients are in the stable region. We should mention that in both cases solution 1 was used in the design process due to the better performance they showed in the simulations and to their dimension's compatibility.

5.2.4 ADS Simulations and Optimizations

The next step in this work is to study the performance of the design in ADS and enhance it by optimization to achieve the aimed results.
First, to find the real lengths of the microstriplines we use ´´Linecalc´´ from ADS with substrate's parameters:
ε_r =10.2, H=0.640mm, T=17 µm, TanD= 0.0022, Zo=50Ω.

The system's circuit is shown in Figure 5.12.

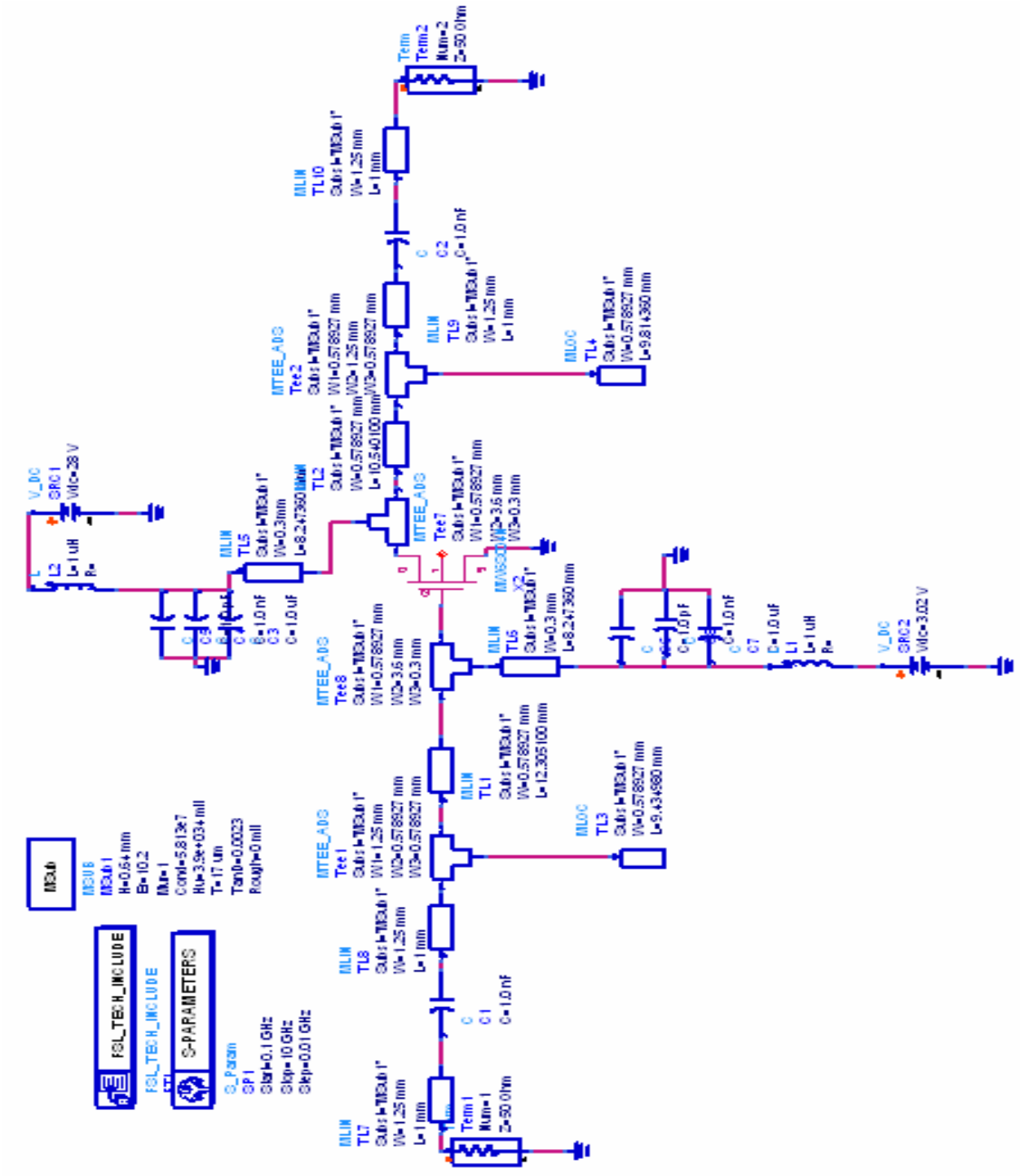


Figure 5.12 Build-up circuit

We notice that two λ/4 lines have been added in the DC trajectory to improve the capability of blocking the RF signal. Also the real equivalent length of both capacitance C1 and C2 have been added to the system due to their influence in the RF trajectory.

The simulation of the above design is shown in Figure 5.13, where it is obvious that the used transistor is designed for lower frequency use. Also we notice that the best performance the system can achieve regarding the gain is not at 3.5GHz. This due to the additional lengths added in the RF trajectories, to the added λ/4 lines, the non idealistic of ADS and finally to the load matching method used which improve the output power at the cost of the gain.

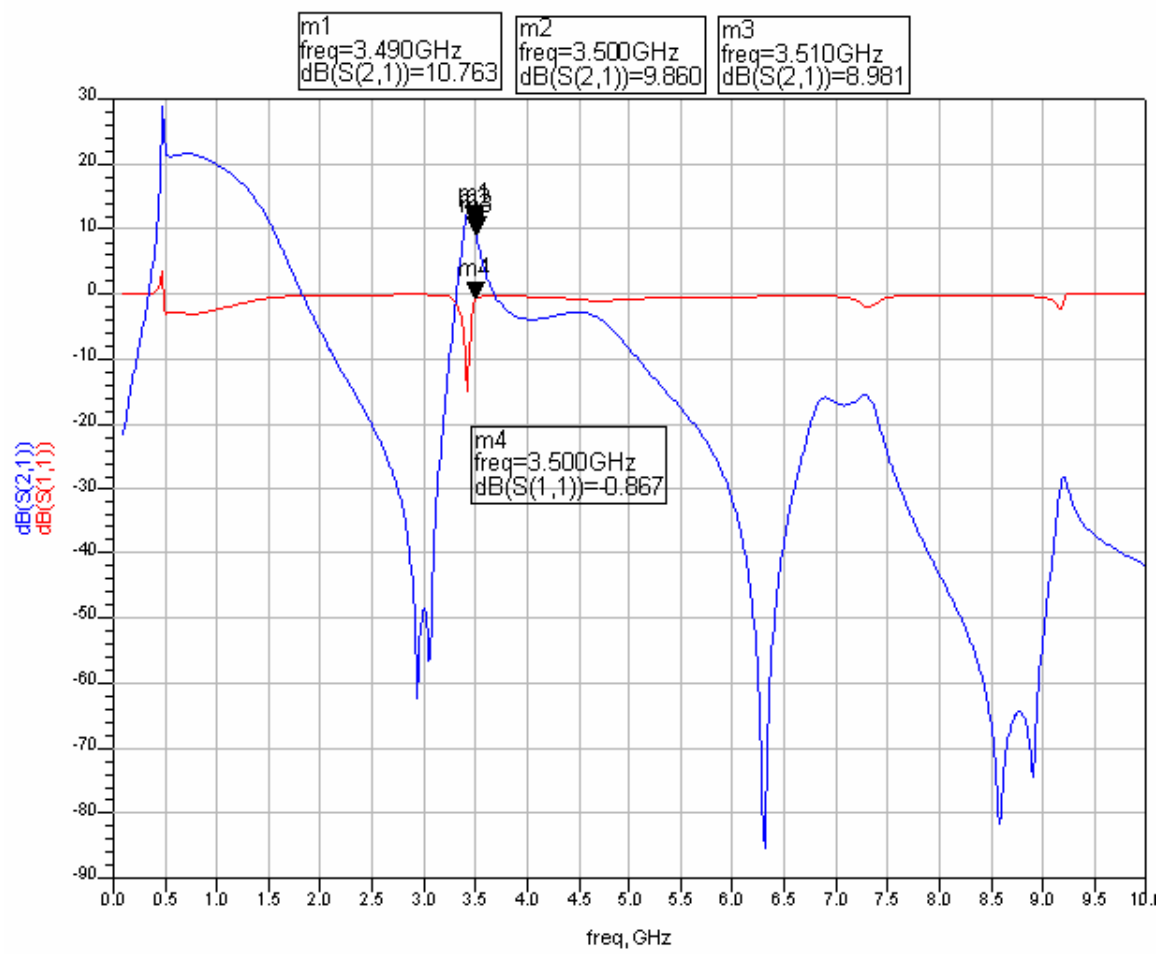


Figure 5.13 First simulation result

To study the performance of the design regarding the output power and efficiency, one tone harmonic balance must be done, for that an HB1TonePAE_Pswp simulation is used from ADS design guide. Two sweeps are made, a coarse one from 10 dBm to 22 dBm input power in steps of 1 dBm, and a fine sweep between 22dbm and 30dBm in steps of 0.01 dBm. This decision is taken after realizing that the 1 dB compression point is approximately at 23 dB input power. Figure 5.14 shows the schematic for the HB1TonePswp.

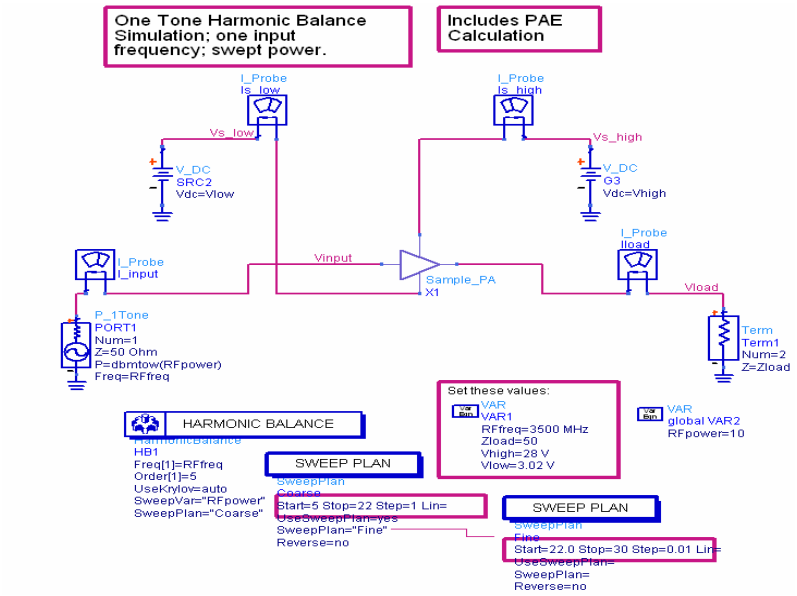


Figure 5.14 Harmonic Balance-non optimized design

The results of the simulation are shown in Figure 5.15.

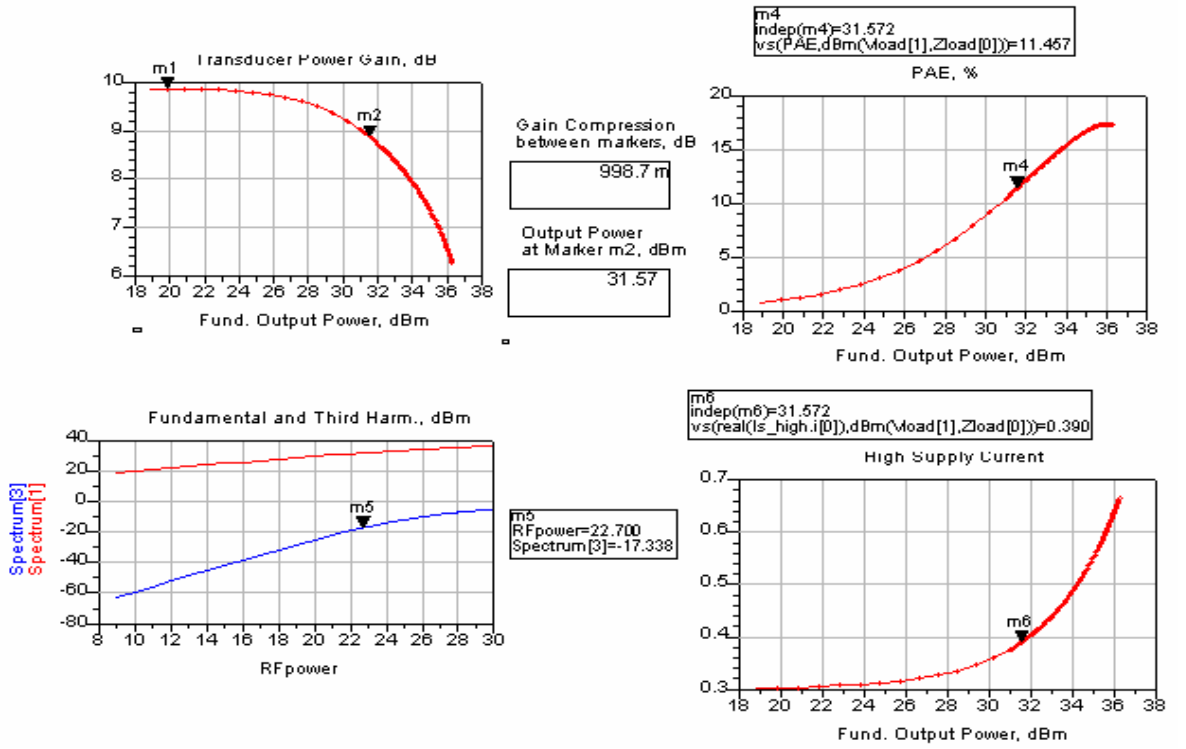


Figure 5.15 Result of HB1Tone_Pswp—non-optimized

From the above simulation we notice that the output power at the 1dB compression point is lower by 4.5 dBm from the typical output power of the transistor, also the efficiency is low, and should be in the range of 30%.

To improve the performance, the system is going to be optimized first regarding the gain, and than regarding the power parameters.

To achieve that, the goal will be set to:

S21=50 dB, S11=-20 dB, S22=-20 dB.

The optimized designed is shown in Figure 5.16

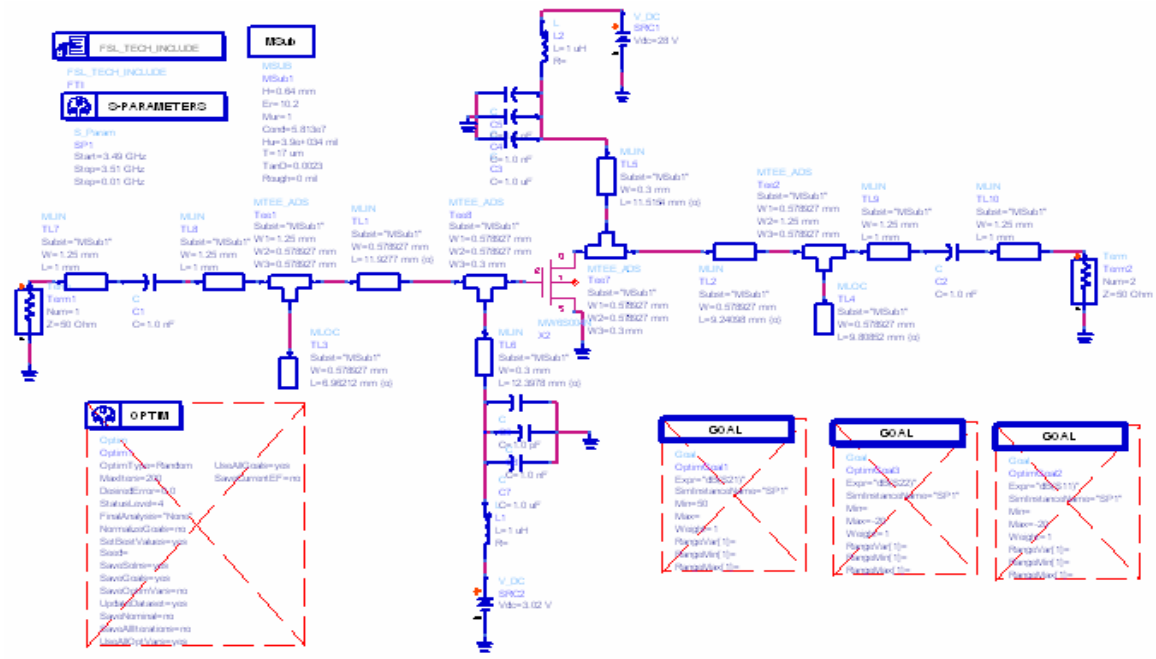
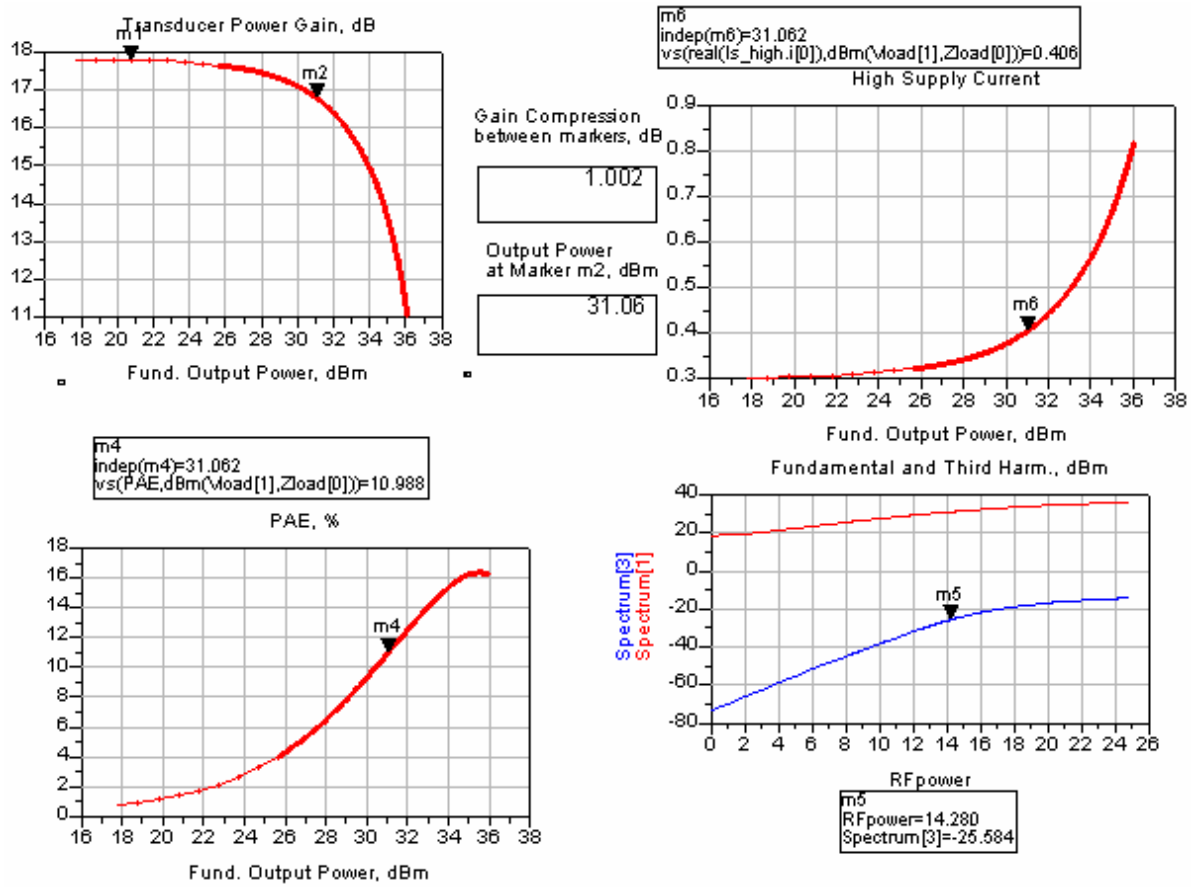


Figure 5.16 Gain optimization

Figure 5.17 show simulated result of the optimized system using HB1Tone_Pswp. As shown, the gain and return loss have been improved at an average of 7 dB, while the output power and the efficiency decreased by 0.5 dB-% respectively.



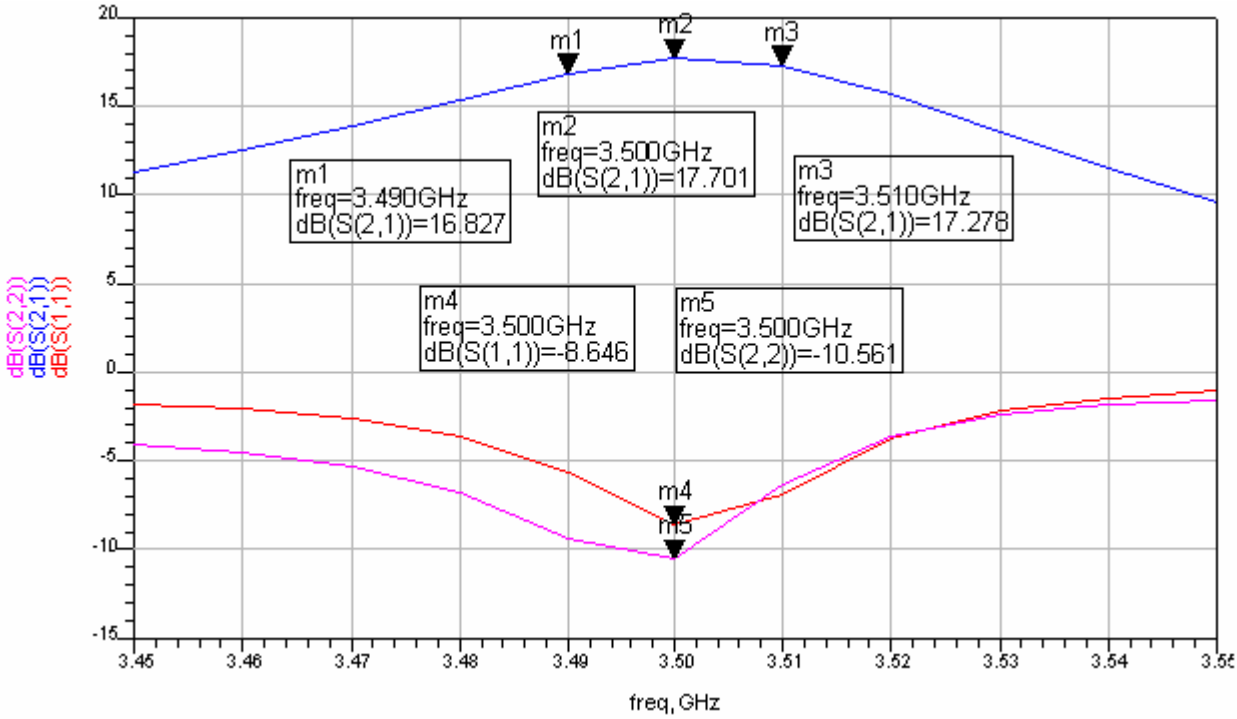


Figure 5.17 Simulation of Gain-optimized system

After increasing the system gain performance, we will optimize the system regarding Pout at 1dB compression, PAE, thermal dissipated power and IM3.
After multiple simulations and adjustments, the following steps have been made:

-Both MTEE have been replaced by two Mcroso to achieve better matching and to reduce the size of the system.
-Additional lengths with steps have been added to the system to improve the soldering of the transistor due to the big difference in the width between the transistor's pins and the 50 Ω lines.
-Additional lines have been added to the I/O and Bias ports to improve the soldering.
-Additional MTEEs and Mcrosos have been added to the DC trajectory to improve the soldering of the capacitances.
-The gate voltage has been reduced to 2.98V, to improve the safety. (It will not affect the class due to the non-idealistic of ADS, and however, the aim of the work is start with a Class A design and after the manufacturing to change the bias in order to improve the performance of the system).
-Finally, the 1ηF capacitances have been replaced by 820ρF capacitances.

The final design is shown in Figure 5.18.

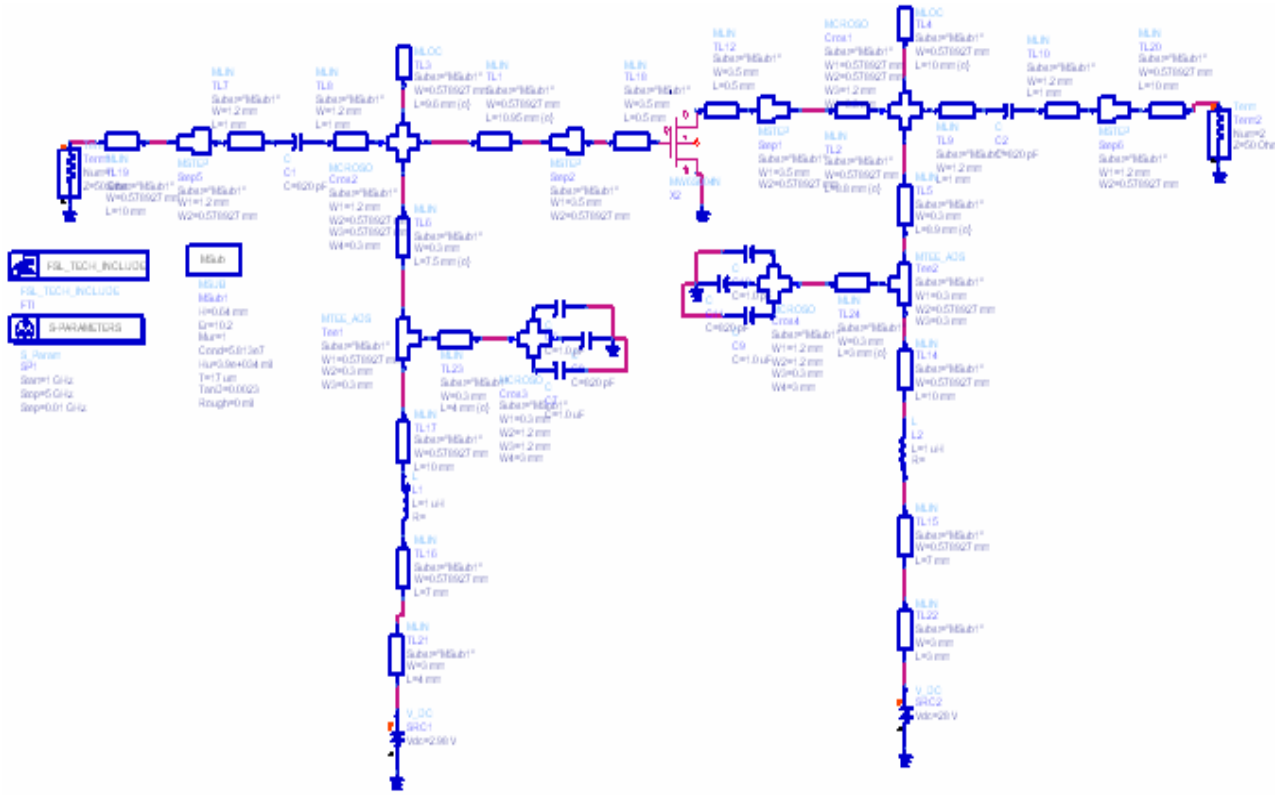


Figure 5.18 Final design

The dimensions of the final design are presented in Annex A.

The optimization of the design covered both bias and matching networks. To achieve the aimed performance, manual optimization was used. In fact, as the transistor was amplifying outside his typical frequency range, the performance of the system was sensible to any small adjustment in the line's lengths.
Also we should mention that the optimization was limited by the low permitted thermal power dissipation, or the safety region, which was passed by 1.9Watts. However, this value is not real and will be reduced in the laboratory adjustments. Better output power and efficiency could be achieved, but the transistor would suffer from self heating.
The results of the final optimized system, using HB1Tone, are presented in Figure 5.19.

As shown, the Pout-PAE optimizations have improved at 1dB compression point the output power and the efficiency. In fact, Pout was improved approximately by 6 dBm than previous values and reached 37.02 dBm; PAE was improved approximately by 20% and reached a value of 31.878%. However the gain dropped to 13.62 dB which is acceptable in power amplifier design.
Regarding the third harmonic, we achieved a good result as the difference between the fundamental output power and the third harmonic was 52.4 dB.

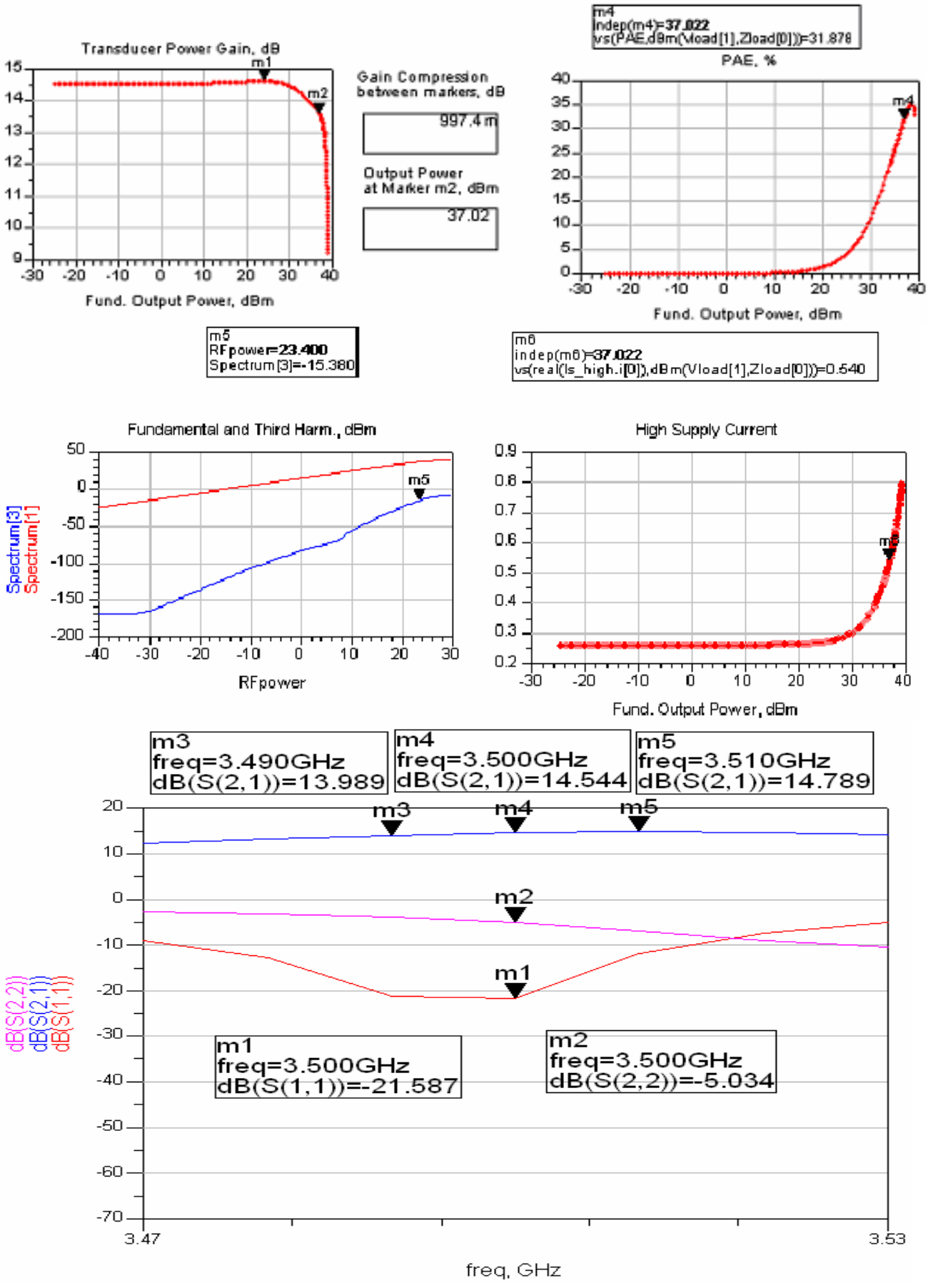


Figure 5.19 Performance of the final design (HB1Tone).

More simulation results regarding dissipated power, harmonics outputs till the fifth are shown in Table 5.2.

Available Source Power dBm	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
0.0000	-48.89	-98.14	-107.2	-126.7
1.000	-48.02	-97.03	-105.3	-124.7
2.000	-47.17	-96.09	-103.5	-121.8
3.000	-46.33	-95.36	-101.9	-118.5
4.000	-45.49	-94.84	-100.5	-115.8
5.000	-44.65	-94.32	-99.40	-114.5
6.000	-43.79	-93.36	-98.75	-115.0
7.000	-42.90	-91.47	-98.64	-117.2
8.000	-41.98	-88.53	-99.14	-114.0
9.000	-41.03	-85.10	-100.4	-107.8
10.00	-40.08	-81.77	-102.4	-103.9
11.00	-39.13	-78.77	-104.0	-102.4
12.00	-38.19	-76.07	-104.2	-102.8
13.00	-37.26	-73.52	-104.1	-103.0
14.00	-36.30	-71.07	-106.1	-101.6
15.00	-35.28	-68.65	-106.1	-99.19
16.00	-34.27	-66.33	-100.4	-98.06
17.00	-33.26	-64.18	-98.33	-97.75
18.00	-32.26	-62.16	-96.65	-96.04
19.00	-31.29	-60.22	-92.20	-92.45
20.00	-30.36	-58.44	-87.52	-87.20
23.00	-27.62	-53.10	-76.63	-77.44
23.05	-27.57	-53.01	-76.54	-77.29
23.10	-27.52	-52.92	-76.44	-77.14
23.15	-27.47	-52.83	-76.35	-76.99
23.20	-27.42	-52.75	-76.27	-76.84
23.25	-27.37	-52.66	-76.19	-76.69
23.30	-27.32	-52.57	-76.12	-76.54
23.35	-27.27	-52.49	-76.05	-76.40
23.40	-27.22	-52.40	-75.99	-76.25
23.45	-27.16	-52.32	-75.93	-76.11
23.50	-27.11	-52.23	-75.89	-75.96

Available Source Power dBm	Fundamental Output Power dBm	Transducer Power Gain	Power- Added Efficiency, %	DC Power Consumpt. Watts	High Supply Current	Thermal Dissipation Watts
0.000	14.570	14.570	0.377	7.323	0.262	7.295
1.000	15.575	14.575	0.475	7.331	0.262	7.296
2.000	16.581	14.581	0.598	7.341	0.262	7.297
3.000	17.587	14.587	0.753	7.353	0.263	7.298
4.000	18.594	14.594	0.948	7.369	0.263	7.299
5.000	19.601	14.601	1.192	7.389	0.264	7.301
6.000	20.608	14.608	1.498	7.414	0.265	7.303
7.000	21.614	14.614	1.880	7.445	0.266	7.305
8.000	22.618	14.618	2.357	7.485	0.267	7.309
9.000	23.619	14.619	2.948	7.535	0.269	7.313
10.000	24.618	14.618	3.680	7.598	0.271	7.318
11.000	25.613	14.613	4.579	7.677	0.274	7.326
12.000	26.602	14.602	5.675	7.777	0.278	7.336
13.000	27.581	14.581	6.996	7.905	0.282	7.352
14.000	28.553	14.553	8.565	8.073	0.288	7.381
15.000	29.511	14.511	10.388	8.297	0.296	7.434
16.000	30.453	14.453	12.451	8.595	0.307	7.524
17.000	31.379	14.379	14.733	8.984	0.321	7.659
18.000	32.289	14.289	17.197	9.484	0.339	7.850
19.000	33.185	14.185	19.790	10.120	0.361	8.114
20.000	34.074	14.074	22.502	10.910	0.390	8.449
23.000	36.693	13.693	30.886	14.474	0.517	9.982
23.050	36.735	13.685	31.013	14.552	0.520	10.017
23.100	36.776	13.676	31.139	14.630	0.523	10.052
23.150	36.817	13.667	31.265	14.709	0.525	10.087
23.200	36.858	13.658	31.389	14.789	0.528	10.123
23.250	36.899	13.649	31.513	14.869	0.531	10.159
23.300	36.940	13.640	31.635	14.951	0.534	10.196
23.350	36.981	13.631	31.757	15.032	0.537	10.233
23.400	37.022	13.622	31.878	15.115	0.540	10.270
23.450	37.062	13.612	31.997	15.197	0.543	10.308
23.500	37.102	13.602	32.116	15.281	0.546	10.346

Table 5.2 Optimized performance

Now to study the linear properties of the amplifier, such as the third order intermodulation (IMD3) and the third order interception point (IP3), we will use the two-tone harmonic balance simulation.
The two-tone signals used have a spacing of 10 kHz, with a 3 dB less input power than the fundamental.
The HB2TonePAE_Pswp build up design is shown in Figure 5.20.

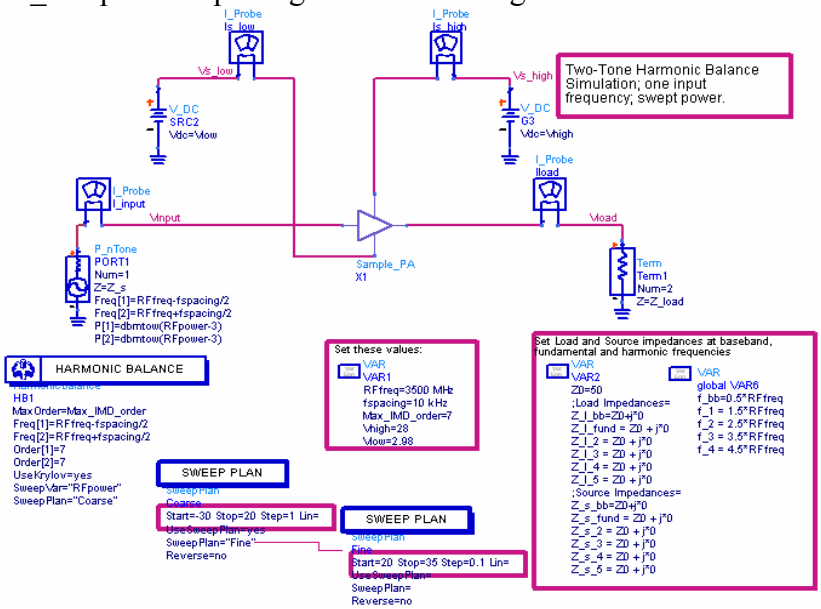
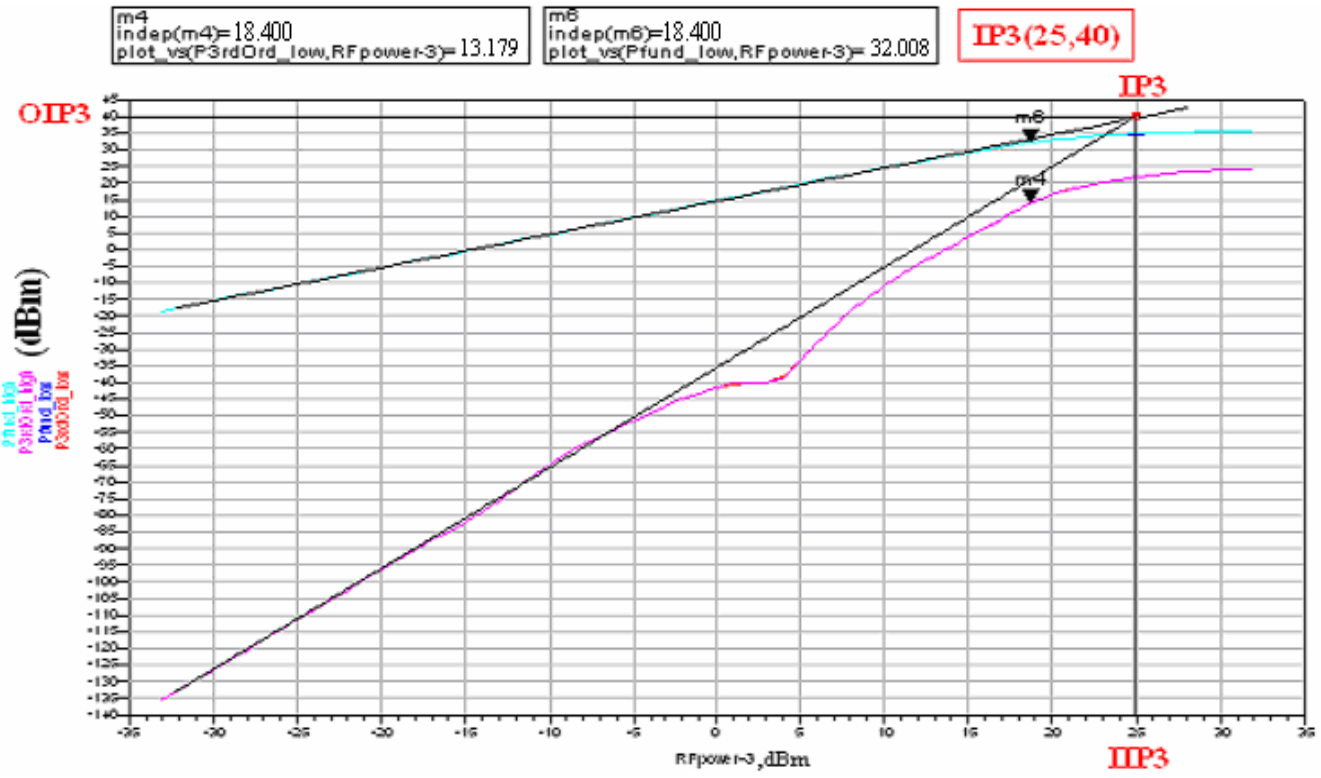


Figure 5.20 HB2Tone_Pswp

Running the simulation in a wide power range will took lot of time, so a decision has been made to use a coarse power sweep from -30 dBm to 20 dBm, and a fine power sweep from 20 dBm to 35 dBm.
The results of the simulation are shown in Figure 5.21.



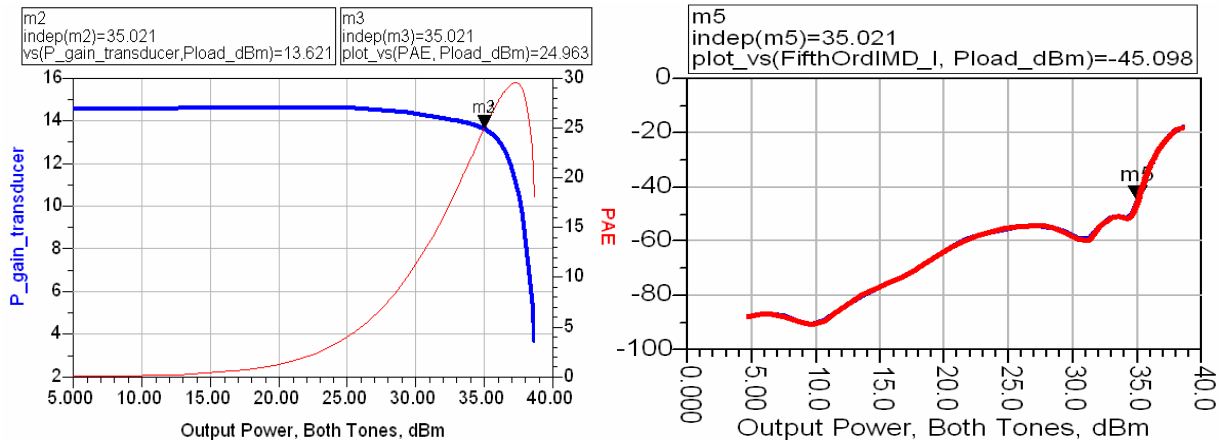


Figure 5.21 HB2Tone_Pswp results

As shown in the above figure, the 1dB-Compression point is at a total input power of 21.4 dBm, which is 2 dBm lower than in the HB1Tone_Pswp.Also the output power and the power added efficiency have dropped respectively to 35.021 dBm and 24.963%.
Regarding the third order distortion, we find that the IMR value, which is the difference between the Pfund (dBm)–IMD (dBm), is equal to 18.829 dB. Also we notice that the IP3 is for input and output value of: IIP3=25 dBm, OIP3=40 dBm.
The above values show a low performance of the system regarding intermodulation distortions.

Chapter6. Implementation and measurements

6.1 First design

ADS layout was used in the manufacturing process, and the amplifier was built on Rogers RT/DUROID 6010 board with a dielectric constant of 10.2.
Figure 6.1 shows a picture of the implemented power amplifier.

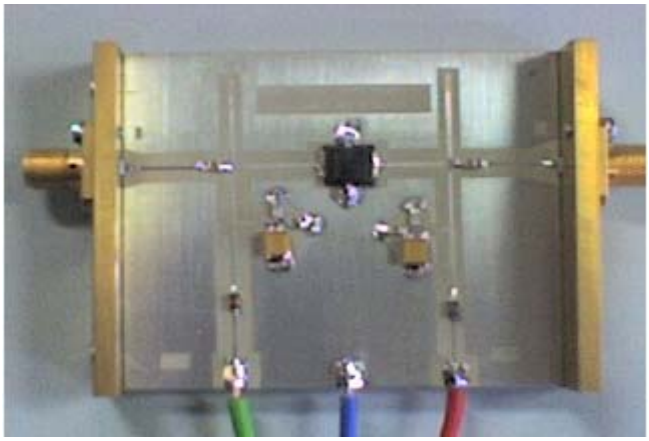


Figure 6.1 Implemented design

Multiple measurements have been made and the results showed a different behaviour compared with the ADS design and simulations (Figure 5.20 & Figure 6.2).
Figure 6.2 shows the measured S-parameters which present an unmatched output system, with a short in gain (1.712 dB) and an oscillation at 4.1 GHz.

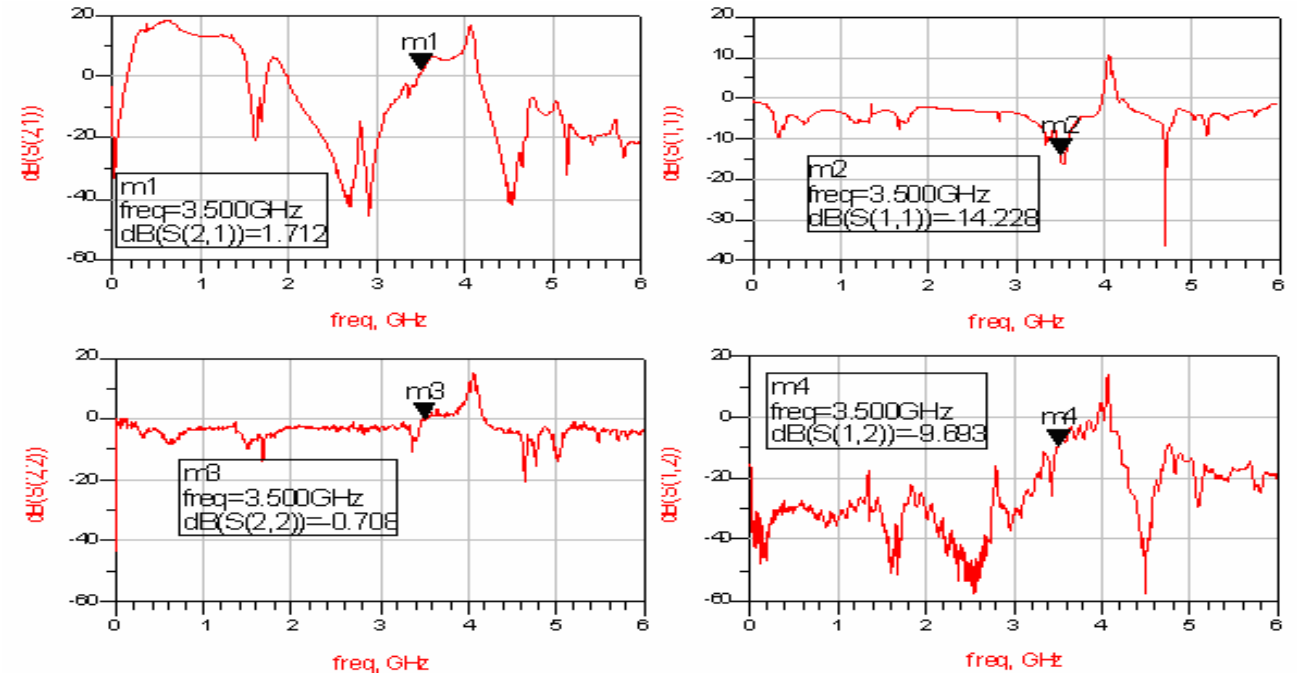


Figure 6.2 Measured S-parameters

In fact, the reason behind this mismatch and that short in gain is the non idealistic of the ADS model which is still under evaluation and improvements, and the operation frequency range of the transistor which is limited to 2GHz.
Also, a major difference in the bias behaviour of the transistor, compared with the ADS model, has been observed. In fact, the threshold of the transistor was measured near 2.9V, which have introduced a shift in the DC characteristics of the system, and lead to a gate voltage of Vgs= 3.6V, Vds=28V and Ids=260mA(In ADS, to achieve the same drain current, the gate was biased to 2.98V).
Another major problem observed in the measurements, is the high self heating of the transistor, which have reduced the achieved gain and degraded the performance of the system due to the temperature dependency of the transistor's characteristics. The main reason behind this heating problem is the poor contact between the transistor's source and the metallic base, which was supposed to be the main dissipation source of the system.
Despite of these system drawbacks, the design has shown a gain of 6 dB at a frequency of 3.6 GHz, which is a very good result regarding the fact that Si-LDMOS PAs are limited to 2 GHz and which will open the door to future improvements in the design.

6.2 Adjusted design

6.2.1 S-parameters measurements

After multiple measurements and adjustments in the bias and matching network, a better behaviour was achieved. In fact, to eliminate the oscillation, the board was soldered in all sides to the metallic and connectors base to assure a common ground level. Also, in both bias path, the inductances position has been changed and soldered directly to the capacitors to improve the $\lambda/4$ effect, and two additional capacitors of 2ρF have been soldered at the corner edge of the $\lambda/4$. The adjusted design is shown in Figure 6.3.

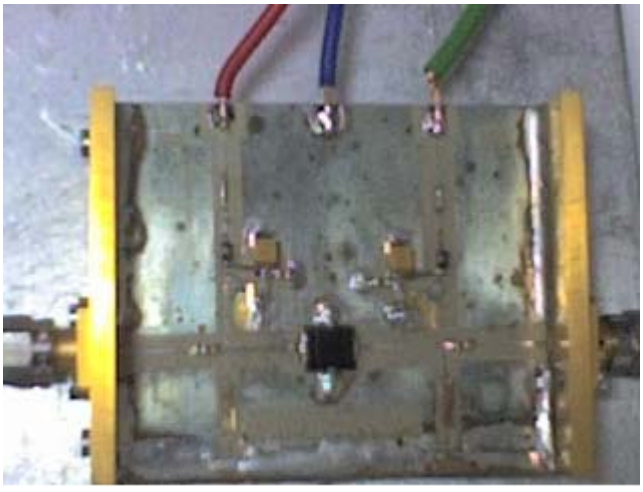


Figure 6.3 Adjusted design

For this adjusted design, a new bias point, Vds=20V, Vgs=3.6V and Ids=242mA has been chosen to reduce the heating problem, and so to improve the performance.

The measured S-parameters are shown in Figure 6.4.

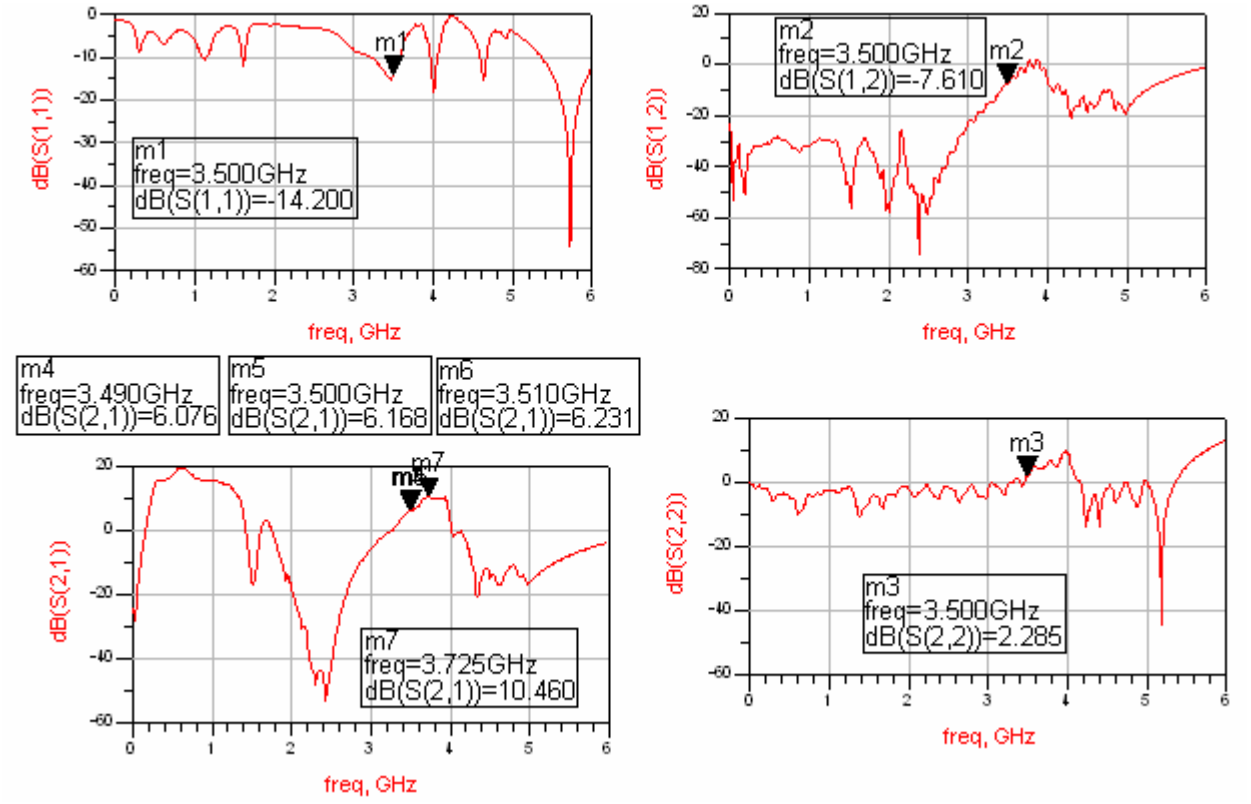


Figure6.4 Adjusted S-parameters

As shown, the performances have been improved regarding the oscillation and the gain; however it still shows a mismatch at the output. The gain have been improved by 4.5 dB, and reached a value of 6.168 dB at 3.5 GHz, with a flatness of 0.155 dB over a 20 MHz bandwidth, which is an outstanding result for a technology not supposed to operate at that frequency range.

6.2.2 Power measurements

To study the power performance of the system, we made 1Tone and 2Tones measurements.

1Tone:

The measurement block diagram is shown in Figure 6.5. The power measurement was performed using a Rohde & Schwarz spectrum analyser. Amplifier Research model was used as the driver amplifier.

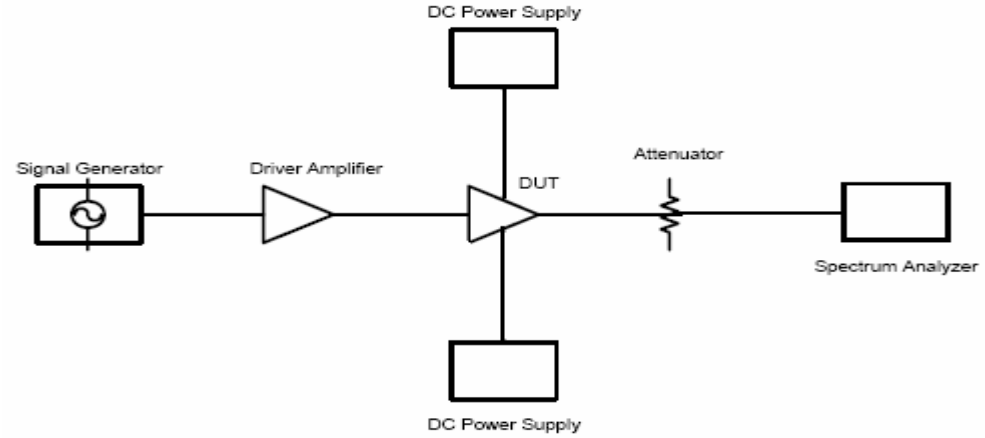


Figure 6.5 1Tone measurement block diagram

The measured gain, output power for both fundamental and third harmonic and efficiency are shown in Figures 6.6, 6.7 & 6.8.

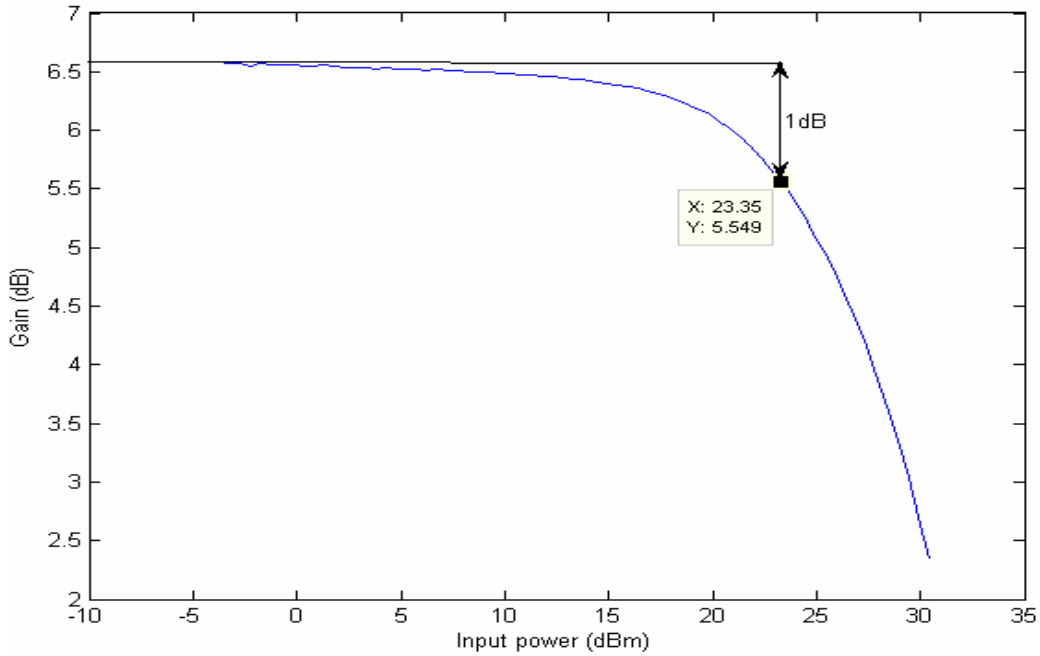


Figure 6.6 1Tone Gain

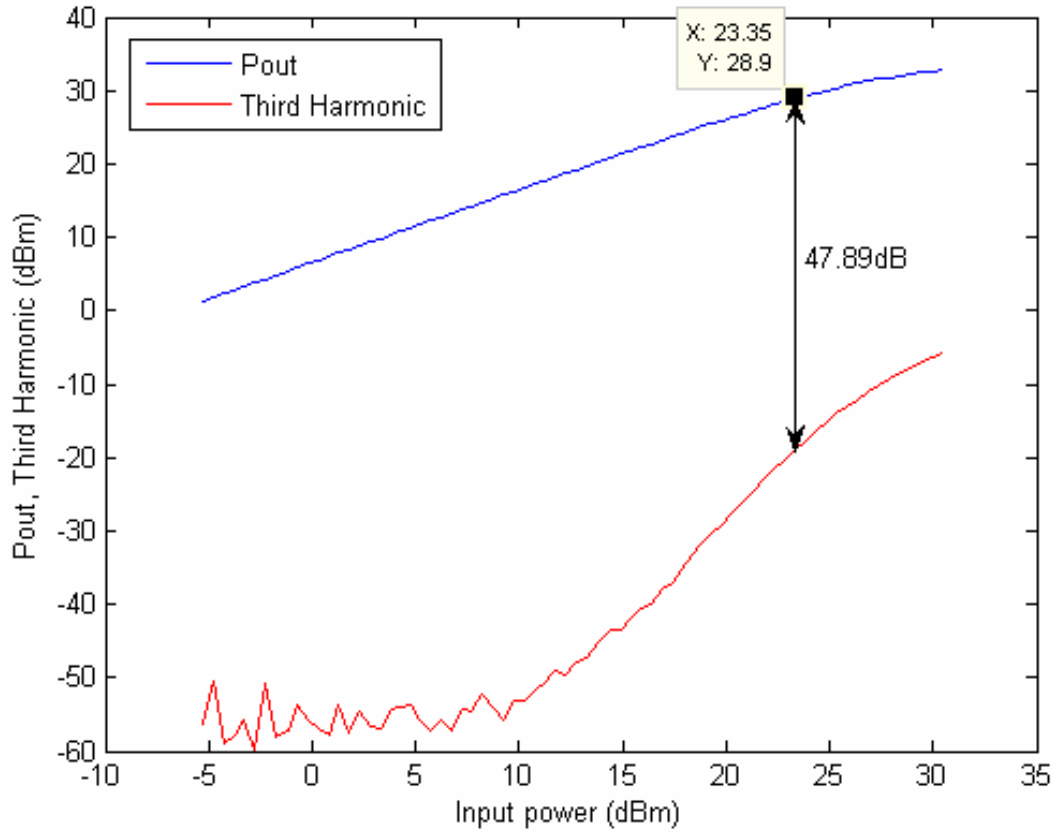


Figure 6.7 1Tone Pout & Third Harmonic

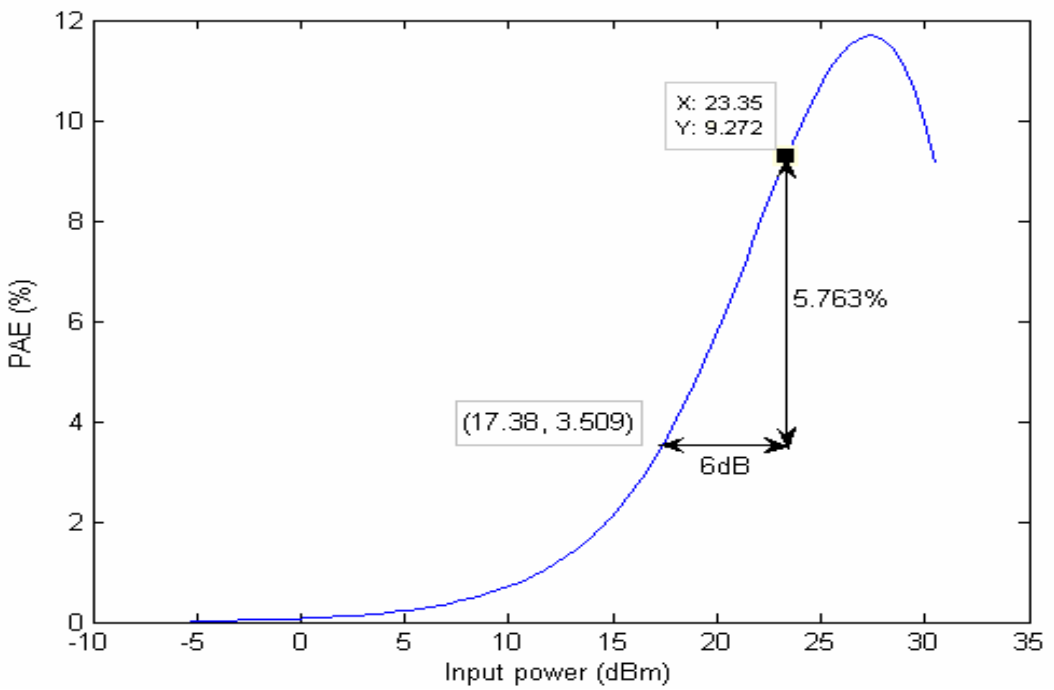


Figure 6.8 PAE

From the above figure we see that the gain of this PA at the 1dB Compression point is 5.549 dB for an output power of 28.9 dBm. This result compared with the ADS simulation (Figure 5.20), presents a short of 8.57 dB regarding both output power and gain.
Regarding the third harmonic distortion, the design shows a good performance with a P3H=-47.89 dBc.
Finally, this design presents an efficiency of 9.272% near the P1dB, and 3.509% for a 6 db backoff which is 22.6% lower than the ADS result (Figure 5.20).

2Tone:

The measurement block diagram is shown in Figure 6.9. The power measurement was performed using a Rohde & Schwarz spectrum analyser. Two amplifiers research model were used as the driver amplifiers. The RF carriers are separated by 10 KHz.

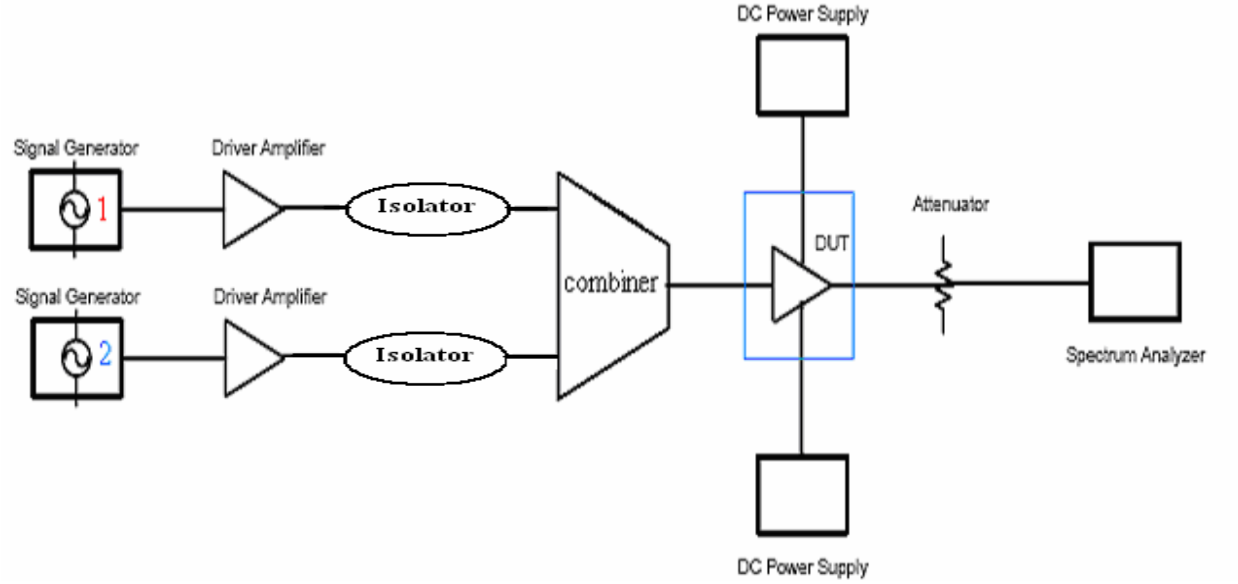


Figure 6.9 2Tones measurement block diagram

The measured gain, output power for both fundamentals and third order intermodulations and the power added efficiency are shown in Figures 6.10, 6.11 & 6.12.

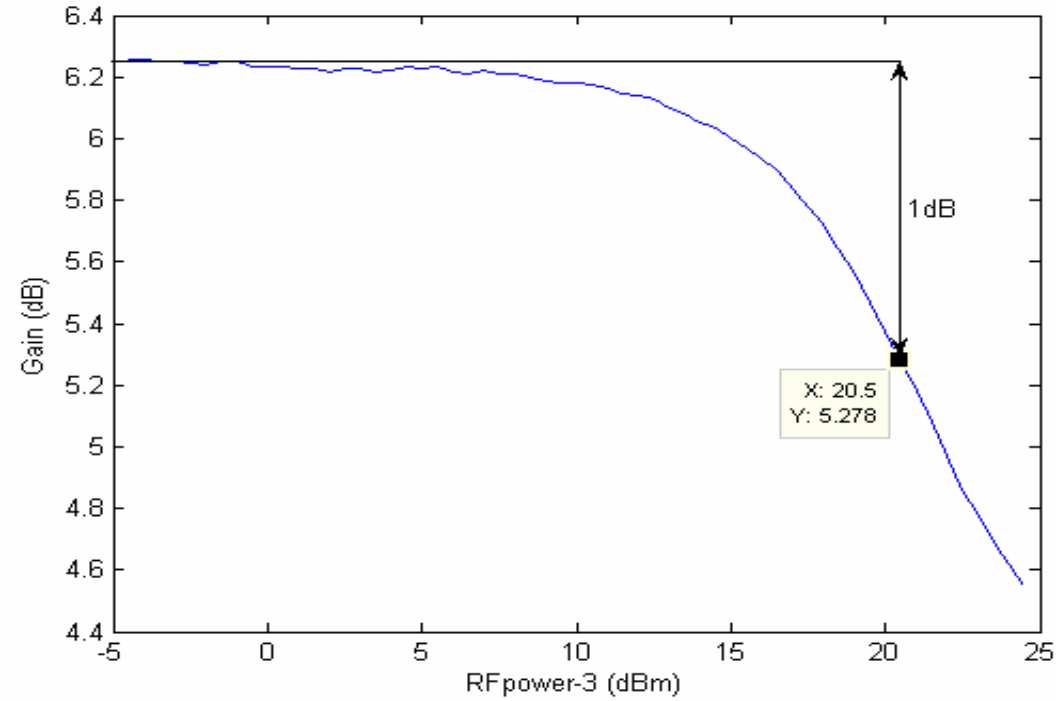


Figure 6.10 gain Vs RFpower-3

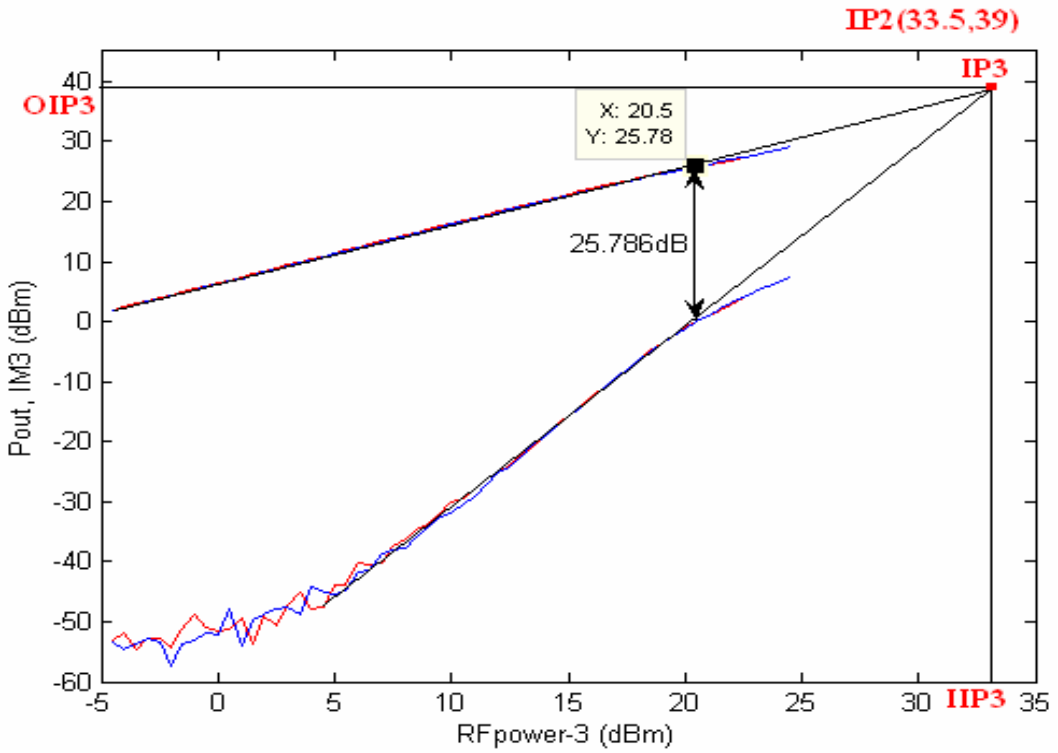


Figure 6.11 2Tones power measurements

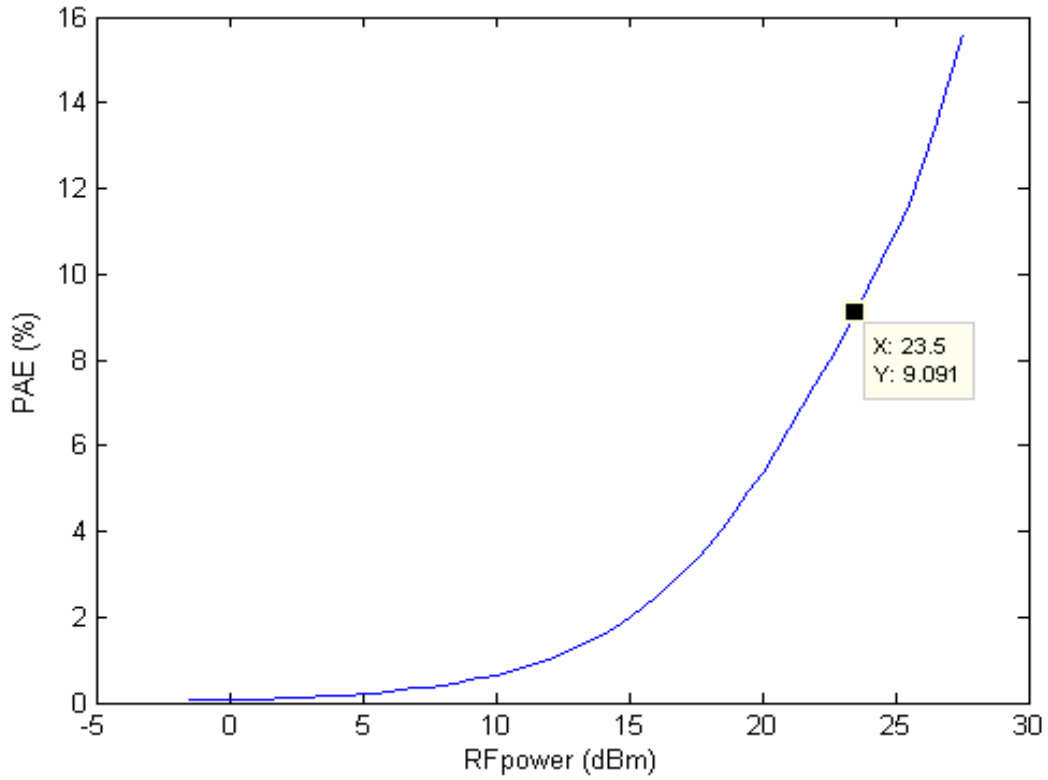


Figure 6.12 2Tones PAE

As shown, the design presents an output power of 25.78 dBm at the 1dB compression point of the fundamentals for an input power of 20.5 dBm and a gain of 5.278 dB. Also the third order interception point of the design is at IP3 (33.5 dBm, 39 dBm).
Despite the fact that the design shows a short in gain and output power compared to the ADS simulation (Figure 5.22), it presents a good improvement regarding the intermodulation distortions, which have been improved by 6dB approximately, having a value of IMD=-25.786 dBc. These results are also approved by the IP3 point whose input position has been increased by 8 dB compared to the ADS one. Regarding the efficiency, it is almost the same as in the 1Tone measurements.
Finally we should mention that the output power and gain could be improved by increasing the biasing; however in these measurements, and due to heating dissipation problem, the bias was chosen at lower value.

Despite all these lack in performance compared with the ADS one, the system is acceptable regarding the WiMAX standards. In fact, its output power is almost near the range of typical WiMAX PAs. Its efficiency at 6dB backoff is 0.5% lower than the limit range which is 4to5%, and its SNDR is 7 dB lower than the standards, 32 dB. These responses will contribute to an Error Vector Magnitude (EVM) a little higher than 2.5% which is the limit when using OFDM technology.

Chapter7. Second Design

7.1 Introduction

As base station power amplifiers demand an output power higher than 29 dBm, and as the previous design have shown a low power performance, it has been decided to redesign the PA in order to achieve these demands. Despite the fact that the ADS model has shown a weak precision, the same design have been used; however several adjustments have been added.

7.2 Adjustments

In order to achieve a higher output power, higher efficiency, higher gain and good matching, several adjustments have been made.

First, in order to reduce the mismatch, a width transformer (TAPPER) has been added at both edges of the transistor. The aim of that is to achieve width continuity in order to reduce the input and output reflections and so improving the gain.

Second, in order to improve the output power and the efficiency, the bias networks have been adjusted. In fact, in order to improve the effect of the DC-Feeding/RF-Blocking in the bias, a wide Butterfly λ/4 stub have been added at the end edge of the tight λ/4 transformers. Its effect is to insure a short level at that point, and so an open level for RF signals at the gate-drain edges. We should mention that one of the advantages of using a butterfly stub is to wider the bandwidth response of the system.

Finally, the bias point have been reduced to Vds=20V, Vgs=3.14V and Ids=370mA. In fact, the previous design was suffering from self heating which have reduced the gain and degrade the performance. So in order to solve that problem, we have reduced the security region to 7.4Watts, and so the PA thermal dissipation at the P1db compression point will remain under the permissible value stated in the data sheet (8.37Watts).

7.3 ADS Simulations and optimizations

The second design was optimized manually regarding output power and PAE as in the previous design; its schematic is shown in Figure 7.1. For manufacturing issues, and in order to assure the best effectiveness position, it has been decided to add the 1ρF capacitors after the implementation.
The dimensions of the final design are given in Annex B.
Figure 7.2 presents the simulation of the above design. As shown, the new design present a good gain and input match, however the output matching problem remains.

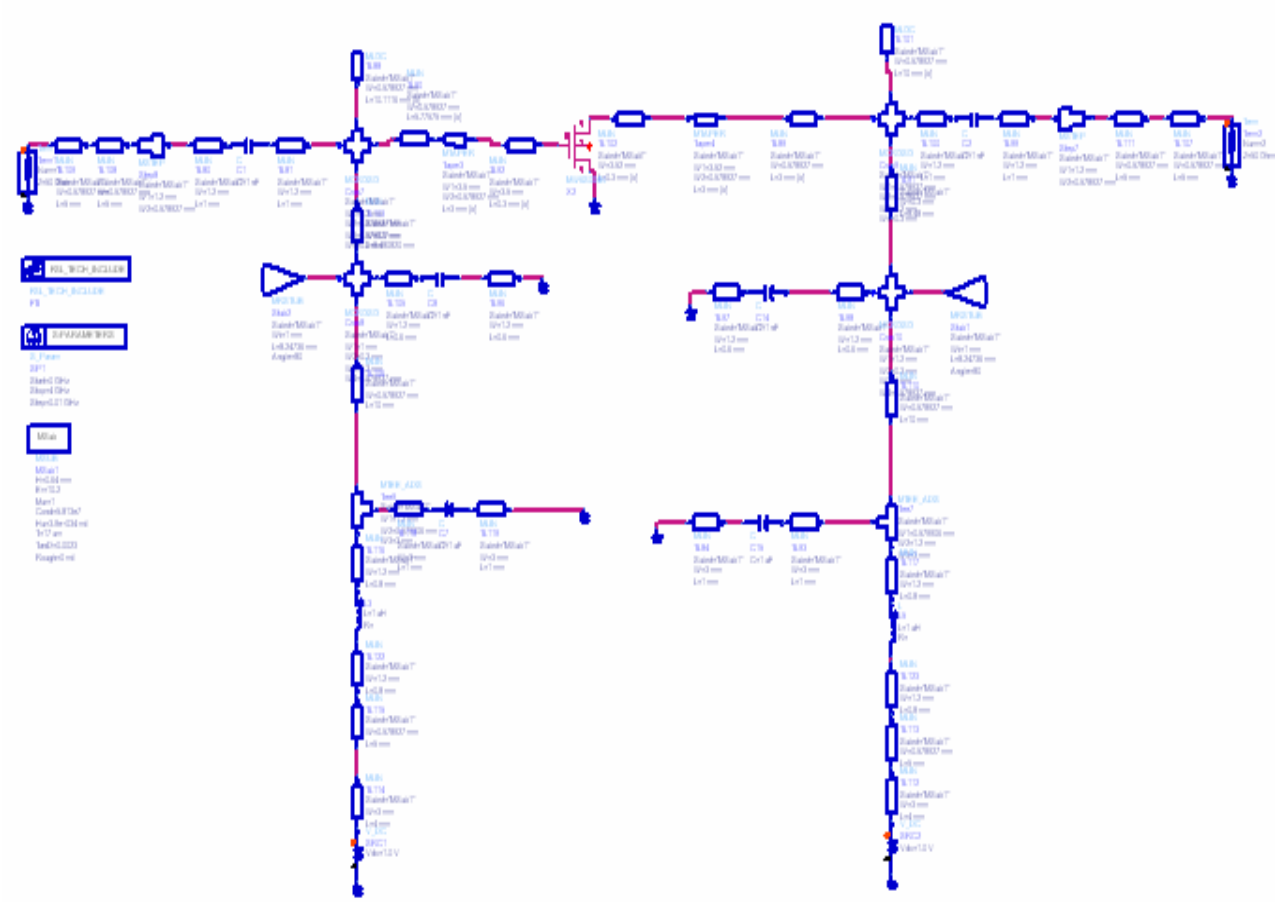


Figure 7.1 Second design

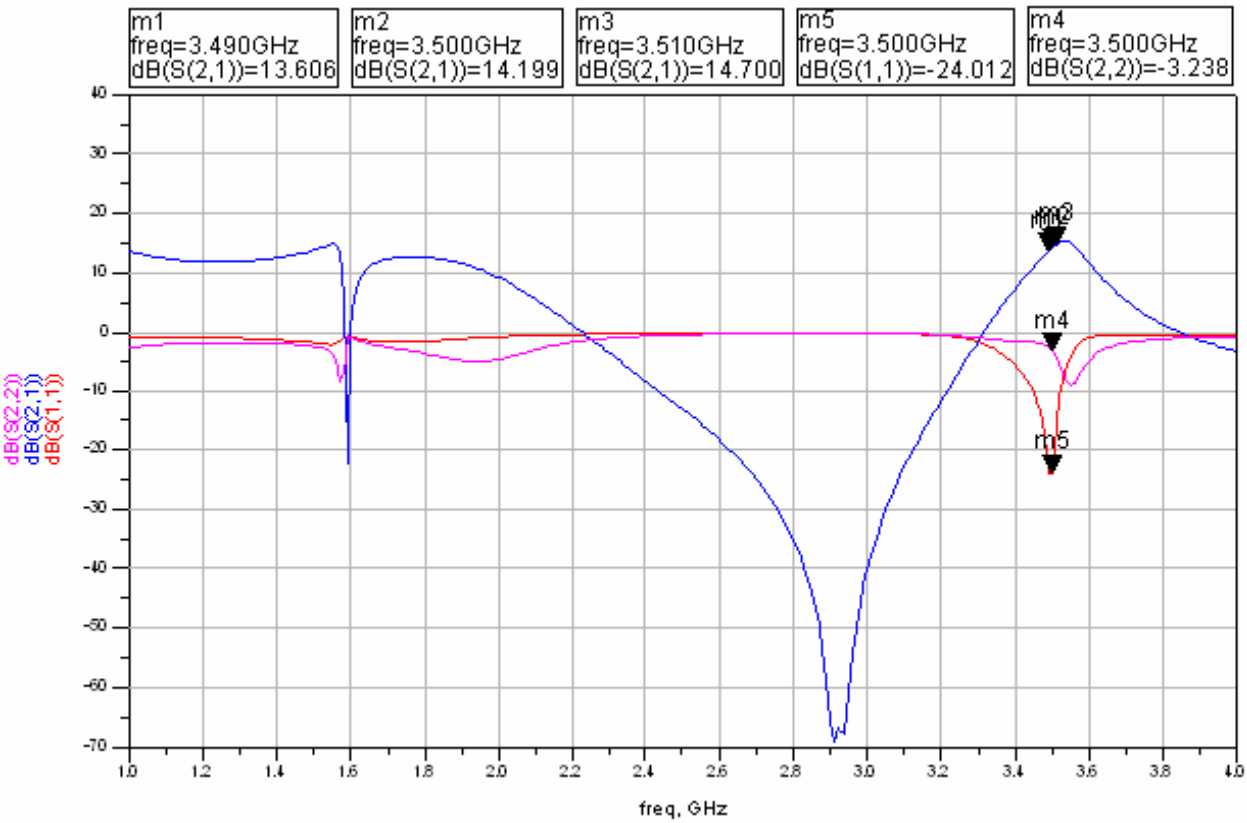


Figure 7.2 S-parameters simulation

In order to study the power performance of the new design we made 1Tone Harmonic balance simulations.
Figure 7.3 shows the results of the 1Tone simulation.

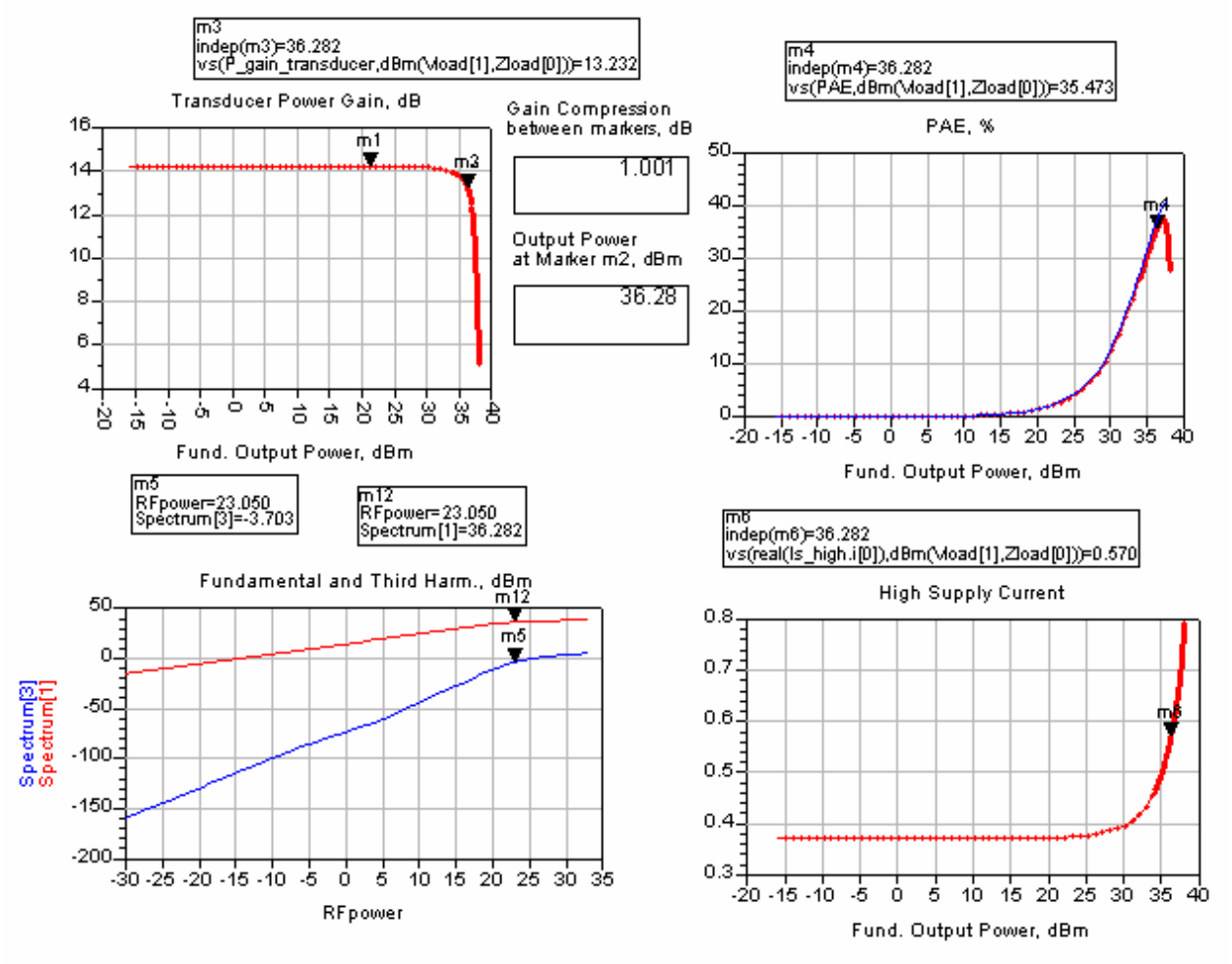


Figure 7.3 1Tone simulation

As shown above, the PAE has increased by 3.7% in comparison with the previous design. However the output power and gain are approximately the same.
Finally to study the performance of the design regarding intermodulation distortion, we made a 2Tones Harmonic Balance power measurement.
Figure 7.4&7.5 shows the results of the 2Tone simulation.

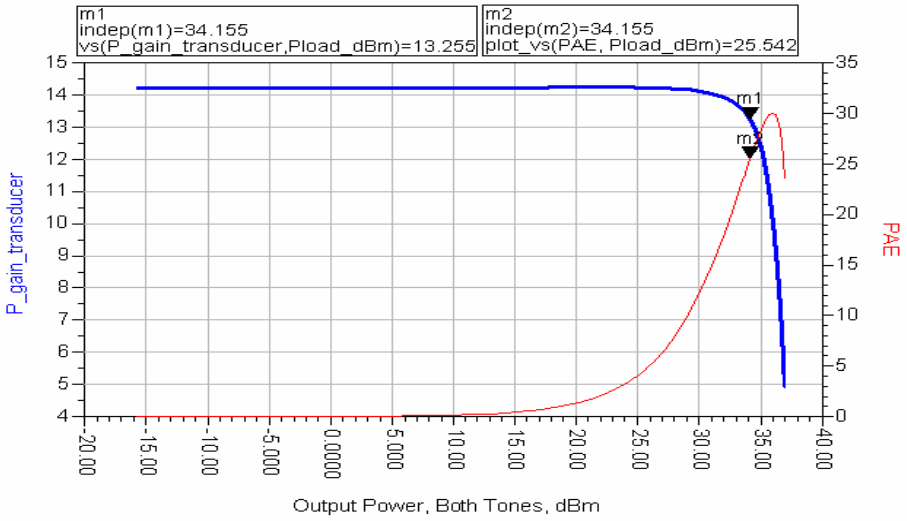


Figure 7.4 2tones simulation

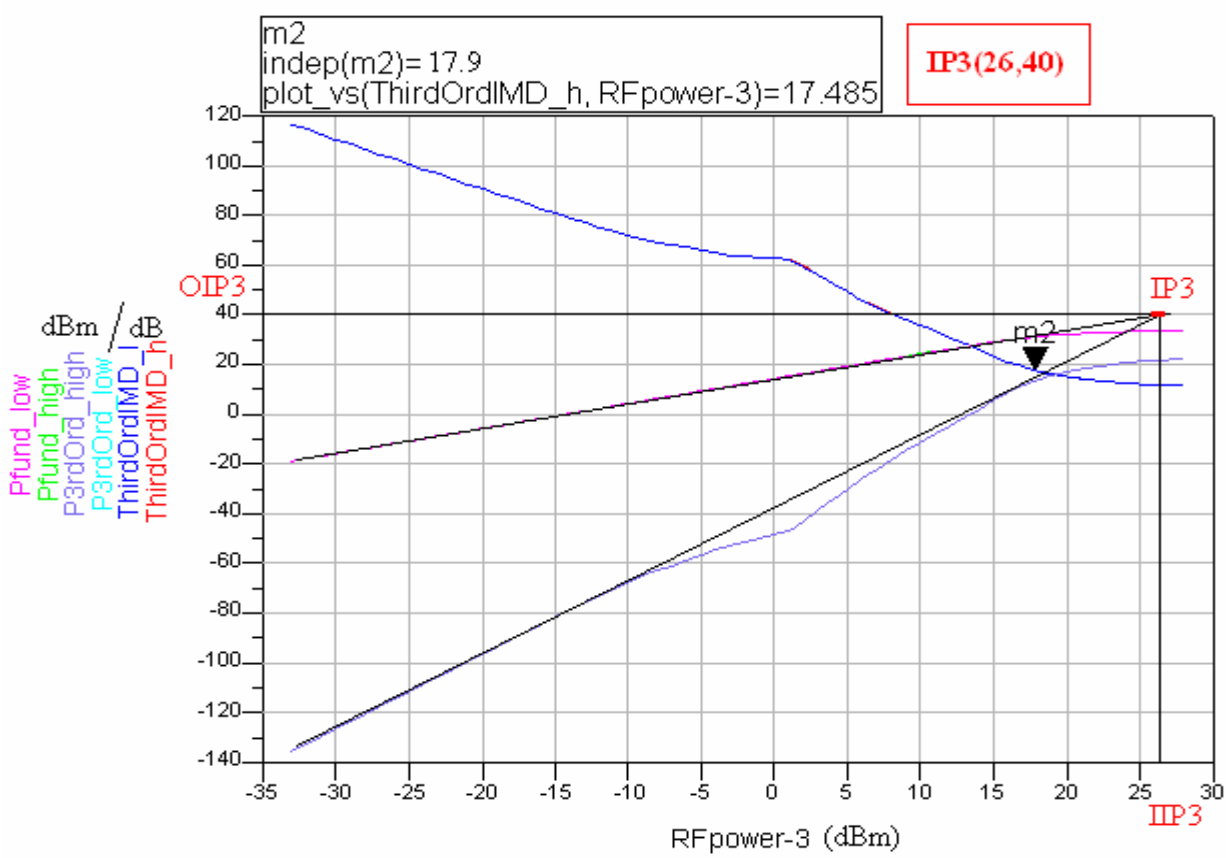


Figure 7.5 Intermodulation distortion

(In the above figure, ThirdOrdIMD is the ADS representation of the carrier to intermodulation distortion ratio, IMR)
As shown in the above figure, the 1dB-Compression point is at a total input power of 20.9 dBm, which is 2.15 dBm lower than in the HB1Tone_Pswp.Also the output power and the power added efficiency have dropped respectively to 34.155 dBm and 25.542%.
Regarding the third order distortion, we find that the IMR value, which is the carrier to intermodulation ratio, is equal to 17.485 dB. Also we notice that the IP3 is for input and output value of: IIP3=26 dBm, OIP3=40 dBm.

7.4 Manufacturing

ADS layout was used in the manufacturing process, and the amplifier was built on Rogers RT/DUROID 6010 board with a dielectric constant of 10.2.
As in the previous design, the system showed a different behaviour compared with the ADS design. It presented an unmatched output system of S22=8 dB, with a short in gain (6 dB) and an oscillation (a peak) at 3.85GHz. The main reason behind that peak is the internal feedback in the transistor, whose aim was to improve the stability of the transistor at a specific frequency band (till 2GHz), however this phenomena at 3.5GHz was transformed into a positive feedback, which create a gain peak of 24 dB at 3.85GHz (the peaks appear in S11-S22-S21 with different values).
Also the design presented a shift in the DC bias and a better heat dissipation in the whole system. However, his gain decreased as the temperature raised; for that reason it was decided to do the measurement for a bias gate current of 270mA.
We tried different adjustment in matching and bias network to improve the design, we eliminate the gain peak however the system remain unmatched at the output. (We should mention that the adjustments of the design were difficult due to the relation between the input and the output; any

change in the output affected the input, and any improvement of the output match reduced the gain).
Despite the fact that the output mismatch could be decreased to 2 dB, at the cost of the gain, we have decided to adjust the design in order to achieve a higher gain.
Figure 7.6 represents the adjusted design for a bias point of Vds=20V, Ids=270mA and Vgs=3.62V. As shown the only adjustment was made to the output matching stub by increasing his length of approximately 3.2mm.

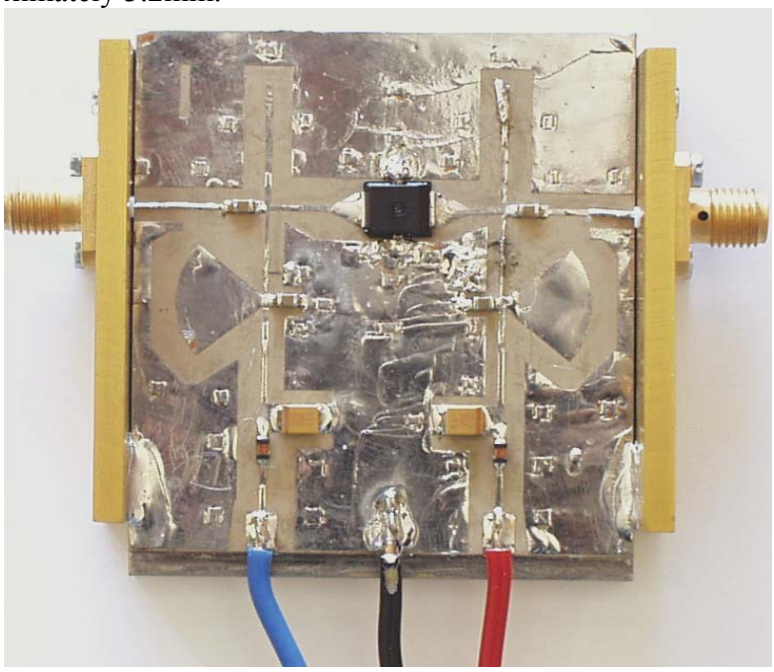


Figure 7.6 Second Design

The measured S-parameters are shown in Figures 7.7&7.8.

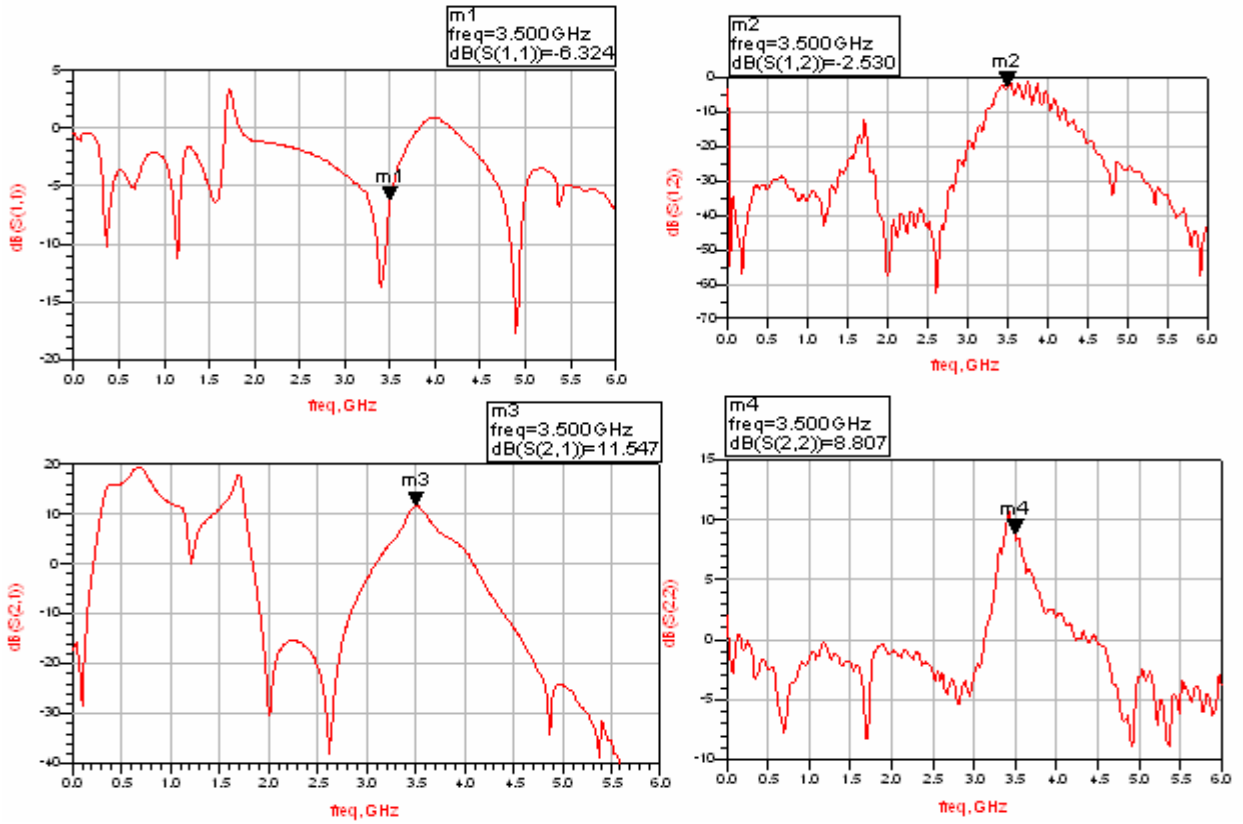


Figure 7.7 S-parameters

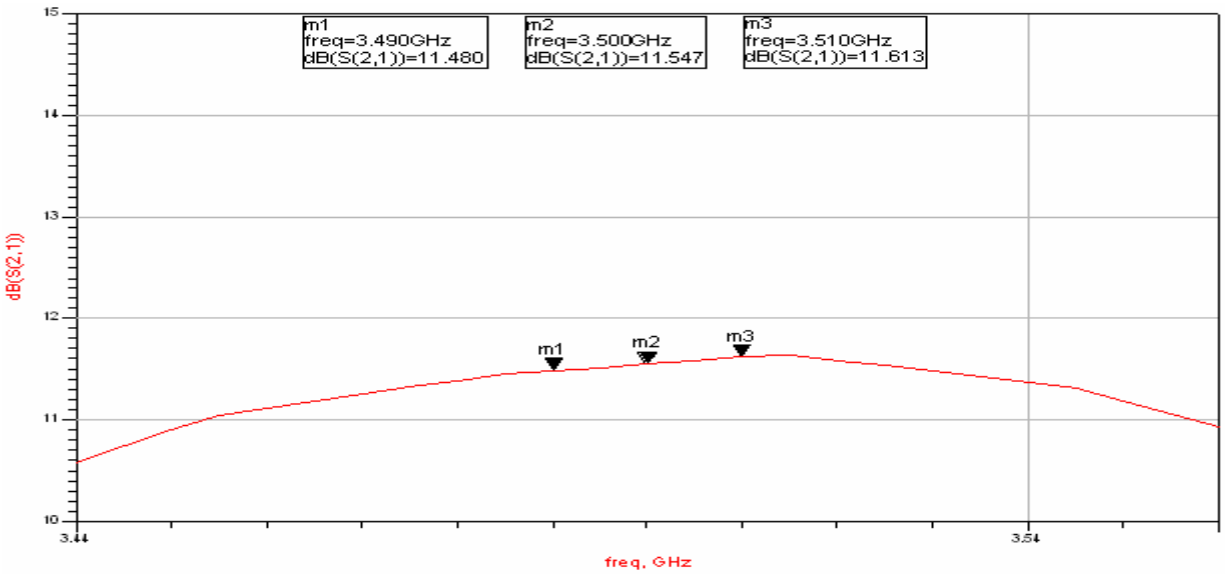


Figure 7.8 Flatness

As shown, the performance has been improved regarding the oscillation and the gain; however it still shows a high mismatch at the output. The gain has been improved to reach a value of 11.547 dB at 3.5 GHz with a remarkable flatness of ± 1dB in a 120 MHz bandwidth which is an outstanding result for a technology not supposed to operate at that frequency range.

7.5 Power measurements

To study the power performance of the system, we will do 1Tone and 2Tones measurements.

1Tone:

The measurement block diagram is shown in Figure 7.9. The power measurement was performed using a Rohde & Schwarz spectrum analyser. Amplifier Research model is used as the driver amplifier.

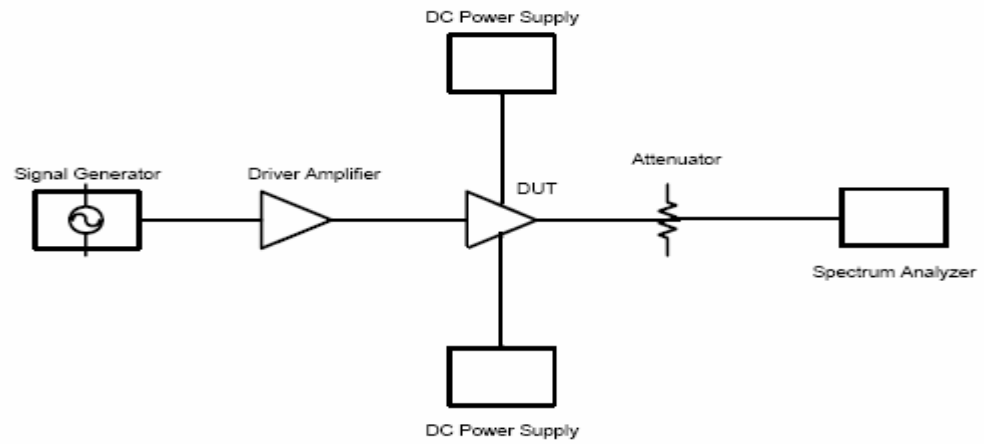


Figure 7.9 1Tone measurement block diagram

The measured gain, output power for both fundamental and third harmonic and efficiency are shown in Figures 7.10, 7.11&7.12.

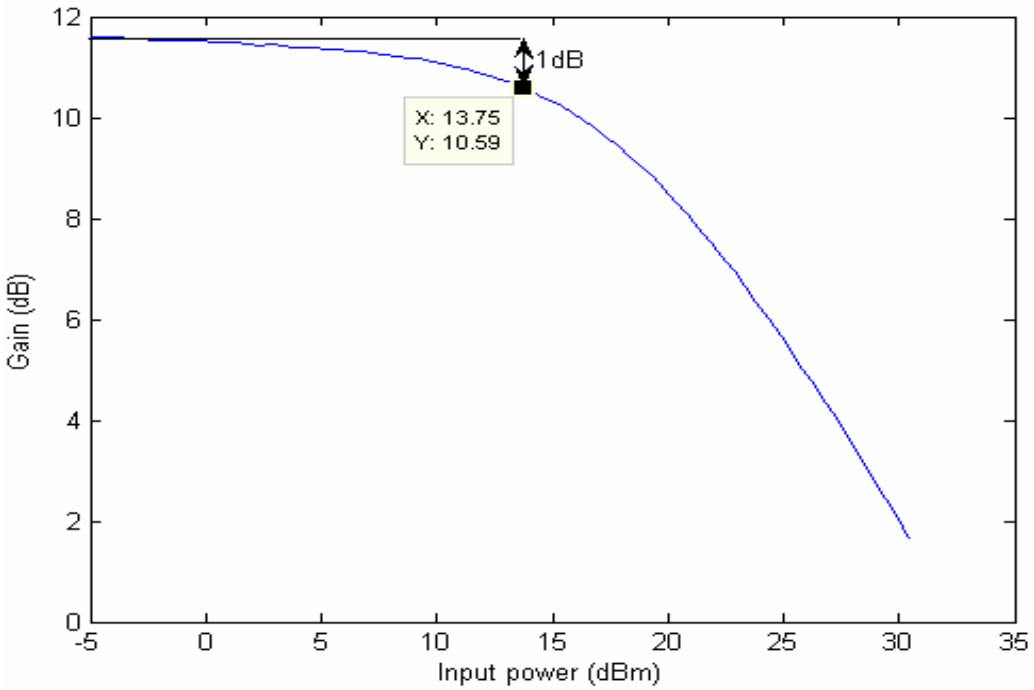


Figure 7.10 1Tone Gain

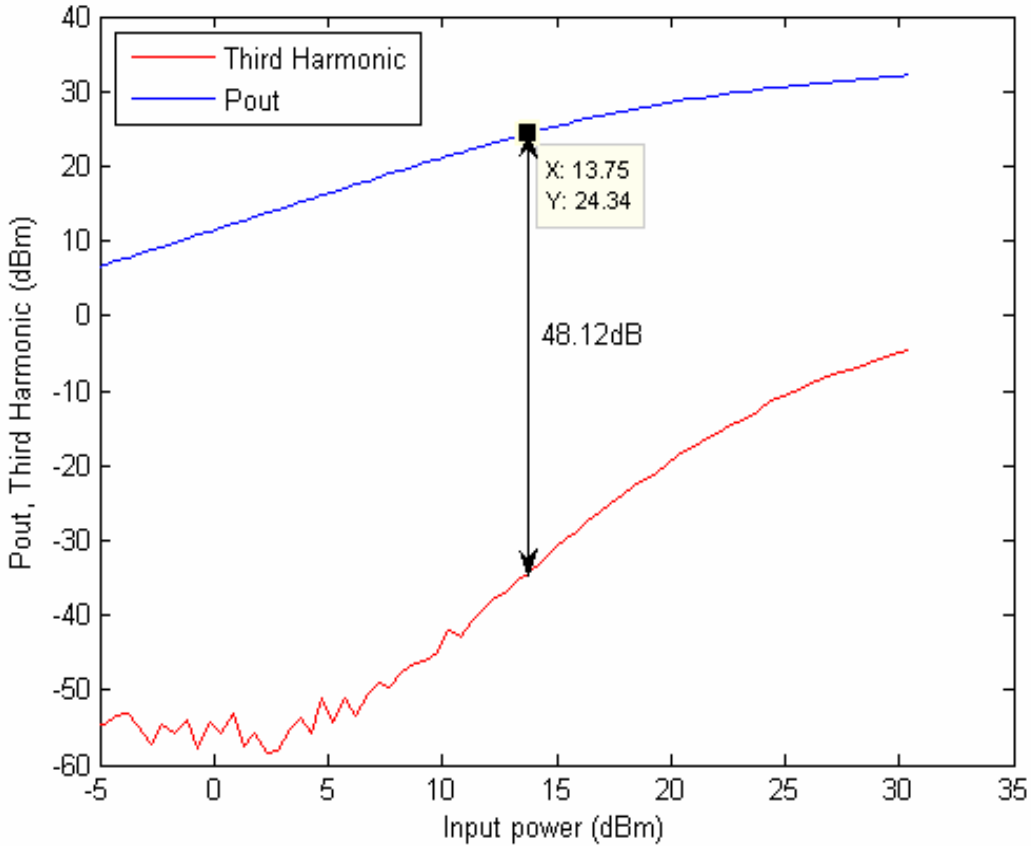


Figure 7.11 1Tone Pout & Third Harmonic

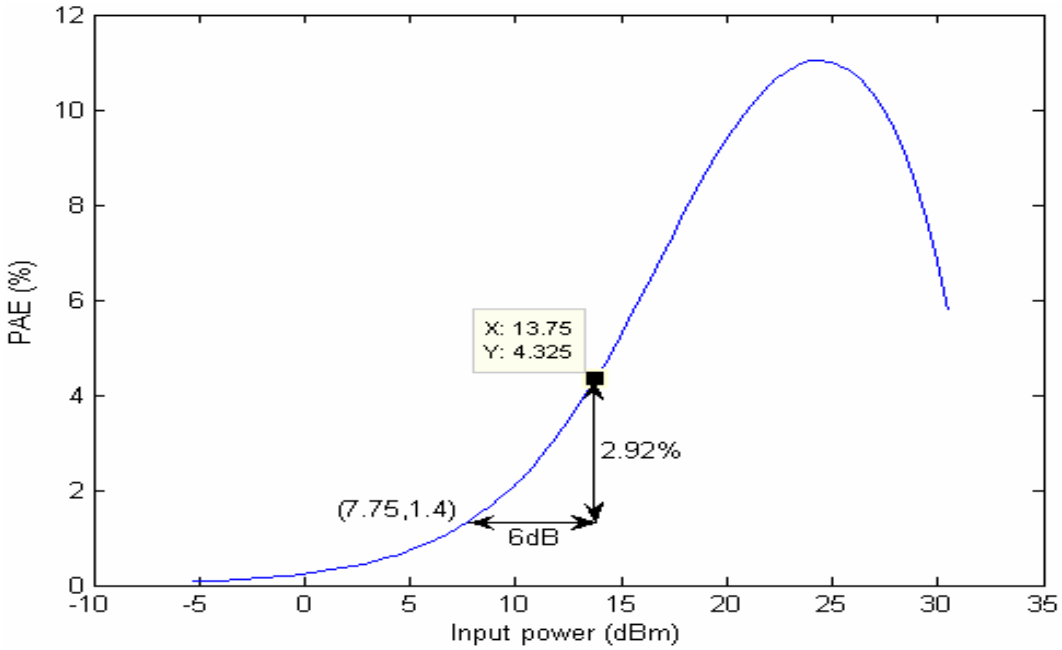


Figure 7.12 PAE

From the above figure we see that the gain of this PA at the 1dB Compression point is 10.59 dB for an output power of 24.34 dBm. Regarding the efficiency, the design show a low performance with a PAE=4.325% near the P1dB, and 1.4% for a 6 dB backoff.
Regarding the third harmonic distortion, the design show a good performance with a P3H=-48.12 dBc.
Despite the fact that we increased the gain of the system by 5.041 dB compared with the previous design, the output power has decreased by 4.56 dB. This short in output power, and so in efficiency is due to the fact that when we adjusted the output matching network in order to eliminate the gain peak, we have changed the load of the system, and so the amplifier became optimized for higher gain and not for higher power.

2Tone:

The measurement block diagram is shown in Figure 7.13. The power measurement was performed using a Rohde & Schwarz spectrum analyser. Two amplifiers research model were used as the driver amplifiers. The RF carriers are separated by 10 kHz.

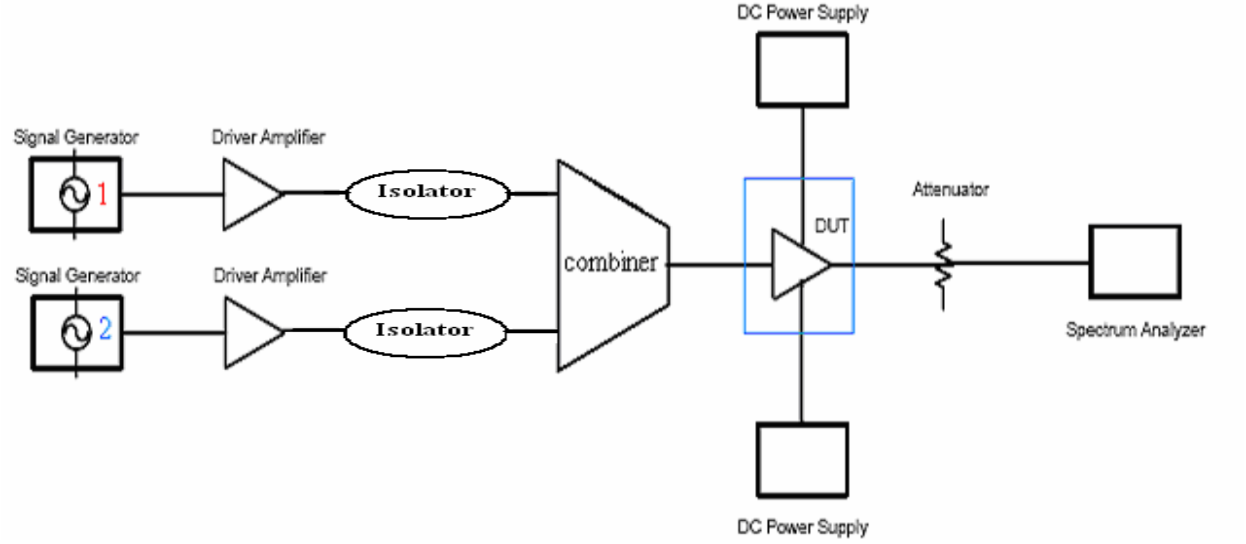


Figure 7.13 2Tones measurement block diagram

The measured gain and output power for both fundamentals and third order intermodulations are shown in Figures 7.14&7.15.

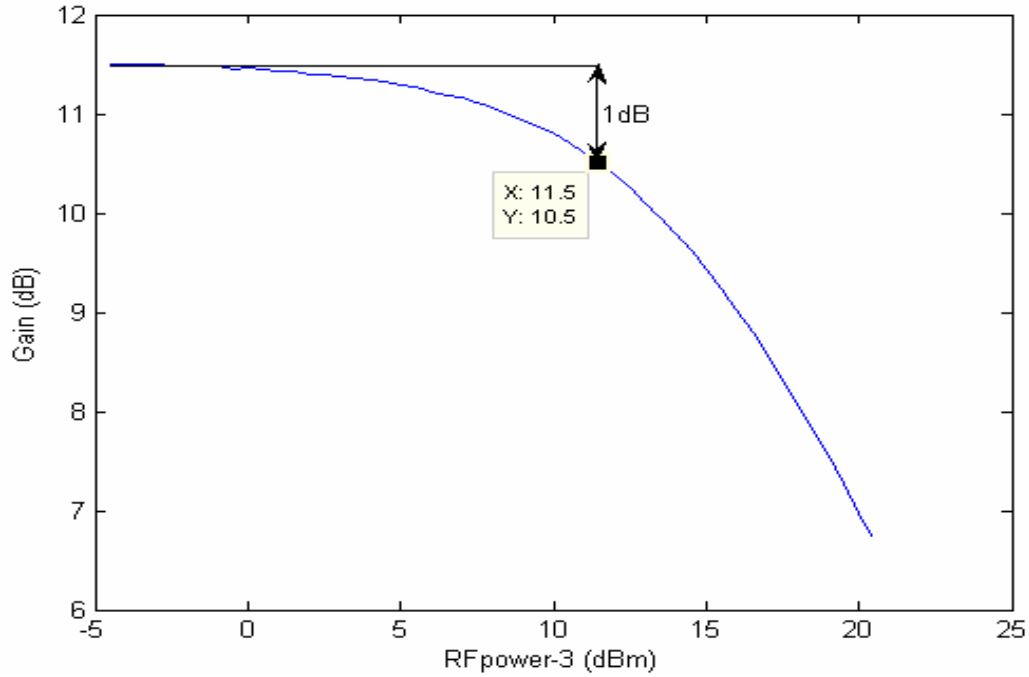


Figure 7.14 gain Vs RFpower-3

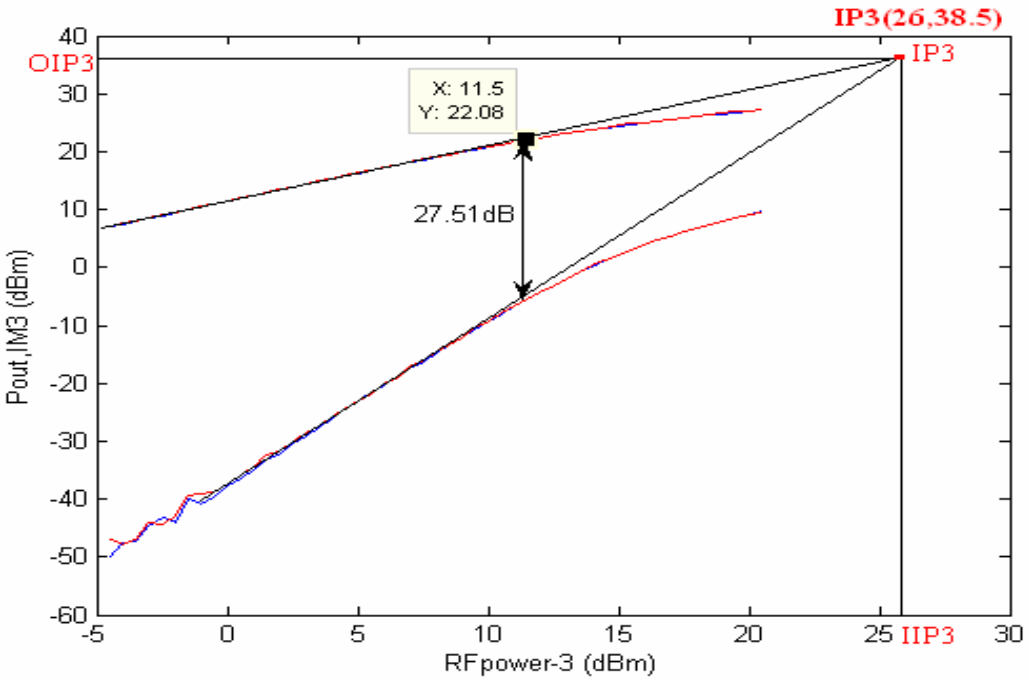


Figure 7.15 2Tones power measurements

Regarding the intermodulation distortion, this design presents a lower performance. In fact the third order interception point (IP3) is for an input level of 26 dBm which is 6 dB lower than in the previous design.

These lacks in power performance are due to the unpredictable behaviour of the transistor at the operating frequency. In fact, any change in the bias or matching network would cause a sever variation of the power performance.

Due to the low power performance of this design, the previous one will just be considered in the following sessions.

Chapter8. Intermodulation Distortions and Memory Effects

8.1 Introduction

The new modulation technologies, such as OFDM, used in the current communication systems require highly linear system. As the power amplifier is the last block in a transmission communication link, his linearity performance is the most important, certainly as he handle the highest power level in the system. To overcome the nonlinearity problem, the amplifier should be operated in the linear region with large back-off. Nevertheless, this back-off solution reduces the efficiency and increase the power consumption and heat dissipation in the system.
Another approach is the use of external linearization techniques, such as Doherty, however their implementation presents several issues such as cost, size, effective bandwidth and difficulty of adjustment. Solving these drawbacks has possessed the interest of engineers. One of the newest linearization achievements is to optimize the PA linearity by searching large signal intermodulation distortion (IMD) sweet spots which will improve the carrier to IM3 ratios (IMR) near the 1dB compression point [15-18].

8.2 New operation class definition

Till now, the amplifier operation classes have been defined regarding the conduction angle θ, which represents the period range where the transistor is ON. This definition is applicable for a linear device having the following transfer function (TF):

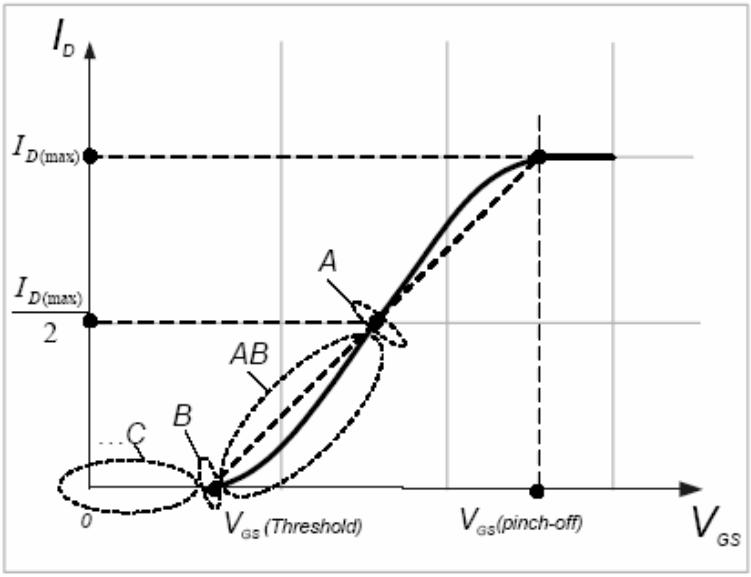


Figure 8.1 Ideal class operation [10].

However, since power amplifier devices are never linear, a new consistent definition of operation classes will be introduced [16]. The nonlinear Volterra series of the output current of a PA in function of its input voltage gives:

$$I_{out}[V_{in}(t)] = I_{out\,DC} + G^* V_{in}(t) + G_2^* V_{in}(t)^2 + G_3^* V_{in}(t)^3 + \ldots \quad (8.1)$$

Where G is the fundamental transducer gain; G_2 is the second order coefficient; G_3 is the third order coefficient which is directly related to the third, harmonic and intermodulation, distortions.

Figure 8.2 presents the variation of these small signal coefficients with the input voltage or bias point.

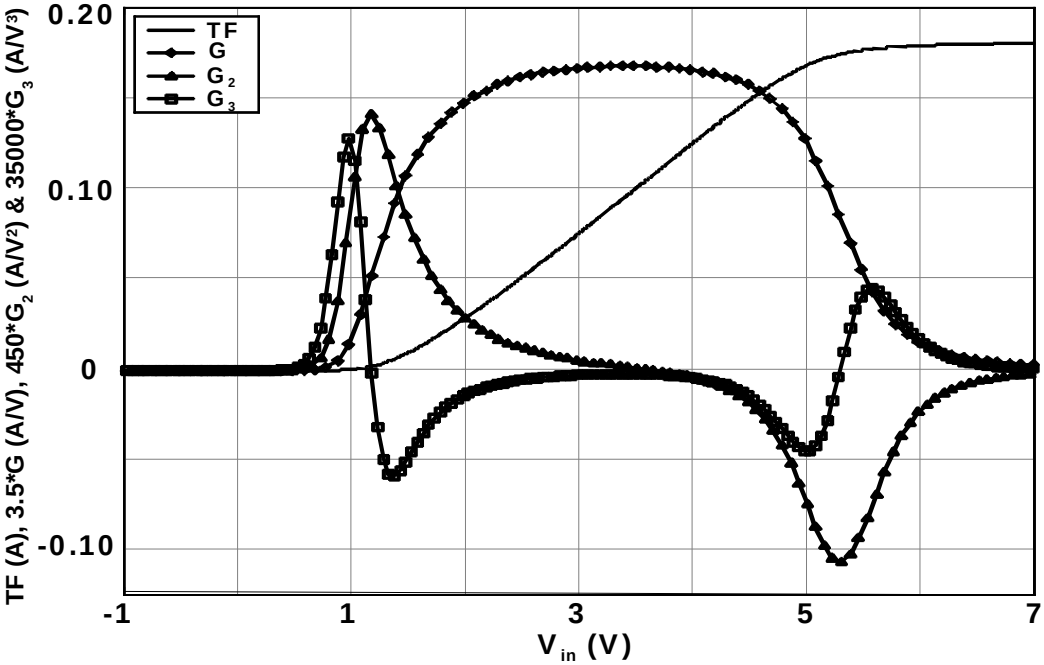


Figure 8.2 Taylor-coefficients variation [16].

The variation of G_3 shown in the above figure indicates that the third order IMD will vary in amplitude and phase with the bias point. Also it shows that $G_{3(V_{in})}$ presents a null near the threshold voltage point, V_T, of the ideal transfer function. These two conclusions lead to the new operations class definition.

If the bias point of this G_3 null point is considered as Class B, than class C will be the below biasing region and class AB and A will be the operating regimes of the PA biased above that point[16].

Moreover, we should mention that the IMD(P_{in}) characteristic of each operation class is characterised by some specific sweet spot. In fact, for large signal operation, the energy balance of the power amplifier determines its nonlinearity. As the PA becomes short in power supply, the phase of the large signal IMD sidebands, with respect to the fundamentals, tends to a constant value of 180^0 which describes its gain compression [15].

Now for a class C operation, Figure 8.2 shows that the small signal IMD phase is opposite to his large signal IMD phase, which proves that near the saturation region the IMD must reverse his phase and so a large signal sweet spot appear.

For class AB, despite the fact that both small and large signal IMD phase are coincident, both in opposite phase with the fundamental, a transition region from 180^0 to 0^0 occur at low output power which generates an IMD sweet spot. After that point, the IMD presents an opposite phase to the large signal IMD, and thus a new sweet spot appear near the 1dB compression region.

Finally in the class A scenario, small and large signal IMD phases are coincident, both opposite to the fundamental, and thus no large signal sweet spot is occurred. Further details on the theoretical explanation of this behaviour can be found in [17-18].

Figure 8.3 shows the general sweet spot representation in the IMD characteristics for different class levels.

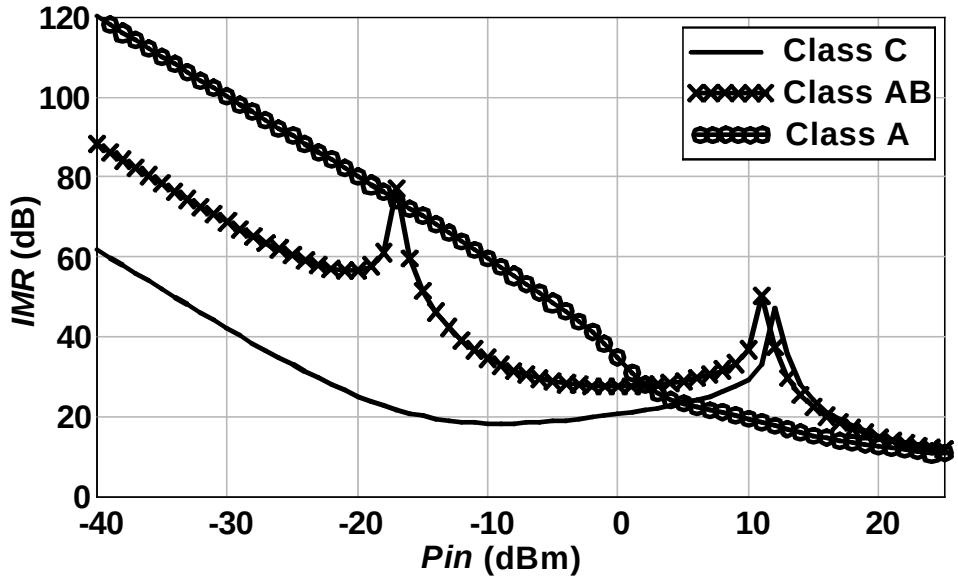


Figure 8.3 IMD sweet spots [16].

8.3 Class simulations and measurements

In this section, we will analyse and find the classes operation of the first design using ADS simulations and measurements.

8.3.1 ADS simulations

HB2Tone simulation is used with RFpower fixed at 0 dBm for small signal analysis, while the gate voltage swept between 1 and 4V (fspacing=10 kHz). The results are shown in Figure 8.4.

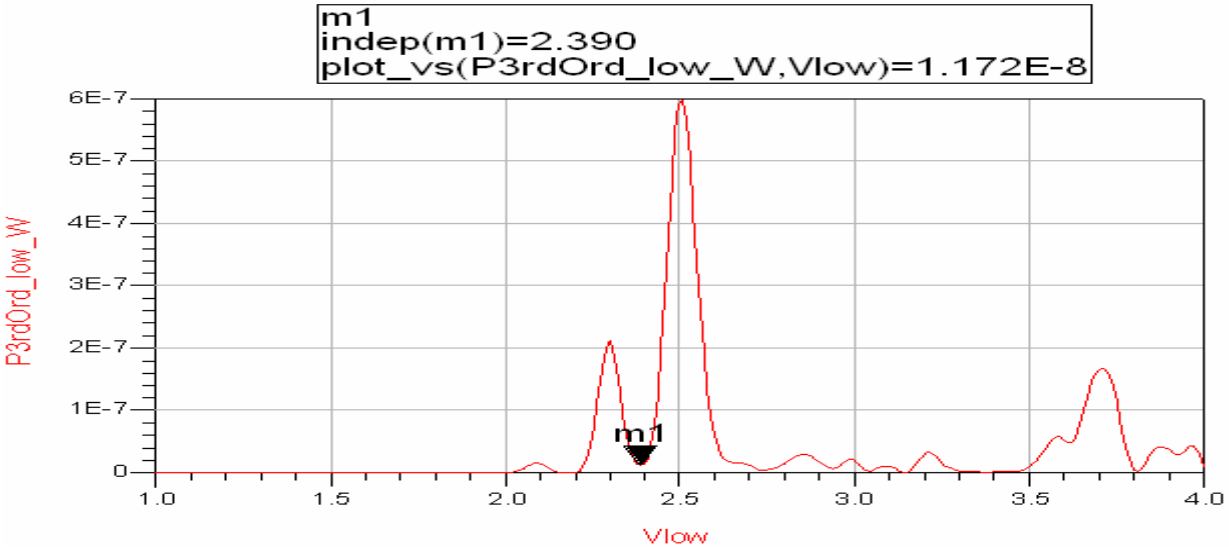


Figure 8.4 IM3 vs. Vlow@0dBm

As shown in the above figure and explained previously, the IM3 (v_{low}) presents a null near the threshold voltage point, for a gate bias of Vgs=2.39V. Due to that, and after multiple simulations, we will choose class AB to be at a bias point of 2.425V (7.81mA), class B at 2.39V (5.27mA) and class C at 2.25V (0.821mA); (Class A at 2.98V, 260mA).
Simulating the design for class A, AB and C respectively, using HB1Tone and HB2Tone, we obtained the following:

Class A:

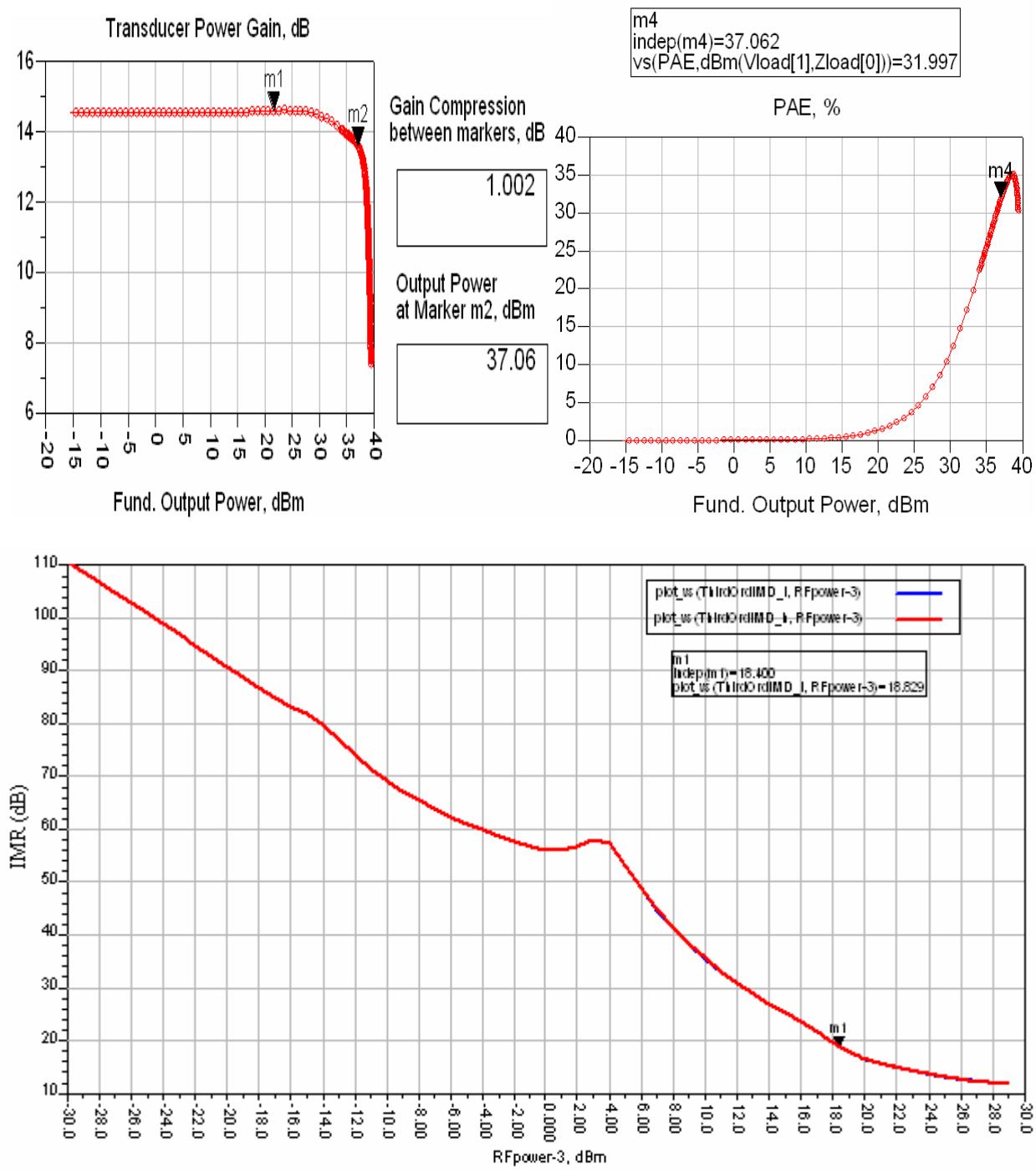


Figure 8.5 Class A

Class AB:

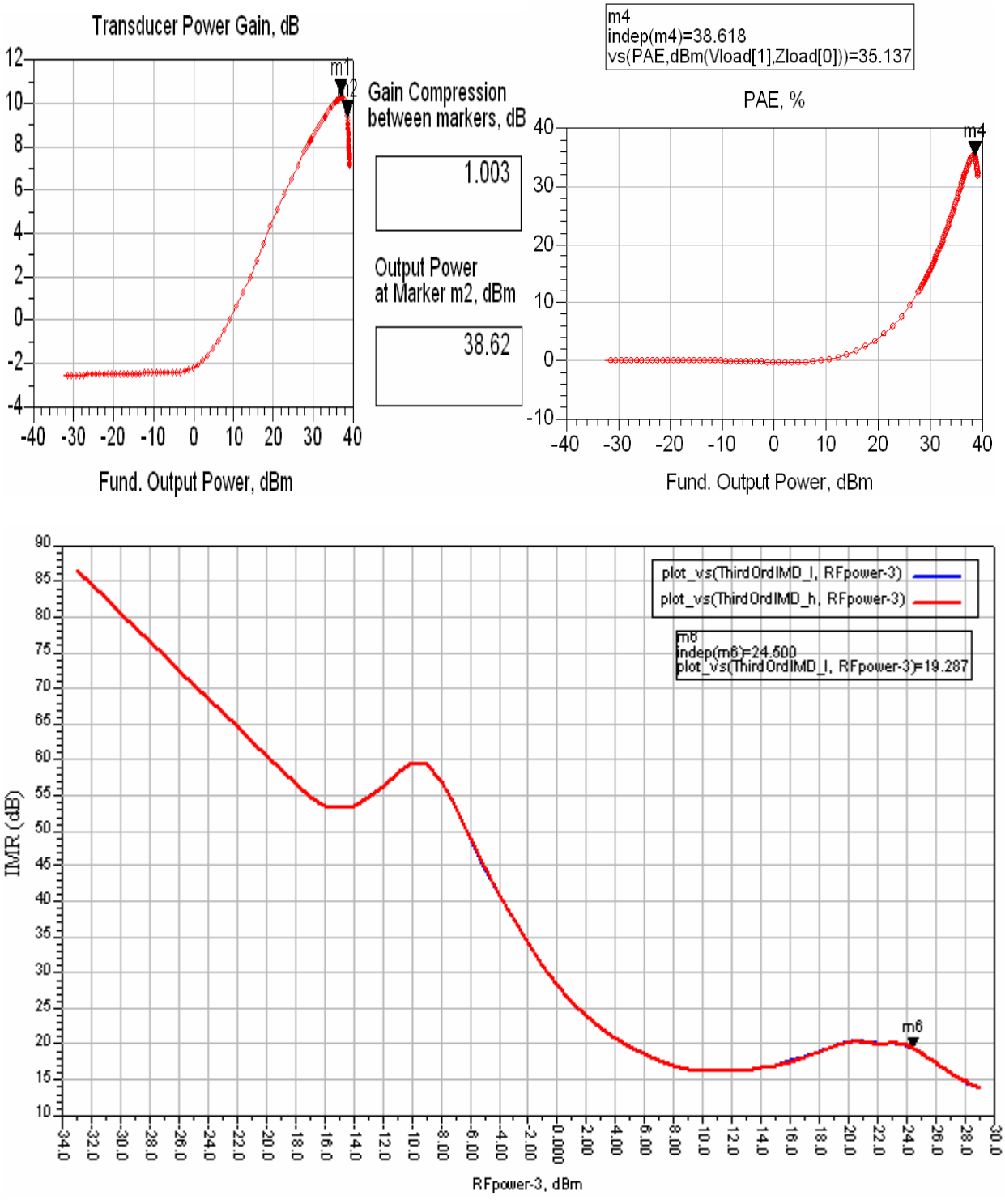


Figure 8.6 Class AB

Class C:

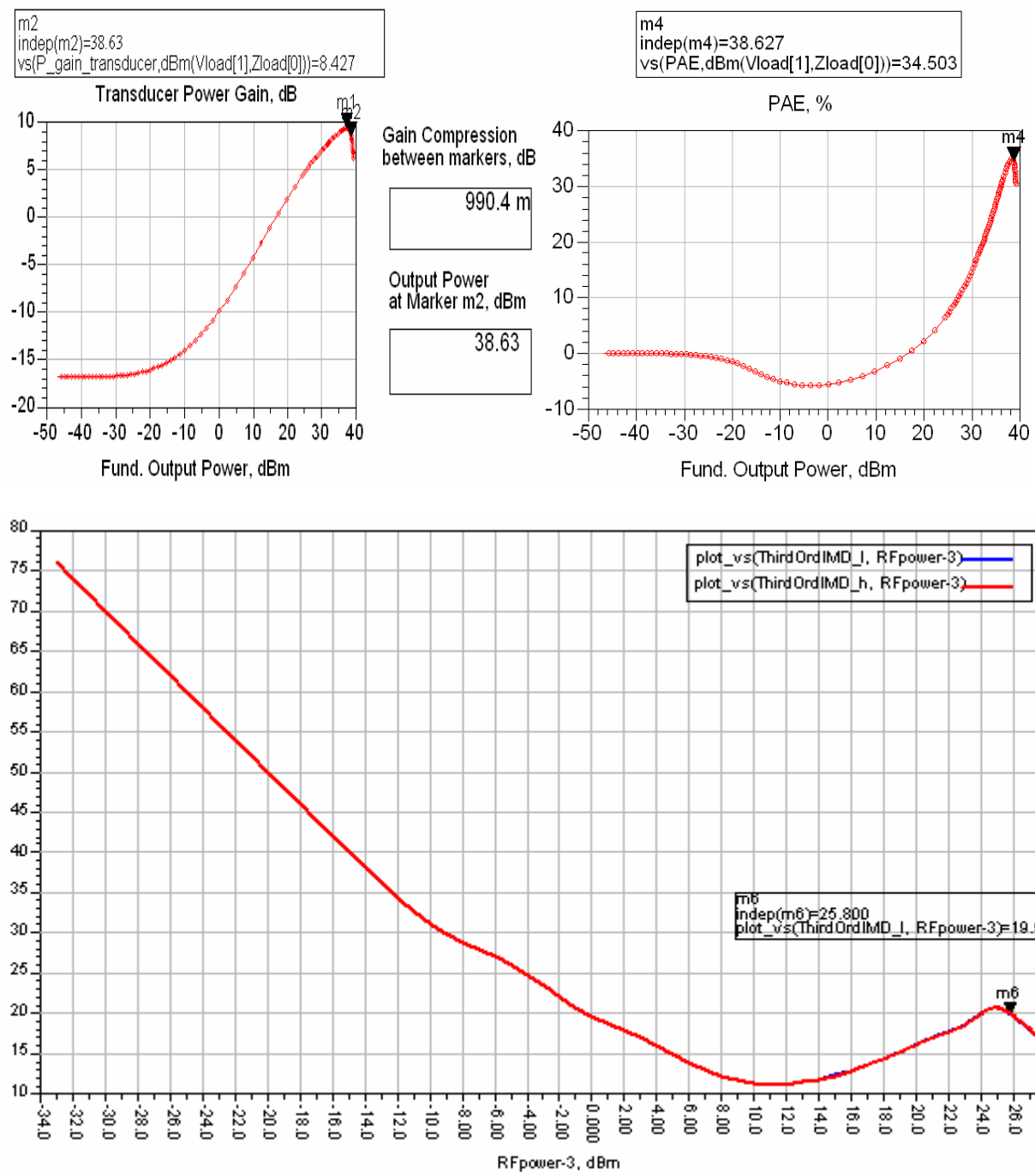


Figure 8.7 Class C

Comparing the above results, we notice the presence of the sweet spots as mentioned before, which have improved the IMR in the system. However, the change from class A to C have reduced the gain of the system and moved the 1dB compression point to higher output power which will increase the thermal dissipation in the system. Also we should mention that the PAE has increased in class AB to 35.137%, but in class C it starts to compress and decrease by small values, which is due to the fact that the design is optimized and matched for class A operation and due to the non idealistic of the ADS model.
Table 8.1 shows results comparison between the four operation classes.

Class(V)	Pout_dBm	ŋ%	PAE%	Gain_dB	Pdc_Thermal	HM3_dBc	IMR_dB
A_ 2.98	37.06	33.33	31.997	13.612	10.270	-52.402	18.829
AB_2.425	38.62	39.250	35.137	9.268	11.623	-49.032	19.287
C_ 2.25	38.630	40.500	34.500	8.410	11.577	-49.243	19.921

Table 8.1 Results comparison

As shown in the above table, the drain efficiency rise rapidly to 39% near class AB, then his slope compress and present a short in improvement.

8.3.2 Measurements

In order to determine the classes operation of the design we will do 2Tones measurements using a spectrum analyser; we will vary the gate voltage with a frequency spacing of 10 KHz and input power 0dBm. Class B will correspond to the voltage that minimizes the IM3 seen at the spectrum analyser. We chose the following:

Class A: Vds=20V, Vgs=3.6V, Ids=242mA.
Class AB: Vds=20V, Vgs=3.07V, Ids=53mA.
Class B: Vds=20V, Vgs=2.98V, Ids=36mA.
Class C: Vds=20V, Vgs=2.9V, Ids=19mA.

(Due to the short in the output power of the drivers, the 1dB Compression point wasn't reached for class AB, B and C).
The measurement results for the different classes are shown in the following:

Class AB

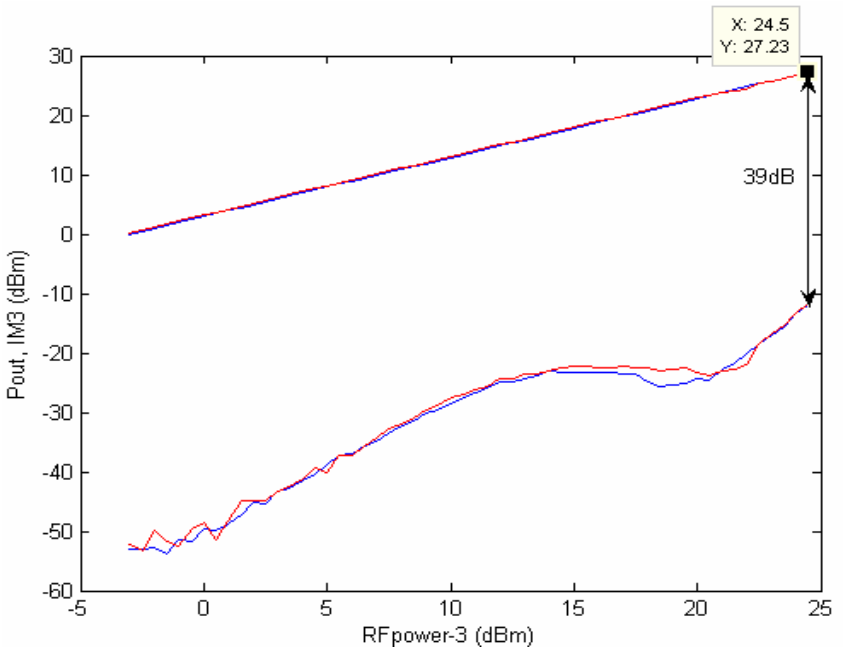


Figure 8.8 Class AB power measurements

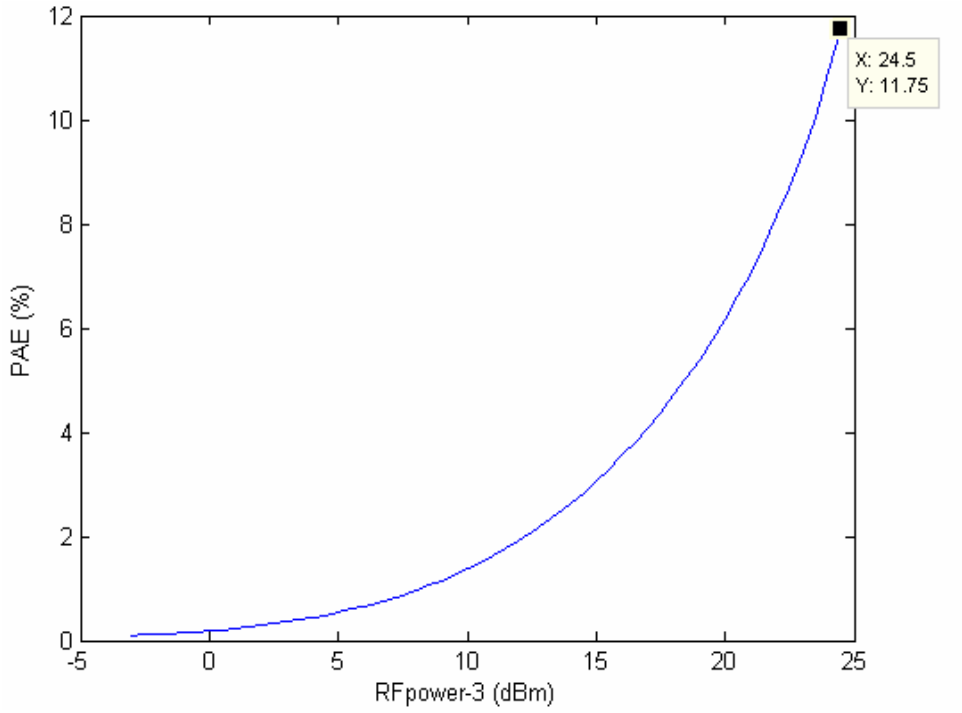


Figure 8.9 Class AB PAE

Class B

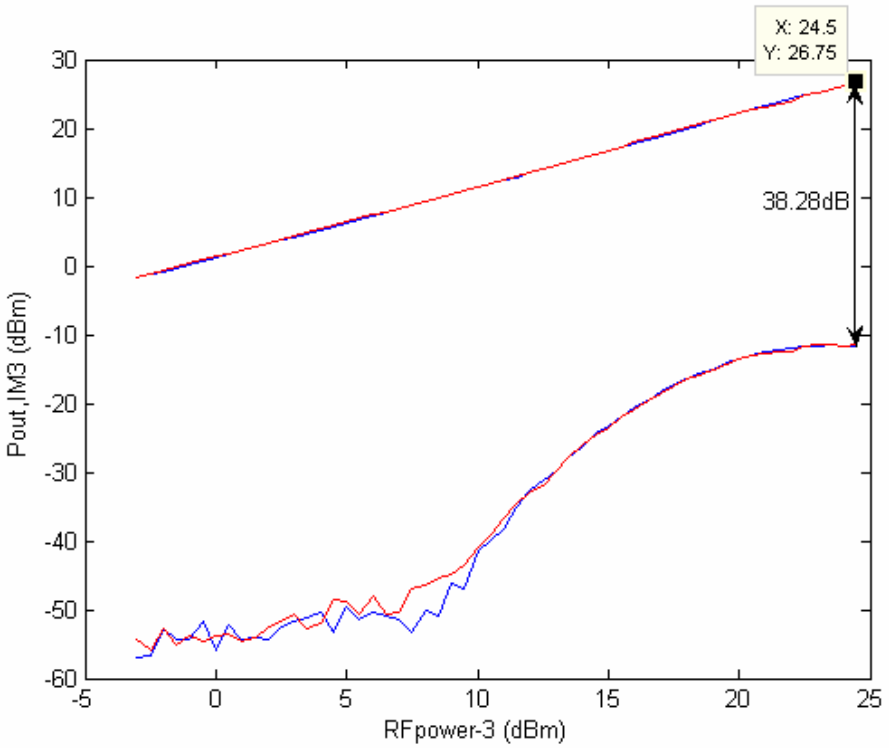


Figure 8.10 Class B power measurements

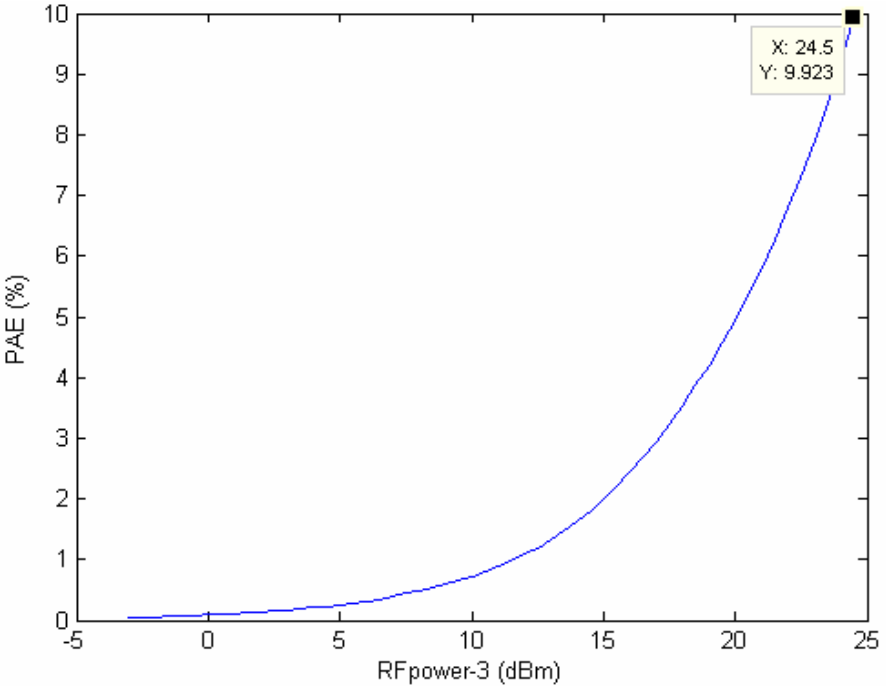


Figure 8.11 Class B PAE

Class C

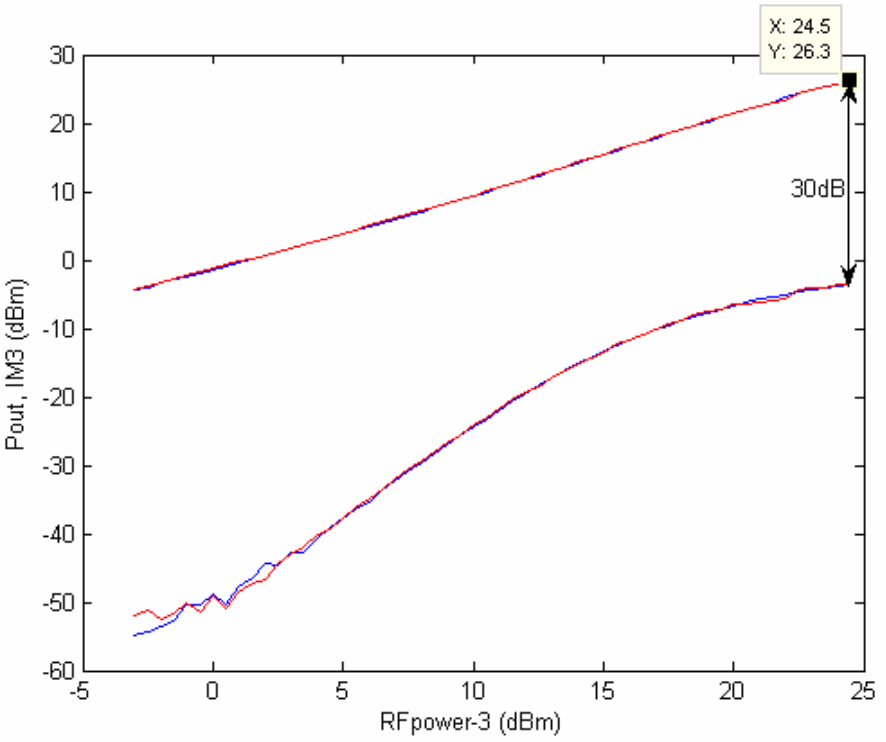


Figure 8.12 Class C power measurements

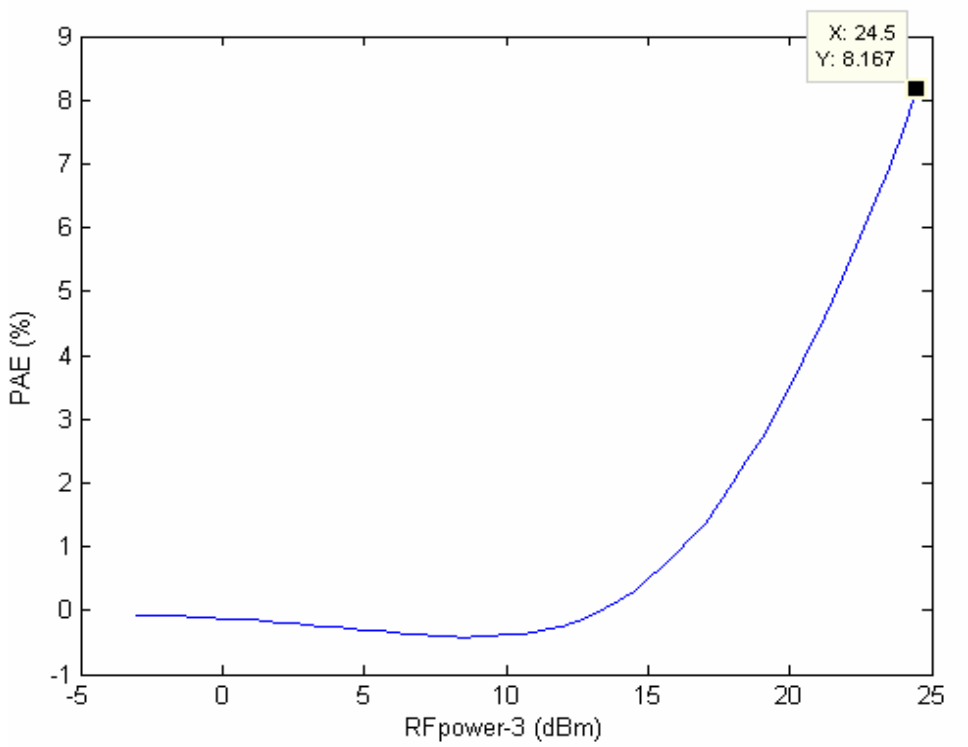


Figure 8.13 Class C PAE

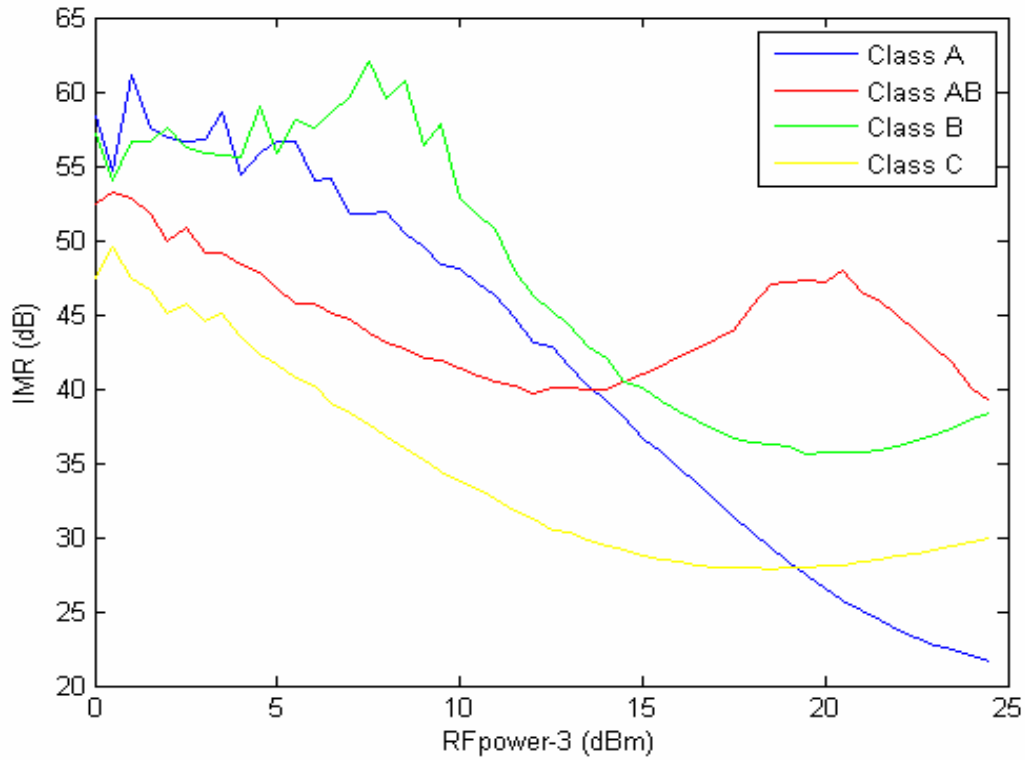


Figure 8.14 Measured IMR

Table 8.2 shows results comparison between the four measured classes.

Class(V)	Pout_dBm(fund.)	ŋ%	PAE%	Gain_dB	IMR_dB
A_ 2.98	25.78	12.9	9.091	5.278	25.786
AB_2.60	27.23	25.21	11.75	2.72	39

B_ 2.36	26.75	24.57	9.923	2.246	38.28
C_ 2.25	26.3	24.1	8.167	1.8	30

Table 8.2 Measurements comparison

As shown in the above results, by changing the operation class to AB we improved the IM3 by 13.2 dB which is due to the presence of the sweet spot. In fact, in class AB both sweet spots are near each other so they appear as one big sweet spot near the 1dB compression point. In addition class AB presents at least a 2.7% improvement of the efficiency which reached at least a value of 5.1% for a 6 dB backoff. Regarding the output power and the gain, class AB shows an output power of at least 1Watts, however the gain dropped to 2.7 dB.
Regarding class B and C, the measurements were limited by the saturation of the pre-driver; however from a general point of view we can conclude that the existence of the sweet spot will improve the carrier to intermodulation ratio.

8.4 Memory effect

8.4.1 Introduction

Today's mobile communication requirements are high-power, efficiency, linearity data rate and broadband for high capacity with better service quality and multi-carrier capability. In such applications power amplifiers (PA) with wideband input signals are used wherein the memory effect cannot be neglected. For that a dynamic characterization of memory effect is required to study and improve the nonlinearity in PA design.
Memory effects are defined as a change in the amplitude and phase of distortion components caused by changes in modulation frequency. Their effects are particularly important when dealing with linearization techniques, espacially when the distortion is reduced by a similar distortion in the opposite phase (Smooth memory effects are not usually harmful to the linearity of the PA itself; A phase rotation of 10º to 20º or an amplitude change of less than 0.5 dB, as a function of modulation frequency, has no dramatic effect on the linearity of the device) [27].
Memory effects are subdivided into two groups:

-Short term
-Long term

Short term memory effects are the easiest to manage as they affect the RF signal. They appear as a short time delay in the impulse response of the system. The output response depends on the current value of the input and on the past samples at the RF time scale. By adjusting the matching network they can be cancelled.
Long term memory effects, also called envelope memory, are the most disturbed sources for the linearizer systems. They appear as a long time delay in the impulse response of the system. The output response depends on the current value of the input and on the past samples at the base-band (envelope) time scale [28].
In the following, we will focus our discussion on the long term memory as their effects are the most dominating in the microwave amplifiers design.

8.4.2 Sources of memory effects

Long term memory effects represent a source of distortion for most of the linearization technique. They are responsible of various system impairments which increase the BER.
The envelope memory effects can be categorized in two groups:

-Thermal effects and trapping
-Electrical effects

Thermal effects and trapping are inherent to the active device itself. They are caused by electro-thermal couplings due to self heating, and these affect low modulation frequencies up to hundreds of kilohertz [19-20]. In fact, any temperature variations caused by the dissipated power are determined by thermal impedance which describes the heat flow from the device. Due to the finite mass of the active device, thermal impedance is not purely resistive; instead it forms a distributed low-pass filter with a wide range of time constants, Figure 8.15. This means that the temperature variation caused by the dissipated power do not occur instantaneously, rather base-band frequency-dependent phase shifts always exists. If any of the electrical parameters of the transistor are affected by temperature, thermal memory effects are unavoidable.

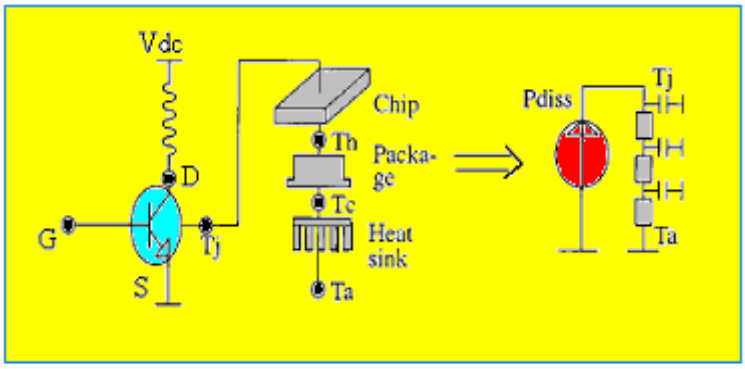


Figure 8.15 Heat flow from the device

Electrical memory effects are caused by varying base-band, fundamental or second harmonic impedances at different modulation frequencies. Fundamental and second harmonic impedance play a minor role as they can easily be kept constant over the entire modulation frequency range due to their narrow range of deviation. The major part of the memory is produced by envelope impedances. Envelope frequency varies from dc to the maximum modulation frequency, which can be as high as a few megahertz. In order to avoid memory effects, the output impedance must be constant or very low over this region. Since node (Input and Output) impedance consists of bias,matching and device impedances, and a large time constant is needed in bias networks as an energy storage, memory effects due to bias network are unavoidable, Figure 8.16. In fact, bias network present two major sources of the electrical memory effects: bias impedance variation and voltage source variation.
The bias tee is supposed to provide a relatively high impedance at RF frequency compared with the impedance of the input and output of the active device and of the matching circuit. However, in the case of a non-constant envelope modulation, the envelope frequency variation will cause a variation in the impedance of the bias network which cause a non-linearity (IMD) variation as a fonction of the envelope frequency. To avoide this envelope frequency dependent bias network, the bias impedance should be a short circuit at envelope frequency and an open circuit at RF frequency which is quite difficult to realize for a wide envelope bandwidth.
Finally, the bias tee is supposed to provide a constant voltage or current to the active device gate and source in order to achieve a certain class of operation. However, when using a non-constant envelope signal, any variation in the bias power supply will introduce a variation in the gate or drain voltage and so cause an additional amplitude modulation of the RF signal. A solution to that is to design the envelope bias tee in a way to isolate the current variations in the power supply and terminated by Short [22-23].

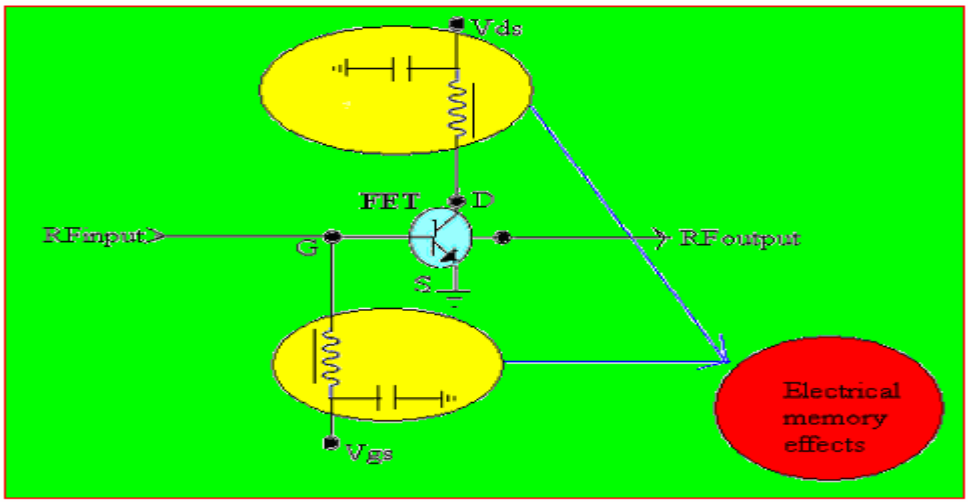


Figure 8.16 Electrical memory effects

8.4.3 Memory effects and IMD

Memory effects are impressed on the envelope by nonlinear mechanisms. Their presence is obvious by 2-tone IMD variation and/or IMD asymmetry with tone spacing. These asymmetries have a degradation impact when dealing with power amplifier linearization techniques.
In fact, asymmetries in the amplitudes of lower and upper intermodulation distortion (IMD) in a 2-tones tests or asymmetries in the low adjacent channel power ratio (ACPR) and upper ACPR in multitones tests are often observed in real microwave devices subject [24]. Their origine is attributed to the relations between IMDs and load termination at the base-band frequency[25].
The evaluation of IMD in a nonlinear component, such as power amplifier, can be gatherd by using a nonlinear Voltera series [13], which leads to [28] :

$$H_3(w_2,w_2,-w_1)=\frac{G_{m3}-\frac{1}{3}G_{md}\left[2H_2(w_2,-w_1)Z_L(w_2-w_1)+H_2(w_2,w_2)Z_L(w_2+w_2)\right]}{\left[1+G_{ds}Z_L(2w_2-w_1)\right]} \tag{8.2}$$

where

$$H_2(w_1,w_2)=\frac{G_{m2}-\frac{1}{2}G_{md}\left[H_1(w_1)Z_L(w_1)+H_1(w_2)Z_L(w_2)\right]}{\left[1+G_{ds}Z_L(w_1+w_2)\right]} \tag{8.3}$$

and

$$H_1(w)=\frac{G_m}{\left[1+G_{ds}Z_L(w)\right]} \tag{8.4}$$

From the above, it is obvious that any variation of the load termination impedance at the base-band frequency will lead to a variation in the IMDs. Figures 8.17-8.18 give a general explanation of this mechanism [13].

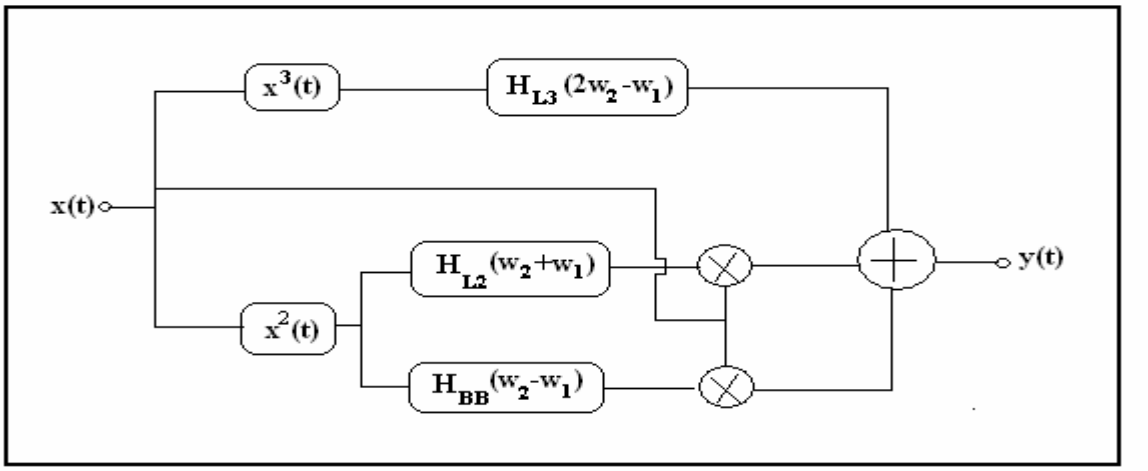


Figure 8.17 IMD mechanisms [28].

The output at the IMD frequency is given by [28]:

$$Y(2w_2 - w_1) = H_{31}(2w_2 - w_1)X(w_2)X(w_2)X(w_1)^* + X(w_1)^*\left[H_{22}(2w_2)X(w_2)X(w_2)\right] + \\ + X(w_2)\left[2H_{BB}(w_2 - w_1)X(w_2)X(w_1)^*\right] \tag{8.5}$$

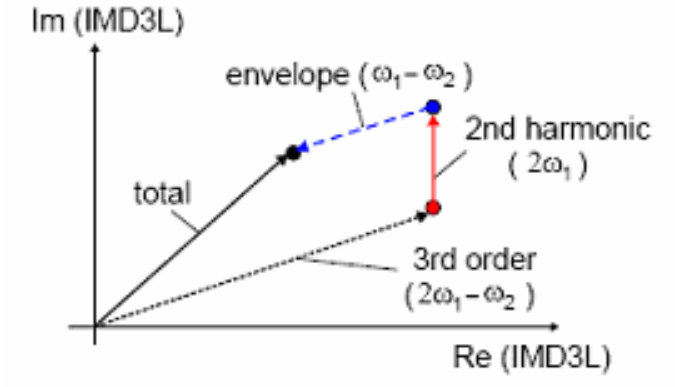


Figure 8.18 IMD output [13].

From these analyses we can conclude the following:

- The amplitude value of the intermodulation distortions will be changed by the impact of the second order coefficient which is a function of the base-band frequencies.
- The variation of the IMDs will only appear if both output impedances at w_2- w_1 and w_2+ w_1 are complex [28].

A deep investigation of the mechanisms causing IMD asymmetry at small-large signal analysis has shown that these asymmetries can only be caused by differences in the imaginary parts of the IMD components which should not be override by their real parts. Since in the asymptotic very large-signal operation, IMD tends to be real and negative, i.e., in opposite phase to the output linear components, large-signal IMD asymmetries may only take place in large-signal IMD sweet spots zones where the dominant real part is cancelled out. Therefore, an important conclusion to be drawn is that large-signal IMD asymmetries will only be evident in large-signal IMD sweet spots and provided that baseband and second harmonic terminations are reactive. Also, these asymmetries will appear at base-band frequencies (w_2- w_1)and (w_2+ w_1) in a revesre way, mean that imaginary parts of their impedance will vary in an opposite way [26].

8.4.4 Memory simulations

In this section, we will analyse the memory effects in the first design using ADS simulations and measurements for a class A operation.

8.4.4.1 ADS simulations

As mentioned in the previously, the best way to specify memory effects in a design is to study the variation of the intermodulation distortions in function of the frequency spacing in a two tones system.
HB2Tone simulation is used with RFpower fixed at 0 and 26 dBm for small and large signal analysis, while the frequency spacing is swept between 10 kHz and 5 MHz.

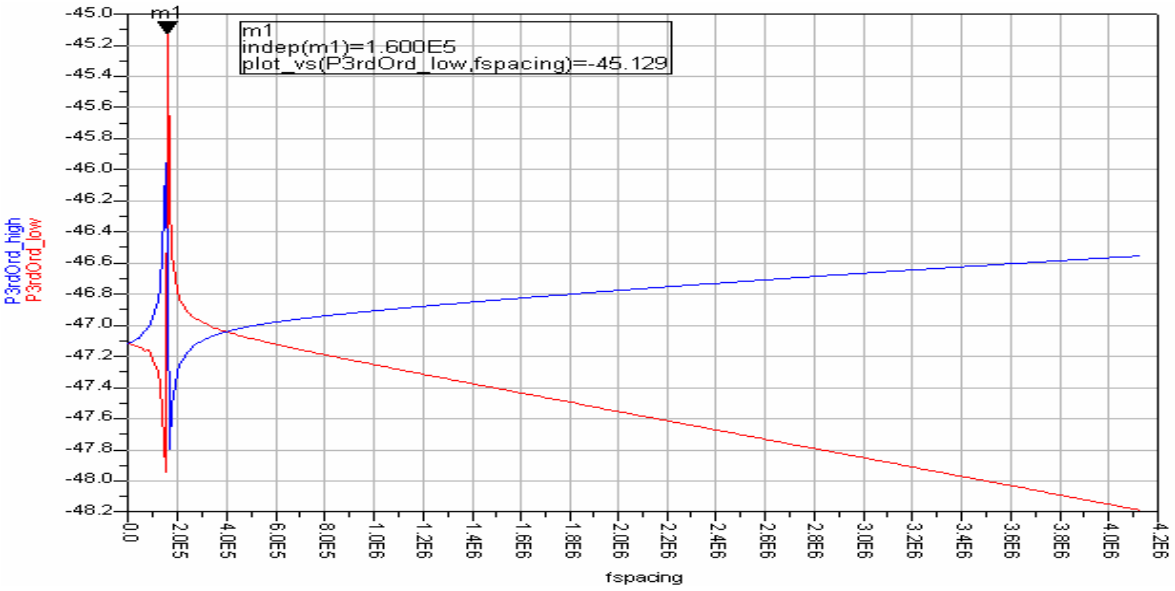


Figure8.19 IM3@0dBm class A

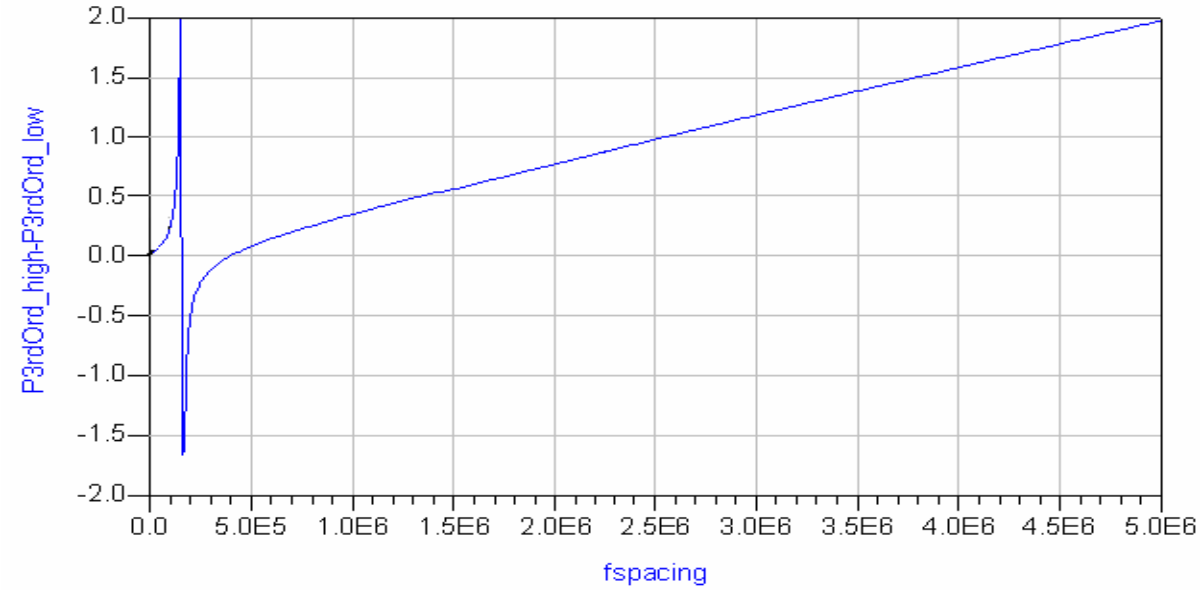


Figure8.20 Asymmetry@0dBm class A

Figure8.19 and 8.20 show the variation of the IM3 and asymmetry in function of the frequency spacing for an input power of 0dBm. As shown, for a spacing range of 150-160 kHz the system

present an asymmetry variation of ±2 dB between the low and high intermodulation products, and then as the spacing increase the asymmetry increase to reach 2 dB at 5MHz.
For an input power of 26dBm the results are shown in figure8.21.

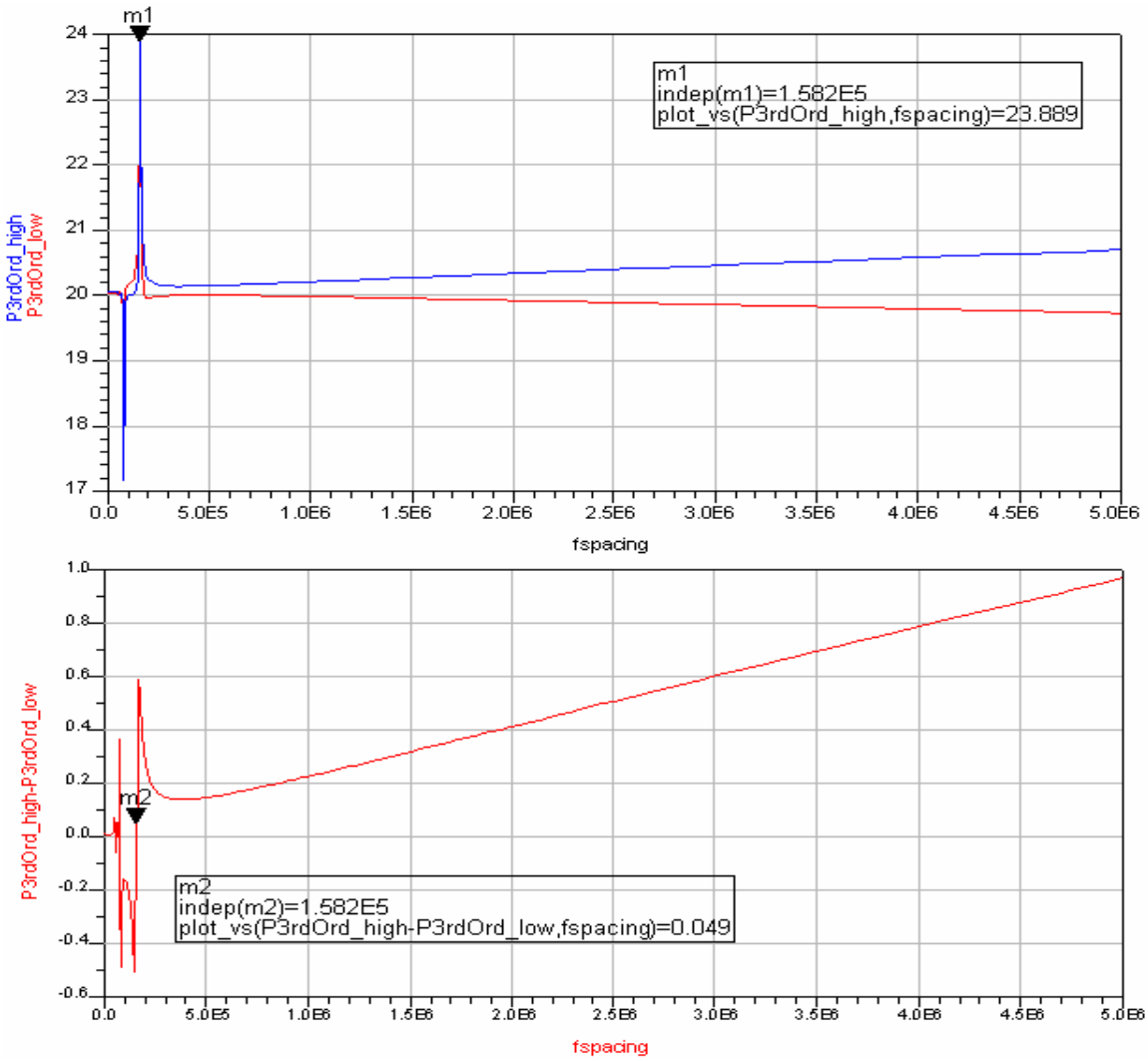


Figure 8.21 Asymmetry@26dBm class A

As shown above, for a spacing range between 150-160 kHz the system present a small asymmetry variation of ±0.5dB between the low and high intermodulation products, and than as the spacing increase the asymmetry increase to reach 1dB at 5MHz.
From the above we conclude that this design presents low memory effects of a maximum value of 2 dB which is an acceptable value when dealing with linearization techniques.
Now to understand the behaviour of the asymmetry-variation near the 160 kHz, we will study the variation of the load at the base band.
Figure 8.22 shows the variation of the load impedance with the frequency spacing. As seen, the sign of the imaginary part changes when passing from 154 kHz to 162 kHz with a value comparable to its real part which, as explained previously, will lead to an asymmetry between the low and high intermodulation product due to the phase contribution in the system.

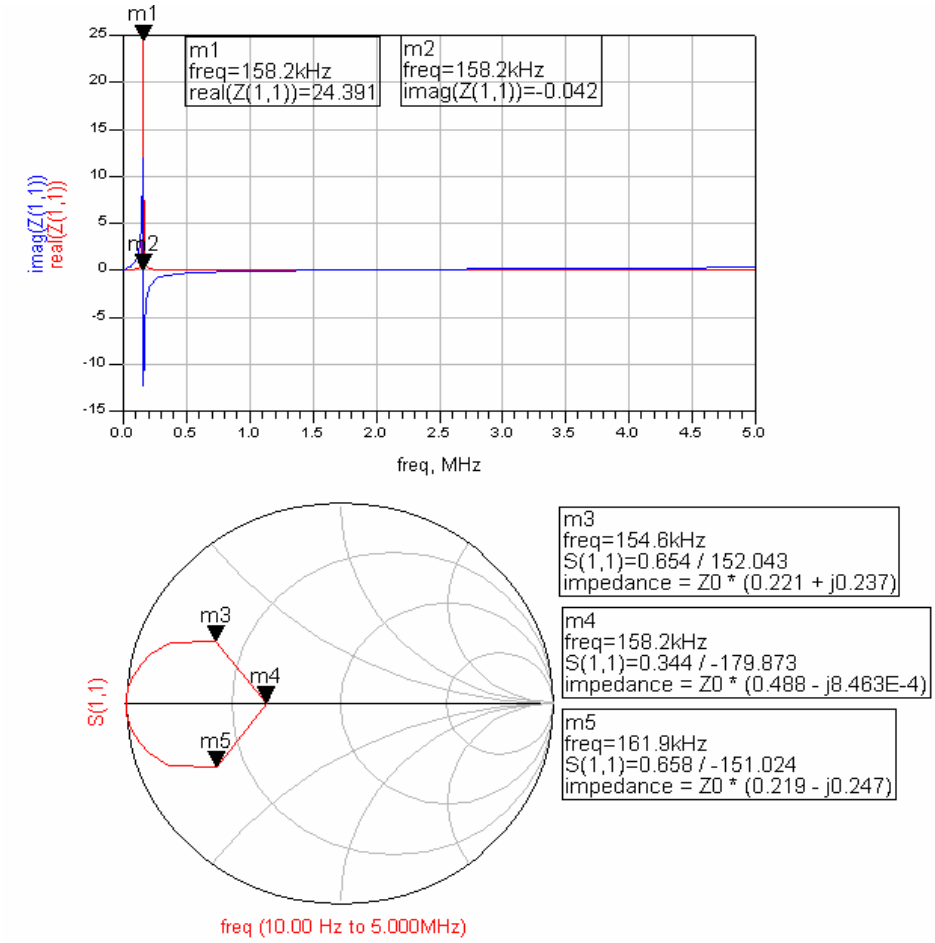


Figure 8.22 Load variations with fspacing

8.4.4.2 Measurements

In order to evaluate the performance of the implemented design regarding memory effects, we will do a 2Tones measurements as in Section 6.2.2 (Vds=20V, Vgs=3.6V and Ids=242mA), however this time; we will sweep the frequency spacing between 10 kHz and 5 MHz in order to study the asymmetry. Figures 8.23, 8.24, 8.25 and 8.26 show the intermodulations and asymmetry variations with frequency for an input power (fundamentals) of 10 dBm and 20.5 dBm respectively.

We conclude from these results that the design is kind of memoryless as he presents a maximum intermodulations asymmetry of 1.3 dB for both input power.

A general evaluation of memory effects in this design is shown in Figure 8.27 where both fspacing and input power are swept. As show the maximum asymmetry between the low and high intermodulation component is equal to 1.4 dB which is a good value when dealing with linearization techniques.

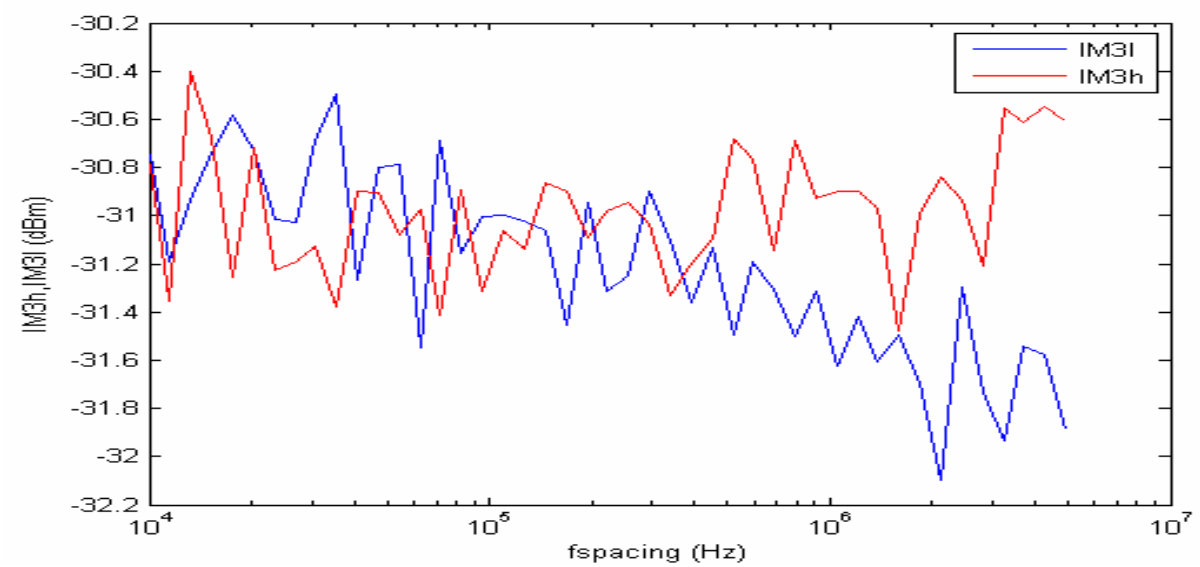


Figure 8.23 IM3L, IM3h Vs fspacing@10 dBm

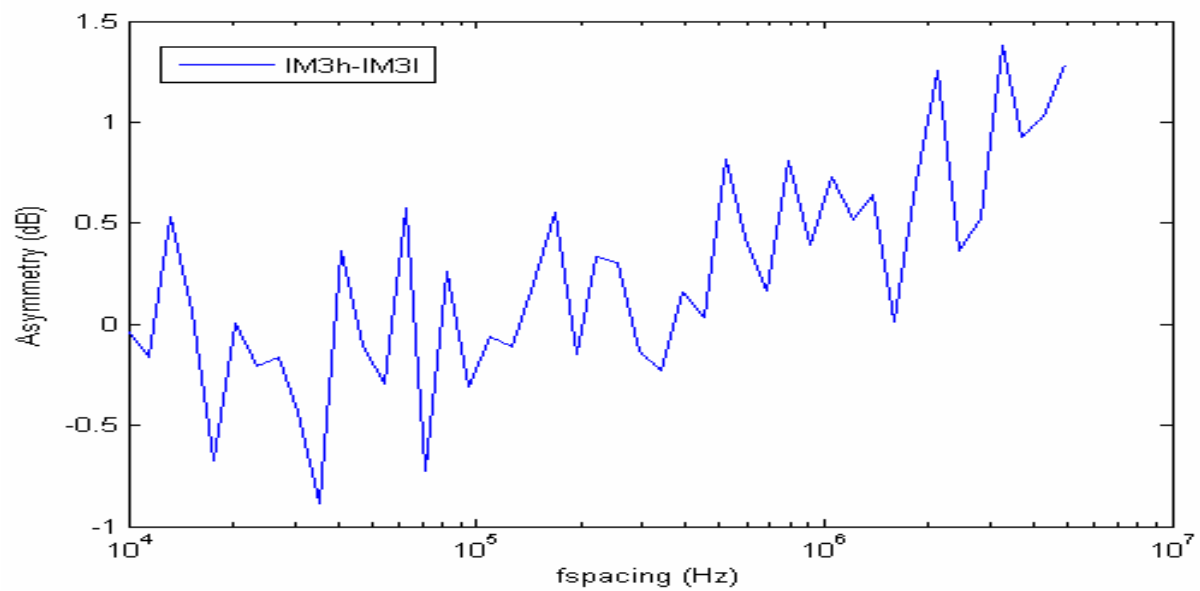


Figure 8.24 Asymmetry Vs fspacing@10 dBm

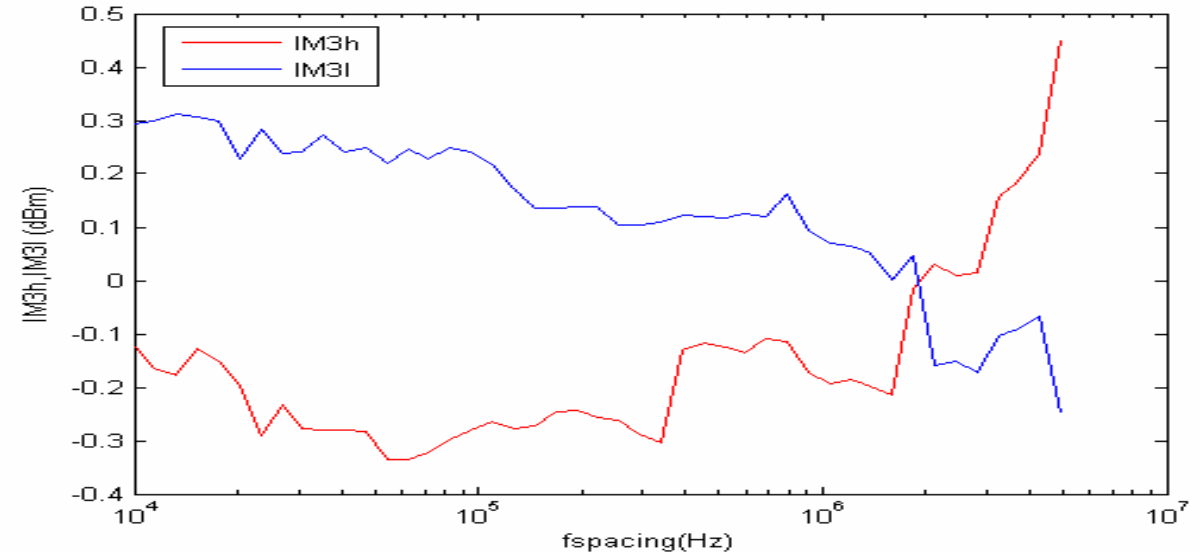


Figure 8.25 IM3l, IM3h Vs fspacing@20.5 dBm

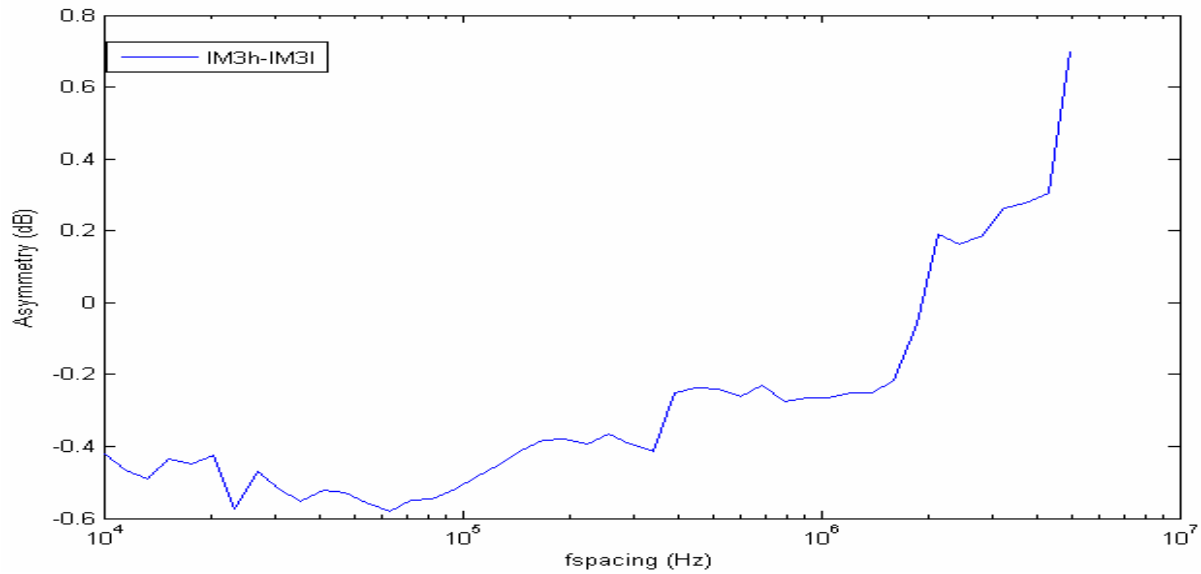


Figure 8.26 Asymmetry Vs fspacing@20.5 dBm

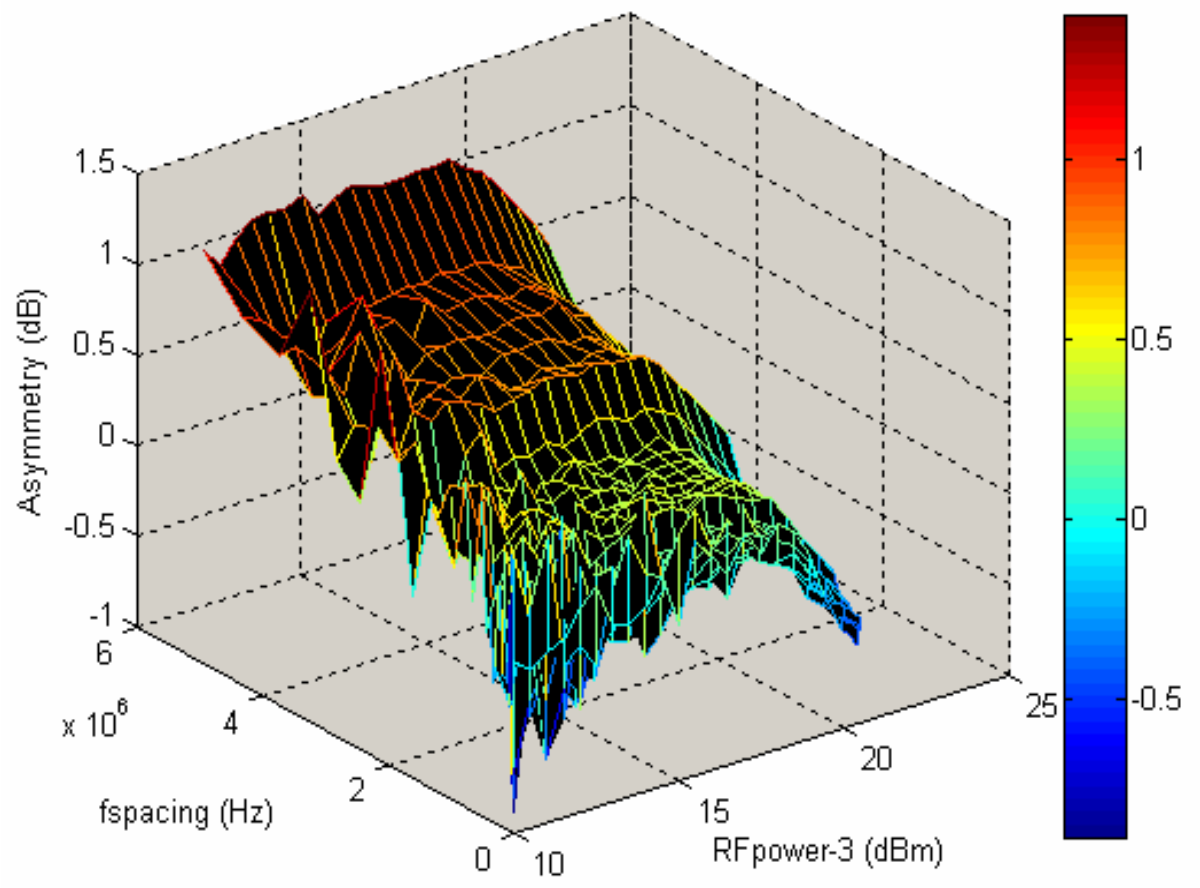


Figure8.27 Asymmetry Vs fspacing and power sweep

In the following we will present the results of memory effects evaluation when changing the class of operation to AB, B and C. Figures 8.28, 8.29 and 8.30 represent the variation of the asymmetry in function of the fspacing and input power. As noticed, the asymmetry between the IM3s is similar to the one found in class A. However class AB presents a high asymmetry of 4 dB near the sweet spot position (approximately at 20.5 dBm) which was discussed theoretically in Section 8.4.3.

Class AB (Vds=20V, Vgs=3.07V and Ids=53mA)

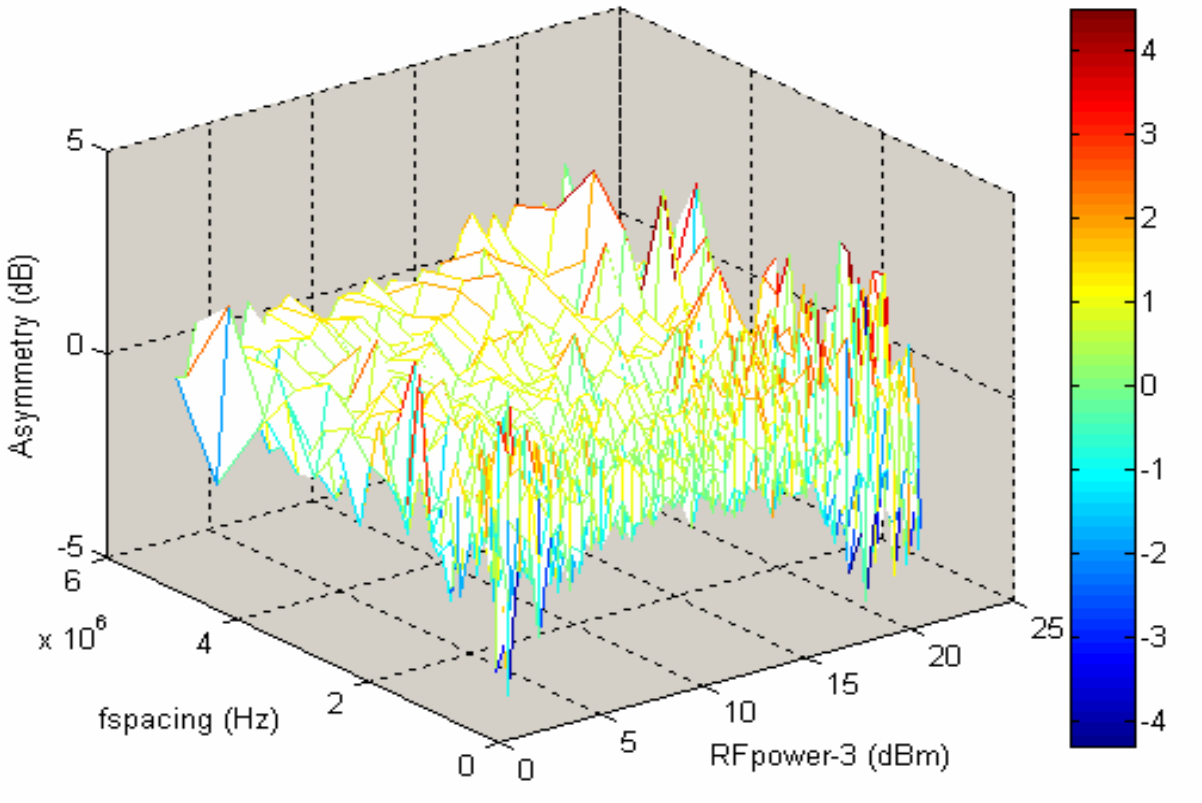


Figure 8.28 Asymmetry Vs fspacing and power sweep

Class B (Vds=20V, Vgs=2.98V and Ids=36mA)

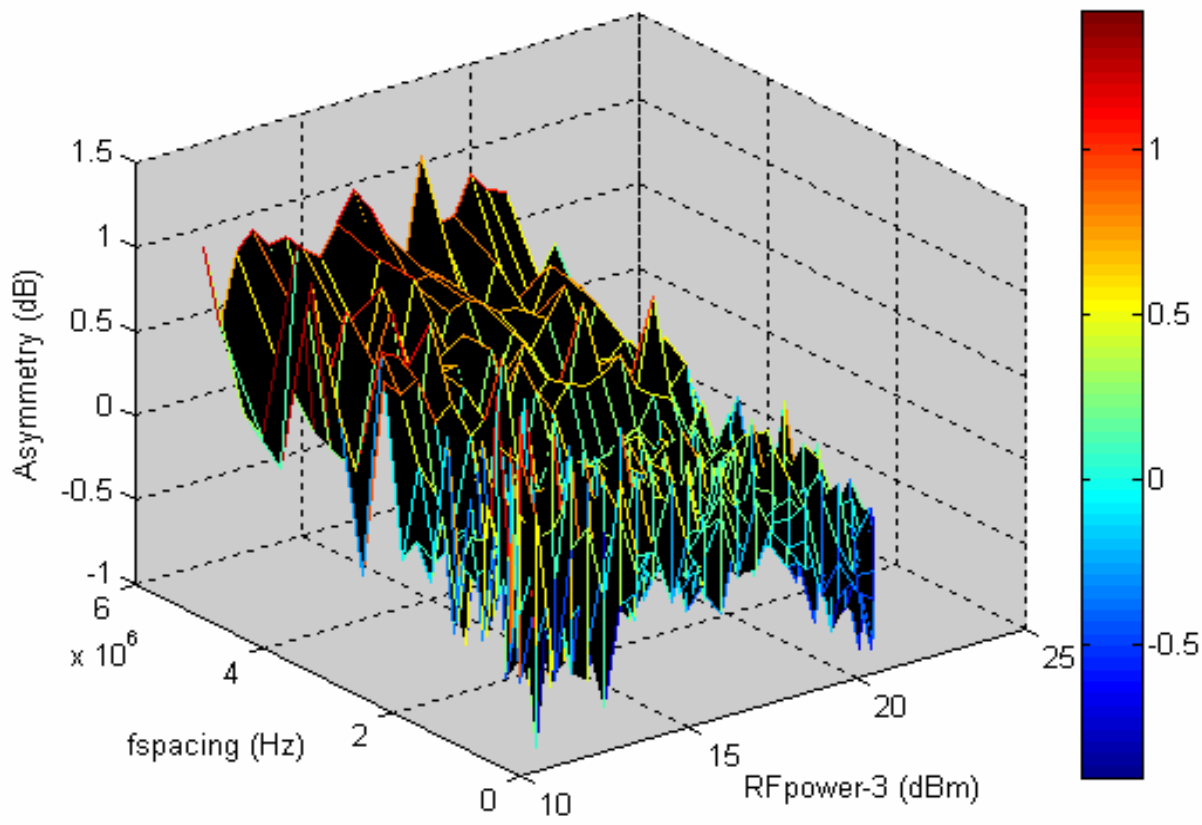


Figure 8.29 Asymmetry Vs fspacing and power sweep

Class C (Vds=20V, Vgs=2.9V and Ids=19mA

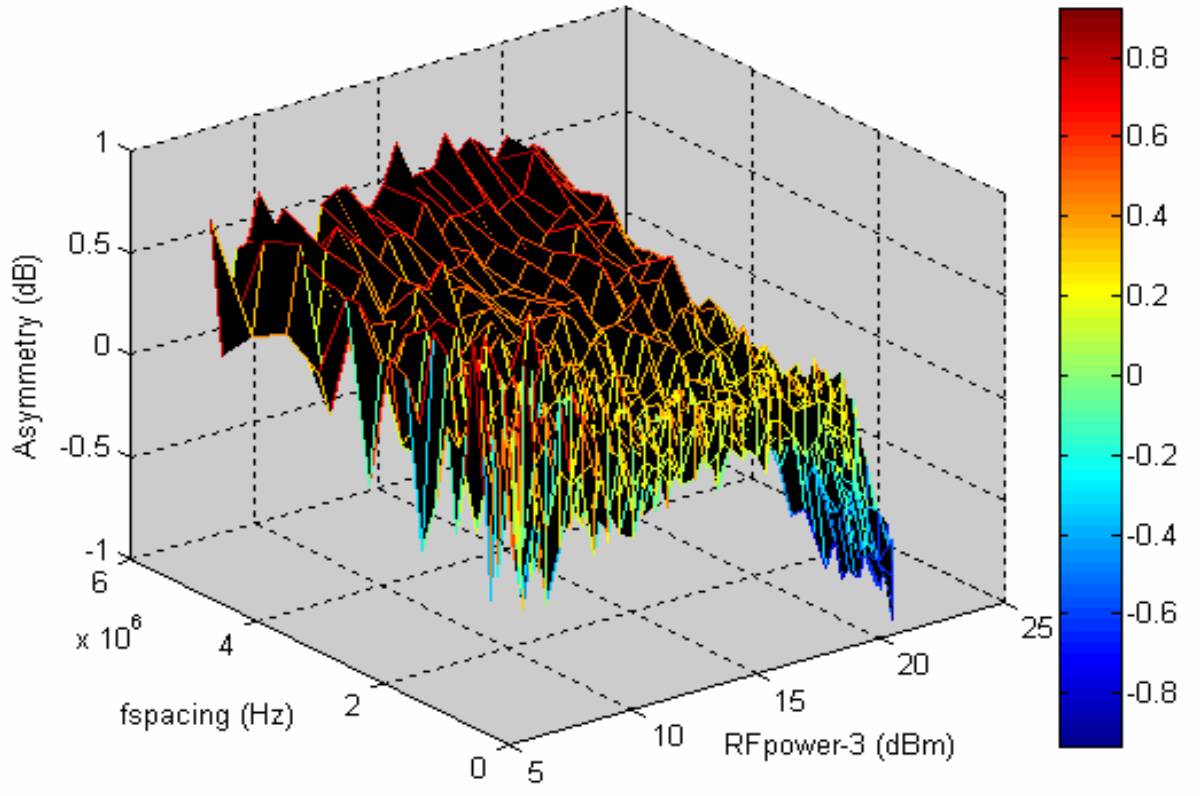


Figure 8.30 Asymmetry Vs fspacing and power sweep

Chapter9. Conclusions and Future Work

9.1 Conclusions

In this thesis work we have designed and manufactured two power amplifiers based on Si-LDMOS for WiMAX applications at 3.5 GHz. In order to achieve that, an ADS model for the transistor, given from Freescale, has been used in the designing process. The achieved results given by the simulations have shown an excellent power performance which allows the use of that technology in the WiMAX systems. However, the implemented designs showed a lake in the power performance compared with the ADS ones. In fact the first design has shown an acceptable behaviour with an output power of 28.9 dBm, a power added efficiency of 9.09% and a gain of 5.549 dB. Also it showed an intermodulation rejection of 25.787 dB and a memoryless behaviour. The second design has shown a lower power performance regarding the output power and the power added efficiency; however it showed a better output gain of 10.59 dB. Table 9.1 presents a resume of the achieved results for the first design.
These two performance are quite different compared with the ADS ones and the main reason behind these behaviour is the non idealistic of the ADS model given by Freescale at the WiMAX frequency which have caused a change in the load value, the matching system and so in the performance of the system. In fact, the implemented design has shown a difference in the biasing of the amplifier which led to a degradation of the performance as the system is temperature dependent.
Another reason behind the lake in the performance is the existence of the internal negative feedback in the transistor chip, which at a frequency up to 2 GHz worked as a stability improver, but at 3.5 GHz it turned into a positive feedback which created a peak in gain and led to an oscillation.

Finally we should mention that the system has shown a better power performance when working in class AB, however the gain dropped dramatically.

Class(V)	Pout_dBm	η%	PAE% At P1dB At 6dB Backoff	Gain_dB	IMR_dB	Memory_dB (Asymmetry)
A_2.98	28.9 Acceptable	12.9	9.091 3.5 Acceptable	5.278	25.786 More Improvements	1.3
AB_2.6	30.23 Good	25.21	11.75 5.1 Good	2.72	39 Good	4

Table 9.1 Achieved results

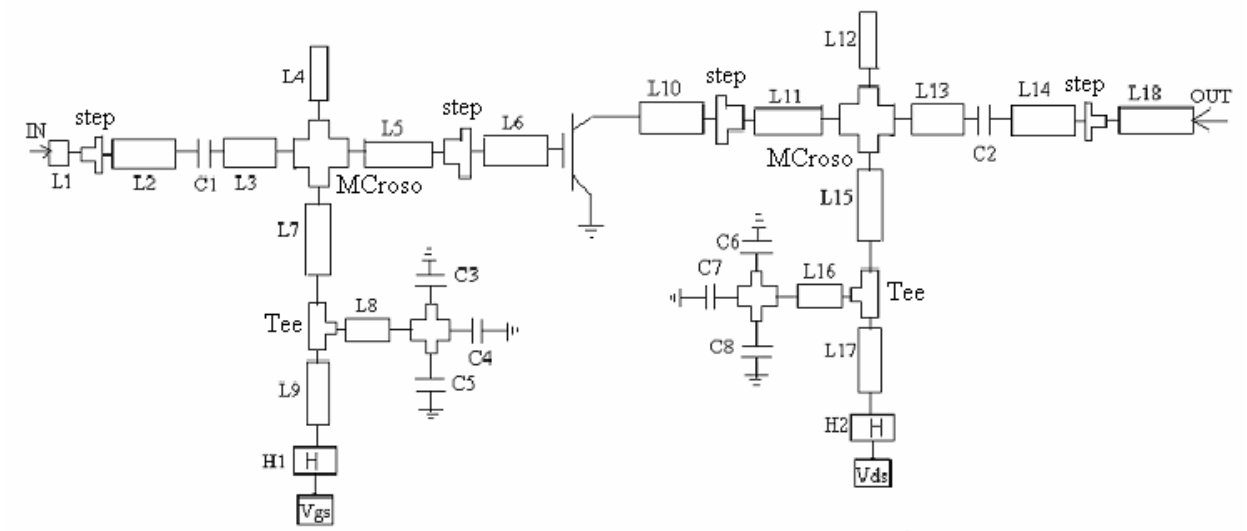
9.2 Future work

In order to improve the performance of the system and achieve a higher output power, the matching system should be designed in a specific way. To achieve that the ADS model should be idealistic and give an equal image of the real behaviour of the system.

So an interesting future work would be to improve the ADS model of the transistor by extracting its parameters and bias characteristics and then to redesign the power amplifier which should lead to a good improvement in the power performance and open the door to the use of the cheap Si-LDMOS technology in high frequency systems.

Annex

A.



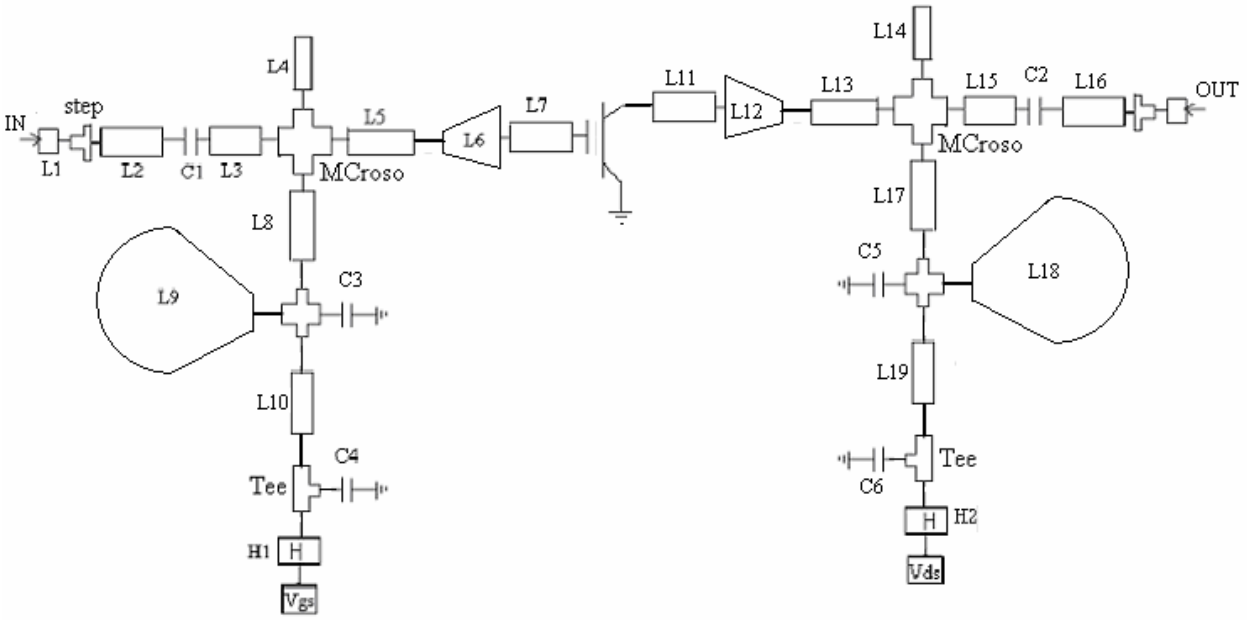
Annex A. Design1 dimensions

L (w(mm), l(mm))
L1 (0.578927, 10)
L2 (1.2, 1)
L3 (1.2, 1)
L4 (0.578927, 9.6)
L5 (0.578927, 10.95)
L6 (3.5, 0.5)
L7 (0.3, 7.5)
L8 (0.3, 4)
L9 (0.578927, 10)
L10 (3.5, 0.5)
L11 (0.578927, 8.8)
L12 (0.578927, 1.2, 1)
L13 (1.2, 1)
L14 (1.2, 1)
L15 (0.3, 8.9)
L16 (0.3, 3)
L17 (0.578927, 10)
L18 (0.578927, 10)

C(w(mm), l(mm))
C1=1ηF (1.2, 2)
C2=1ηF (1.2, 2)
C3=1ηF (1.2, 2)
C4=1μF (3, 4)
C5=1ρF (1.2, 2)
C6=1ηF (1.2, 2)
C7=1μF (3, 4)
C8=1ρF (1.2, 2)

H(w(mm), l(mm))
H1=1μH (1, 2)
H2=1μH (1, 2)

B.



Annex B Design2 dimensions

L (w(mm), l(mm))
L1 (0.578927, 10)
L2 (1.2, 1)
L3 (1.2, 1)
L4 (0.578927, 10.1116)
L5 (0.578927, 5.77575)
L6 (3.5---0.578927, 3)
L7 (3.5, 0.3)
L8 (0.3, 8.480820)
L9 (Wi=1, L=8.24736, Angle=80)
L10 (0.578927, 10)
L11 (3.52, 0.3)
L12 (3.52---0.578927, 3)
L13 (0.578927, 3)
L14 (0.578927, 10)
L15 (1.2, 1)
L16 (1.2, 1)
L17 (0.3, 8.48)
L18 (Wi=1, L=8.24736, Angle=80)
L19 (0.578927, 10)

C(w(mm), l(mm))
C1=1ηF (1.2, 2)
C2=1ηF (1.2, 2)
C3=1ηF (1.2, 2)
C4=1μF (3, 4)
C5=1ηF (1.2, 2)
C6=1μF (3, 4)

H(w(mm), l(mm))
H1=1μH (1, 2)
H2=1μH (1, 2)

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