Highly Efficient MMIC Class-F Power Amplifier

Luís Ramos Gomes*, José Carlos Pedro** and Nuno Borges Carvalho**
* - Network Quality - Radio Performance Group – TELECEL
Ed. SIKA, Rua de Santarem, 113, 4400 VILA NOVA de GAIA. E-mail – gomesl@telecel.pt
** - Instituto de Telecomunicações – Universidade de Aveiro
Campus Universitário, 3810 – AVEIRO. E-mails – jcpedro@ieee.org and nborges@ieee.org

Abstract

This work presents a design procedure for highly efficient power amplifiers dependent on low supply voltages. The impact that active device conduction angle and load impedance terminations at all major signal components have on the compromise between output power and efficiency was studied. Then, optimum conditions for these design constraints were derived, and theoretical predicted conclusions were validated by the construction of an S-band GaAs-MMIC class-F power amplifier.

I. INTRODUCTION

The rapid growth of mobile telecommunications services, like GSM, created an increased demand for highly efficient amplifiers dependent on small supply voltages. Because the transmitter RF power amplifier is one of the most determinant to the handset total power consumption, and battery capacity determines the final weight of modern portable phones, the importance of research efforts on this RF circuit is evident. Furthermore, the tight compromise between maximum output power, Pout, and power added efficiency, PAE, is also widely recognised on limited supply voltage amplifiers, which makes the optimisation of these circuits a continuous worth studding field.

The main objective of this work is to present a design procedure for the simultaneous optimisation of Pout and PAE on low voltage supply power amplifiers. A careful study of the impact of conduction angle, load impedance and harmonic terminations on these amplifier characteristics, showed that their optimum values can be strongly influenced by the low supply voltage operation.

In traditional silicon BJT single carrier amplifiers, where signal distortion is not critical, incomplete conduction cycles are possible, making class-AB, B or C the right solution. However, a power MESFET presents a thick channel, requiring high negative gate bias for its complete depletion, which usually implies Vgd bias greater than the threshold of gate-drain breakdown. Thus, in modern microwave MESFET based power amplifiers, not only it may be impossible to bias the device at, or below, cut-off, as it is known that maximum Pout and power gain would drop as drain source current, Ids, was pushed into very low conduction angles[1], [2]. This leads to a sub-optimum PAE, even if DC-RF conversion efficiency is optimised. The result is the almost general use of class-AB. In the case of amplifiers driven from low voltage supplies, quiescent point restrictions imposed by gate-drain breakdown can be relaxed, but maximum peak output current limitations will have a stronger impact on maximum reachable RF output power.

In order to test the results of the study on the limiting factors of Pout and PAE in power amplifiers, a 100mW S-Band MMIC amplifier was built and characterised. A performance of about 19.5dBm and 50% PAE was achieved.

II. CONDUCTION ANGLE SELECTION

In this Section optimum conduction angle was studied. It was already said that very low conduction angles reduces the value of PAE and Pout that can be achieved. So, in order to choose the best conduction angle and confirm the above stated, some simulations were performed using a typical power amplifier scheme with a 3V 4x150µm MESFET and an ideal parallel resonant circuit at the output. Various conduction angles were tested corresponding to Class-A, A-B and C. Two different operating conditions were considered: 1dB compression point and maximum PAE, since they represent two different driving points of practical significance: on-set of saturation for high power and moderate nonlinearity and strong compression for improved efficiency, respectively. The results summarised in table Tab. 1 show that class-AB is the best option, since it is where the best compromise between Pout and PAE for both modes of operation is achieved.

Tab. 1 – Simulation results of Pout and PAE for different classes of operation.

Input Driving Point	η_{DC} (%)	PAE (%)	Pout (dBm)
Class-A			
P_{1dB}	45	43	17.6
PAE_{Max}	58%	57	18.8
Class-AB			
P_{1dB}	59	59	17.8
PAE_{Max}	61	61	18.1
Class-C			
P_{1dB}	49	48	15.0
PAE_{Max}	62	61	17.6

III. LOAD LINE SELECTION

An important issue on low voltage power amplifier design is optimum load impedance selection. Due to the known rise of knee voltage for higher Vgs output Ids(Vds) curves, traditional load-line selection (e. g. using the Cripps [3] method) leads to a much lower output voltage swing, and so reduced DC-RF conversion efficiency.

Fig. 2 shows theoretical simulated results obtained from the simultaneous direct resolution of the nonlinear equations that describe the device's Ids(Vgs,Vds) output curves (in this case the MESFET Statz Model was considered [4]):

$$Ids(Vgs,Vds)=\frac{\beta(Vgs-Vt)^2}{1+\theta(Vgs-Vt)}(1+\lambda Vds)Tanh(\alpha Vds) \qquad (1)$$

and the boundary condition imposed by R_L under a power supply voltage of 3V, as can be observed in Fig. 1.

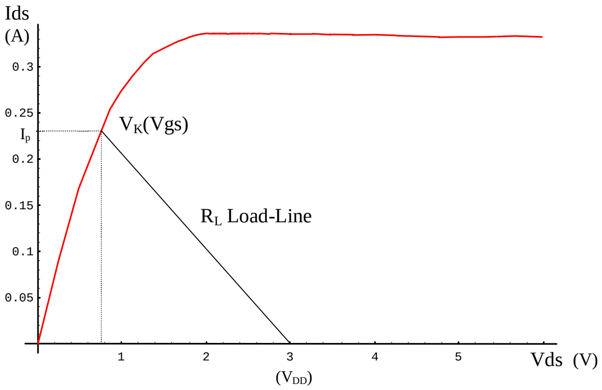

Fig. 1 – Output voltage swing imposed by V_K dependence on gate bias and load line selection.

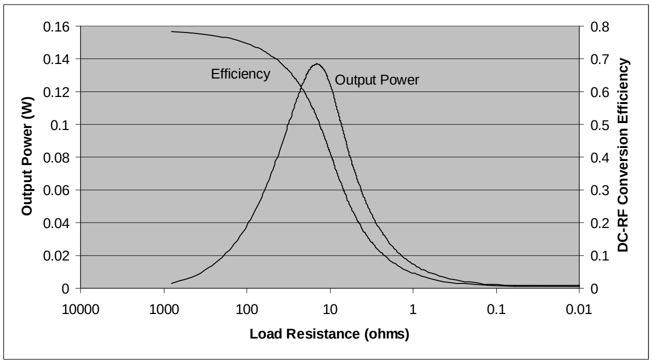

Fig. 2 – Calculated output power and DC-RF conversion efficiency versus load resistance of ideal MESFET power amplifier.

A compromise between optimum load selection for maximum efficiency or output power is clear. In fact, that theoretical study induces a general conclusion that the best load line, when PAE and Pout are to be simultaneously optimised, is reasonably more horizontal than the one that would be used in a unlimited supply voltage design. The reason for that resides on the fact that MESFET's knee voltage, V_K, which is 1V to 2V typical, represents a considerable part of V_{DD} supply voltage. Thus, the output voltage excursion will not be limited to Vgd breakdown, as is usual in common large V_{DD} power designs, but by that V_K restriction. Nevertheless, it is also known from the ancient days of field effect device's nonlinear modelling that this V_K presents a strong variation with Vgs, decreasing significantly when the device approaches pinch-off. A more horizontal load-line than the one proposed by Cripps takes advantage of this effect allowing for significant improvement in drain efficiency.

With the present device, a maximum Pout of near 21dBm, with an associated efficiency of 52%, could be reached for about 15Ω (Cripps load line), while a better value of near 30Ω leaded to 65% efficiency with only one 1dB loss in output power capability.

IV. HARMONIC IMPEDANCE TERMINATION STUDY

Finally, the impact of harmonic load impedance terminations were also evaluated. This study was based on the fact that, if the active devices are set into a strong nonlinear operation mode, high amplitude harmonic contents, specially for the 2nd and 3rd components, will take place on Vds and Ids. So, it should be expected that with a correct termination at those frequencies we could make use of them in order to increase the performance of the amplifier, concerning Pout and PAE. This idea has already been presented by several authors [5],[6].

To accomplish this, a 4x150μm MESFET based amplifier was simulated with an Harmonic-Balance package. In order to study the influence of 2nd and 3rd harmonic terminations, the fundamental output resonant circuit was removed and substituted by an ideal two-port [S] matrix network. This two-port network, described by a set of three S parameter matrices (for ω_0, $2\omega_0$ and $3\omega_0$), allowed an independent and flexible control of all three terminations, $Z_L(\omega)$. The best compromise of simultaneous maximisation of Pout and PAE were obtained for two different harmonic terminations: A-[$Z_L(2\omega_0)=0$, $Z_L(3\omega_0)=\infty$] and B-[$Z_L(2\omega_0)=\infty$, $Z_L(3\omega_0)=0$]. Case A, which is usually named class-F operation, traduces the traditional procedure of short-circuiting 2nd harmonic while developing an important 3rd harmonic drain voltage component. Case B, however, seemed to be rather surprising as it represents the inverse solution of A. For this reason, it was recently referred as Inverse Class-F mode [7]. Comparison of drain voltage and current waveforms (see Fig. 5 of next Section) provided an explanation for this situation. The presence of a strong 2nd harmonic at the drain voltage, produced a very high voltage peak (near 8.5V for a 3V bias), which somehow compensates the reduced voltage swing (V_{DD}-V_K) imposed by the limited supply voltage.

V. MMIC IMPLEMENTATION

In order to validate the above conclusions for optimum conduction angle, load-line and harmonic terminations, a GaAs MESFET MMIC power amplifier was designed and tested. Because of its increased research interest, Case B for the harmonic component's terminations was adopted. Due to future mobile communications applications, central frequency was chosen as 2.15GHz, while specified output power was 20dBm. The available MMIC process was F20 from GEC MARCONI which is a small signal low noise implant foundry process, not primarily intended for power applications.

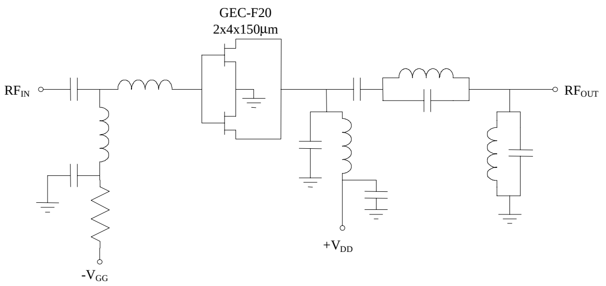

Fig. 3 - Simplified schematic diagram of the implemented 3V GaAs MMIC power amplifier chip.

Fig. 3 shows a simplified schematic diagram of the 3V implemented amplifier. Total MESFET gate periphery is 1200μm, which gives a combined Idss of near 200mA. The input circuit is simply a L matching network of inductors, designed for maximum power transfer. Due to the required load impedances at fundamental, 2nd and 3rd harmonics, the output network is more complex. It consists of three different resonant circuits. The first one, near the 50Ω load is tuned for the fundamental, while the one located between the FETs and the load guarantees the required high impedance at $2\omega_0$. Finally, the parallel resonant circuit directly connected to the FET's drain terminals impose the designed low impedance at $3\omega_0$ and drain bias.

Simulation results of this circuit, with lossless passive components, gave 77% for PAE and 21.4dBm for Pout, which are very good results for a 3V amplifier. When the ideal reactive elements were substituted by their low Q MMIC equivalents, these values dropped to final simulated PAE of only 52% and 20dBm of Pout, as can be verified in Fig. 4. Nevertheless, they fully validate the design methodology above proposed.

Fig. 5 shows simulated final drain voltage and current waveforms, where the expected voltage peak induced by the 2nd harmonic is evident. The result of this study was implemented on a MMIC. The resulting layout is presented in Fig. 6.

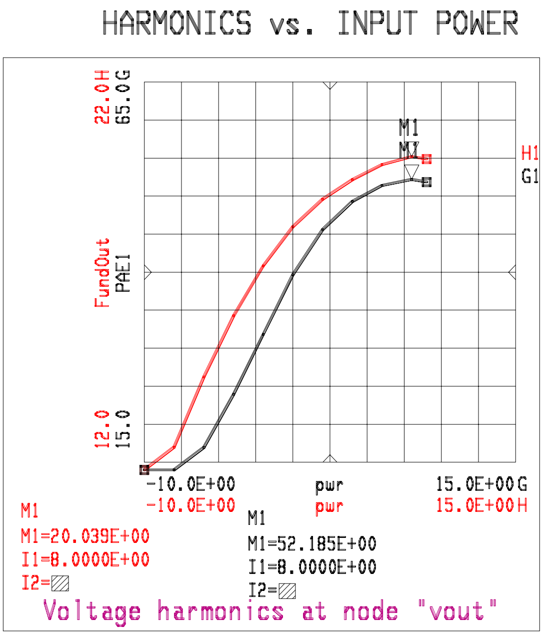

Fig. 4 - Simulated Pout and PAE versus RF source available power.

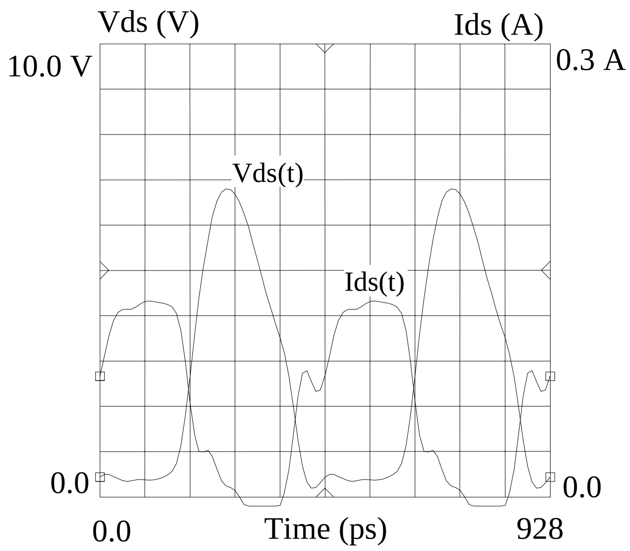

Fig. 5 – Simulation results of drain source current and voltage of the implemented MMIC amplifier.

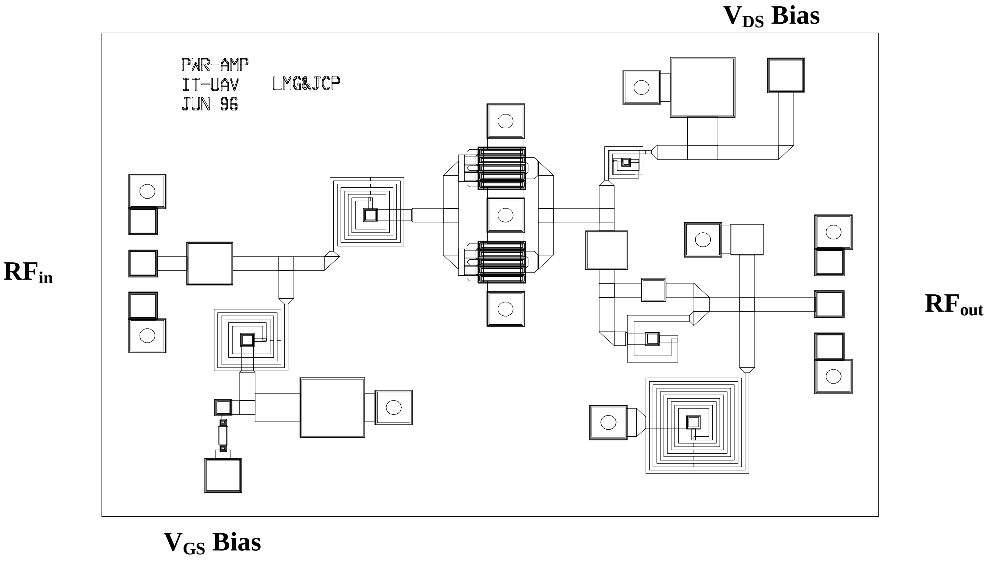

Fig. 6 – MMIC S Band power amplifier layout.

Fig. 7 represents measured Pout and PAE versus RF source available power. An observed Pout of 19.5dBm and a maximum PAE of 50% are very close to the simulated values.

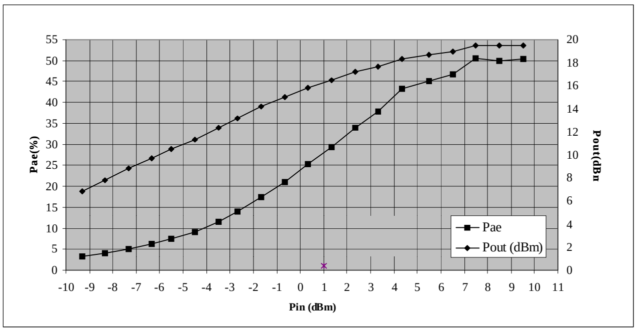

Fig. 7 - Measured results of PAE and Pout.

VI. CONCLUSIONS

In conclusion, a comprehensive design method for limited supply voltage power amplifiers was presented, which was validated by a practical design. Also, it was found that MMIC reactive component's parasitics play a very important role on the maximum efficiency that may be expected from this type of RF circuits.

VIII. ACKNOWLEDGEMENTS

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