Optimum Load Selection for Maximized Large Signal IMD Sweet Spots

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Abstract

Large Signal IMD (Intermodulation) Sweet Spots are a definite goal when designing highly linear power amplifiers. Despite that large signal sweet spot generation have been explained and studied, few comments had been stated for the selection of the optimum load for its maximization.
This paper presents some design rules in order to select optimum load impedance values for optimized Large Signal IMD Sweet Spots.

I. Introduction

Wireless communication growth is demanding for highly digital modulated techniques that allow the communication society to transmit more information maintaining the spectral occupation.

Nevertheless nonlinear distortion, imposed by different transmitting and receiving blocks, degrades the spectral occupancy by generating spectral regrowth. That is the main reason why the use of linear devices is a must.

Since the main system block that generates nonlinear distortion is the final stage power amplifier, most of recent study efforts for linear operation have been focused on that component [1-4].

Different approaches have been used in order to achieve that linearization improvement. The most used one is external linearization schemes, but that is normally obtained by an increase in the number of components and complexity. Other solutions include the understanding of the nonlinear distortion mechanisms in order to optimize and diminish its generation.

One of these studies is based on the existence of large signal IMD sweet spots, these are output IMD values that present minimums at certain input power excitations, and thus called sweet.

In references [1-4] the generation of large signal IMD sweet spot is explained, and its behavior with bias point and input power level is studied in order to design highly linear circuits with improved power added efficiency.

Nevertheless, and despite the study of out of band load impedances have been presented in [4], nothing is said, or presented, relative to the optimum load that must appear at the output of the power amplifier circuit, in order to maximize the large signal IMD sweet spot.

This is the principal theme that is addressed in this paper. First the IMD sweet spot generation studies will be revisited. Then the optimum load selection for maximized large signal sweet spot is presented.

Finally some conclusions will be drawn.

II. Large Signal IMD Sweet Spot Revisited

Large signal IMD sweet spots are generated every time the small and large signal IMD components have opposite signal phases.

For instance remembering input-output characteristic functions of a MESFET, Fig.1, it is found [4] that the optimum bias point for the generation of an IMD sweet spot is the one where the small signal IMD is in phase with the fundamental component. This behavior is usually associated with power expansion.

Since in large signal zones IMD phase tends to be opposite relative to the fundamental, due to compression requirements [4], Fig.2, then in the intersection of these two zones a large signal IMD sweet spot will appear.

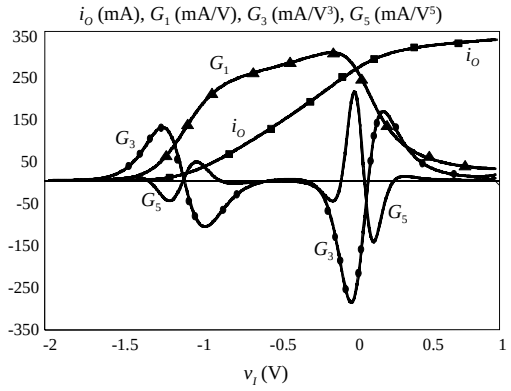
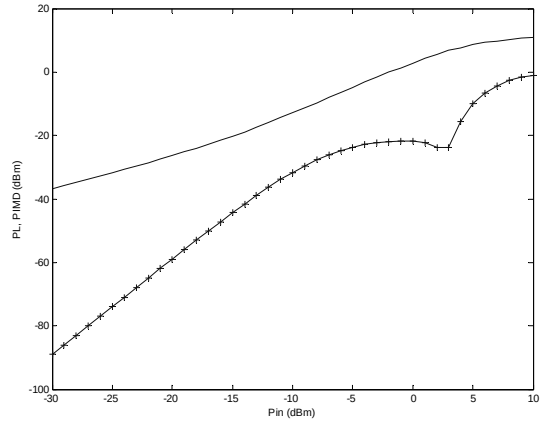


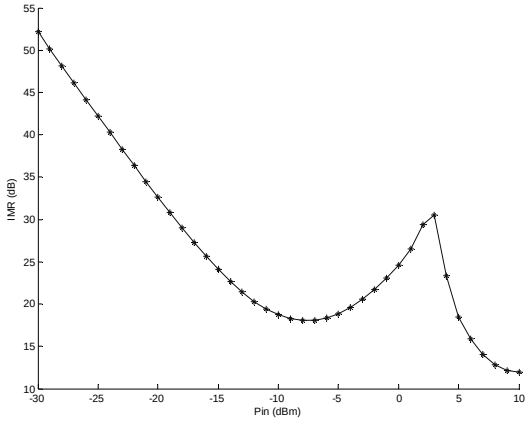
Fig. 1 MESFET active device characteristic function and its first three derivatives.

Other type of active devices, e.g. MOSFET's present the same IMD behavior, but contrary to MESFET's not only in large signal operation, but also at medium signal [2-3].

Nevertheless the IMD sweet spot mechanism is equal:
Change of phase between small and medium or large signal excursions.



a)



b)

Fig. 2 Generation of large signal IMD sweet spot, a) Output and Intermodulation power and b) Intermodulation ratio versus input power.

III. Optimum load selection for maximized Large Signal IMD Sweet Spot

The first approach to this type of analyze is done by considering an intrinsic device without any type of parasitics and purely memoryless, Fig.3.

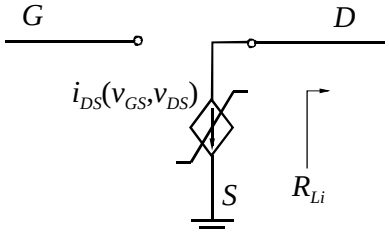


Fig. 3 MESFET ideal model.

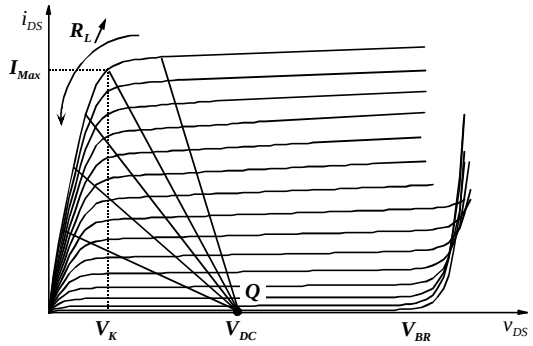
In this case the optimum load for maximized IMD sweet spot's will be from [4] the one that allows a signal swing from the cut-off till the entering in the triode or linear zone. From [4] it was proved that is exactly the entering in the triode zone that generates power compression and thus the seek opposite phase relative to the small signal excursion.

A change on R_L in Fig.3, will impose that the signal swing enters sooner, or later, in the triode zone, and thus generates an IMD sweet spot for smaller, or larger, values of input power.

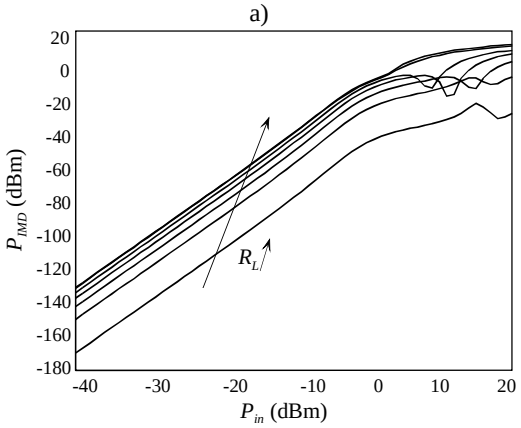
That is what can be observed form Fig. 4a) and b), where different values of R_L have been used.

Despite the change of input power for which we have a minimum IMD sweet spot, the value of that minimum is ideally always zero.

This led us to an interesting conclusion, which states that every intrinsic resistive load generates and IMD minimum. The impact of that load only affects the value of input power for which the minimum appears, or in other words the gain of the amplifier.



a)



b)

Fig. 4 Impact of resistive PA load resistance, R_L, on large-signal IMD sweet spots.

Unfortunately real devices are not purely resistive as the one presented on Fig.3, but include reactive parasitics, Fig.5.

In that case, the selection of the optimum load should be the one that after de-embedding the parasitics, presents a pure resistive load to the intrinsic device.

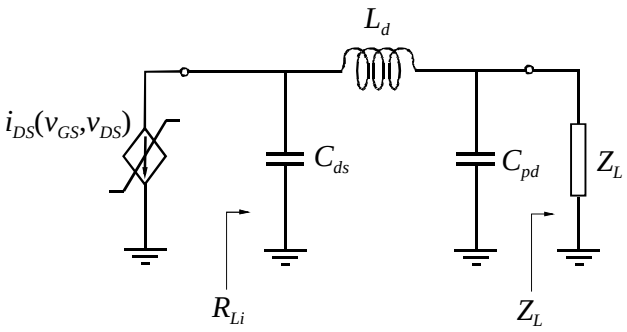


Fig. 5 MESFET output equivalent circuit including parasitics.

Theoretically the value of Zload for the case of Fig. 5 can be calculated as:

$$Z_L = \left\{ \left[\left(R_{L_i}^{-1} - j\omega C_{ds} \right)^{-1} - j\omega L_d \right]^{-1} - j\omega C_{pd} \right\}^{-1} \qquad (1)$$

This expression should be calculated for each resistive load considered, or in this case, for every point in the pure resistive axis of the smith chart.

The application of expression (1) to the resistive axis of the smith chart, will impose a rotation on that axis, Fig.6,

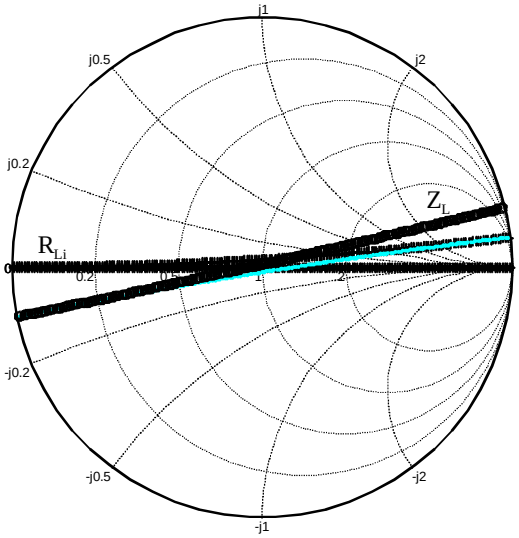


Fig. 6 Rotation of the resistive axis, C_{ds}=C_{pd}=.1pF and L_d=40nH in Fig.5.

III. Simulation Validation

In order to validate those theoretical results an active device biased for presenting IMD large signal sweet spots, and with an input matching network optimized for maximized gain, was simulated for various output loads, filling out most of the smith chart impedances.

The active device equivalent circuit is presented on Fig.7.

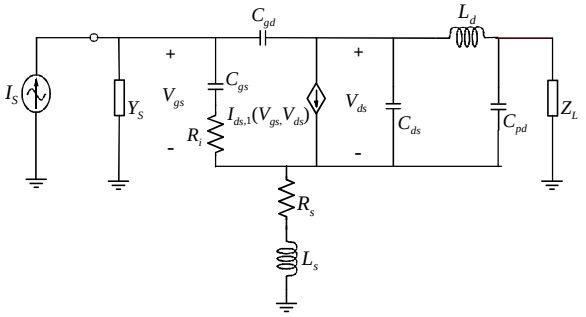


Fig. 7 Active device equivalent.

The built-in setup is the one presented on Fig. 8, where a two tone was inserted at the input of the power amplifier and a tuning device at the output.

The tuning device was simulated considering a one port S parameter, and the values of its magnitude and phase varied.

The simulated load pull curves are presented on Fig. 9 and 10, where the rotation of the resistive axis is visible for the maximized IMD sweet spot, this result is equivalent to the theoretical one presented in the previous section.

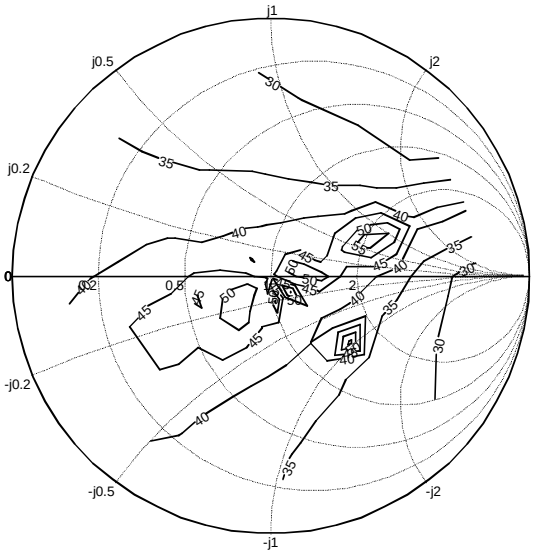


Fig. 9 IMR values at the IMD sweet spot after Load pull simulation.

Other values of load impedance, different from the ones obtained by the parasitic rotation, present lower values of intermodulation ratio, since they impose non resistive values of impedance to the intrinsic active device, which lead to non perfect IMD cancellation.

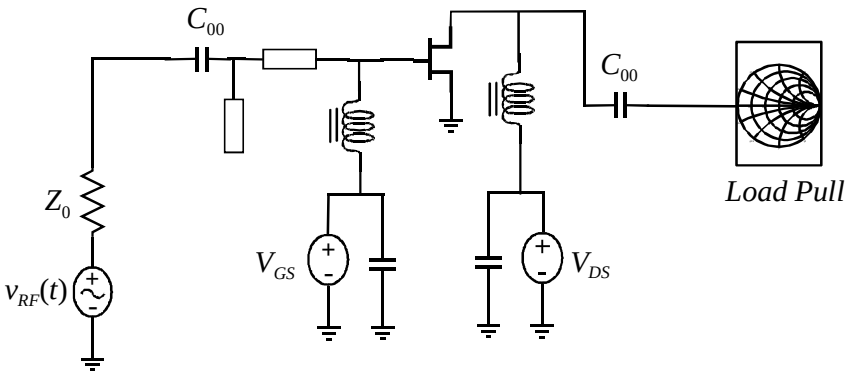


Fig. 8 Load-pull simulated set-up used for evaluating the impact of load impedance on large-signal IMD performance.

Since we are dealing with a power amplifier, it is fundamental that it delivers the maximum power available, so a load pull was simulated for maximum output power too, Fig. 10.

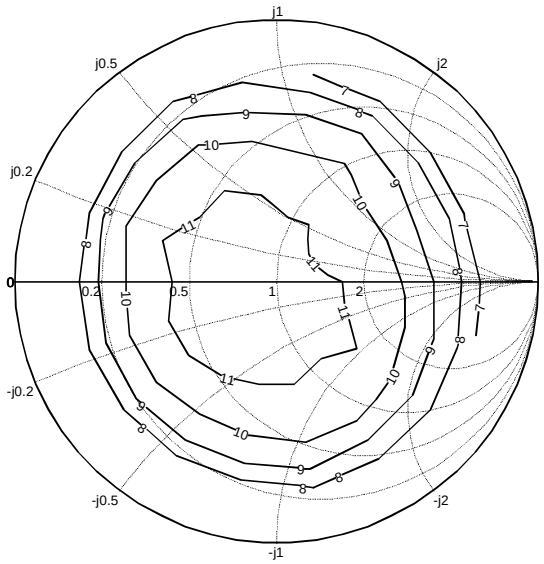


Fig. 10 Load pull results for maximized output power.

As can be seen from Fig.10, the value of the maximum output power is over the line of the maximum IMD large signal sweet spot, which reveals that it is always possible to have a maximum value of IMD sweet spot for a maximized output power.

Finally, a word on the optimum harmonic load selection should be given. From [4] it was seen that an optimum short-circuit at the second harmonic and at the base band is the best selection for IMD sweet spot maximization while the harmonic load at the third harmonic zone is not so important.

This is due to the fact that a non zero impedance at the 2nd order harmonics can have a strong impact on the small signal third order IMD phase, mainly when the device is biased below cut-off.

V. Conclusions

In this paper the optimum load selection for maximized IMD sweet spot was presented, it was observed that all the pure resistive smith chart's axis is able to generate IMD large signal sweet spots, but those occur at different values of input power.

When a real active device is considered, including all the parasitics, then the resistive axis rotates an angle imposed by the reactive parasitics. It was also observed that it is possible to select a load capable of simultaneously maximize output power and IMD sweet spots.

Acknowledgements

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References

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