A Si LDMOS-Based UHF Power Amplifier

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Abstract

The design, implementation and performance tests of an Si LDMOS-Based power amplifier for UHF is presented. The amplifier, conceived for medium power GSM-900 base-station applications, consists of a Class-AB single stage circuit designed for maximum output power capability, and optimized efficiency. It showed a 1dB compressed output power of 6.3W with an associated power added efficiency of 60%.

I. INTRODUCTION

As mobile communications networks spread in services and grow in quality, new challenges are posed on their supporting RF electronics. One of the circuits where this push forward has been mostly sensed is the RF power amplifier, PA, either in its hand-held or base-station versions. For the latter one, maximized output power, power added efficiency and linearity are requirements difficult to be simultaneously reached. For example, this has prevented the use of a single RF antenna driver in nowadays multi-frequency base-stations.

So, system designers have continuously demanded for innovative PA designs and new solid-state devices. One of these emerging technologies, which have presented promising capabilities in terms of output power, Pout, power added efficiency, PAE, and nonlinear distortion, is the Silicon Lateral-Diffused Metal-Oxide Field Effect Transistor, Si LDMOS. As any other RF MOSFET, it shows high power gain in the whole operating frequency range (which for these devices now extends up to C-Band), and especially at HF and the low end of VHF where it poses quite hard problems of out-of-band stability. But, contrary to other RF devices, the RF LDMOS shows very high breakdown voltages and low die-to-package temperature resistance, which enables its use in high power PA's. Associated to that, LDMOS based PA's also show surprisingly good linearity and power gain, even when the quiescent current is as low as 20% of maximum drain-source current. Therefore, the industry of LDMOS devices has been claiming these transistors constitute a novel era of RF power devices capable of simultaneously optimizing Pout, PAE and intermodulation distortion or spectral regrowth. These claims motivated the present work, which evaluates the performances obtained of a Class-AB PA design.

II. MODELING THE LDMOS ACTIVE DEVICE

The device used in this project is a PTF10136 from Ericsson [1], which is rated for 6W @ 900MHz, when biased for V_{DS}=28V.

Nowadays, an equivalent circuit nonlinear representation constitutes an essential tool for any RF circuit design, either if it is manually done or with the aid of an appropriate CAD/CAE package. However, since the LDMOS is a young technology, its foundries have not yet disclosed the necessary characterization. So, due to the lack of modeling information offered on the PTF10136 data sheet, we decided to extract the minimum set of information necessary for our PA design. That included I/V characteristics for bias circuitry design and PAE evaluation, and also a set of bias dependent equivalent circuit models for a first estimate of the achievable RF performance.

We thus begin by extracting a set of output I/V characteristics, which are plotted in Fig. 1.

This device can handle drain-source currents up to somewhat more than 0.5A, with drain-source voltages as high as 65V (drain-source breakdown voltage). Obviously, heat dissipation constraints limited these DC values to only I_{DS}<0.5A and V_{DS}<29V, as seen in Fig. 1. Because, this data corresponds to continuous DC values, not extracted from any form of pulsed excitation, they are affected by temperature variations in the device. This justifies the observed decrease in I_{DS} versus V_{DS} for high I_{DS} values, which is clearly in contrast with the monotonic increase detected for lower currents. Actually, that behavior does not correspond to any real negative output conductance, but simply to the increased MOSFET channel resistance determined by the augmented lattice atoms' kinetic energy.

This DC I/V characterization was then followed by a linear equivalent circuit model extraction. For that, bias dependent S parameters were then measured from 30KHz to 3GHz, which enabled the extraction of the components' values of the circuit schematic shown in Fig. 2. Although the adopted equivalent circuit model could be more complex, the circuit depicted on Fig. 2 was found to be the best trade-off between modeling accuracy and model parameter set extraction simplicity.

Two different equivalent circuit extraction procedures were followed.

[1] This work was undertaken as the Electronics and Telecommunications Engineering degree Final Project of its two first authors.

The first one simply consisted in an optimization process. Such a method necessary leads to a reasonable modeling accuracy, as the optimization goal is exactly the minimization of the error between measured and predicted data. Nevertheless, it was rapidly abandoned as it generated unrealistic values for important parameters as the transconductance, Gm, or the output conductance, Gds. In fact, a comparison between measured DC Gm and RF Gm showed the extraction was physically meaningless. What happened was that a ridiculous small value of Gm was compensated by another absurd small value of Gds.

The second approach was a direct extraction based on the work of [2]. In a first step, the extrinsic elements were found from S parameter measurements of the LDMOS biased in extreme bias points selected from cut-off ($V_{GS}<V_T$) and from the triode zone ($V_{DS}=0$):

$Rg = 0.7\,\Omega \qquad Lg = 1\,nH$

$Rs = 0.2\,\Omega \qquad Ls = 0.052\,nH$

$Rd = 1.2\,\Omega \qquad Lg = 1.2\,nH$

The second step consisted in de-embedding S parameters measured in the sought bias point from these parasitic elements, and then extracting the remaining intrinsic elements: Gm, Gds, Cgs, Cgd and Cds.

An illustrative picture of the predicting capabilities of the extracted model is shown in Fig. 3, where measured and simulated S parameters are compared. A reasonably good agreement is apparent, except may be for S_{12}, which is clearly the most difficult parameter to describe. The noise associated with the measured values is due to an imperfect TRL calibration of the vector network analyzer.

III. LDMOS RF Power Amplifier Design

From the measured device's I/V curves, a quiescent point leading to approximately 5% Ids_{Max} (70mA) was chosen. (70mA, 28V) determines Class-AB operation, a PA class recognized for its good trade-offs in terms of output power, gain and power-added efficiency [3].

The amplifier design was then carried on for maximized output power by first choosing the Cripps load line as the output terminating impedance. For that, the optimum intrinsic load resistance was determined from the measured I/V curves ($R_L \approx 27\Omega$), and then reflected to the output LDMOS terminals using the device's extracted drain network [4]. Because Pout and PAE are almost independent on source impedance, the input termination was selected for optimized gain. With the load impedance previously identified, a linear procedure was followed to determine the input conjugate matching. As load impedance was chosen for optimized output power instead of gain, load mismatch guaranteed the necessary in-band stability.

Source and load impedances obtained in this approximated manner compared well with the ones proposed in the device's data sheet, who were probably derived from time-consuming and very expensive source/load-pull data [1].

Out-of-band stability is a very important issue for these transistors, especially at very low frequencies, where the device presents an extremely high gain. An HF oscillation was in fact detected in our design, which was eliminated using short RF choke terminals, high tantalum capacitors and resistive biasing.

Fig. 4 is a photograph of the implemented LDMOS PA. Microstrip input and output-matching networks built with a low cost epoxy-fiber glass substrate are shown, along with the gate and drain biasing circuits.

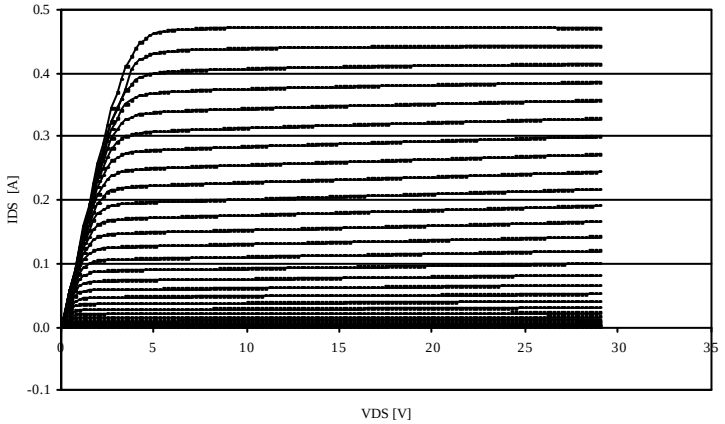


Fig. 1 – PTF10136 output I/V characteristics for constant V_{GS} curves ($3.5<V_{GS}<6.2$).

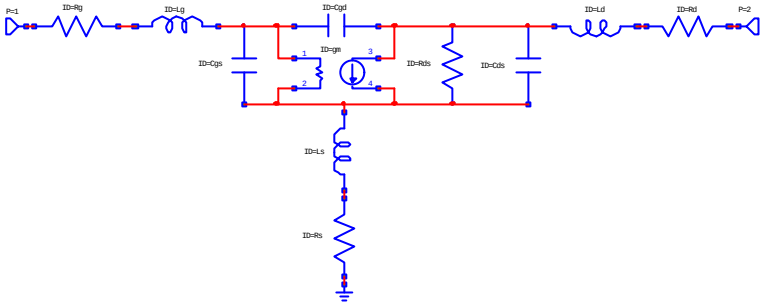
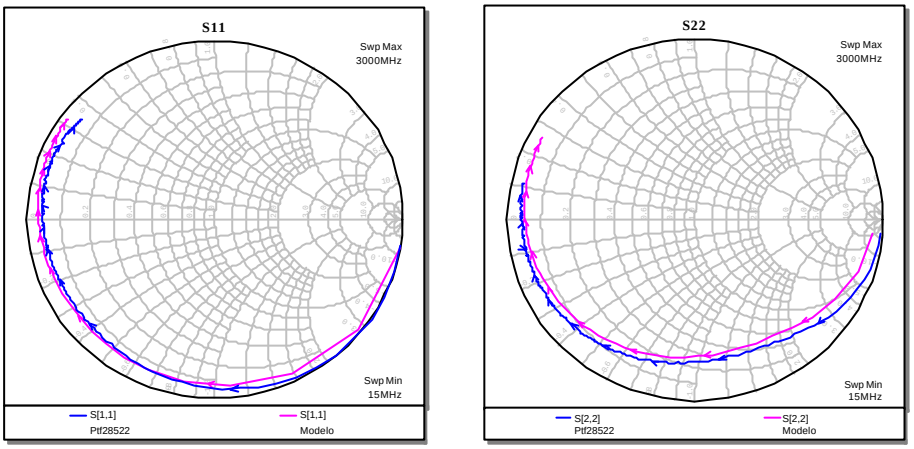
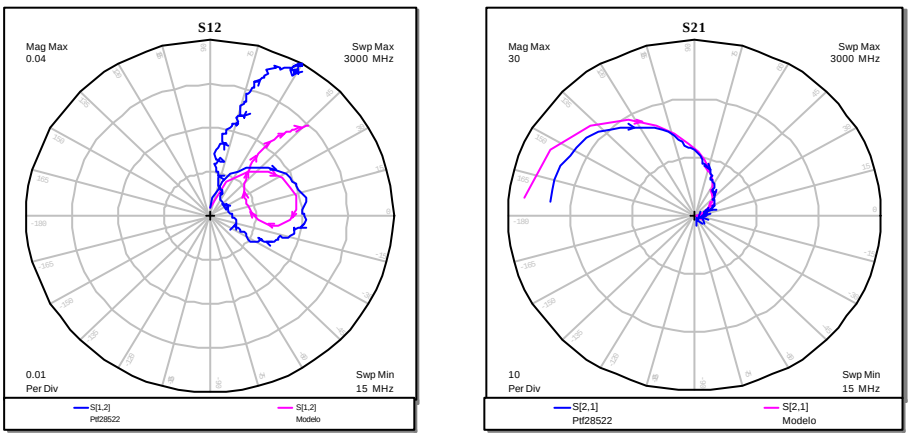


Fig. 2 – Bias dependent linear equivalent circuit model of the PTF10136 LDMOS.



a) **b)**



c) **d)**

Fig. 3 – Measured and simulated S parameters for VDS= and IDS=. a) S_{11}, b) S_{22}, c) S_{12} and d) S_{21}.

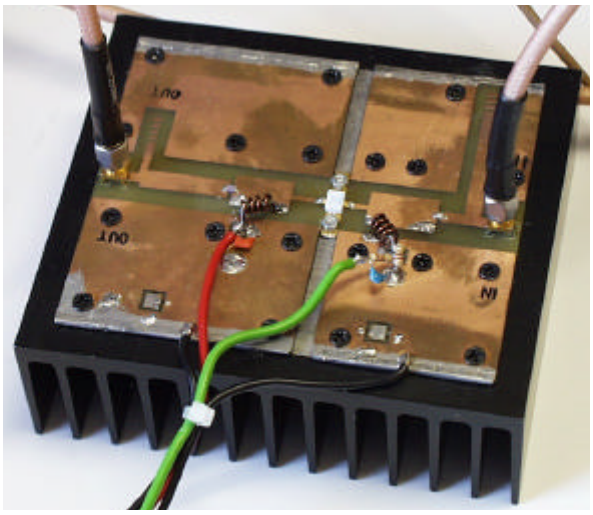


Fig. 4 – Photograph of the implemented LDMOS PA design.

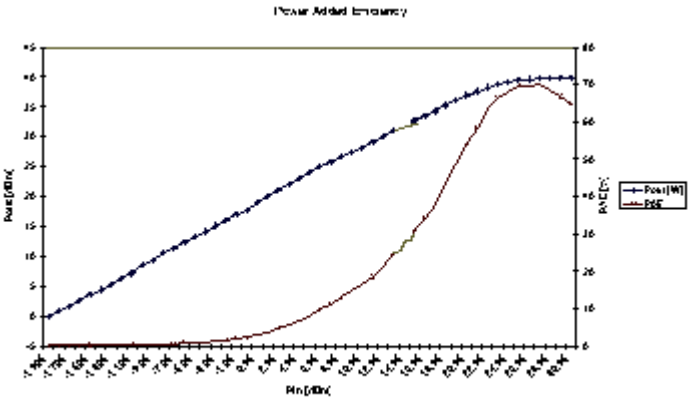


Fig. 5 – Measured output power, Pout, and power added efficiency, PAE.

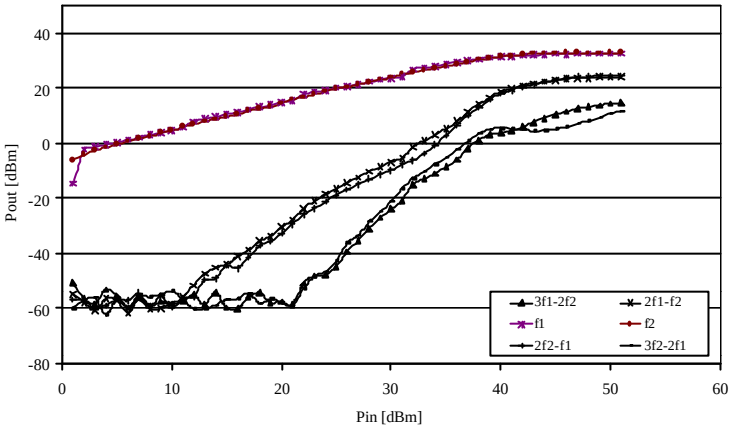


Fig. 7 – Measured output power (P_{f_1}, P_{f_2}) and nonlinear distortion under a two-tone test ($P_{2f_1-f_2}$, $P_{2f_2-f_1}$, $P_{3f_2-f_1}$, $P_{3f_1-f_2}$).

One-tone measurement tests showed a 1dB compression point of P_{1dB}=6.3W with an associated PAE of 60% as depicted in Fig. 5. These values constitute quite good results when compared with the ones present in the data sheet (6W<P_{1dB}<7.5W and 50%<PAE<57%), which validate the design procedure and the low cost implementation adopted.

Finally, Fig. 7 shows two-tone IMD measurements for nonlinear distortion assessment.

From fig. 7, similar results, for the IMD behavior, than in the MESFET case can be observed, for example in a class AB, no IMD large signal sweet spots [5] are generated.

IV. Conclusions

This paper reported the design of a Si LDMOS RF power amplifier for mobile radio applications. The design methodology was founded on a bias dependent equivalent circuit model extraction, and the Cripps load-line technique. The implemented PA showed 6.3W of output power (P_{1dB}) and an associated 60% efficiency (PAE), which were good results as compared to the ones specified for the device in use.

Acknowledgements

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References

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