

Design Techniques for Highly Efficient Class-F Amplifiers Driven by Low Voltage Supplies

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Abstract

The present paper provides design techniques for highly efficient microwave power amplifiers driven by low voltage power supplies. Main power amplifier design variables, such as conduction angle and fundamental and harmonic load impedance terminations, are studied, to enable the selection of the optimum parameter set under small voltage operating conditions. Theoretical predicted conclusions are then validated with a practical S-band GaAs monolithic microwave integrated circuit, MMIC, class-F power amplifier.

1. Introduction

The rapid growth of mobile telecommunications services, like GSM or DCS1800, created an increased demand for highly efficient RF and microwave power amplifiers dependent on small supply voltages [1]. In fact, since it is widely known that the RF power amplifier is one of the most critical blocks, in terms of DC power consumption, and that battery capacity determines the final height of modern handsets, it is clear that this RF circuit deserves increased design research.

The design of amplifiers with power added efficiencies, PAE, in excess of some 50% requires the use of small conduction angles, 2θ , and thus class-B or C operation [2]. That design strategy can compensate the potential loss of output power capability, P_{out} , imposed by the reduced conduction angle, using larger voltage excursions and peak currents. If voltage supply is diminished (because of the need for reduced battery size), P_{out} and PAE may be kept at the specified values by further increasing the active device output peak current. At microwave frequencies this scenario is worsened because of the transistor used: GaAs MESFET's. In fact, this type of device presents three important disadvantages for power amplification, when compared to the traditional BJT used at lower bands [3], [4]. First, they show a natural maximum current capability determined by the input junction conduction and saturated channel widening. Second, class-B or C are generally not tried, because high power devices usually show gate-channel breakdown before bias cut-off can be achieved. And third, they have a much greater

RF knee voltage (defined as the transition between triode and saturated regions). Therefore, a bigger impact in output power and efficiency should be expected for MESFET based power amplifiers driven by low voltage supplies, when compared to their VHF or UHF counterparts.

Beyond that, it should be also clear that very small conduction angles are not a good option at higher frequencies, since for similar output current excursions the input voltage swing must be greater. An increase in RF input power consumption is sensed, which corresponds to a decrease in power gain. Therefore, PAE can not pass a certain upper limit, even if DC-RF conversion efficiency, η_{DC} , (some times called collector or drain efficiency), is optimised [3], [4].

To circumvent these problems, at least two different design strategies have been proposed [2], [4], [5]. The first one controls loading of higher harmonic current contents, while the other concentrates on the optimum selection of fundamental frequency load impedance. The main objective of this paper is to evaluate the impact of these two design parameters on P_{out} and PAE, and to derive a set of general design rules useful for their selection. For that, we began by a theoretical study on the dependence of P_{out} and PAE on load impedance at the fundamental. This enabled the conclusion that, in voltage limited power amplifiers, there is a strong compromise between maximum P_{out} and PAE. It could be shown that optimum load line corresponds to an intrinsic load resistance greater than the one predicted by the traditional Cripps rule, which simply maximises P_{out} [4], [6]. Then, a rigorous simulation scheme was used to derive optimum conduction angle and load impedance at 2nd and 3rd harmonics. According to what was previously published, it appears that the best conduction angle leads to class-AB type of operation. However, in the case of harmonic impedances not one, but two different sets were found. The first one, is the widely known short circuit at 2nd harmonic and open circuit at 3rd, to create an almost rectangular output voltage wave form [2], [5]. The second one is exactly the opposite to that, i.e., open circuit to the 2nd harmonic and short circuit to the 3rd. In order to test this rather surprising results an 100mW S-Band MMIC

power amplifier was built and characterised, using these new design rules. A P_{out} of about 19.5dBm and 50% PAE could be measured, which fully validates the proposed conclusions.

2. Optimum Load Line Selection

To study the impact of load line selection on P_{out} and PAE of a voltage limited power amplifier, a general MESFET circuit was considered. The intrinsic device was represented by a simple unilateral equivalent circuit, where the drain source current, $I_{ds}(V_{gs}, V_{ds})$, was modelled by one of its traditional nonlinear models, the Raytheon-Statz model [7]. Gate-source voltage, V_{gs} , control of channel current was thus considered approximately quadratic, while triode to saturation transition was represented by an hyperbolic tangent of drain-source voltage, V_{ds} . Input voltage excitation was assumed sinusoidal, but corresponding to typical class-AB operation. Output voltage and current were calculated by solving the nonlinear equations imposed by the MESFET $I_{ds}(V_{gs}, V_{ds})$ current, and the output boundary conditions defined by R_L and a power supply voltage of 3V. The load resistance (which is simply the inverse, and symmetric, of the load line's slope) was then varied from zero to infinity, and P_{out} and DC-RF conversion efficiency calculated for each of the simulated values. Fig. 1 shows the results of this study.

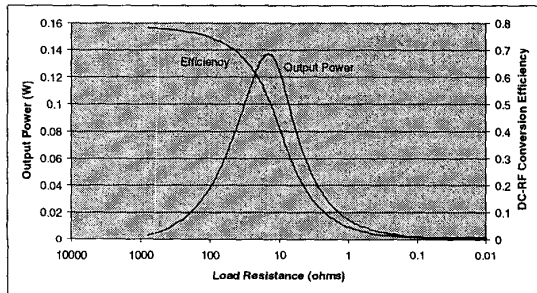


Fig. 1. Calculated output power and DC-RF conversion efficiency versus load resistance of ideal MESFET power amplifier.

A compromise between optimum load resistance for maximum output power and efficiency is now clear from that figure. The optimum condition for maximised P_{out} is encountered for some 15Ω , which results in P_{out} and PAE near 21dBm and 52%, respectively. (Since, in this ideal situation, it is assumed that the device's RF input power consumption is null, η_{DC} and PAE are equal). That resistance corresponds to the standard Cripps load line selection [6]. However, if an higher resistance were tried, the slight decrease in P_{out} could be compensated by an important rise in PAE. That is the case of a 30Ω

load resistance where a 1dB loss in P_{out} allowed a 13% rise in PAE.

From the above study one can conclude that, in general voltage limited MESFET based amplifiers, the optimum load line that simultaneously optimises P_{out} and PAE, should have a slope significantly less than the one obtained for only P_{out} .

3. Optimum Conduction Angle Selection

Selection of the best conduction angle for maximised P_{out} and PAE is now addressed. First, it should be said that, since V_{DS} bias is fixed at the power supply voltage V_{DD} , choosing a conduction angle is equivalent to selecting an appropriate quiescent point $I_{DS}(V_{GS}, V_{DS})$. As was said in the Introduction, reduced conduction angles induce lower output power capabilities and may not be able to improve PAE, even if η_{DC} could be constantly increased. Therefore, to choose the optimum conduction angle we decided to simulate a typical 3V MESFET power amplifier circuit with a nonlinear microwave Harmonic-Balance package. Various conduction angles were tested, corresponding to class-A - $2\theta=360^\circ$, class-AB - $180^\circ < 2\theta < 360^\circ$, and class-C - $0^\circ < 2\theta < 180^\circ$. The results thus obtained are summarised in Table 1.

Observation Point	η_{DC} (%)	PAE (%)	P_{out} (dBm)	G_T (dB)
Class-A				
1dB Compression	45	43	17.6	12.7
Maximum PAE	58%	57	18.8	9.8
Class-AB				
1dB Compression	59	59	17.8	7.8
Maximum PAE	61	61	18.1	7.1
Class-C				
1dB Compression	49	48	15.0	5.0
Maximum PAE	62	61	17.6	4.6

Table1. P_{out} and PAE performance figures of typical MESFET power amplifier versus conduction angle.

In order to get a complete view of the dependence of amplifier characteristics on conduction angle, η_{DC} and transducer power gain, G_T , were also registered. Also, two different driving points were considered. The first one refers to the onset of saturation, herein considered as the 1dB compression point. The other one is the point of maximum PAE, which corresponds to an already strongly saturated regime. It should be noted that, in this latter case, the output current wave form is clearly distorted not only by cut-off, but also by the entrance in the FET's triode region. Thus, $I_{ds}(t)$ left its previous form of sinusoidal pulses, and the traditional theoretical predictions of η_{DC} dependence on conduction angle [2]

no longer apply. This justifies the intuitive knowledge that the device's wave forms should be almost independent on the quiescent point, if it is hardly driven into saturation. That can be perfectly observed from Table 1 which shows maximum PAE values varying from only 57% to 61% when the amplifier is biased for class-A, AB or even C mode of operation.

In fact, it is clear that, in terms of optimised efficiency, class-AB, B or C are very similar, although class-AB should be preferred if the amplifier is expected to operate near the 1dB compression point. Also important is the observed decrease in power gain: class-C gain was reduced to less than one fourth of the maximum G_T obtained for class-A. In conclusion, it seems that in voltage limited microwave power amplifiers quiescent points corresponding to class-AB operation should be adopted. In other words, optimum conduction angle can be considered approximately the same, whether or not the MESFET amplifier output signal excursion is limited by a small power supply voltage.

4. Harmonic Loading Optimization

Finally, the impact of load impedance terminations at 2nd and 3rd harmonics was also investigated. For that, the previous power amplifier was again simulated in the HB package. According to the former analysis, the load impedance at the fundamental was maintained at its optimum value determined with the procedure explained in Section 2. However, now the output high Q resonant circuit was substituted by an ideal two-port [S] matrix network. This two-port allowed a very easy and free definition of the amplifier's output matching circuit. Transmission (S_{21}) was considered unity for ω_0 and null

for $2\omega_0$ or $3\omega_0$. Four purely reactive terminations were then independently assumed for $2\omega_0$ and $3\omega_0$, $S_{11}=[+1, +j, -1, -j]$, and all possible sixteen combinations simulated. Simultaneous maximisation of Pout and PAE was observed for two different harmonic terminations: A - [$Z_L(2\omega_0)=0, Z_L(3\omega_0)=\infty$] and B - [$Z_L(2\omega_0)=\infty, Z_L(3\omega_0)=0$]. Case A traduces the traditional procedure of creating a square wave output voltage, by increasing its odd harmonic contents [5]. Improved PAE is guaranteed by the switching mode of operation that characterises all class-E and F power amplifiers [2]. Case B, however, seems a rather surprising result as it represents the inverse of case A. The explanation encountered for that situation is that the presence of a strong 2nd harmonic component at the drain voltage produced a very high peak (about 8.5V for a 3V V_{DD}) which somewhat compensates for the loss a voltage swing imposed by the limited supply voltage.

5. MMIC S-Band Power Amplifier Design

In order to validate the above conclusions drawn for optimum load line, conduction angle and harmonic loading a GaAs MESFET MMIC power amplifier was design and tested. Because of its increased research interest, Case B for the harmonic component's terminations was adopted. Due to future mobile communications demands, central frequency was fixed at 2.155GHz and specified output power at 20dBm. The available MMIC process was the F20 from GEC MARCONI, which is a small signal-low noise implant foundry process, not primarily intended for power applications.

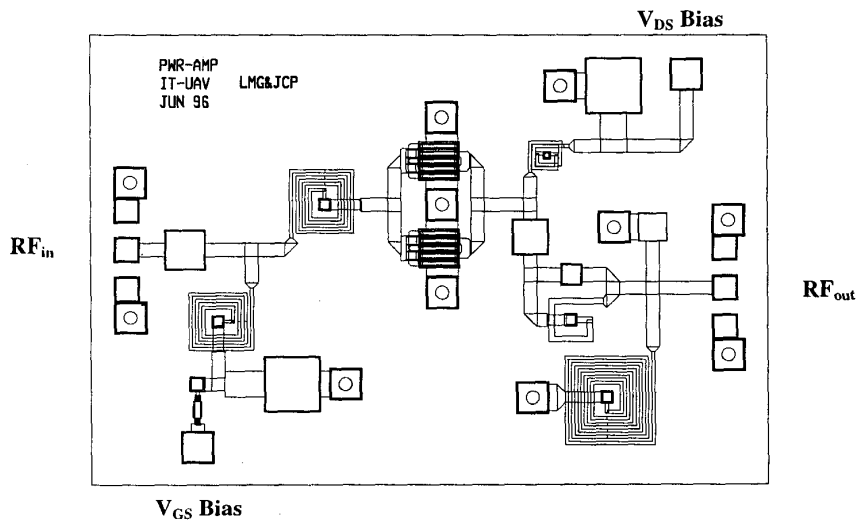


Fig. 2. Layout of the implemented 3V GaAs MMIC power amplifier chip.

Fig. 2 is the layout of the 3V MMIC implemented amplifier. The equivalent active device is composed of two $4 \times 150 \mu\text{m}$ MESFET's in parallel, which gives a combined I_{DSS} of near 200mA. The input matching circuit is simply an L network of inductors, designed for maximum power gain. Because of the required load impedances at the fundamental, 2nd and 3rd harmonics, the output network is significantly more complex. It is composed of three resonant circuits. The one nearest to the external 50Ω load is tuned for the fundamental, while the one located between the FETs and the load, guarantees the required high Z_L at $2\omega_0$. Finally, the parallel resonant circuit directly connected to the FETs' drain terminals provides the necessary low 3rd harmonic termination and V_{DS} bias, without significantly disturbing the load impedances at ω_0 and $2\omega_0$. Simulation results of this amplifier, with lossless passive components, gave 77% PAE and a P_{out} of 21.4dBm, which are remarkable results for a 3V amplifier. Although, those values dropped to 52% and 20dBm when the ideal reactive elements were substituted by their low Q MMIC equivalents, they fully validate the design methodology proposed in the former sections. Fig. 3 presents simulated drain current and voltage wave forms of the MMIC prototype, in its maximum PAE driving point. There is an evident saturation behaviour of I_{ds} , along with the high V_{ds} peaking provided by the high $Z_L(2\omega_0)$. Finally, Fig. 4 represents measured P_{out} and PAE versus RF source available power, after the chip was placed onto a microstrip carrier and connectorised. Results of 50% and 19.5dBm for PAE and P_{out} , respectively, were found to be very close to the predicted ones.

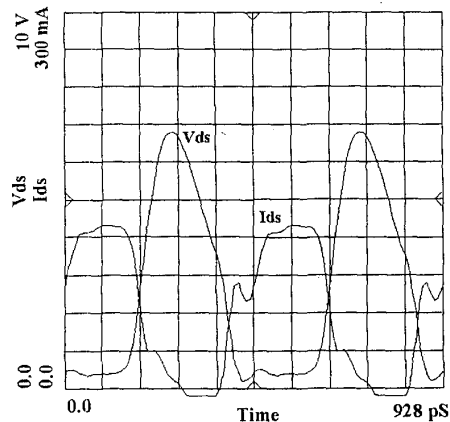


Fig. 3. Simulation results of drain source current and voltage of the implemented MMIC amplifier.

6. Conclusions

In conclusion, selection of the most important amplifier parameters was discussed when the circuit is powered by a low voltage supply. Design rules for load line, 2nd and 3rd harmonic terminations, and quiescent point were derived for a general circuit, and then validated with an 3V S-Band GaAs MMIC amplifier chip.

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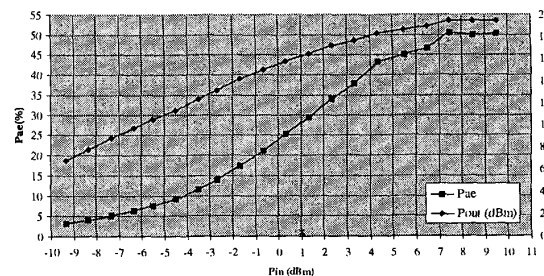


Fig. 4. Measured results of power added efficiency, PAE, and output power, P_{out} , of the connectorised MMIC amplifier.