Intermodulation Distortion Behavior in LDMOS Transistor Amplifiers

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Abstract— An analysis of the intermodulation distortion (IMD) behavior of LDMOS transistor amplifiers is presented. It is shown that the turn-on region abruptness compared to most other devices is important for explaining measured IMD behavior such as sweet-spots. The analysis is validated using two-tone measurements at low frequency for different classes of operation. A 1.9 GHz LDMOS power amplifier is designed and characterized to investigate the IMD behavior also at higher frequency.

Index Terms--LDMOS, intermodulation distortion, power amplifiers

I. Introduction

In many modern wireless systems, the linearity requirements put strong restrictions on the power amplifiers used. It has been found that LDMOS transistors exhibit better intermodulation distortion (IMD) performance compared to competing technologies [1, 2]. LDMOS transistors are therefore widely used in power amplifiers at microwave frequencies in commercial applications such as base-station transmitters.

A good understanding of the device characteristics is necessary to take full advantage of the LDMOS technology when building amplifiers—for optimization of IMD performance it is even crucial.

The IMD behavior of MESFET power amplifiers has been analyzed in [3]. However, since the LDMOS characteristics are different from the MESFETs' it is necessary to revise the analysis to predict measured IMD behavior.

In this paper it is shown that the sharp turn-on of the LDMOS compared to MESFET plays an important role in explaining additional IMD minima that appear in class B and AB [1]. This may also be a clue to the superior linearity of LDMOS transistors.

IMD measurements made at low frequency corresponding to different classes of operation are used to verify the analysis and give an overview of the LDMOS IMD behavior.

Finally, measurements made on a 1.9 GHz LDMOS amplifier are used to examine how the IMD behavior is affected at higher frequencies.

II. Intermodulation Distortion Analysis

In [3] the IMD behavior of power amplifiers was analyzed by studying the input voltage/output current transfer function, $I_{out}(V_{in})$. The transfer function is determined from the load impedance in conjunction with the transistor $I_{ds}(V_{gs},V_{ds})$ characteristic, Fig. 1.

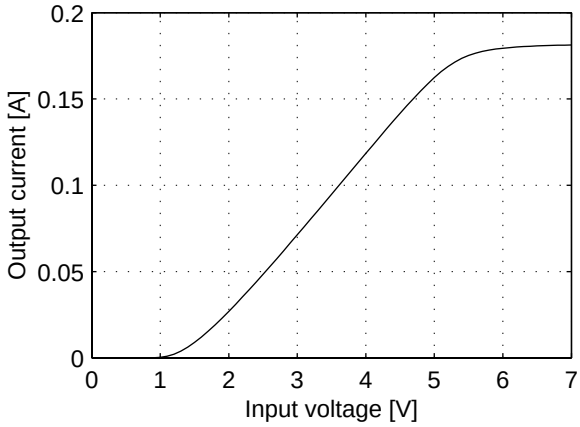

Fig. 1. Typical LDMOS transfer function, $I_{out}(V_{in})$.

Since the transistor is biased in the saturated region for amplifier operation, the transfer function is essentially equal to the transistor $I_{ds}(V_{gs})$ characteristics for low input power. At higher input power, the output current is saturated by either the load-line entering the triode region, or the JFET-effect in the LDMOS drift region [4].

For low input power a Volterra series analysis may be used to calculate the IMD behavior [3]. The analysis is based on a Taylor series expansion of the transfer function,

$$I_{out}(v_{in}) = I_{out,DC} + G_1 v_{in} + G_2 v_{in}^2 + G_3 v_{in}^3 + G_4 v_{in}^4 + G_5 v_{in}^5 \quad (1)$$

where the coefficients, G_n, represent the transfer function derivatives and v_{in} the applied time-varying input voltage (see Fig. 2). Usually a two-tone sinusoidal input signal is applied to assess the IMD characteristics. The 3-dB/dB slope of the third order intermodulation distortion (IM3) power at low input power can then be predicted. It has also been found that an interaction between third and fifth order non-linearities can give rise to an IMD sweet-spot if they

are of opposite signs [3]. However, since the influence of the fifth order derivative is typically much smaller, this usually happens at an input power beyond the validity of the Volterra series analysis.

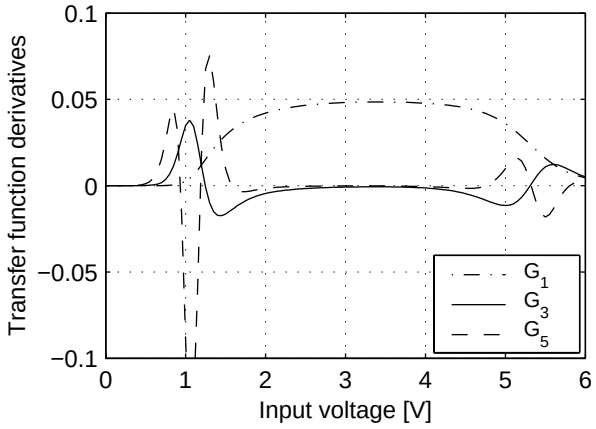

Fig. 2. Typical LDMOS transfer function, $I_{out}(V_{in})$, derivatives versus input voltage, V_{in}.

The Volterra analysis is used up to a power where the input or output signal excursion reaches a strong non-linearity. The strong non-linearities usually considered are: breakdown, compression due to the load-line entering the triode-region or the gate-diode forward conduction in MESFETs.

In LDMOS transistors the turn-on knee is sharper than in MESFETs. A very high order power series is therefore necessary to describe the current also beyond this point as shown in Fig. 3. This is also seen from the large value of G_5 in this region in Fig. 2.

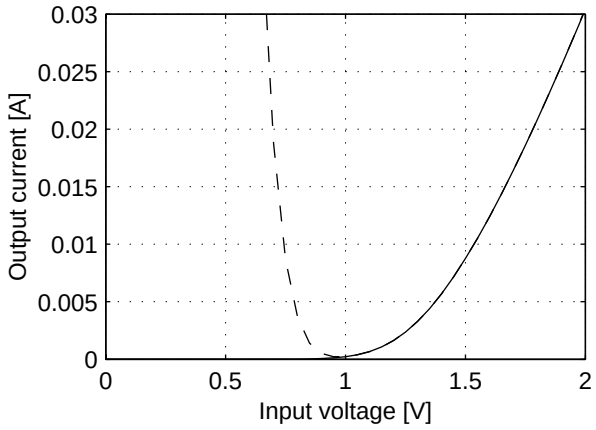

Fig. 3. Detailed view of the turn-on region, showing I_{out} (solid) and a 10th order Taylor series expansion (dashed) around V_{in} = 1.5 V.

The turn-on can be described by a transition from an exponential sub-threshold region to a quadratic region [5]. It can be shown, using a Two Sinusoidal Input Describing Function analysis, that such a non-linearity results in a positive IM3 contribution that increases with input power as soon as the input signal traverses the turn-on knee. This means that the turn-on region represents an expanding non-linearity where the amount of positive IM3 contribution is determined by the turn-on region abruptness.

As the input power increases further, the output power compresses which implies that IM3 must become negative [3].

The expanding and compressing non-linearities of the turn-on and saturation regions respectively can counteract each other to create an overall more linear operation. The same principle is in fact used in pre-distortion linearization of amplifiers [6].

III. Measured IMD Behavior

Two-tone measurements on a high-voltage LDMOS transistor [7] have been performed to study its IMD behavior. The transistor used has I_{dss} = 175 mA and was biased at $V_{ds,dc}$ = 20 V during the measurements, which were made at 100 MHz with 1 MHz frequency separation in a 50 Ω environment.

Depending on the class of operation different IMD characteristics can then be described using the behavioral analysis in the previous section.

A. Class C operation

From Fig. 2, the third order derivative of the transfer function is seen to be positive in class C, $V_{in,\ dc}$ = 0.9 V. This implies that IM3 is also positive for low input levels [3]. The additional positive contribution from the turn-on region increases the slope of the IM3 curve. However, when the output power saturates, IM3 must become negative. Hence, an IMD minimum occurs near the compression point. Fig. 4a shows the measured output power and IM3 for this case. Similar IMD behavior has been observed in class C MESFET and BJT amplifiers [1, 3, 8].

These kinds of sweet-spots near the output power compression point, give locally a very large carrier to intermodulation (C/I) ratio. However, in real amplifiers the input power may vary. It is therefore difficult to make use of this phenomenon for sufficient IMD suppression in those applications.

B. Class AB operation

To achieve better IMD performance, still having acceptable gain and efficiency, amplifiers are commonly designed to operate in class AB. This corresponds to a negative G_3 as seen in Fig. 2. The measured output power and IM3 for two bias voltages, at $V_{in,\ dc}$ = 1.2 V and $V_{in,\ dc}$ = 1.3 V, in class AB are shown in Fig. 4b and Fig. 4c, respectively.

The first of the two minima appear when the negative contribution from G_3 is cancelled by the positive IM3 contribution from the turn-on region. Since the turn-on region influence is much larger, the minimum appears as soon as the input signal reaches that region. The minimum will therefore occur at a higher input power if the transistor is biased further away from turn-on. This is confirmed by comparing the IM3 measurements. As the input power increases further, IM3 will remain positive until the output power compresses and IM3 becomes negative. This shift of

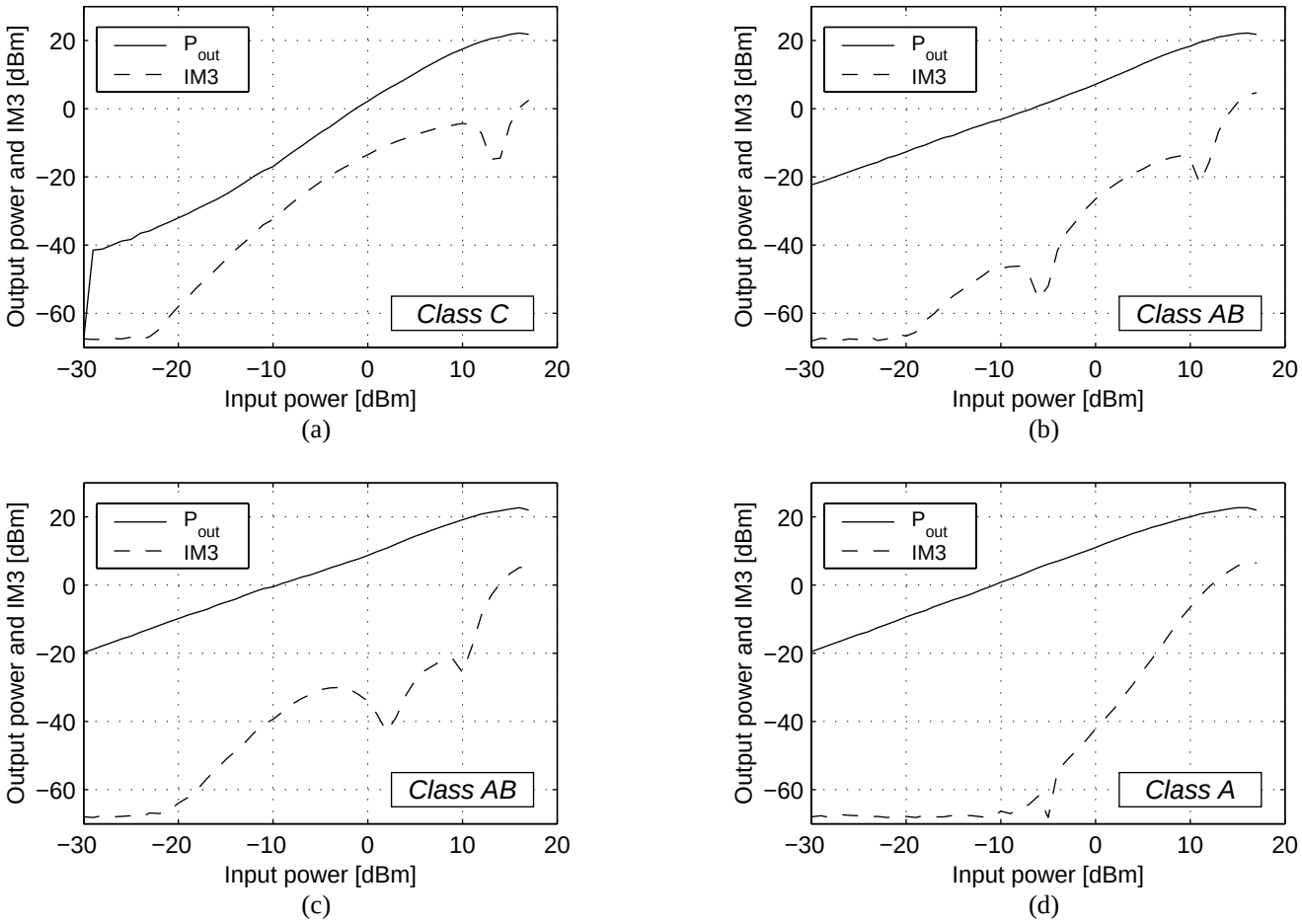

Fig. 4. Output power (P_{out}) and third order intermodulation distortion power (IM3) measured at 100 MHz for: (a) Class C, $V_{in,dc}$ = 0.9 V. (b) Class AB, $V_{in,dc}$ = 1.2 V. (c) Class AB, $V_{in,dc}$ = 1.3 V. (d) Class A, $V_{in,dc}$ = 2.5 V.

sign in IM3 creates another sweet-spot, close to the compression point.

By a proper choice of gate bias, the two minima can be combined to create a large C/I ratio over a much wider input power range near the compression point compared to class C operation (see Fig. 4c).

C. Class A operation

As the bias is increased towards class A, G_3 will remain negative. The difference compared to class AB is that the input signal will now reach the power saturation region before the turn-on region. IM3 will therefore remain negative and thus no IMD minimum is observed in Fig. 4d.

Class A is usually considered the most linear mode of operation. Fig. 4 shows however that class AB may in fact be more linear at a wide input power range due to the double minima present. Recognizing that the efficiency is also substantially better in class AB makes this behavior very attractive.

IV. Power Amplifier Circuit Example

A 1900 MHz power amplifier for 28 V supply voltage was built using the same device as in the previous section to examine the IMD behavior also at higher frequencies. The amplifier was designed to operate in class AB with the input matched for maximum gain and the output impedance chosen for maximum output power [9]. The output network was designed to short-circuit signals at second harmonic and base-band to improve the IMD behavior [3].

The saturated output power was measured to be approximately 27 dBm with a small-signal gain of 12 dB. The maximum power added efficiency (PAE) is 20%. The output power and efficiency are shown versus input power in Fig. 5.

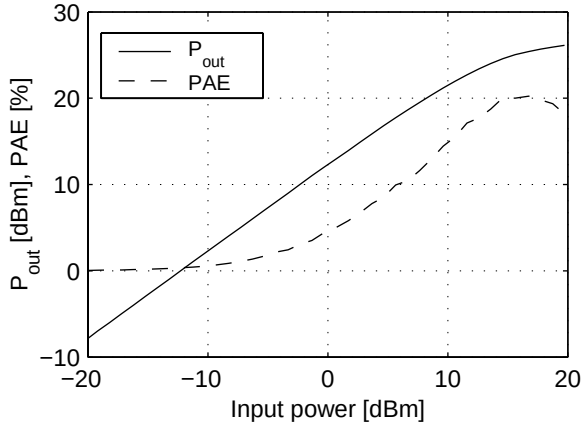

Fig. 5. Measured output power and efficiency versus input power at 28 V supply voltage.

The IMD performance was measured using a two-tone test with 1 MHz frequency separation. Fig. 6 shows measured C/I for various input bias voltages. The measured sweet-spot is less pronounced at 1.9 GHz compared to 100 MHz and the sweet-spot that appear near the compression point at lower frequency also seem to have disappeared.

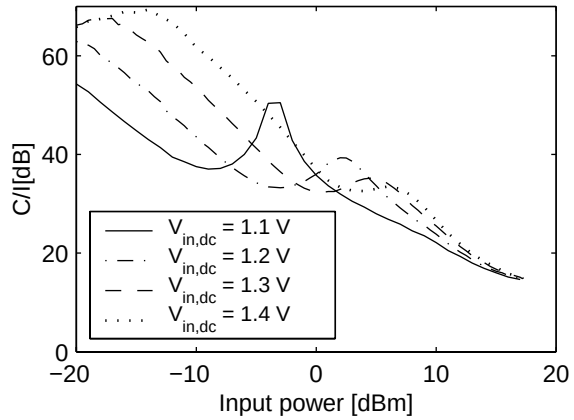

Fig. 6. Measured carrier to intermodulation ratio (C/I) versus input power at different input bias voltages.

Since the $I_{out}(V_{in})$ transfer function is dominated by the gate voltage dependence, the IMD behavior should ideally not be very dependent on the frequency of operation. However, capacitive feedback of $2f_{in}$ from the transistor output creates quadrature phase IMD components that can explain that the IMD minima are less pronounced at higher frequency [3].

As predicted in the analysis for operation in class AB, the measurements validate however that a bias-dependent IMD sweet-spot is present also at higher frequencies.

V. Conclusions

A behavioral analysis of the IMD in LDMOS amplifiers is presented and validated using measurements under various operating conditions. The analysis relates the device characteristics such as $I_{out}(V_{in})$, compression point, and turn-on knee to the measured IMD behavior. It has been shown that relative abruptness of the turn-on region compared to other technologies may explain the surprisingly linear nature of LDMOS transistors in power amplifier applications.

Differences between measurements made at 100 MHz and 1.9 GHz highlight the importance of accurate device models, including non-linear capacitances, for accurate prediction of IMD behavior also at higher frequencies. Nevertheless, the existence of a bias-dependent IMD sweet-spot was accurately predicted from the low frequency analysis.

The results obtained are important from an industrial point of view, since they explain how a linear class AB power amplifier, based on LDMOS technology, can be designed to present high values of C/I. Thus showing an improvement compared to MESFET based designs where only class B or C could be used.

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References

[1] S. R. Novis and L. Pelletier, "IMD parameters describe LDMOS device performance," *Microwaves & RF*, vol. 37, pp. 69-74, July 1998.

[2] J.-J. Bouny, "Advantages of LDMOS in high power linear amplification," *Microwave Engineering Europe*, pp. 37-40, Apr. 1996.

[3] N. B. Carvalho and J. C. Pedro, "Large- and small-signal IMD behavior of microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, pp. 2364-74, Dec. 1999.

[4] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and characterization of an 80 V silicon LDMOSFET for emerging RFIC applications," *IEEE Transactions on Electron Devices*, vol. 45, pp. 1468-78, July 1998.

[5] Y. Tsividis, *Operation and modeling of the MOS transistor*, 2 ed. Boston: WCB/McGraw-Hill, 1999.

[6] P. Kenington, *High linearity RF amplifier design*. Norwood, MA: Artech House, 2000.

[7] A. Soderbarg, B. Edholm, J. Olsson, F. Masszi, and K. H. Eklund, "Integration of a novel high-voltage Giga-Hertz DMOS transistor into a standard CMOS process," *Proc International Electron Devices Meeting*, pp. 975-8, 1995.

[8] C. C. Blanco, "Gain expansion and intermodulation in a MESFET amplifier," *Electronics Letters*, vol. 15, pp. 31-2, July 1979.

[9] S. C. Cripps, *RF power amplifiers for wireless communications*. Boston: Artech House, 1999.