Load-Impedance Selection for Maximized Large-Signal IMD Sweet-Spot Effects

Nuno Borges Carvalho,[1] José Angel García,[2] Edurne Azpitarte,[2] José Carlos Pedro[1]

[1] Instituto de Telecomunicações, Universidade de Aveiro, Portugal
[2] Universidad de Cantabria, España

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ABSTRACT: This work describes the impact of the output termination impedance on large-signal intermodulation distortion (IMD)—sweet spots appearing in FET-based power amplifiers. Theoretical studies validated by appropriate measurement results lead to a systematic methodology for selecting the optimum load-impedance value at the fundamental to be presented at the device output. © 2005 Wiley Periodicals, Inc. Int J RF and Microwave CAE 15: 434–440, 2005.

Keywords: power amplifier; IMD; nonlinear circuits

I. INTRODUCTION

The growth of wireless communications has steadily increased the demand for highly efficient digital-modulation techniques, which enable the transmission of more information while maintaining a minimum of spectral occupation.

However, spectral regrowth, a common form of the nonlinear distortion generated by some transmitting and receiving blocks, constitutes a serious obstacle to this goal. This is one of the most important reasons why the use of linear devices has became a necessity.

Since the final stage of the transmitter chain—the power amplifier (PA)—plays a key role in nonlinear-distortion generation, most recent efforts to enforce linear operation have been focused on that component [1–4].

Different approaches have been employed to achieve this type of linearity improvement. The use of external linearization schemes has been the most common solution. However, these schemes present many problems, such as an increased number of components, circuit complexity, increased power consumption, sensitivity to signal bandwidth and environmental conditions, and so forth. Thus, other alternatives that focus on an understanding of mechanisms for nonlinear distortion generation and its direct reduction have also been proposed.

One of these methods is based on the existence of large-signal intermodulation distortion (IMD) sweet spots. These are minimum-output IMD values appearing at certain input-power levels that are thus called "sweet".

Although several articles have already dealt with this interesting feature, the core of those works has been the study of the technology behind the PA, and the correct selection of the bias point. For example, in [5] a MESFET was studied, while in [6, 7] an LDMOS and a CMOS were respectively characterized.

Although recognized in both theory and practice as another important parameter, output termination has been largely left uncovered.

In this article, the impact of the load-matching circuit on the IMD sweet spot is thoroughly studied, and a systematic methodology for load-impedance selection is proposed. Section II provides a brief revision of the interesting points of the IMD versus the

Correspondence to: Nuno Borges Carvalho; e-mail: nborges@ieee.org.

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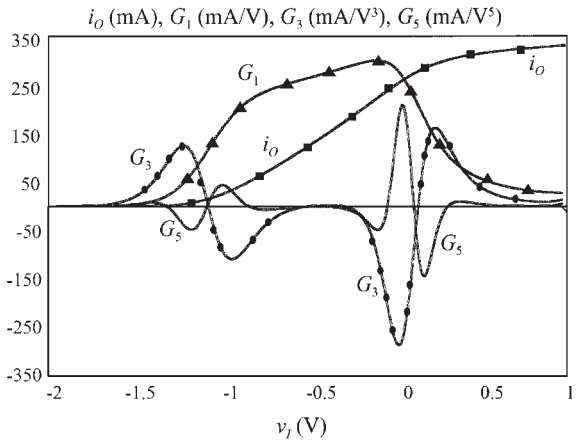

Figure 1. MESFET characteristic function and its first three odd-order derivatives.

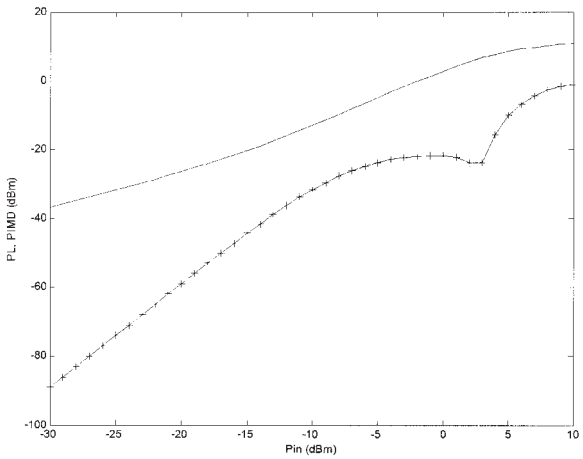

Figure 2. Generation of large-signal IMD sweet spot: output (——) and intermodulation-distortion (-+-) power evolution with input power, when the transistor is biased below cutoff in a positive value of G_{m3}.

input power pattern. Then, section III presents a study of the optimum impedance value that should be seen at the device output. Finally, some measurement results are given in section IV in order to validate the proposed theoretical conclusions.

II. LARGE-SIGNAL IMD SWEET SPOTS REVISITED

Large-signal IMD sweet spots are generated every time the small- and large-signal IMD components interact with opposite signal phases. For instance, consideringing the input-output characteristic functions of a MESFET, as shown in Figure 1, it is found that the optimum bias point for the generation of an IMD sweet spot is one where the small-signal IMD is in phase with the fundamental component [5]. Since, for a large signal, compression mechanisms impose an IMD whose phase tends to oppose that of the fundamental, a large-signal IMD sweet spot will appear in the boundary between these two zones of excitation level (see Fig. 2).

Other types of active devices, for example, MOSFETs, present a similar IMD behavior. Compared to MESFETs, these points continue to appear not only in large-signal operation, but they can also arise for medium-signal levels [6, 7]. Nevertheless, the IMD sweet-spot mechanism is still the same: an inversion of the IMD phase between small-signal and medium- or large-signal excursions is accompanied by a corresponding IMD amplitude null.

III. OPTIMUM LOAD STUDY

The first step in studying the impact of load impedance in the IMD sweet spot considers a simplified situation in which the active device is assumed to be memoryless and without parasitics, as shown in Figure 3.

In this case, the optimum load for maximized linearity will be the one that allows a signal swing from the cutoff up to the triode zone. As was advanced in [5], it is exactly the entrance in the triode zone that is responsible for power compression and, consequently, for the sought phase opposition with respect to the small-signal IMD response.

A change on R_{Li} in Figure 3 will determine if the signal swing enters sooner or later in the triode zone, thus generating an IMD sweet spot for smaller or larger values of input power. That can be observed in Figures 4(a) and (b), where different values of the load resistance have been tested.

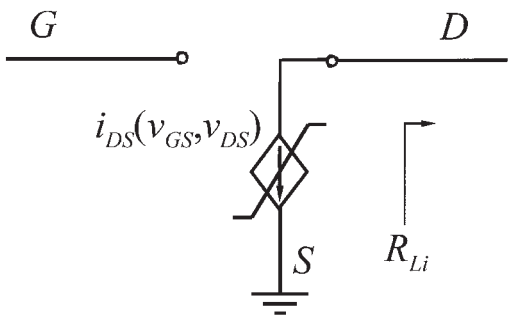

Figure 3. MESFET ideal model.

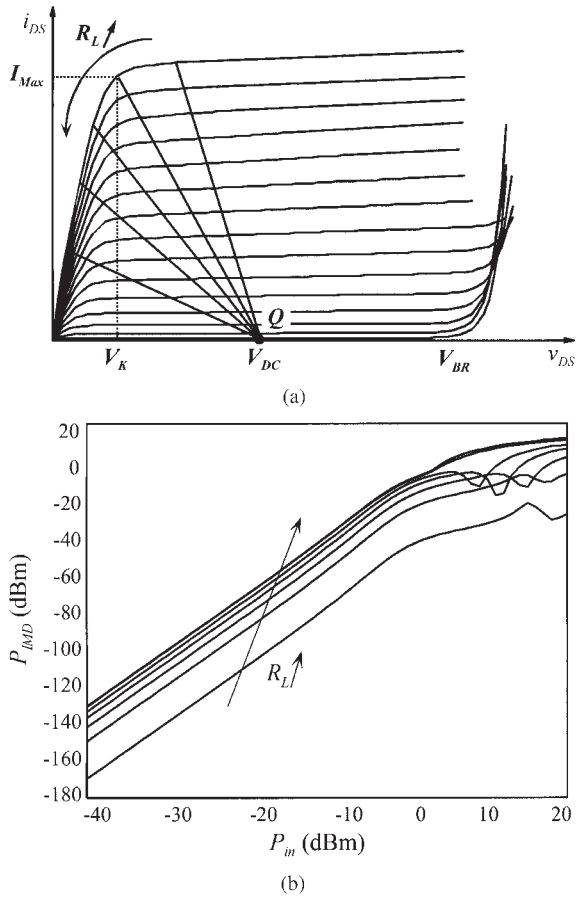

Figure 4. Impact of load resistance R_{Li} upon the large-signal IMD sweet spots in a memoryless PA.

No matter where the observed shift in input power for which the IMD sweet spot is seen, there is always an IMD minimum for each intrinsic resistive load. That input-power shift is merely a reflex of the voltage swing necessary to reach output-signal clipping and voltage gain.

Unfortunately, real devices are not purely resistive, but include reactive parasitics, as illustrated in Figure 5 for the device output. In that case, the optimum load

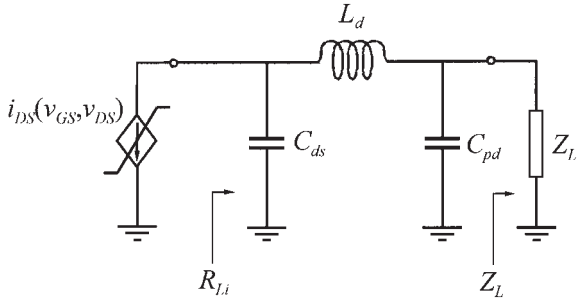

Figure 5. MESFET output equivalent circuit including parasitics.

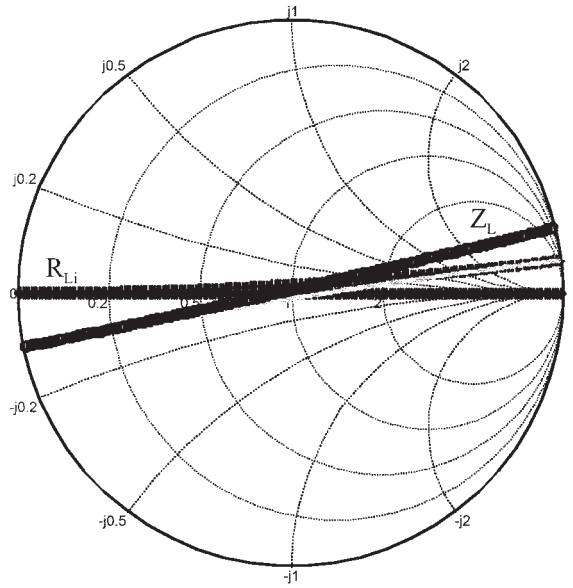

Figure 6. Rotation of the resistive axis $C_{ds} = C_{pd} = .1$ pF and $L_d = 40$ nH in Fig. 5.

impedance can no longer be purely resistive. It should be selected as the one that, after the parasitics are de-embedded, is converted into the desired resistive load at the intrinsic device.

Theoretically, this procedure closely follows the de-embedding process associated with the Cripps' load-line theory [8]. When applied to the parasitics network depicted in Figure 5, it would lead to an optimum extrinsic-load impedance, Z_L, of:

$$Z_L = \{[(R_{L_i}{}^{-1} - j\omega C_{ds})^{-1} - j\omega L_d]^{-1} - j\omega C_{pd}\}^{-1}. \quad (1)$$

In an attempt to determine the load-pull pattern that arises from such a de-embedding process, eq. (1) should be applied to all possible resistive values. This corresponds to an approximate rotation of the Smith Chart real axis, as shown in Figure 6.

When a true parasitics network (similar to the one presented in Fig. 7) is considered, we have to deal

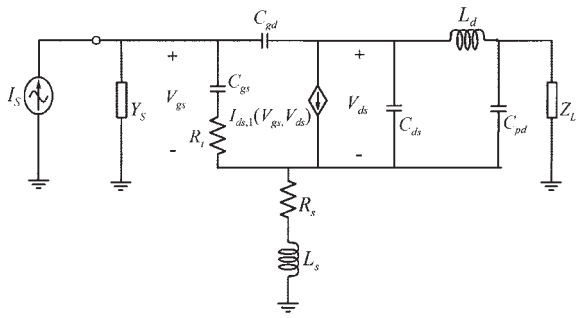

Figure 7. FET active-device equivalent circuit.

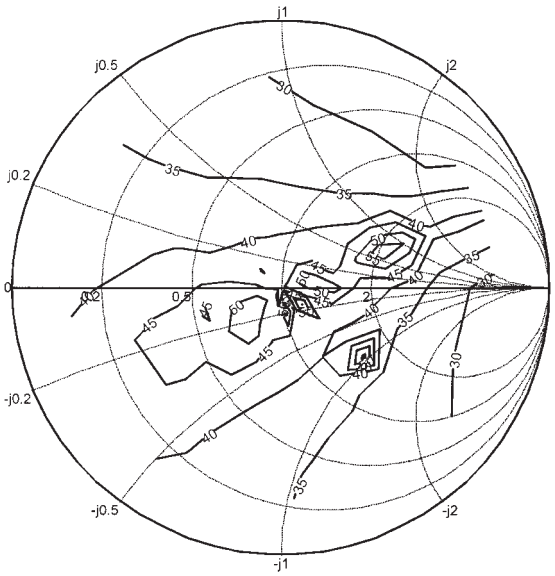

Figure 8. IMR values at the IMD sweet spot after load-pull simulation.

with feedback elements, beyond the ones already considered, as connected in series and parallel. It this case, the de-embedding process can no longer be expressed in closed form, and a load-pull simulation will better fit our needs.

The simulation setup consists of a transistor biased for presenting large-signal IMD sweet spots and terminated by a variable load. A two-tone excitation is applied to the input of the power amplifier, while a tuning device must be placed at the output. The tuning device can be simulated as a one-port *S*-parameter vector, whose reflection coefficient's magnitude and phase values are varied.

Examples of simulated load-pull curves for the ratios between the output signal and IMD power levels, IMR, are presented in Figure 8. Maximum IMR values identify the presence of the IMD sweet spot, and corroborate the above hypothesis that they should stand in a rotated version of the real axis.

Load-impedance values, other than the ones obtained by the parasitic de-embedding rotation, result in lower intermodulation-distortion-ratio values. Indeed, as they impose nonresistive impedance values to the intrinsic active device, the output-generated IMD will have a phase determined by the load impedance that will differ from the idealized 180°. Hence, nonperfect IMD cancellation is obtained and the referred suboptimum IMR is observed.

Obviously, such a load-pull simulation for IMD performance should always be accompanied by a similar load-pull test for output power, as illustrated in Figure 9.

As can be concluded from Figures 8 and 9, the load-impedance value for maximized output power is closely located to the one already obtained for improved IMR. This is not an accident, but a direct consequence of the fact that the extrinsic load reactance necessary to take full advantage of the IMD large-signal IMD sweet spot coincides with the one resulting from the traditional Cripps method of optimized output-signal excursion [8].

This conclusion has the important practical significance of revealing that it is always possible to have an optimized IMD sweet spot for a maximized output power.

IV. MEASUREMENT RESULTS OVER A PHEMT AMPLIFIER

In order to validate the above study, a PHEMT-based amplifier was tested under various conditions of load impedance. A voltage-controlled impedance-transforming network was designed to be connected at the device drain side. This circuit, in addition to providing a simple way to test the impedance impact, can be also useful for implementing a sort of envelope-tracking load-control technique [4].

A schematic of the circuit is presented in Figure 10. It consists of two low-pass L-C-L networks in a tee configuration, connected in cascade. One of them employs a varactor for transforming the 50Ω termination into approximately any lower resistive value,

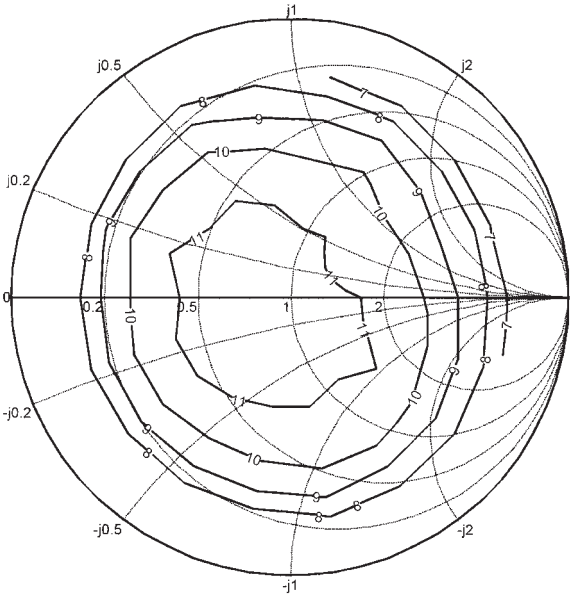

Figure 9. Load-pull results for maximized output power at the 1-dB compression point.

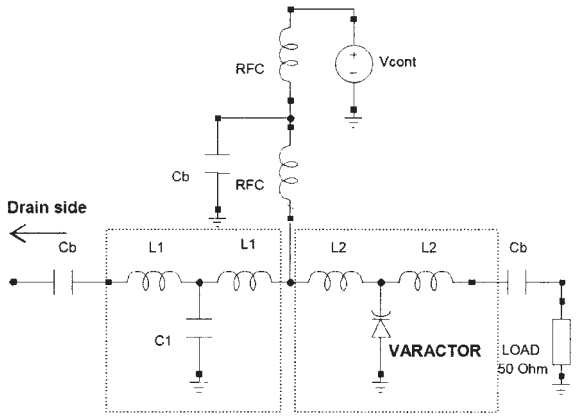

Figure 10. Schematic of the voltage-controlled impedance transformer.

thus nearly covering the left resistive semi-axis in the Smith chart. The other acts as a lumped-element equivalent circuit of a transmission-line section able to rotate the control path around the center of the Smith chart. With this simple topology, the desired impedance range can be conveniently covered. Care was taken in the selection of the varactor diodes to prevent undesired IMD generation in the impedance transformer at the handled power levels.

The results of the obtained load impedance control are shown in Figure 11. As can be seen, a load variation between 210Ω and 75Ω is assured with minimum reactive components. This range was found to be sufficient to "move" the sweet-spot, considering the characteristics of the tested NE3210s01 device.

After the impedance transformer was characterized, it was connected to the device output. Then a classical

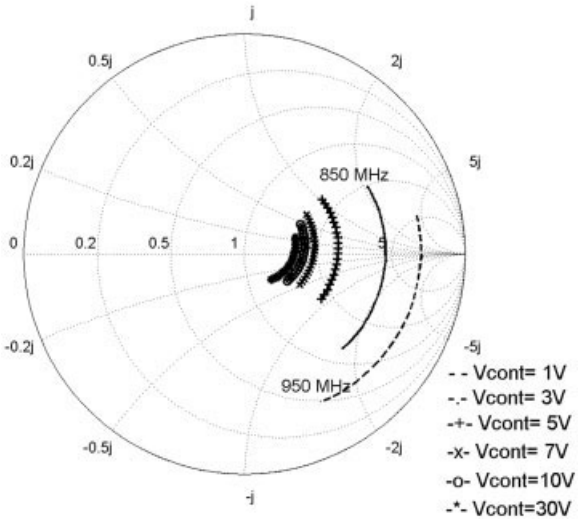

Figure 11. Load control in terms of the applied varactor voltage.

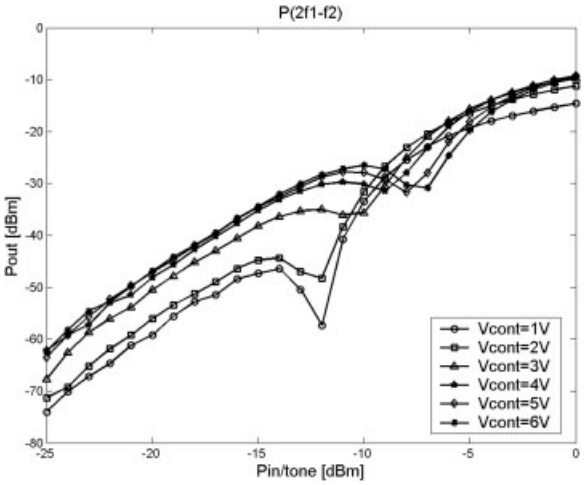

Figure 12. Measured two-tone sweet-spot evolution with the load impedance-control voltage.

linearity test was made, using two tones in the 900-MHz band. Special attention was paid to the bias tee design, in order to avoid undesired low-frequency memory effects [9]. The device was biased in a class C point, with $V_{GS} = -0.5$ V and $V_{DS} = 3$ V.

On the other hand, the impedance values at the higher harmonic bands were left completely unconstrained (some comments about this particular issue are made at the end of this section).

In Figure 12, the results of the 3rd-order in-band IMD power level are plotted for different varactor-control voltages.

When increasing the control voltage, the load resistance was reduced (see Fig. 11) and the sweet spot appears at a higher input-power level, thus confirming the above theoretical analysis. The load reactance could not be kept minimum all along the range, and a reduction in the sweet-spot valley was observed in some of the points. Above $V_{cont} \approx 5$ V, the change in varactor-capacitance with control voltage is not significant, resulting in a small load variation and, consequently, an inappreciable IMD sweet-spot displacement.

To prove the usefulness of these conclusions for the design of PAs required for handling real telecommunication signals, a linearity experiment was also made using a digitally modulated excitation. A QPSK signal, with the characteristics employed in the IS95 standard, was used. The results for the adjacent channel-power level, measured over a 30-kHz bandwidth, are plotted in Figure 13.

The stochastic nature of these excitations determines that the triode region will be reached with more or less probability, depending on the average power level. So, the previous concept of a certain determin-

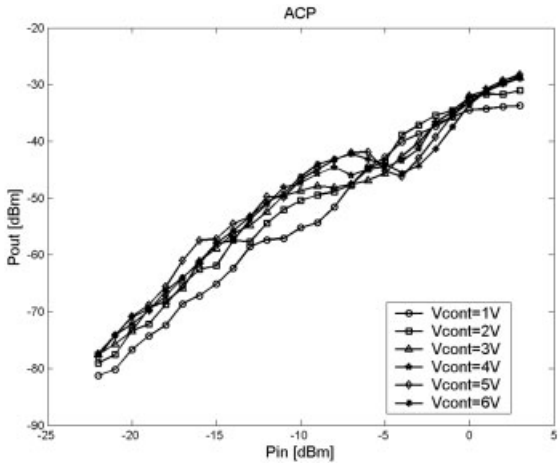

Figure 13. Measured sweet-spot evolution for excitation with a digitally modulated signal.

istic amplitude excitation whose output-voltage swing establishes the large signal IMD sweet spot is lost, and the dip in the IMD profile is turned into a smooth valley. Nevertheless, it should be noted that the impact of the load impedance upon the sweet spot is still the same [10].

Finally, a word on the optimum selection of the out-of-band loads should be given.

As was previously shown by many authors using both simulation and laboratory measurements, the most important out-of-band impedances that control in-band IMD are the ones seen by the even-order products at the base-band and the 2nd harmonics. In fact, considering again a two-tone input, it is clear that the $i_{DS}(v_{GS})$ even-order nonlinearities — particularly significant if the device is biased near pinch-off — will generate output-current components at $\Delta\omega = \omega_2 - \omega_1$ (the base-band) and $\omega_{h2} = 2\omega_2$, $\omega_{h1} = 2\omega_1$ (the 2nd harmonics). These will then be converted into output voltage, when they circulate through the corresponding output out-of-band load impedances. Remixed with the fundamental $v_{DS}(t)$ voltages in the output $i_{DS}(v_{DS})$, and with the fundamental $v_{GS}(t)$ in the cross-terms of $i_{DS}(v_{GS}, v_{DS})$, even order nonlinearities, these voltages will generate new odd-order IMD components at $\omega_{IMD1} = 2\omega_2 - \omega_1 = \omega_2 + \Delta\omega = \omega_{h2} - \omega_1$ and $\omega_{IMD2} = 2\omega_1 - \omega_2 = \omega_1 - \Delta\omega = \omega_{h1} - \omega_2$. As these new IMD components have a magnitude and phase directly dependent on $Z_L(\omega_h)$ and $Z_L(\Delta\omega)$, it should be of no surprise that the resulting addition with the direct odd-order-generated IMD products varies with those terminations.

The mechanism imposing these IMD changes is the same as that which determines the PA IMD asymmetry [9].

Unfortunately, the intricate amplitude and phase relations shown between these indirect and direct IMD products impede any general conclusion about the best out-of-band impedances. And, although it is recognized that a careful load design, especially of $Z_L(\Delta\omega)$, can be used as a linearization tool [actually, any dynamic-output bias adjustment made by envelope injection can be understood as a form of active $Z_L(\Delta\omega)$ controlled load-pull], the usual conservative attitude is either to set both $Z_L(\Delta\omega)$ and $Z_L(\omega_h)$ to zero, in order to prevent such possibly uncontrolled interactions, or to set only $Z_L(\Delta\omega)$ to zero and use $Z_L(\omega_h)$ as a means to manipulate current and voltage output waveforms for efficiency optimization.

The work referred to in [5] is one such example, where it was concluded that an optimum short circuit at the 2nd harmonic and at the base-band was the best choice for IMD sweet-spot maximization, while the load at the 3rd-harmonic band was not found to be important. This is also due to the fact that a nonzero impedance at the 2nd-order harmonics can have a strong impact on the small-signal 3rd-order IMD phase, mainly when the device is biased below cutoff.

V. CONCLUSION

In this article, the impact of the load-matching circuit on the large-signal IMD sweet spot has been addressed. The theoretical studies and measurement results have shown that, provided the device is properly biased, every intrinsic resistive load generates an IMD minimum. Only the input-power value for which it will be visible will change. The base-band and 2nd-harmonic impedances should also be kept under control, if a maximization of the carrier-to-intermodulation-distortion ratio is sought.

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BIOGRAPHIES

Nuno Borges Carvalho was born in Luanda, Portugal, in 1972. He received his diploma and doctoral degrees in Electronics and Telecommunications Engineering from the University of Aveiro, Aveiro, Portugal in 1995 and 2000, respectively, where he was an Assistant Lecturer (1997 to 2000) and a Professor (2000). Currently, he is an Associate Professor at the same university and a Senior Research Scientist at the Telecommunications Institute. He has worked as a Scientist Researcher at the Telecommunications Institute, engaged in different projects on nonlinear CAD and circuits. His main research interests include CAD for nonlinear circuits and design of RF-microwave power amplifiers. He is a member of the Portuguese Engineering Association and an IEEE member. He was the recipient of the 1995 University of Aveiro and Portuguese Engineering Association Prize for the best 1995 student at the Universidade de Aveiro, the 1998 Student Paper Competition (third place) presented at the IEEE International Microwave Symposium, and the 2000 IEE Measurement Prize. He has been a reviewer for several magazines and is a member of the *IEEE Transactions on Microwave Theory and Techniques* Reviewer Board. He is co-author of the book "Intermodulation in Microwave and Wireless Circuits" (Artech House, 2003).

José Angel García was born in Havana, Cuba, in 1966. He received his Telecommunication Engineering degree (with honors) from the Instituto Superior Politécnico "José A. Echeverría" (ISPJAE), Cuba, in 1988, and the Ph.D. degree from the University of Cantabria, Spain, in 2000. From 1988 to 1991, he was a Radio System Engineer at the High-Frequency Communication Center, where he designed antennas and RF circuits. In 1991, he was appointed as an Instructor Professor in the Telecommunication Engineering Department, ISPJAE. From 1999 to 2000, he was a Radio Design Engineer in Thaumat Global Technology Systems. He also worked as Microwave Design Engineer and Project Manager at TTI Norte from 2000 to 2001, in charge of the research line on software-defined radios while also involved in LNA and active antenna design. Since January 2002, he has been working as a Senior Research Engineer at the University of Cantabria. His main research interests include nonlinear characterization and modeling of active devices, intermodulation distortion control on RF and microwave applications, reconfigurable terminals, and active antennas. He received one of the prizes from the Spanish Official Board of Telecommunication Engineers fir the Best 2000 Doctoral Thesis Work, and was co-recipient of the GaAs Prize for best paper in the 2001 European Microwave Week. He has also served as a reviewer for several magazines.

Edurne Azpitarte was born in Azkoitia, Spain. She received her Technical Telecommunication Engineer degree from the University of Cantabria in 2004, and is currently working towards her full Telecommunication Engineer degree. Her research interests include nonlinear characterization and modeling of active devices, with emphasis on intermodulation distortion control.

José C. Pedro was born in Espinho, Portugal on March 7, 1962. He received his diploma, doctoral, and habilitation degrees in electronics and telecommunications engineering, from the University of Aveiro, Portugal, in 1985, 1993 and 2002, respectively. From 1985 to 1993 he was an Assistant Lecturer at University of Aveiro, where he became a Professor in 1993. Currently, he is a Professor at the same University and a Senior Research Scientist at the Institute of Telecommunications. His main scientific interests include active device modeling and the analysis and design of various nonlinear microwave and optoelectronics circuits, in particular, the design of highly linear multicarrier power amplifiers and mixers. He is the leading author of "Intermodulation Distortion in Microwave and Wireless Circuits" (Artech House, 2003), has authored or co-authored several papers in international journals and symposia, and has served the IEEE as a reviewer for the *MTT Transactions* and the *MTT-IMS*. He received the Marconi Young Scientist Award in 1993 and the 2000 Institution of Electrical Engineers (IEE) Measurement Prize.