Nonlinear Device Model of Microwave Power GaN HEMTs for High Power-Amplifier Design

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***Abstract*—This paper presents a nonlinear equivalent circuit model of microwave power GaN high electron-mobility transistors (HEMTs), amenable for integration into commercial harmonic balance or transient simulators. All the steps taken to extract its parameter set are explained, from the extrinsic linear elements up to the intrinsic nonlinear ones. The predictive model capabilities are illustrated with measured and simulated output power and intermodulation-distortion data of a GaN HEMT. The model is then fully validated in a real application environment by comparing experimental and simulated results of output power, power-added efficiency, and nonlinear distortion obtained from a power amplifier.**

***Index Terms*—Intermodulation distortion (IMD), modeling, power amplifiers (PAs), power transistors.**

I. Introduction

THE deployment of modern digital telecommunication systems, with continuously increasing capacity, has demanded a steady improvement of the RF front-end's performance in terms of bandwidth, power-added efficiency (PAE), and signal fidelity. This is especially true in microwave power amplifiers (PAs), for which many advances on design and active device technology have been made public.

In this respect, despite recognized device processing infancy, one of the most promising technologies is the one based on wide-bandgap materials, such as GaN high electron-mobility transistors (HEMTs). Already offering power transistors of unbeaten breakdown voltages, they are, therefore, capable of delivering very high output power (Pout) figures [1].

Also significant is the high linearity provided by these devices. In fact, the observed valleys of intermodulation distortion (IMD) versus input drive level patterns, frequently observed in class-AB PA operation, constitute a great help in achieving a good compromise between Pout, IMD, and PAE, [2], [3]. Unfortunately, the critical dependence of these IMD valleys, the so-called large-signal IMD sweet spots, on almost unsuspected issues like: 1) out-of-band terminations [4]; 2) strong and mild device nonlinearities [2], [3]; and 3) quiescent point (not unusually in ranges of only a few tenths of Volt) have raised the quality standards of common PA design methodologies and nonlinear device models.

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As concerns the nonlinear device model, it is known, from Volterra-series analysis, that if one wants to describe adjacent channel distortion, or close sideband IMD, over moderate signal levels, one will need to have a model capable of accurately reproducing the *I/V* and *Q/V* characteristics, at least up to the third order, while an alternate channel distortion level would need, at least, fifth-order detail. In mathematical terms, this implies that third- or fifth-order derivatives of *I/V* and *Q/V* functions must be carefully extracted and approximated.

Unfortunately, even such a local model is not capable of reproducing the full range of large-signal device characteristics. For that, an accurate description of the device's strong nonlinearities like saturation to triode-zone transition, current cutoff, gate–channel diode conduction, and gate–channel breakdown are also required. This leads to the necessity of a nonlinear global model.

Although various nonlinear global models obeying these requirements have been proposed for many different microwave device types [3], GaN power HEMT modeling activities are still making their first steps so that, to the best of the authors' knowledge, no nonlinear model conceived to reproduce distortion properties has ever been published. Indeed, Green *et al.* [5] and Lee *et al.* [6] introduced a Curtice cubic nonlinear model, which has very poor IMD prediction capabilities [7], [8]. More recently, Raay *et al.* [9] used the Angelov–Zirath model, but no IMD data have also been presented.

This paper addresses the extraction of such a model for a microwave GaN power HEMT device, paying particular attention to the prediction of small- and large-signal Pout and IMD. For that, measured and simulated results are compared when the device is operated in a 50-Ω termination environment and in a real class AB PA.

This paper is divided into five different sections. Section I introduces the study. Section II briefly presents the most important characteristics of the device used. Section III describes the proposed model and its extraction. Section IV discusses the model predictive capabilities. Finally, Section V presents conclusions and summarizes the most important achievements.

II. GaN HEMTs Characterization

The device used was a GaN HEMT on an Si substrate with 2-mm gate periphery, encapsulated in a standard high-power microwave package.

Fig. 1(a) shows measured $I_{\rm DS}$ versus $V_{\rm DS}$ characteristics, under static conditions, for six different $V_{\rm GS}$ biases and Fig. 1(b) depicts its transfer characteristic and transconductance for a fixed $V_{\rm DS}$ of 6 V.

As seen, this is a depletion-mode transistor with a $V_{\rm pinch\ off}$ of -4.3 V, an $I_{\rm dss}$ of 1 A and a $G_{m\,\rm MAX}$ of 330 mS.

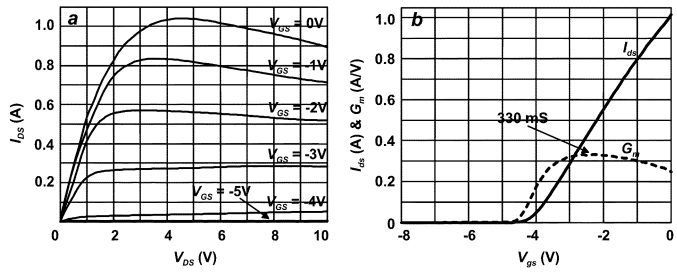

Fig. 1. (a) Typical $I_{\rm DS}$ versus $V_{\rm DS}$ curves measured under static conditions for six different $V_{\rm GS}$ biases. (b) $i_{\rm DS}(v_{\rm GS})$ transfer characteristic (—) and $G_m(v_{\rm GS})$ (- -) for a fixed $V_{\rm DS}$ of 6 V.

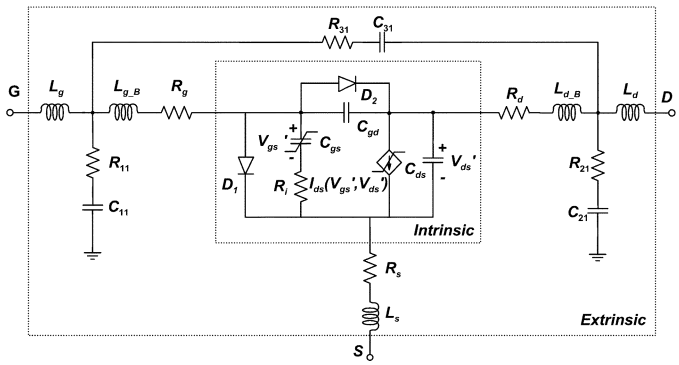

Fig. 2. Equivalent-circuit model topology used.

Although intrinsic $G_m, C_{\rm gs}$, and $C_{\rm gd}$ values would lead to an f_T of nearly 14 GHz, parasitic capacitances associated to the nonideal substrate and the package reduce this value to a more conservative figure of approximately 8 GHz.

III. Nonlinear Equivalent-Circuit Device Model

This section presents an empirical large-signal model amenable for integration into any standard harmonic balance or transient simulator. The model is based on the equivalent circuit topology shown in Fig. 2, which includes both linear extrinsic and linear or nonlinear intrinsic elements.

In the former group, R_g, R_s, and R_d represent contact and semiconductor bulk resistances; while $L_{g\_B}, L_s, L_{d\_B}, L_g$, and L_d model combined effects of bond wires and lumped inductance representations of the package.

Besides these usual extrinsic field-effect transistor (FET) elements, this equivalent circuit includes three R–C series networks, which are: 1) one at the gate (R_{11} and C_{11}); 2) one at the drain (R_{21} and C_{21}); and 3) another connecting both ports (R_{31} and C_{31}). These fairly low Q networks were first introduced by Chumbes *et al.* [10] and then by Manohar *et al.* [11]. They are meant to reproduce the impact of the lossy p-Si/GaN/metal structure on the S-parameters, especially a pronounced resistive component observed under channel current cutoff (cold FET operation).

As concerns the intrinsic elements, both $C_{\rm ds}$ and R_i were taken as bias-invariant elements. Furthermore, since such devices are primarily intended for highly efficient and low-distortion PA applications, and are thus usually kept in the saturation region, $C_{\rm gd}$ was also assumed to be approximately linear and $C_{\rm gs}$ only dependent on $v_{\rm GS}$. The remaining intrinsic elements $i_{\rm DS}$ and the gate–source and gate–drain diodes were considered as nonlinearly dependent on $v_{\rm GS}$ and $v_{\rm DS}$, and on $v_{\rm GS}$ and $v_{\rm GD}$, respectively.

TABLE I
Extrinsic Elements' Values

Element	Value	Units
R_g	1.67	Ω
R_d	0.9	Ω
R_s	0.1	Ω
L_g	0.9	nH
L_d	1.7	nH
L_s	0.1	nH
L_{g_B}	0.7	nH
L_{d_B}	1.0	nH
R_{11}	20	Ω
C_{11}	2.3	pF
R_{21}	70	Ω
C_{21}	1.2	pF
R_{31}	5	Ω
C_{31}	0.1	pF

TABLE II
Invariant Intrinsic Elements' Values

Element	Value	Units
R_i	5	Ω
C_{gd}	0.3	pF
C_{ds}	3.0	pF

A. Extrinsic Elements' Extraction

The determination of all series resistances and inductances was performed using S-parameter measurements, taken under forward gate bias conditions, as described by Dambrine *et al.* [12]. This was possible since, as reported in [11], the transversal R–C networks have minimum effect on the Z-parameters measured under this 0-V $V_{\rm DS}$ operating mode.

The remaining extrinsic elements' values were extracted from an optimization of the cold FET ($V_{\rm DS} = 0$ V, $V_{\rm GS} = -8$ V) S-parameter data using a linear microwave computer-aided design (CAD) tool.

All S-parameter measurements were taken from 30 kHz up to 3 GHz.

The extrinsic elements' values finally obtained are shown in Table I.

B. Intrinsic Elements' Extraction

Invariant intrinsic elements were extracted using the standard method of [12]. As previously stated, $C_{\rm ds}, R_i$ and $C_{\rm gd}$ were taken as approximately linear and, thus, independent of bias. Their values are shown in Table II.

Considering the intended microwave PA application, a quasi-static global model is needed for each of the nonlinear elements: drain–source current and gate–channel junction. $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ will be represented by a standard voltage-dependent current source, while the gate–channel junction was split into two independent voltage-controlled current sources and corresponding voltage-controlled charge sources.

The latter are represented in the equivalent circuit of Fig. 2 by the diode symbols, a nonlinear (depletion capacitance) $C_{\rm gs}(v_{\rm GS})$, and linear (constant depletion capacitance) $C_{\rm gd}$.

1) Channel–Current Nonlinear Model: Since we are using HEMT devices, a first modeling attempt was based on the standard Chalmers, or Angelov–Zirath, model [13]. Unfortunately, the hyperbolic tangent adopted for representing $i_{\rm DS}(v_{\rm GS})$ led to a bell-shaped transconductance showing a pronounced even symmetry over the threshold voltage. This was found impossible to fit to the $G_m(v_{\rm GS})$ extracted and depicted in Fig. 1(b) [14].

On the other hand, the G_m asymmetric behavior—i.e., a sudden rise near turn-on followed by a smooth decrease toward 0 V—directed our attention to the in-house FET model previously proposed by Fager *et al.* for S_i LDMOS [15]. Intended for detailed nonlinear distortion description, it relies on behavioral device data of both dc and small-signal $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$: first derivative in order to $v_{\rm DS}, G_{\rm ds}$, and first-, second-, and third-order derivatives in order to $v_{\rm GS}, G_m, G_{m2}$, and G_{m3}, respectively [15].

This model states that the threshold voltage V_T, (unclear in $i_{\rm DS}(v_{\rm GS})$ due to the FET's soft turn-on) can be precisely extracted from the $G_{m2}(v_{\rm GS})$ peak or $G_{m3}(v_{\rm GS})$ null [3]. Its dependence on $V_{\rm DS}$ can be acquired from several third-order harmonic or intermodulation tests so that, for each $V_{\rm DS}$, the $V_{\rm GS}$ value in which a third-order intermodulation distortion (IM3) null occurs gives the value of V_T. The parameter γ can then be extracted to fit these measured $V_T(v_{\rm DS})$ as follows:

$$V_T\left(v_{\rm DS}\right) = V_{T0} + \gamma \cdot v_{\rm DS}. \tag{1}$$

A curious aside of this extraction was that our device showed an almost constant V_T over a wide $V_{\rm DS}$ range that spanned the linear and saturation regions ($\Delta V_T = 0.1$ V when $V_{\rm DS}$ was swept from 0 V up to over 20 V).

The complete $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ model is given by

$$i_{\rm DS}(v_{\rm GS}, v_{\rm DS}) = \frac{\beta \cdot v_{\rm GS3}^2}{1 + \dfrac{v_{\rm GS3}^{\rm plin}}{V_L}} \cdot (1 + \lambda \cdot v_{\rm DS}) \tanh\left(\frac{\alpha \cdot v_{\rm DS}}{v_{\rm GS3}^{\rm psat}}\right) \tag{2}$$

where $v_{\rm GS3}$, an intermediate $v_{\rm GS}$ function, is given by

$$v_{\rm GS3}\left(v_{\rm GS2}\right) = {\rm VST} \cdot \ln\left(1 + e^{{\rm v_{GS2}}/{\rm VST}}\right) \tag{3}$$

while $v_{\rm GS2}$ is

$$v_{\rm GS2}\left(v_{\rm GS1}\right) = v_{\rm GS1} - \frac{1}{2}\left(v_{\rm GS1} + \sqrt{\left(v_{\rm GS1} - VK\right)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{4}$$

and $v_{\rm GS1}$ is the FET's intrinsic $v_{\rm GS}$ scaled by V_T as follows:

$$v_{\rm GS1}\left(v_{\rm GS}\right) = v_{\rm GS} - V_T. \tag{5}$$

Note that, for accurately describing the FET's sub-threshold conduction and soft turn-on, the expression used for $i_{\rm DS}(v_{\rm GS})$ is a smoothed version of the usually assumed piecewise characteristic. Hence, the smoothness provided by (3) presents the desired continuity of the $i_{\rm DS}(v_{\rm GS})$ function and its derivatives.

The auxiliary $v_{\rm GS}$ function of (4) and the rational function adopted for the dependence of $i_{\rm DS}$ on $v_{\rm GS3}$ determines a smooth

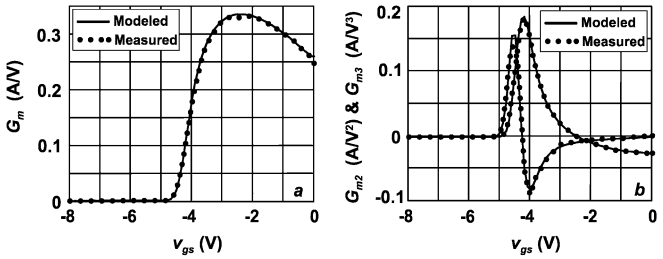

Fig. 3. (a) G_m and (b) G_{m2} and G_{m3} measured ($\cdot$) and modeled (–) with the in-house model for a constant $V_{\rm DS}$ of 6 V.

TABLE III
IN-HOUSE $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ MODEL PARAMETER VALUES

Parameter	Value	Units
β	0.40	A/V^2
V_{T0}	-4.425	V
VST	0.15	V
VK	4	V
Δ	5	V
V_L	1.35	V
λ	0.0256	V^{-1}
α	0.40	V^{-1}
psat	-0.62	-
plin	1	-
γ	0	-

$i_{\rm DS}(v_{\rm GS})$ current level off and, thus, the desired controlled transconductance collapse for high $v_{\rm GS}$ bias.

Basically, the various fitting parameters of those expressions are used to set the position (in $v_{\rm GS}$) of these transitions in behavior and their relative abruptness. As their contributions can be traced to each of these effects, this allows an almost one-by-one first parameter set extraction. Unfortunately, since there is no absolute orthogonality, the final parameter set must be obtained from a fine optimization of the modeled and measured G_m, G_{m2}, and G_{m3}.

As concerns the $i_{\rm DS}(v_{\rm DS})$ dependence, the model relies on the traditional Curtice hyperbolic tangent function to set the linear to saturation regions' transition beyond a linear factor to account for the nonnull $G_{\rm ds}$ in saturation. However, the argument of the $\tanh\left(v_{\rm DS}\right)$ was modified to reproduce the displacement of the knee voltage with $v_{\rm GS}$.

Fig. 3(a) and (b) shows the resulting prediction of the small-signal $G_m(v_{\rm GS})$ and its derivatives $G_{m2}(v_{\rm GS})$ and $G_{m3}(v_{\rm GS})$.

Note the remarkable good agreement, up to third order, obtained with this $i_{\rm DS}(\cdot)$ model.

Table III presents the obtained $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ model parameter set.

2) Gate–Source Capacitance Nonlinear Model: For the nonlinear gate–source capacitance $C_{\rm gs}(v_{\rm GS})$, we used the model proposed in [15] as follows:

$$C_{\rm gs}(v_{\rm GS}) = C_{\rm gs0} + \frac{A_{C_{\rm gs}}}{2}\left(1 + \tanh\left[K_{C_{\rm gs}} \cdot \left(v_{\rm GS} - V_{C_{\rm gs}}\right)\right]\right). \tag{6}$$

As expressed in (6), a constant $(C_{\rm gs0})$ plus a hyperbolic tangent are used to describe $C_{\rm gs}$ behavior with $v_{\rm GS}$, which determines a ramp plus a $\ln[1 + \exp(v_{\rm GS})]$ charge. As in the $i_{\rm DS}(\cdot)$ model, the parameters of (6) are used to control the position

TABLE IV
IN-HOUSE $C_{\rm GS}(v_{\rm GS})$ MODEL PARAMETERS

Parameter	Value	Units
C_{gs0}	1.5	pF
A_{Cgs}	2.0	pF
K_{Cgs}	2.0	V^{-1}
V_{Cgs}	-4.5	V

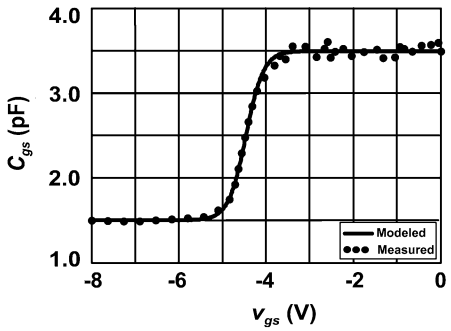

Fig. 4. Comparison between measured ($\cdot$) and predicted (–) $C_{\rm gs}(v_{\rm GS})$ values for a constant $V_{\rm DS}$ of 6 V.

TABLE V
GATE–CHANNEL JUNCTION MODEL PARAMETERS

Parameter	Value	Value
I_S	3.25e-4	A
η	26	-

$(V_{\rm Cgs})$ and the abruptness $(K_{\rm Cgs})$ of the transition between the residual $C_{\rm gs0}$ and the actual depletion capacitance. The complete $C_{\rm gs}(v_{\rm GS})$ parameter set is shown in Table IV.

Fig. 4 shows the comparison between measured and modeled values of $C_{\rm gs}(v_{\rm GS})$.

As seen in Fig. 4, there is again a good agreement between measured and simulated data.

3) Schottky Junction Nonlinear Model: Finally, the gate–source and gate–drain diodes were considered as approximately equal and modeled by the conventional Schottky formula. The inverse saturation current I_S and ideality factor η were extracted from a semilog plot of measured I_G versus $v_{\rm GS}$ data when source and drain were short circuited. That led to the parameters shown in Table V.

A note on these values is obviously required as they seem very far from the ordinary ones observed in similar GaAs- or Si-based metal–semiconductor (MES) junctions. They are a direct consequence of the measured low currents for the comparably large applied voltages. In fact, currents on the order of a few milliamperes could only be observed for applied voltages of nearly 1.5 V, while 100 mA were measured for unexpected values of around 3.5 V. Furthermore, the rather large I_s value was verified against the diode currents measured under reverse bias. Although some process variation was observed for those values, they all seemed to be much larger than the ones of GaAs and Si devices. If such a trend is confirmed in other GaN technologies, this could be an indication that such wide-bandgap HEMTs allow a very high input voltage excursion before gate–channel junction clamping takes place.

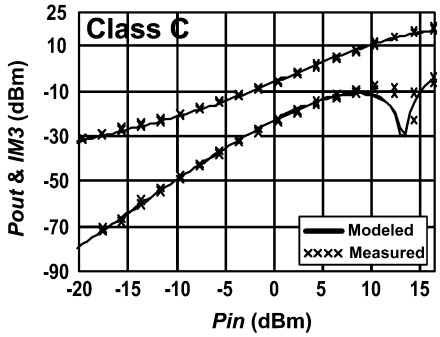

Fig. 5. Measured (×) and simulated (–) Pout and IM3 versus Pin for class-C operation.

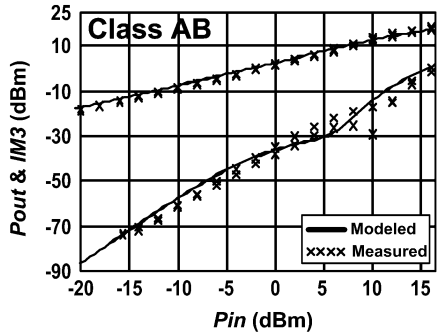

Fig. 6. Measured (×) and simulated (–) Pout and IM3 versus Pin for class-AB operation.

IV. MODEL VERIFICATION

In this stage, the model was implemented in a standard harmonic-balance simulator in order to prove its ability in describing our GaN HEMT device behavior.

A. Pout *and IMD Testing Under 50-Ω Terminations*

As described in [14], first tests were conducted on a device terminated with a broad-band 50-Ω load at both the input and output.

Several output power (Pout) and IM3 versus input power (Pin) measurements were taken for a reasonably fine grid of $V_{\rm GS}$ values (thus, of quiescent $I_{\rm DS}$ bias currents), while $V_{\rm DS}$ was kept constant at 6 V.

These figures, associated with those obtained from simulation, allowed a thorough study of the device model behavior for various PA operation classes: C, AB, and A at 900 MHz.

For class C (Fig. 5)—i.e., biasing the device below V_T [3]—in addition to a very good small-signal IMD description, our model can also predict, with very good accuracy, the observed large-signal IMD sweet spot.

A handy and practical property of these GaN HEMTs can be observed at class AB—i.e., biasing the device slightly above V_T [3] (Fig. 6). The presence of a notorious distortion valley in the IMD versus Pin pattern can be used as an important tool to design highly efficient wireless PAs also of very good linearity since it is known that, in this operation class, the device tends to present its optimized values of Pout and PAE. Previous studies conducted for other FET device types [2], [15] led to the conclusion that those valleys or, sometimes, even double minima, can be explained as the interaction of small- and large-signal IMD. Their prediction is thus determined by the model's ability

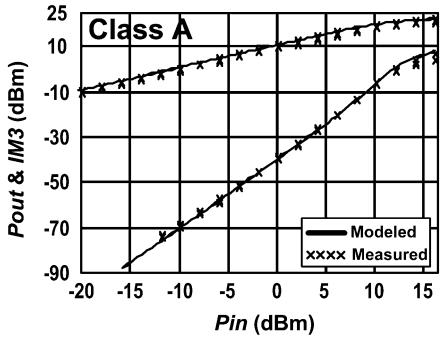

Fig. 7. Measured (×) and simulated (–) Pout and IM3 versus Pin for class-A operation.

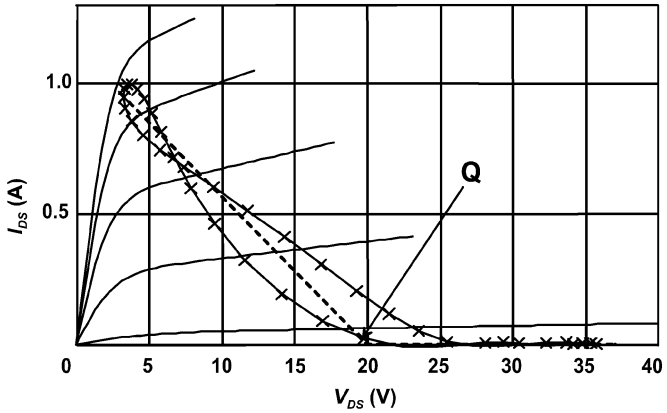

Fig. 8. Simulated $i_{\rm DS}$ versus $v_{\rm DS}$ characteristics for six different $v_{\rm GS}$ values (—) and desired (- -) and obtained (- × -) dynamic drain load line.

in precisely describing the $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ higher order derivatives [3], [7], [8], as discussed in Section III-B.1.

In class A—i.e., biasing the device well above V_T [3] (Fig. 7), no large-signal IMD sweet spot is either predicted by the model or observed in the measurements.

As seen in these figures, measured and simulated results compared remarkably well in all operation classes. Indeed, not only the general Pout and IMD behavior is represented, as also the details of the IMD versus Pin pattern are accurately described.

1) 900-MHz Class-AB PA Design: In order to test the model in a real application environment, the next validation step was the design of a PA simultaneously optimized for Pout, PAE, and signal-to-intermodulation ratio (IMR).

Although the equivalent-circuit model parameters had been extracted for a constant $V_{\rm DS}$ of 6 V, we decided to move it up to 20 V to take full profit of the device's output voltage and current excursion capabilities.

$V_{\rm GS}$ bias (PA operation class) was selected to maximize the IMR. After a few tests around V_T (i.e., close to classes B and AB) it became clear that the best performance could be achieved when the device presented double minima in the IMD versus Pin pattern. This led to a quiescent point of approximately $V_{\rm GS1} = -4.20$ V or 4% of $I_{\rm DSS}$.

Maximization of Pout and PAE demanded a careful selection of the Cripps load line and fine tuning of the even harmonics [16]. A two-stub output matching network was designed to guarantee the calculated intrinsic 34-Ω load line at 900 MHz (central frequency) and a short circuit at 1.8 GHz (second harmonic).

Fig. 8 shows the simulated $i_{\rm DS}$ versus $v_{\rm DS}$ characteristics for six different $v_{\rm GS}$ values and superimposed the desired and obtained dynamic drain load line.

Comparing the $I_{\rm DS}$ versus $V_{\rm DS}$ characteristics presented in Fig. 1(a) and predicted $i_{\rm DS}$ versus $v_{\rm DS}$ data of Fig. 8, it is possible to see that the simulated curves do not collapse. This was expected since, conceived to describe dynamic behavior, and extracted to fit measured RF G_m and $G_{\rm ds}$, our model does not include any self-heating or trapping effects. Although this will obviously affect the model predictions at dc, it will not compromise the primarily sought ac Pout and IMD characteristics.

After designing the output matching network, the next stage was to conceive an input network capable of providing possible source matching and optimized gain without in-band instability. Finally, a broad-band stability analysis was carried on, which showed further problems at VHF. These were solved by the design of convenient lossy networks in the gate and drain bias paths.

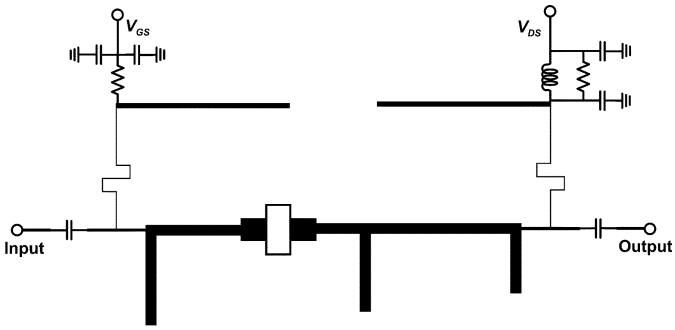

Fig. 9. PA circuit schematic.

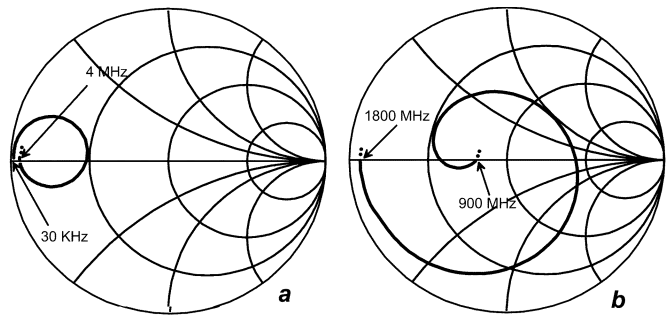

Fig. 10. Output matching response seen at the drain: (a) from 30 kHz to 4 MHz and (b) from 900 to 1800 MHz.

Fig. 9 shows the PA circuit schematic.

However, since it is known that the bias networks also determine the device terminations at the envelope frequencies, they were retuned to guarantee very low impedances at most of the envelope bandwidth (4 MHz). In fact, it could be confirmed during the simulation, and then in the PA testing, that these low-frequency terminations can either jeopardize IMD performance or even introduce undesired sideband asymmetries (a symptom of long-term PA memory effects) [17].

Fig. 10(a) and (b) shows the simulated output matching response at the drain from 30 kHz to 4 MHz and from 900 to 1800 MHz, respectively.

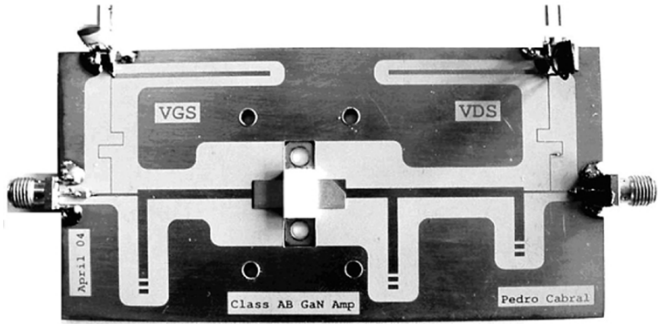

Fig. 11. Photograph of the implemented PA MIC board.

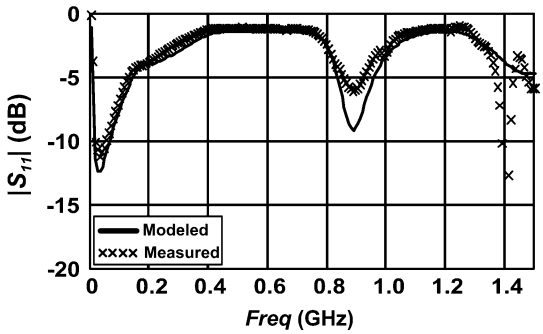

Fig. 12. Measured (×) and modeled (–) PA $|S_{11}|$.

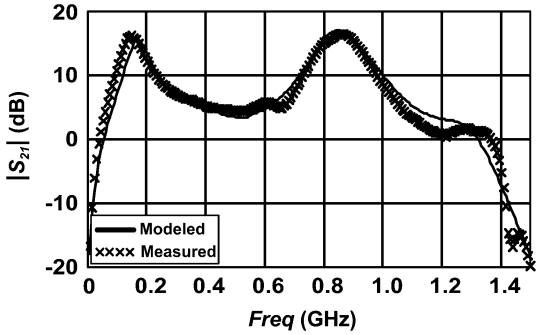

Fig. 13. Measured (×) and modeled (–) PA $|S_{21}|$.

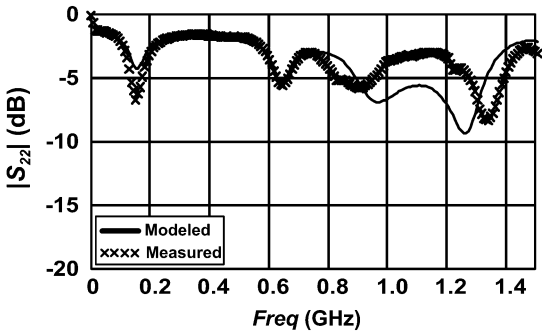

Fig. 14. Measured (×) and modeled (–) PA $|S_{22}|$.

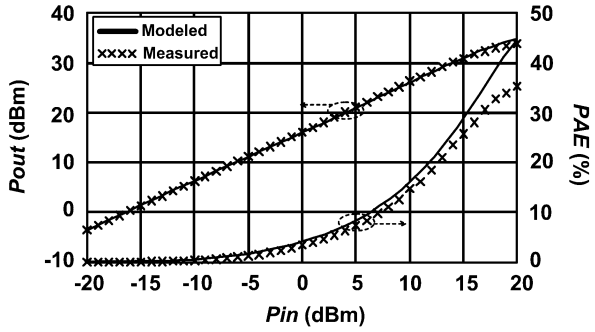

Fig. 15. Measured (×) and modeled (–) Pout and PAE under CW operation.

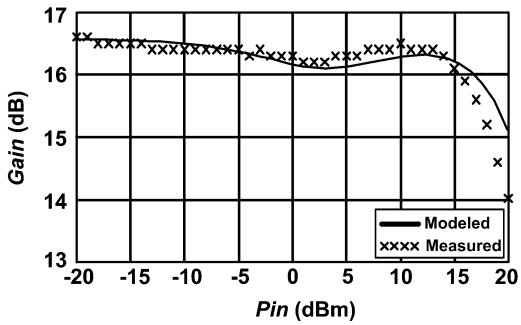

Fig. 16. Measured (×) and modeled (–) Gain versus Pin under CW operation.

The PA was then implemented in microwave integrated-circuit (MIC) technology using an RT/Duroid high-frequency laminate with $\varepsilon_r = 10,2$. Fig. 11 shows a photograph of the implemented amplifier board.

2) Small-Signal S-Parameter Measurements: The first PA test was a set of broad-band small-signal S-parameter measurements. Figs. 12–14 show measured and modeled values of $|S_{11}|$, $|S_{21}|$, and $|S_{22}|$, respectively.

There is a reasonable good agreement between measured and modeled results. This attests the quality of the model's small-signal predictions both in terms of the nonlinear functions' consistency and equivalent-circuit element extraction. The discrepancy in the $|S_{22}|$ of Fig. 14 is estimated to be caused by the difference between $V_{\rm DS}$ values used in model extraction (6 V) and in amplifier design (20 V). Even so, the general shape of the curves is similar.

3) Large-Signal One-Tone Measurements: The second test step consisted of several continuous wave (CW) experiments to evaluate transducer power gain (Gain), Pout, and PAE versus input drive level.

As seen in Fig. 15, the PA presents a 1-dB compression point of 2 W with an associated Gain of 15 dB and a PAE of nearly 32%. Compared to the model predictions, it is clear that the efficiency came somewhat lower than expected, while the Pout and Gain deviations were within the measurement error.

Nevertheless, one remarkable result that should be pointed out is the correct prediction of the Gain versus Pin pattern (Fig. 16) despite its rather complex behavior. First, for small-signal levels, the PA presents gain compression, which is then followed by gain expansion, to end up again in gain compression, for a very large signal. This is a direct consequence of the selected bias point, and is consistent to the double-minima IMD pattern aimed at the PA design phase [3].

4) Large-Signal Two-Tone Nonlinear Distortion Measurements: Afterwards, PA IMD performance was tested. The excitation was a two tone centered at 900 MHz and separated by 100 kHz. As seen from the data depicted in Fig. 17, there is a good agreement between the predicted and observed results.

More important than the capacity of accurately predicting the observations of a particular bias point is the model's capability

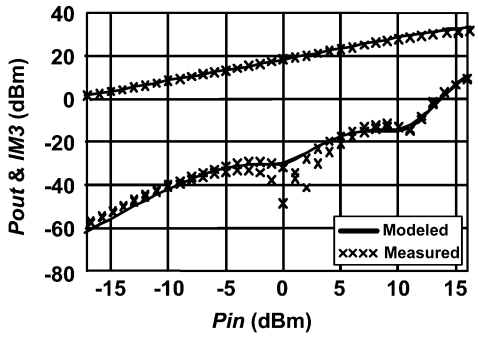

Fig. 17. Measured (×) and simulated (–) PA Pout and IM3 versus Pin for $V_{\rm GS1}$.

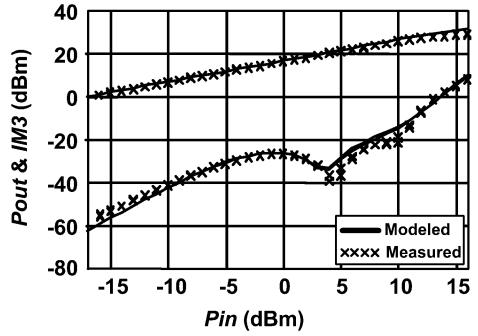

Fig. 18. Measured (×) and simulated (–) PA Pout and IM3 versus Pin for $V_{\rm GS2}$.

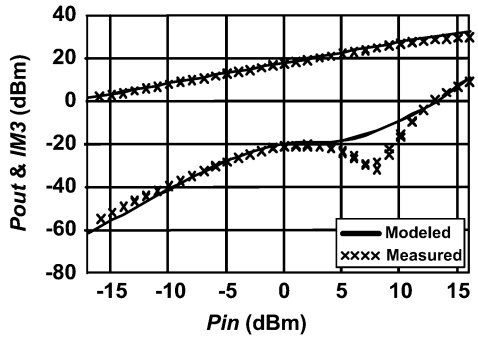

Fig. 19. Measured (×) and simulated (–) PA Pout and IM3 versus Pin for $v_{\rm GS3}$.

to reproduce the dramatic variations of IMD versus Pin pattern when there is a change of bias. Indeed, Figs. 18 and 19 show measurements and simulations taken for two more bias points still under class-AB operation ($V_{\rm GS2} = -4.15$ V and $v_{\rm GS3} = -4.10$ V).

Note the possibility of changing the double minima position to achieve broader or narrower Pin zones of high IMR. That is important for real signal operation since, today, communication systems use disparate modulation schemes and wide-band signals, which present a statistical amplitude distribution that is quite different from the one of a simple CW or two-tone excitation [18].

5) Multitone Nonlinear Distortion Measurements: In order to test the PA under a real multitone excitation, we selected a 3.84-MHz wide-band code-division multiple-access (W-CDMA) signal centered at 900 MHz and generated using Agilent's ESG-D E4433B.

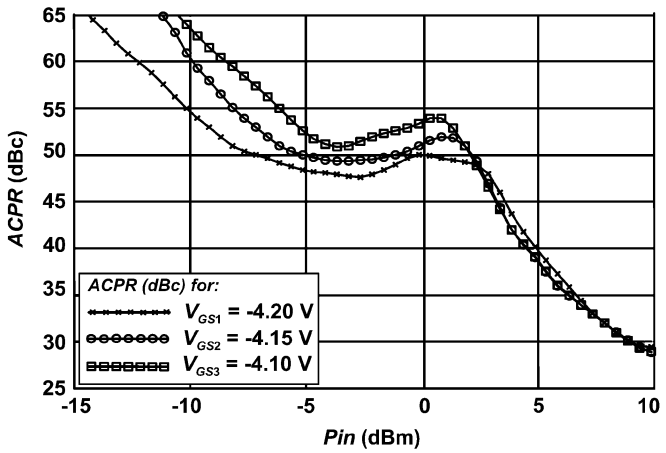

Fig. 20. ACPR measurements with the PA under class AB for three different $V_{\rm GS}$ values ($V_{\rm GS1}V_{\rm GS2}$ and $V_{\rm GS3}$).

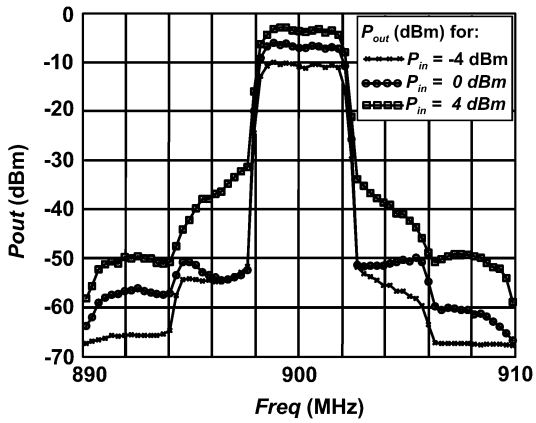

Fig. 21. PA output spectra for a W-CDMA input signal with −4-, 0-, and 4-dBm input drive level.

Adjacent channel power ratio (ACPR) values (3.84 MHz to each side of the center frequency in a 20% channel bandwidth) were measured for each of the three $V_{\rm GS}$ bias points already used in the two-tone tests. Fig. 20 shows measured ACPR versus input drive level. The obvious presence of an ACPR minimum justifies the effort put in accurately modeling the device's IMD sweet spots, and validates the PA design under the available two-tone excitation prototype.

Fig. 21 is a detailed view of the amplifier's output spectra when biased at $V_{\rm GS1}$ for three different input drive levels around the observed IMD sweet spot: −4, 0, and 4 dBm, respectively.

V. Conclusion

An equivalent-circuit nonlinear global model has been formulated and extracted for a 2-mm GaN power HEMT. Modeling studies have proven that the form now adopted for the $i_{\rm DS}(v_{\rm GS}, v_{\rm DS})$ characteristic was found more flexible than the standard HEMT model developed for GaAs devices. That allowed a precise fitting of measured small-signal $G_m(v_{\rm GS})$ and, thus, of its higher order derivatives. As expected, this played a paramount role in the accurate prediction of the device's output power and IMD characteristics.

Indeed, the remarkable good agreement obtained between measured and simulated Pout and two-tone IM3 in a practical

class-AB 2-W PA circuit validated the developed nonlinear GaN HEMT model and clearly showed its value for nonlinear microwave CAD.

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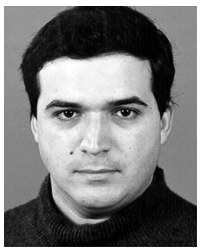

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