Prediction of IMD in LDMOS Transistor Amplifiers Using a New Large-Signal Model

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***Abstract*—In this paper, the intermodulation distortion (IMD) behavior of LDMOS transistors is treated. First, an analysis is performed to explain measured IMD characteristics in different classes of operation. It is shown that the turn-on region plays an important role in explaining measured IMD behavior, which may also give a clue to the excellent linearity of LDMOS transistors. Thereafter, with this knowledge, a new empirical large-signal model with improved capability of predicting IMD in LDMOS amplifiers is presented. The model is verified against various measurements at low as well as high frequency in a class-AB power amplifier circuit.**

***Index Terms*—Intermodulation distortion, large signal, LDMOS, model, power amplifiers.**

I. Introduction

IN MOST MODERN wireless systems, the linearity requirements put strong restrictions on the power amplifiers used. It has been found that LDMOS transistors exhibit better intermodulation distortion (IMD) performance compared to competing technologies [1], [2]. LDMOS transistors are, therefore, widely used in power amplifiers at microwave frequencies in commercial applications such as base–station transmitters.

IMD behavior in MESFET amplifiers has been treated in [3]. The analysis combines Volterra series for low input power with describing functions and harmonic balance for higher input power. It is shown that transitions between these input power regimes can explain measured IMD behavior such as sweet-spots in MESFETs.

Using a similar approach, we show in this paper that the sharp turn-on region, compared to MESFETs, makes it necessary to revise the analysis in [3] for LDMOS transistors. The appearance of double third-order IMD (IM3) minima in class AB that has been observed by other authors [1], [4] can then be explained.

The double IMD sweet-spots close to the compression point in class AB present a great potential advantage since similar linearity performance as for class A then can be achieved at a substantially improved efficiency.

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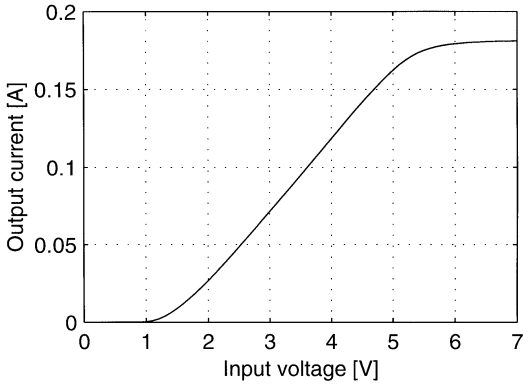

Fig. 1. Typical LDMOS transfer function $I_{\rm out}(V_{\rm in})$.

Commonly used LDMOS large-signal models [5]–[8], including the industry-standard MET-model, do not treat the turn-on region carefully enough and thus cannot predict measured IMD accurately.

A new empirical LDMOS large-signal model is therefore formulated in which the turn-on region of the transistor characteristic is treated independently from other modeling regions. As a result simulated IMD as well as output power and efficiency agree well with measurements. The model is formulated in a way similar to the MET model and is, therefore, easy to adopt.

II. IMD Analysis

The IMD is analyzed by studying the input voltage/output current transfer function (TF), $I_{\rm out}(V_{\rm in})$. The TF is found from the transistor $I_{ds}(V_{gs}, V_{ds})$ characteristics in combination with the drain bias, load impedance, and transistor parasitic elements. For MESFETs this has been done in [3]. Fig. 1 shows a typical TF obtained at low frequency for an LDMOS transistor in an amplifier application.

Since the transistor is usually biased with low quiescent current in the saturated region, the TF is essentially the $I_{ds}(V_{gs})$ characteristic for low output currents. At higher currents, it is saturated by either the load-line entering the triode region, or compression due to the JFET-effect in the LDMOS drift region [9].

To study the LDMOS IMD behavior, a two-tone test is often used. The input voltage will then have the form

$$v_{\rm in}(t) = A\left(\sin(\omega_1 t) + \sin(\omega_2 t)\right). \tag{1}$$

At low excitation power, a Volterra series analysis may then be used to calculate the IM3 in $I_{\rm out}(v_{\rm in})$. IM3 is here used as a

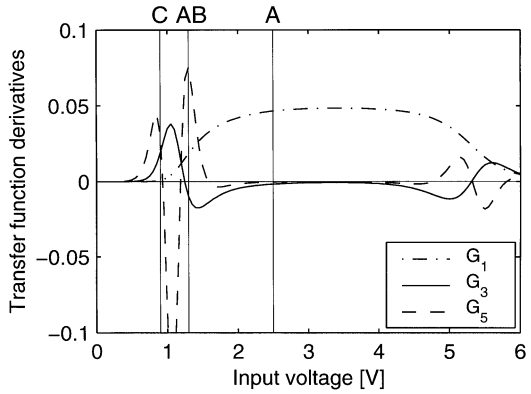

Fig. 2. Typical LDMOS transfer function derivatives versus input voltage $V_{\rm in}$. The bias voltages for different classes of operation are indicated on top of the figure.

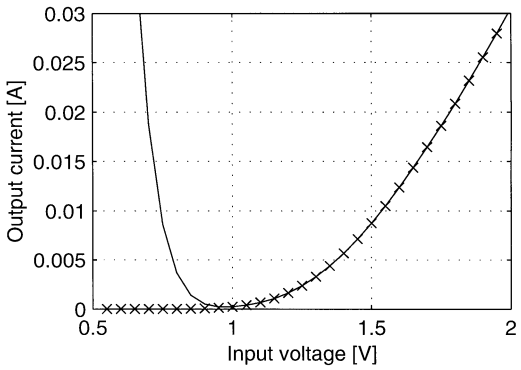

Fig. 3. Detailed view of the turn-on region, showing $I_{\rm out}(\times)$ and a tenth-order Taylor series expansion (line) around $V_{\rm in} = 1.5$ V.

general notation for the IMD sidebands appearing closest to the carriers, even if they usually are composed of also higher order IMD components.

The small-signal upper sideband IM3 at $2\omega_2 - \omega_1$ in $I_{\rm out}$ is given by [10]

$$\begin{aligned} I_{\rm out,SS}&(\omega_1,\omega_2) \\ &= 2\cdot{\rm Re}\left[\frac{3A^3}{8}H_3(\omega_2,\omega_2,-\omega_1)e^{j(2\omega_2-\omega_1)t}\right. \\ &\qquad \left. + \frac{50A^5}{32}H_5(\omega_2,\omega_2,-\omega_1,\omega,-\omega)e^{j(2\omega_2-\omega_1)t}\right] \\ &= 2\cdot{\rm Re}\left[I^{[-1,2]}_{\rm out,SS}(\omega_1,\omega_2)e^{j(2\omega_2-\omega_1)}\right] \end{aligned} \tag{2}$$

where the superscript [−1,2] indicates the frequency component considered. $H_3(\cdot)$ and $H_5(\cdot)$ are nonlinear transfer functions and φ_1 and φ_2 phase constants. At low frequency, the Volterra series analysis turns into a power series analysis of the TF around the quiescent voltage [10]. The TF is then described by

$$I_{\rm out}(v_{\rm in}) = I_{\rm out,DC} + G_1 v_{\rm in} + G_2 v_{\rm in}^2 + G_3 v_{\rm in}^3 + G_4 v_{\rm in}^4 + G_5 v_{\rm in}^5 \tag{3}$$

where the coefficients G_n represent the TF derivatives.

Fig. 2 shows typical LDMOS TF derivatives obtained using a large-signal model (see Section IV). The coefficients G_n are related to the nonlinear transfer functions so that the IM3 content in $I_{\rm out}$ can be expressed as [3]

$$I^{[-1,2]}_{\rm out,SS} = \frac{3A^3}{4}G_3 + \frac{25A^5}{8}G_5. \tag{4}$$

At low input power, IM3 is dominated by the third-order G_3 term, which results in a 3-dB/dB slope of IM3 versus input power. Equation (4) also shows that an interaction between third- and fifth-order derivatives of opposite signs can give rise to a large-signal IMD sweet-spot [3]. However, since the contribution from the G_5 term is usually much smaller, this happens at an input power level beyond the validity of the low-order Volterra series analysis used.

As the input power is increased, the signal excursion eventually reaches a region where the low-order power series in (3) no longer describes the TF adequately. These regions usually correspond to strong nonlinearities such as breakdown, gate forward conduction, or saturation due to the load line entering the triode region. In [3], a two sinusoidal input describing function (TSIDF) has been used to analyze the IMD for this purpose. The TSIDF for the IM3 product at $2\omega_2 - \omega_1$ is, in this case, defined as

$$\begin{aligned} &I^{[-1,2]}_{\rm out,LS}(\omega_1,\omega_2) = \\ &\frac{2j}{AT_1T_2}\int_{-T_1/2}^{T_1/2}\int_{-T_2/2}^{T_2/2} I_{\rm out}\left(v_{\rm in}(t_1,t_2)\right)e^{j\omega_1 t_1}e^{-j2\omega_2 t_2}dt_1dt_2 \end{aligned} \tag{5}$$

where $v_{\rm in}(t_1,t_2) = A(\sin(\omega_1 t_1) + \sin(\omega_2 t_2))$. It can be shown that $I^{[-1,2]}_{\rm out,LS}(\omega_1,\omega_2)$ becomes negative as the input signal amplitude approaches infinity—or simply as the output signal compresses. Therefore, depending on the sign of IM3 found from the small-signal analysis in (4), different IM3 versus input power patterns can be predicted. Such results are presented for MESFET's in [3].

For LDMOS transistors, the high-order derivatives in the turn-on region are much larger than the ones presented for MESFETs (see Fig. 2). This indicates that high-order terms are necessary for describing the transition appropriately. Fig. 3 shows how even a tenth-order Taylor series expansion fails to describe the TF beyond the turn-on knee.

For LDMOS transistors, the IMD behavior must therefore be analyzed with large-signal TSIDF techniques not only when the saturation region is reached, but also as soon as the input signal traverses the turn-on knee.

It is shown in the Appendix that the turn-on knee gives a positive IM3 contribution and therefore is an expanding nonlinearity as soon as the input signal traverses the knee. The amount of positive contribution is determined by the knee abruptness and the input amplitude.

Different distinct IMD characteristics can now be depicted from transitions between the contributions in the small-signal, turn-on, and large-signal regions. For example, the expanding and compressing nonlinearities of the turn-on and saturation regions, respectively, can counteract each other to create an overall more linear operation. The same principle is in fact used in predistortion linearization of power amplifiers [11].

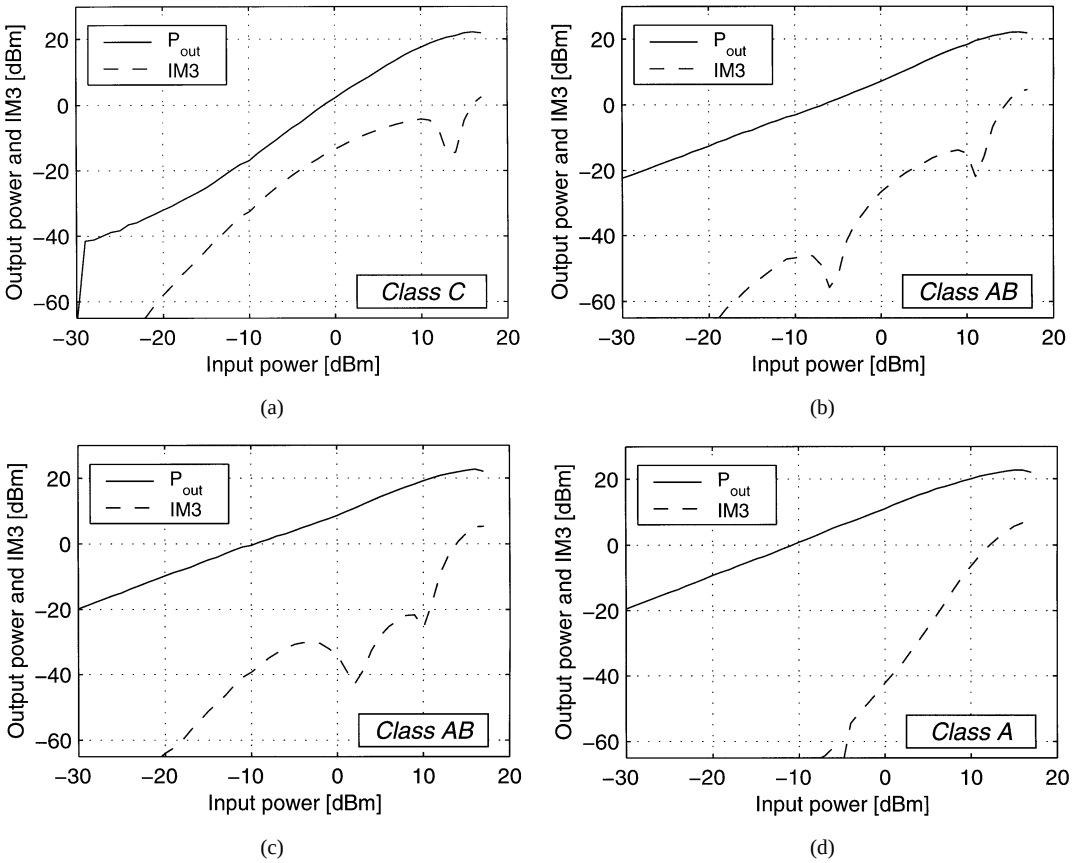

Fig. 4. Output power ($P_{\rm out}$) and third-order intermodulation distortion power (IM3) measured at 100 MHz for: (a) Class C, $V_{gs,\rm dc} = 0.9$ V; (b) Class AB, $V_{gs,\rm dc} = 1.2$ V; (c) Class AB, $V_{gs,\rm dc} = 1.3$ V; and (d) Class A, $V_{gs,\rm dc} = 2.5$ V.

III. Measured IMD Behavior

Two-tone measurements, shown in Fig. 4, have been performed to study LDMOS IMD behavior. The transistor used has $I_{dss} = 175$ mA and was biased at $V_{ds,\rm dc} = 20$ V [12]. The measurements were made in a 50 Ω environment at 100 MHz with 1-MHz frequency separation.

Depending on the class of operation, the different distinct IMD characteristics can now be explained using the behavioral analysis in the previous section.

A. Class-C Operation

From Fig. 2, the third-order derivative of the transfer function is seen to be positive in class C, $V_{\rm in,dc} = 0.9$ V. Thus, from (4) this implies that IM3 is also positive for low input power levels. The additional positive contribution from the turn-on region results in a further increase in the slope of the IMD curve and gain expansion. However, when the output power saturates, IM3 must become negative. Hence, an IMD minimum occurs near the compression point. Fig. 4(a) shows the measured output power and IM3 for this case. Similar IMD behavior has been observed in class-C MESFET amplifiers [1], [3], [13].

This kind of sweet-spot near the output power compression point, gives locally a very large carrier-to-intermodulation (C/I) ratio. However, in real amplifiers the input power may vary. It is therefore difficult to make use of this phenomenon for sufficient IMD suppression in those applications.

B. Class-AB Operation

To achieve better IMD performance while maintaining acceptable gain and efficiency, amplifiers are commonly designed to operate in class AB. This corresponds to a negative G_3 as seen in Fig. 2. The measured output power and IM3 for two bias voltages $V_{\rm in,dc} = 1.2$ V and $V_{\rm in,dc} = 1.3$ V in class AB are shown in Fig. 4(b) and (c), respectively.

The first of the two minima appears when the negative contribution from G_3 is cancelled by the positive IM3 contribution from the turn-on region. Since the turn-on region influence is much stronger, the minimum appears as soon as the input signal reaches that region. The minimum will therefore occur at higher input power if the transistor is biased further away from turn-on. This is confirmed by comparing the IM3 measurements. As the input power is further increased, IM3 will remain positive until the output power compresses and IM3 must again become negative. This change of sign creates another sweet-spot, close to the compression point.

By a proper choice of gate bias, the two minima can be combined to create a large C/I ratio over a much wider input power range near the compression point compared to class-C operation [(see Fig. 4(c)].

Note that this behavior is only possible because of the expanding nonlinearity of the sharp turn-on knee in LDMOS transistors. The same behavior is generally not observed in MESFETs.

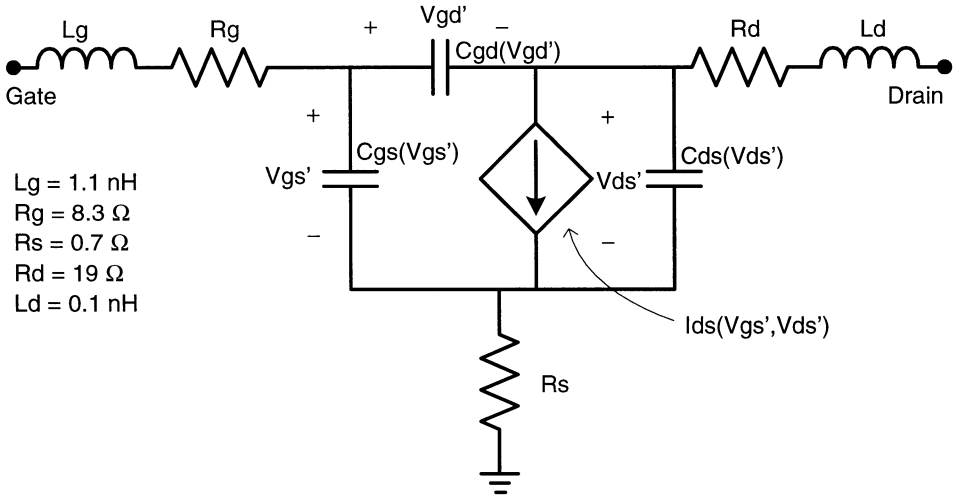

Fig. 5. Simple LDMOS large-signal model topology used.

C. Class-A Operation

As the bias is increased toward class A, G_3 will remain negative. The difference compared to class AB is that the input signal will now reach the output power saturation region before the turn-on region. IM3 will, therefore, remain negative and thus no IMD minimum is observed in Fig. 4(d).

Class A is usually considered the most linear mode of operation. Fig. 4 shows, however, that class AB may in fact be more linear over a wide input power range due to the double minima present.

The results in this and the previous section present a great potential advantage for LDMOS transistors, due to the existence of two IMD minima in class AB. Thereby, similar IMD performance as in class A can be achieved with a significantly improved efficiency.

The turn-on region, which is found very important for IMD when biased in class AB, is not accurately described in commonly used LDMOS large-signal models. In the following section, a new large-signal model is, therefore, presented where special care is taken to properly model the turn-on region. Thereby, IMD as well as output power and efficiency may be predicted very well.

IV. Large-Signal Model

In this section, a new empirical large-signal model is proposed. A simple model topology, shown in Fig. 5, has been used, where the parasitic and intrinsic small-signal parameter values have been found for various bias voltages using a robust multi-bias extraction technique [14].

First, modeling of the nonlinear current source $I_{ds}(V_{gs}, V_{ds})$ is treated.

A. Nonlinear Drain Current Model

Fig. 6 shows measured I_{ds} and extracted small-signal transconductance (g_m) plotted versus V_{gs} when the LDMOS is biased in the saturated region. The transconductance characteristics can be divided in different regions, each having its dominant physical origin. As discussed in previous sections,

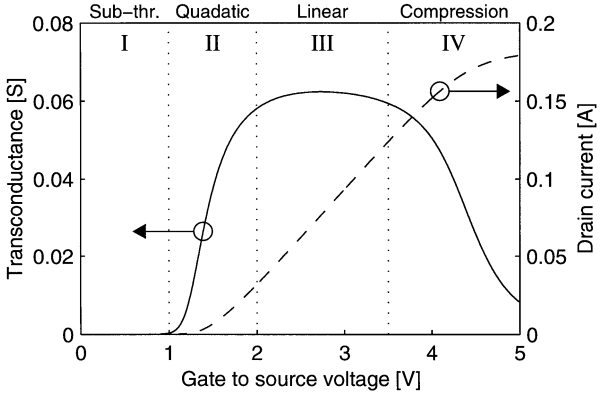

Fig. 6. Typical LDMOS transconductance g_m and drain current I_{ds} with different operating regions indicated.

accurate description of the knee-region is very important for prediction of IMD in LDMOS transistors.

In region I, the subthreshold region, the drain current is usually taken to depend exponentially on the gate voltage [15]. When the voltage is further increased, the current starts to rise quadratically (region II), which implies that g_m should rise linearly. The quadratic behavior is observed in MOS and LDMOS transistors [15]–[17].

The current in and between the subthreshold and quadratic regions is often modeled with [16], [17]

$$V_{gs1} = V_{gs} - V_t \tag{6}$$

$$V_{gst} = VST \ln\left(1 + e^{V_{gs1}/VST}\right) \tag{7}$$

$$I_{dsq} = \beta V_{gst}^2 \tag{8}$$

where VST controls the turn-on abruptness, V_t the turn-on voltage, and β the slope in the quadratic region.

For higher voltages (region III), short channel effects such as velocity saturation make I_{ds} approach a linear dependence on V_{gs} with a resulting constant transconductance.

Devices are usually designed to present constant transconductance over a region as wide as possible to achieve better IMD performance. This gives good linearity in class A operation but,

as shown in previous sections, it is no guarantee for better IMD performance in high efficiency linear amplifier applications.

Many large-signal LDMOS models, including the industry-standard MET model, do not address the quadratic region, but make the transition directly from the exponential subthreshold region to the linear region [4], [6], [8]. Thus, no parameters are available to define the turn-on knee abruptness and the knee tends to be too smooth. As described in Section II, this may severely affect its ability of predicting IMD behavior properly.

We have chosen to implement the transition from quadratic to linear regions using the following empirical expression:

$$I_{ds} = \frac{\beta V_{gst}^2}{1 + \frac{V_{gst}^{p\mathrm{lin}}}{VL}} \tag{9}$$

where the parameter VL in combination with β controls the slope of the quadratic region and transition to the linear region. The parameter $p\mathrm{lin}$ is added to tune the transconductance slope in the linear region. In most cases, $p\mathrm{lin} = 1$.

For higher V_{gs}, the transconductance will drop and the current compresses (region IV). This is typical for LDMOS transistors and is caused by the low-doped drift region acting as a grounded gate JFET in series with the intrinsic MOSFET transistor. For high currents, the JFET will force the intrinsic MOSFET to operate toward lower drain voltages where the transconductance is substantially lower [9]. A successful way of modeling this, which is used in the MET model, is to introduce an effective V_{gs} that saturates at a constant voltage, VK. The effective V_{gs} is given by [5]

$$V_{gs2} = V_{gs1} - \frac{1}{2}\left(V_{gs1} + \sqrt{(V_{gs1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right). \tag{10}$$

The proposed set of equations defining the nonlinear current source is given as follows:

$$V_{gs1} = V_{gs} - V_t \tag{11}$$

$$V_{gs2} = V_{gs1} - \frac{1}{2}\left(V_{gs1} + \sqrt{(V_{gs1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{12}$$

$$V_{gs3} = VST \ln\left(1 + e^{V_{gs2}/VST}\right) \tag{13}$$

$$I_{ds} = \frac{\beta \cdot V_{gs3}^2}{1 + \frac{V_{gs3}^{p\mathrm{lin}}}{VL}} \cdot (1 + \lambda V_{ds}) \tanh\left(\frac{\alpha \cdot V_{ds}}{V_{gs3}^{p\mathrm{sat}}}\right) \tag{14}$$

where the drain voltage dependence is taken from the MET model [5], [7]. λ and α are standard model parameters [5], [7], [16]. The parameter $p\mathrm{sat}$ controls the transition from triode to saturated region.

A simple thermal *R–C* circuit was also added to take care of self-heating effects [4].

Some of the parameters used may be nonconstant, depending on the accuracy required, e.g,

$$V_t = V_{t0} + \gamma V_{ds} \tag{15}$$

$$\beta = \beta_0 + \beta_1 (T - T_{\mathrm{nom}}) \tag{16}$$

$$\alpha = \alpha_0 + \alpha_k V_{gst} \tag{17}$$

$$VK = VK_0 + \gamma_{sat} V_{ds}. \tag{18}$$

Various possible dependencies of the model parameters—such as temperature, bias, and scaling effects—are beyond the scope of this paper, but have been investigated in [6] and [16].

B. Nonlinear Capacitances

At normal operating frequencies, the influence of nonlinear capacitances also has to be considered [7], [18]. The voltage dependence of the capacitances may be studied from the small-signal parameter extraction. Fig. 7 shows the extracted capacitances and the simple nonlinear models used.

For C_{gs} and C_{gd}, simple empirical hyperbolic tangent expressions have been used

$$C_{gx}(V_{gx}) = C_{gx0} + \frac{A_{Cgx}}{2}\left(1 + \tanh\left[k_{Cgx}\left(V_{gx} - V_{Cgx}\right)\right]\right) \tag{19}$$

where C_{gx0} is the offset value and A_{Cgx} affects the magnitude of the capacitance nonlinearity. V_{Cgx}, and k_{Cgx} control the center and abruptness of the capacitance nonlinearity, respectively. A simple depletion capacitance model is used for C_{ds}[15]

$$C_{ds}(V_{ds}) = \frac{C_{ds0}}{\sqrt{1 + \frac{V_{ds}}{V_{ds0}}}} \tag{20}$$

with C_{ds0} and V_{ds0} being the model parameters.

C. Model Verification

The current-source model parameters were found using a manual fitting procedure where extracted small-signal transconductance and measured pulsed and static drain current characteristics were used. Table I shows the total set of model parameters obtained.

Fig. 8 shows measured and modeled I/V characteristics for pulsed and static conditions.

It is well known that a model should predict not only I_{ds} but also its higher order derivatives to predict IMD accurately [19], [20]. Fig. 9 shows measured and modeled derivatives. Since static nonisothermal measurements were used, thermal effects make extraction of g_m and its derivatives more uncertain at high V_{gs}.

The derivatives have been extracted at 10 MHz and $V_{ds} = 20$ V using a setup presented in [19]. In the setup, sinusoidal signals of low amplitude and slightly different frequency are applied simultaneously to the gate and drain terminals. By studying the resulting intermodulation products in the drain current using a spectrum analyzer, and knowing the small-signal equivalent circuit, makes it possible to determine the nonlinear current source derivatives. The resulting measurement accuracy is very good as indicated by the regularity of the measured derivatives.

The accuracy of the nonlinear current part of the model is demonstrated by its ability to predict the IMD measurements shown in the previous section. Fig. 10 shows measured and modeled IM3 at $V_{gs} = 1.3$ V.

Similar measurements showing double IMD sweet-spots have been presented in [4], where it was simply concluded

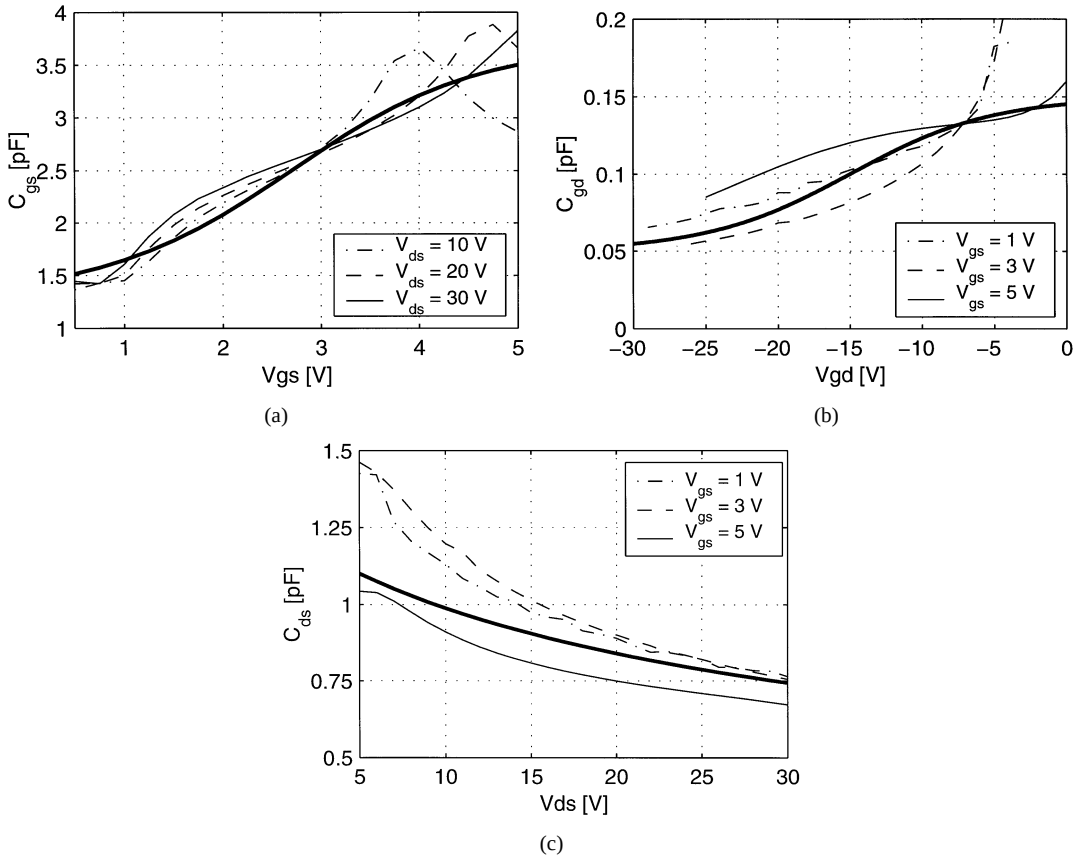

Fig. 7. Extracted small-signal capacitances (thin lines) and the corresponding nonlinear capacitance models (thick lines).

TABLE I
CURRENT-SOURCE MODEL PARAMETERS.

Parameter	V_{t0} [V]	VST [V]	β [A/V^2]	λ [1/V]	α [1/V]	VL [V]	$VK0$ [V]	Δ [V]
Value	1.15	0.13	0.082	0.003	1.32	0.9	2.7	0.56

Parameter	$plin$	$psat$	γ	γ_{sat}	R_{th} [°C/W]	C_{th} [J/°C]	β_1 [A/KV^2]
Value	1.02	1.1	-0.007	0.05	9.6	10^{-4}	-0.001

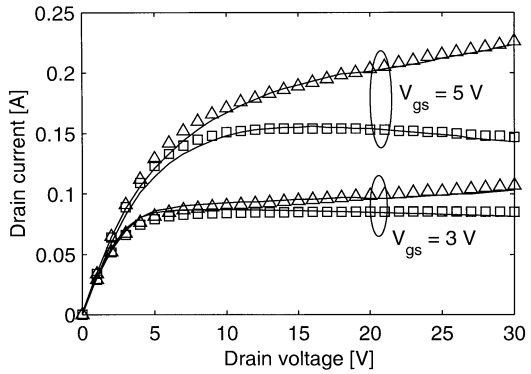

Fig. 8. Measured (markers) and modeled (lines) drain current for static (□) and pulsed (△) conditions.

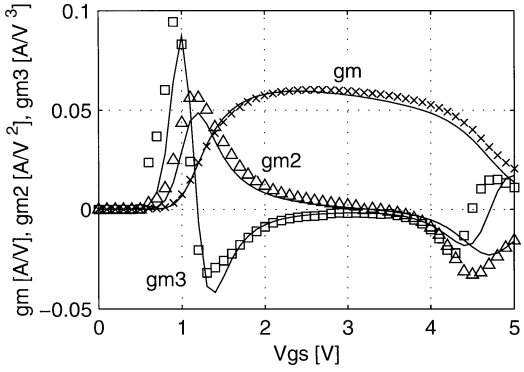

Fig. 9. Measured and simulated I_{ds} derivatives versus V_{gs} at $V_{ds} = 20$ V.

that "the [IMD] data has unusual structure." The MET model used in that case did not predict the existence of double IMD sweet-spots.

At high frequency, large influence of nonlinear capacitances on intermodulation generation has been reported for MESFET's and LDMOSFET's [7], [18]. This is confirmed in Fig. 11 where a false IMD minimum is simulated near the compression point when constant capacitances, taken as the small-signal values at the bias point, are used.

Compared to the measurements at low frequency, the nonlinear capacitances tend to smoothen the IMD behavior making only one less pronounced sweet-spot appear. Thus, the IMD improvements compared to class A are reduced. However, proper

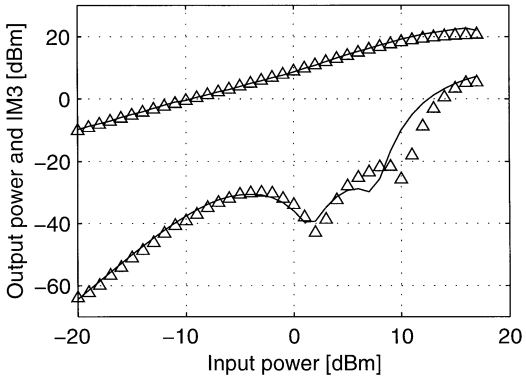

Fig. 10. Measured (markers) and simulated (lines) output power and IM3 at $V_{gs} = 1.3$ V, $V_{ds} = 20$ V, and $f = 100$ MHz.

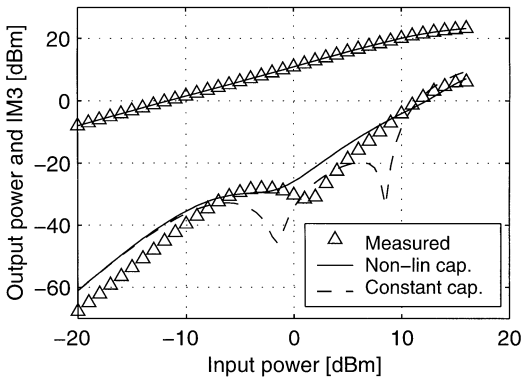

Fig. 11. Comparison between measured and simulated output power and IM3 for the cases of nonlinear and constant capacitances. The comparison is made at $f = 1.9$ GHz, $V_{gs} = 1.2$ V, and $V_{ds} = 28$ V. Terminating impedances were adjusted for maximum output power.

tuning of the harmonic terminating impedances might restore the performance.

A slight shift toward lower power level is seen in the simulation for the sweet-spot.

V. Power Amplifier Circuit Example

A 1900-MHz power amplifier for 28-V supply voltage was built using the same device as in previous sections to examine the IMD behavior at high frequency in a real circuit environment. The amplifier was designed to operate in class AB with the input matched for maximum gain and the output impedance chosen for maximum output power [21]. The output network was designed to short-circuit signals at second harmonic and baseband to improve the IMD behavior [3].

Measured and simulated output power and efficiency are shown versus input power in Fig. 12. The simulations were made using the model presented in Section IV.

The maximum power added efficiency (PAE) is quite low, 20%. It can be explained by the large drain resistance $R_d = 19\,\Omega$ in the extracted model. R_d is set by losses in the substrate and the low-doped drift region. However, simulations indicate that the efficiency rises drastically at lower frequency as the reactive currents through R_d are reduced.

The IMD performance was studied using a two-tone test with 1-MHz frequency separation. Fig. 13 shows measured C/I

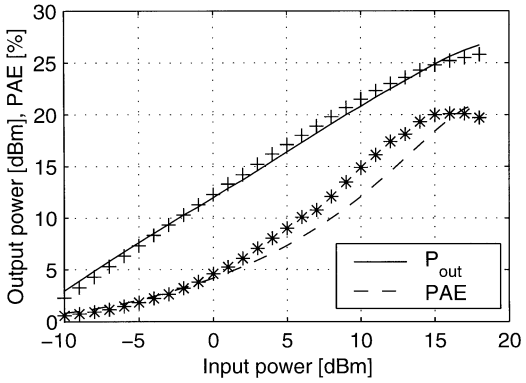

Fig. 12. Measured (markers) and simulated output power and PAE.

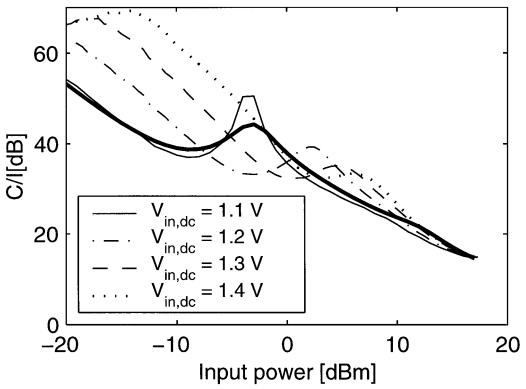

Fig. 13. Measured C/I versus input power at different input bias voltages. The thick line corresponds to a simulation made at $V_{\mathrm{in,dc}} = 1.2$ V.

for various input bias voltages. A simulation is also shown for $V_{\mathrm{in,dc}} = 1.2$ V.

The results in Fig. 13 agree well with the simulation except for a 0.1-V bias voltage offset. As discussed in Section IV, only one IMD sweet-spot is present at high frequency due to the nonlinear capacitances.

Nevertheless, as predicted in the low frequency analysis for operation in class AB, the measurements validate however that a bias-dependent IMD sweet-spot is present also at higher frequencies.

VI. Conclusions

First, the IMD behavior in LDMOS transistor amplifiers has been analyzed using a behavioral analysis. The analysis has shown that the sharp turn-on knee compared to, e.g., MESFETs plays an important role in understanding measured IMD behavior. The existence of two IMD sweet-spots in class AB operation could be predicted, and presents an important advantage for LDMOS transistors. Better efficiency may then be achieved with similar linearity as in class A.

Since most commonly used large-signal models do not address the turn-on region, specifically, a new large-signal model was also presented with special treatment of the turn-on knee for accurate prediction of the observed IMD sweet-spots. Nonlinear capacitances are also shown to play an important role for prediction of IMD at high frequency. The model predicts various low- and high-frequency measurements of dc, output power, IMD, and efficiency characteristics well.

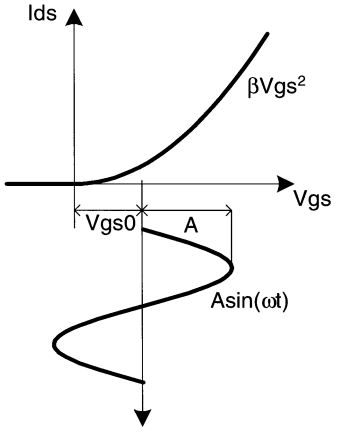

Fig. 14. Idealized description of the transistor turn-on region and the applied input signal.

APPENDIX

It will be shown that the turn-on region gives a positive IM3 contribution and, therefore, is an expanding nonlinearity as soon as the input signal traverses it.

The harmonic generation from a single sinusoidal input signal is used since the third harmonic content is a direct measure of the IM3 generation that will occur in a two-tone test.

To ease algebraic calculations, the turn-on region is idealized as shown in Fig. 14, where the current goes abruptly from zero to a quadratic V_{gs} dependence.

The sinusoidal input signal in Fig. 14 can be expressed as

$$V_{gs}(t) = V_{gs0}(1 + a\cos(\omega t)) \tag{A1}$$

where $a = A/V_{gs0}$.

If $a < 1$ the input signal does not reach the knee. Then, since a purely quadratic nonlinearity is considered, I_{ds} will not contain any odd-order harmonics other than the fundamental frequency and no IM3 can be generated. The fundamental frequency content of I_{ds} is in this case given by

$$I_{ds}^{[1]} = 2a\beta V_{gs0}^2. \tag{A2}$$

When $a > 1$, the output waveform will be clipped. This occurs at $\tau = \pm \arccos(-1/a)/\omega$. The fundamental and third harmonic content in I_{ds} will then be given by

$$I_{ds}^{[1]} = \frac{2}{T}\int_{-\tau}^{\tau} \beta V_{gs}^2(t)\cos(\omega t)\,dt \tag{A3}$$

$$I_{ds}^{[3]} = \frac{2}{T}\int_{-\tau}^{\tau} \beta V_{gs}^2(t)\cos(3\omega t)\,dt \tag{A4}$$

where $T = 2\pi/\omega$, which yields

$$I_{ds}^{[1]} = 2a\beta V_{gs0}^2\left[1 - \frac{1}{\pi}\arccos\left(\frac{1}{a}\right) + \frac{\sqrt{a^2-1}}{3\pi}\left(2 + \frac{1}{a^2}\right)\right] \underset{a\gg 1}{\longrightarrow} 2a\beta V_{gs0}^2\left(\frac{1}{2} + \frac{2a}{3\pi}\right) \tag{A5}$$

$$I_{ds}^{[3]} = \frac{4\left(a^2-1\right)^{5/2}\beta V_{gs0}^2}{15\pi a^3} \underset{a\gg 1}{\longrightarrow} \frac{4a^2\beta V_{gs0}^2}{15\pi}. \tag{A6}$$

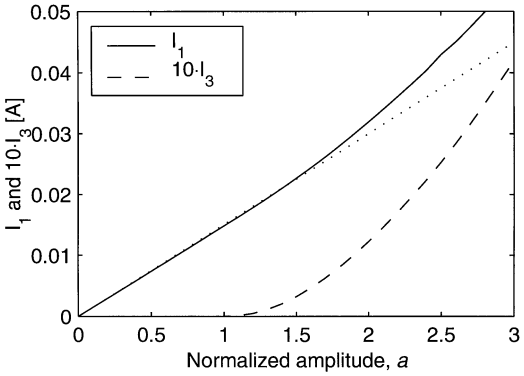

Fig. 15. Harmonic generation versus normalized input amplitude a. The dotted line indicates the extended linear $I^{[1]}$.

These equations show that the knee-region represents in fact an expanding nonlinearity with a positive IM3 contribution as soon as the input signal traverses the turn-on knee.

Fig. 15 presents the fundamental and third harmonic content in I_{ds} versus normalized input drive level, a. The parameters are chosen to match the device used. Comparison with a more accurate model for the turn-on knee shows small difference.

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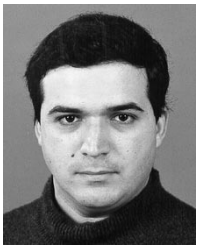

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