GEM-P Progress Report
Electronics
(July2006)

1. Introduction

GEM collaboration now proceeds towards the 5GHz radiometer upgrade for polarimetry measurements of the Milky Way synchrotron emission.

The block diagram of the favored solution that describes the radiometer is presented in Figure 1. The blocks in green are numbered according to execution order. The IF receiver parts are being developed first due to their intrinsic simplicity and lab test availability.

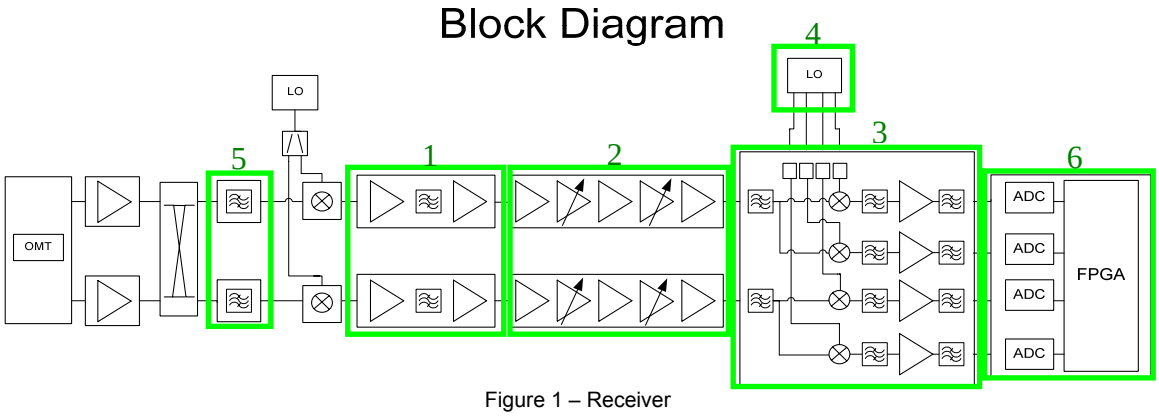

Figure 1 – Receiver

This radiometer was designed to select a portion of the available output power of the antenna, that is a certain bandwidth B around a given center frequency. In our case we have selected a bandwidth B of 200MHz around 5GHz (as decided by the GEM team at LBNL).

Note: *The center frequency for GEM-P operation was, however, changed to 4.900GHz, after concerns about band protection expressed by the Portuguese radio spectrum ruling board (ANACOM). Protection can be guaranteed only in the range 4.8-5.0GHz.* The initial signal power at the OMT is about 10K (signal + CMB + atmosphere + antenna setup), or -105dBm. This value is above the minimum noise power (-174dBm) presented in the environment. The table below (Excel sheet) justifies the calculations, where we use typical approximate values for each of the components characteristics along the receiver. It includes all the values of gain and attenuation suffered along the receiver in figure 1:

Antenna		Cryogenic Amplifier	Mixer 4,4GHz	PassBand Filter	Amplificador1	Digital Control Attenuator	Amplifier2	Mixer 600 MHz	LowPass Filter	OPAMP
		Gain (dB)	Attenuation (dB)	Attenuation (dB)	Gain (dB)	Attenuation(dB)	Gain (dB)	Attenuation (dB)	Attenuation (dB)	Gain (dB)
		25	7	3	37	0	75	8	0	25
Kelvin	dBm	dBm	dBm	dBm	dBm	dBm	dBm	dBm	dBm	dBm
10	-106	-81	-88	-91	-54	-54	21	13	13	38

Vin(ADC)	1Vp-p
Vrms(Vin(ADC))	0.7Vrms
P(watts)(Vin)ADC)	0.01
P(dBm)Vin(ADC)	10
Gain AMPs	153
Total Gain	116

The first design consideration for this circuit was the choice of the right ADC to digitize the signal. To achieve the highest value at the input of the ADC we need to get into account the contribution of all the components present at the radiometer. The analog input range of the ADC is 1Vp-p (0,7Vrms), or 10dBm in terms of power, at the OMT we have 105dBm, so the receiver will need a total gain of 115dB.

After getting all the specifications we created the circuits for each block. All the circuit simulations were made using the **Advanced Design System (ADS)**, a very convenient software tool for analog, RF, and microwave circuit simulation.

2. Block Description

a. IF Preamplifier

The first block is the **IF Preamplifier (1)**. The function of this block is to make an initial gain contribution to the system with a band pass filter. At this point, we have already performed a down conversion from 4,9GHz to 600MHz. This system includes a bandpass filter of 200MHz bandwidth centered at 5GHz. While designing this block care has been taken in accounting for the behavior of the amplifiers at these frequencies (ripple within the passband has to be very low), in order to avoid feedback oscillations. Special attention was thermal fluctuation in this block. Therefore, an amplifier with negligible gain variation with temperature was chosen. A necessary step to minimize temperature variations is to put all the elements in a box, specially designed, so as to protect the circuit from outside influence. The large gain of this block (≈37dB) also imposes careful layout techniques in order to avoid unwanted feedback, which could at certain frequencies become positive.

It's time to proceed towards layout design. The layout was created using the tool Layout Plus from ORCAD.

The following picture shows the soldering process of the components on the PCB board:

Figure 2 – Soldering the components

The physical result of the layout drawn is presented in the next picture:

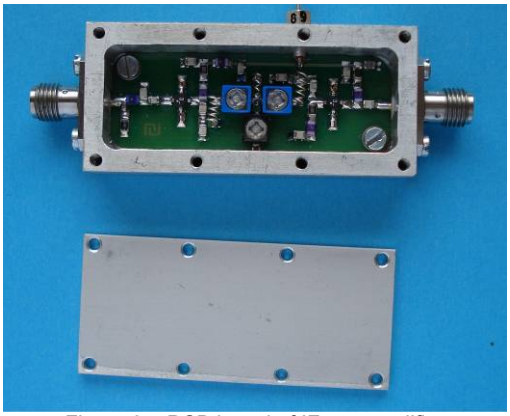

Figure 3 – PCB board of IF pre-amplifier

The implementation and test phase are being performed, using, among other instruments, a Hewlett Packard 8702A and an Agilent E8361A Network Analyzers, along with a spectrum analyzer, as you can see in the picture below:

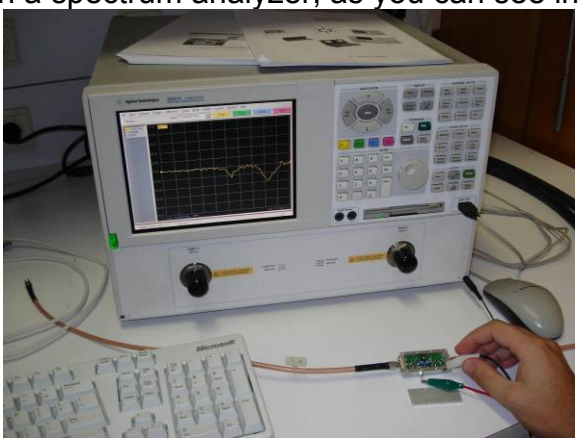

Figure 4 – Testing phase

The first results obtained are acceptable, now it's time to adjust the filter using the trimmers of the filter, among other component variation, like the air inductances, that need to be enhanced.

b. IF Amplifier

This block (2) provides the greatest contribution of gain of the total system. As we see in Figure 1 it is made up of a group of amplifiers (5) and two digitally controlled attenuators. These attenuators enable the user to control the signal at the input of the ADC. The choice of the amplifiers was made using the same criteria as for the IF preamplifier. Gain considerations were taken into account as well. Amplifiers selected exhibit a slow variation of gain with frequency within the pass band. At this point in the system we have 41dB, of gain, but with normal losses, the real gain will become about 37dB, to get 115dB, is still 78dB short of the final gain.

The picture below shows the final aspect of this block, in this picture was taken while soldering the components.

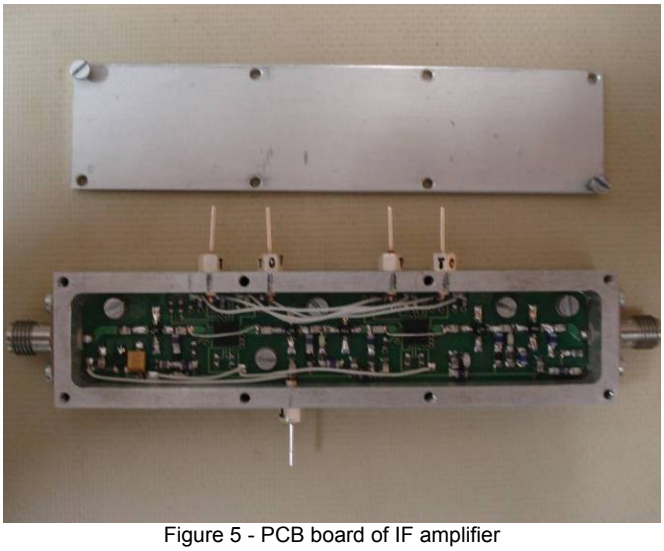

Figure 5 - PCB board of IF amplifier

c. Converter

There will be two branches in this block (3), in two boards, four branches in the total. The above mentioned signals have information have an in-phase (I) and a quadrature (Q) component. In order to obtain these components the signal is combined with a $\pi/2$ delayed version of itself The output of this block will be a group of two signals, one that contains information about I and the other that contains information about Q, both signals having a bandwidth of 100MHz. The signal that comes from the antenna is divided in RCP (right circular polarization) and LCP (left circular polarization), so we will have four branches in this block. We decided to perform these operations in two separate, but identical, boards.

At this point in the system, we are still at 600MHz, Now, because the data is going to be acquired at 100MHz in the FPGA, we need to do a second down conversion, from 600MHz to DC, maintaining the necessary 100MHz of bandwidth to the FPGA.

This block is constituted by a power splitter, to guarantee a perfect separation of power in the two channels; a mixer, responsible for the frequency conversion; a diplexer, to match the higher frequencies without reflections; a high order (N=7) low pass filter with a cutoff frequency of 100MHz, and an OPAMP, the last gain contribution of the system. This is a non-inverting configuration, with at least 25dB of gain. This block concludes with another low order low pass filter, to eliminate spurious signals caused by imperfections of the OPAMP.

The filters used in this block are of the same type as the filter at the IF preamplifier. The first has order N=7, and a cutoff frequency of 100MHz. The other has lower order (N=3), with the same cutoff frequency.

The real aspect of the PCB board is the following:

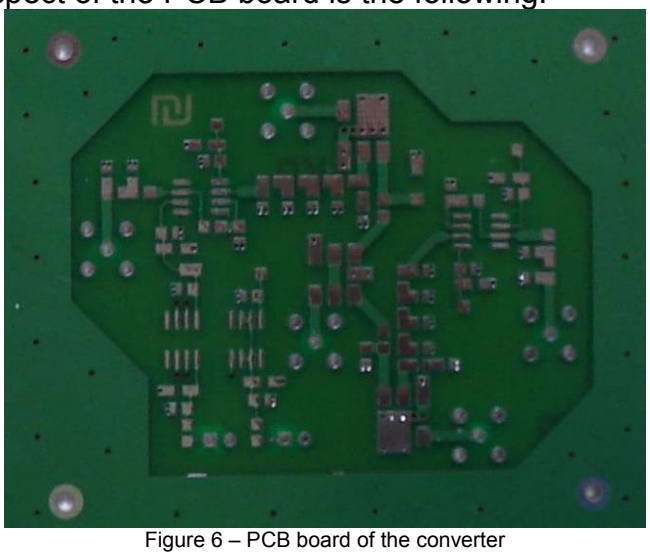

Figure 6 – PCB board of the converter

d. Local Oscillator

This block (4) feeds the mixers from the converter. Its components are a voltage controlled oscillator, some gain blocks and a PLL (Phase-locked loop).

The most important component of this block is the oscillator, chosen to obey certain specifications, namely the frequency of oscillation and its power output. Together with the variable voltage, to control the local oscillator, we have a PLL low power frequency synthesizer.

In comparison with other signals in the system, the ones in this block will have much lower power, so we need to protect this circuit, as was done before in the converter, with a box. The external signals cannot pass into the circuit, to avoid damage in the block operation. The same care had been employed in the track lengths, since all the four distances will be equal. The ground plane around the circuit eliminates any parasitic capacitance.

The PCB board result is shown next:

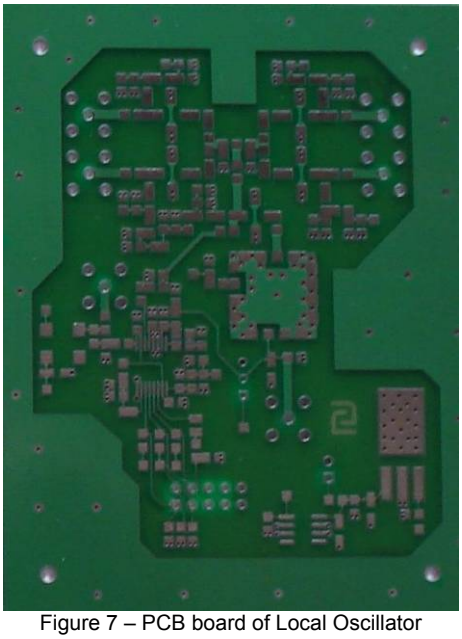

Figure 7 – PCB board of Local Oscillator

e. Microstrip filter (coupled line)

This block (5) will eliminate frequencies outside our band, so it is centered at 4.9GHz with a bandwidth of 500MHz. This microwave filter is made by coupled line filters, implemented using the Design Guide of ADS, Passive Circuit Design. We had some problems with the simulation results, the band we needed is good, but there are some imperfections of the filter at higher frequencies. The solution tried was to introduce stubs at the input and output, of the same type and separated from the filter by a 50 ohm line. The problematic bands disappeared. The filter layout in ADS is similar to the one shown on Figure 3:

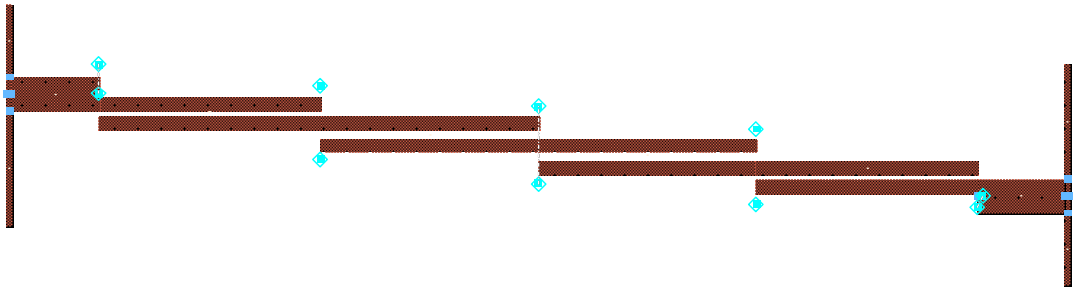

Figure 8 – Layout of Microwave Filter

In this filter, the 50 ohm line at the input and output where the SMA connectors will link are missing.

Momentum is a 3-D planar electromagnetic (EM) simulator used for passive circuit analysis. It accepts arbitrary design geometries (including multilayer structures) and accurately simulates complex EM effects including coupling and parasitics. Accurate EM simulation enables RF/MMIC designers to improve passive circuit performance and increases confidence that the manufactured product will function as simulated. Due to problems derived from

bad interconnections between lines, the first simulations had several bad results. The solution was to snap the lines to grid in they were automatically interconnected by the software. Once these problems were solved, and after several adjustments, for getting the desired results we have obtained the following results:

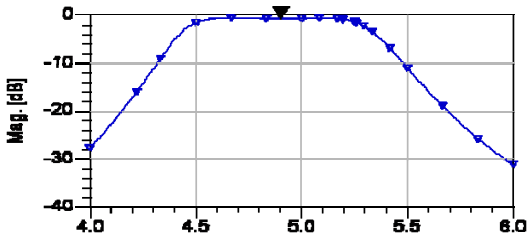

Figure 9 – S21 parameters of Filter

Like the IF pre-amplifier and IF amplifier, this block is going to be in a special isolation box. The PCB board is being fabricated, using a specific substrate (RO4003C), which has better characteristics than the one used in the other PCB boards (ε_r higher, lower thickness).

f. ADC and FPGA

This block (6) is where the signal is going to be sampled, digitized, auto correlated, integrated and transmitted to an acquisition system (PC). We are going to use a FPGA that will work at 100MHz, with sufficient I/O ports to receive the data from the ADC, calculate the auto correlations and transmit the desired data. The Cyclone II was our option, and fulfills all our needs, it has 36 multipliers of 9 bits and 208 ports, and works perfectly at 100 MHz.

The ADC we chose has an output (DS+ DS-) that could help for all ADCs synchronization. For the clock circuit we feed the FPGA with one crystal oscillator (a trigger output can also be derived from this circuit). The FPGA will feed the clocks of the ADC's. The ADC chosen has a better performance for single ended operation so we need to transform a single ended signal into differential. The schematic is being finished needing only some little adjustments.

g. PC

At this moment we have only decided the PC we are going to use. We need a embedded PC104, with low power consumption, working at least at 300MHz, and supporting RS232, IDE, ISA, Ethernet, Graphical interfaces and without fan. It will work in a Linux environment.

h. Hardware for antenna and encoders control

To interface the motors from the antenna, and the controller we designed the following circuit:

It is divided in two parts, the power control and the index of the motors. The power control is simply a MOSFET power transistor giving the necessary voltage to switch the relay of 12V to feed the motor. The four relays are for the four directions (LEFT, RIGHT, UP and DOWN). The indexes indicate the position of the antenna when passing trough certain positions. This circuit interfaces this information from the indexes to the controller. The diodes are for circuit protection, and an optocoupler is used to isolate signals between the indexes and controller. The encoders of the antenna need a differential clock, and different circuits to provide the differential CLOCK and differential DATA. The PCB boards are made and ready to be mounted.