A 1.8V/5GHz CMOS WLAN Low Noise Amplifier Integrated with Active BALUN

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***Abstract* — This paper presents the design and simulation of a 5GHz monolithic low-noise amplifier integrated with an active Balun. Intended to WLAN applications, the fully integrated circuit was implemented in a 0.18µm CMOS technology. The simulations, optimized to noise performance, gain and minimum differential phase and magnitude error, were performed with BSIM3 model. Circuit simulations present 23dB differential power gain at 5GHz, a phase and a transducer gain magnitude errors less than 1º and 0.2dB, respectively, in a 100MHz span around 5GHz, NF =3.6dB, 1dB$_{CP}$ = -22dBm, IIP3 = -8dBm, 50Ω input and output match, while drawing 8mA from a 1.8V power supply.**

***Keywords* — Balun, CMOS, Low Noise Amplifier (LNA), RF Integrated Circuit, Phase Converter, Wireless Communications.**

I. INTRODUCTION

Wireless local-area networks (WLANs) have been deployed as office and home communications infrastructures worldwide. The diversification of the standards, such as IEEE 802.11 series demands the design of RF front-ends. Low power consumption is one of the most important design concerns in the application of those technologies. To maintain competitive hardware costs, CMOS has been used since it is the best solution for low cost and high integration level, allowing analog circuits to be mixed with digital ones.

The development of high performance monolithic RF transceivers requires innovative RF circuit design to make the best of a good technology. In the receiver chain, the low noise amplifier (LNA) is one of the most critical blocks. The sensitivity is mainly determined by the LNA noise figure (NF) and gain. Furthermore, since it is the first gain stage, care must be taken to provide accurate input match, low NF, good linearity and a sufficient gain over a wide band of operation.

A fully differential approach is usually preferred, due to its well-known properties. Although the differential approach must be preserved inside the chip, there are cases where the input signal is single-ended such as RF image filters and IF filters in a RF receiver. In these situations, a stage able to convert single-ended into differential signals, known as Balun[1], is needed.

This work reports the design and implementation [1] of a low power LNA, integrated with an innovative high-performance monolithic Balun on a 0.18µm CMOS process.

The circuits presented here are aimed at IEEE 802.11a for WLAN applications. All the required circuits are integrated on the same die and are powered by 1.8V supply. The simulated results are shown, promising excellent experimental performance.

Section II describes LNA and Balun topologies and the interconnected circuit design. Section III shows the simulated performance results focused at gain, phase/amplitude balance and noise figure. Finally, the last section draws conclusions and future work.

II. DESCRIPTION OF THE CIRCUIT DESIGN

A. Low Noise Amplifier topology

The LNA must provide enough gain to reduce the impact of the following stages in the overall NF. As a first stage of receiver architecture, considerations like low NF and high gain must be taken into account during the LNA design. Besides that, linearity, input and output impedance match and stability (K_f) must also be considered. A classical noise matching technique was used. This technique, firstly reported in 1960 [2], was recently re-studied and reported in [3][4].

To allow a good compromise between high gain and low noise, a common source topology is preferable. A schematic of the proposed LNA is shown in Figure 1. It is a cascode common source topology, with a simple input and output matching network to enable wide band. Both input and output ports are matched to 50Ω. The predominant capacitive matching networks makes use of all parasitic elements to optimize input/output matching.

B. Active Balun topology

Several active Balun topologies have been proposed in the literature. The most cited and a strong candidate for use as active Balun is the differential topology shown in Figure 2.

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[1] BALUN - BALanced from UNbalanced signal converter.

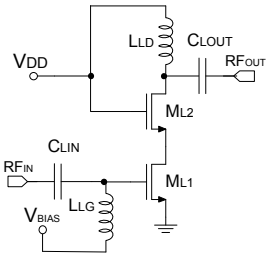

Fig. 1. Cascode common source LNA topology.

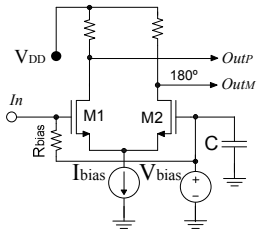

Fig. 2. Differential topology for active Balun.

Consisting on a differential pair stage with one of the two inputs grounded, is capable of providing high gain and ideally split equally between the output pair, the RF signal applied to the other input. In ideal conditions, it provides 180º phase shift between the two output signals.

However, this solution has some drawbacks when implemented monolithically. The differential architecture shown in Figure 2 uses double common sources to obtain differential output. If implemented in a monolithic technology, it is impossible to obtain a perfect ground at the gate of M_2 due to the bond-wire used for grounding and bond pad parasitic capacitance. Also, as reported in [5], the impedance of the non-ideal current source is not as high as required to equal signal distribution. The two drawbacks point to an imbalance between the two output signals, meaning that a correct differential phase and equal magnitudes are unobtainable.

In contrast with the referred above, the proposed new Balun topology, presented in Figure 3, takes place in two distinct modes to obtain differential output, one using a common source and other a common gate. This provides two main advantages: no dependency of series gate impedance and no special care on parasitic bond-wire connection to ground. Dedicated simulations have confirmed this behavior.

Even using different source and gate common modes in each input branch, both output loads see similar impedances. With a proper layout design the circuit achieves good phase/gain balance. This solution overcomes the limitations

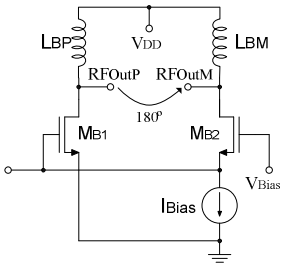

Fig. 3. Balun topology used in this work.

of the circuit of Figure 2 and has several advantages when compared with other reported monolithic active Baluns [5][6].

C. Active Balun integrated with LNA

The schematic of the integrated LNA/Balun circuit is shown in Figure 4. Due to the additional noise of the LNA/Balun following stages, it is necessary to mitigate the noise effects of these circuits. The single-input and the differential outputs are all matched to 50Ω. The 50Ω output loads were just used just for testing purpose.

Inter-stage matching network makes use of the parasitic elements of the active devices M_{L2}, M_{B1}, M_{B2} and I_{Bias} current source and the capacitor C_{LOut}, to optimize matching. Coupling capacitor C_{LOut} is also needed to achieve DC isolation between the active devices of both blocks. Inductors L_{LG} and L_{LD} contributes also to matching.

Since external source currents are preferable, the V_{BIAS1} is created using an extra current source to internal voltage reference bias, not shown for simplicity. The current I_{Bias} is generated by a current mirror reference, also not shown for simplicity. V_{Bias1} and V_{Bias2} are off-chip current-controllable for testing purpose only.

All the active devices used are in stack and have a fixed width of 5µm with variable number of fingers. The input common-source device M_{L1}, with size of W/L=100µm/0.18µm, is optimized for noise and input match. The device M_{L2}, which has the same size of M_{L1}, is optimized for noise and inter-stage match with Balun input. The size of the devices M_{B1} and M_{B2} is 50µm/0.18µm. The output stage

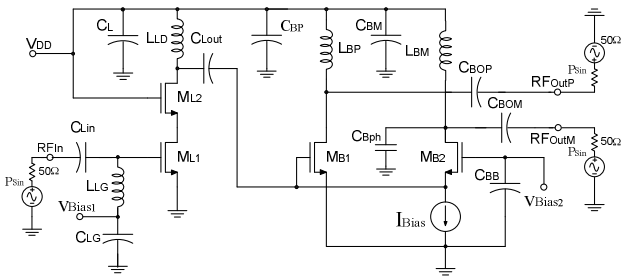

Fig. 4. LNA/Balun schematic.

is AC coupled to differential outputs loads with C_{BOP} and C_{BOM} capacitors. Inductors L_{BP} and L_{BM}, which are DC coupled to the common-source and common-gate, respectively, are essential elements to achieve the 50Ω impedance match in both differential outputs. On-chip spiral inductors play a significant role in realizing fully integrated RF circuits. Due to the substrate losses, they exhibit poor performance in terms of their quality factor, strongly limiting circuit results. However, even with low Q, it is possible to obtain good results with the new topology, as shown in the following section.

III. Circuit Simulation Results

The proposed circuit was simulated using Spectre from Cadence [7] with the 0.18µm/1.8V-RFCMOS process from UMC [8]. The circuit was simulated over a large variety of conditions. In the 4.5GHz to 5.5GHz frequency band, the results were taken with a 1.8V supply voltage and using 50Ω single-ended input and output ports. Noise figure, transducer gain, return loss and linearity were optimized by adjusting I_{Bias}, V_{Bias1} and V_{Bias2}. The simulation results are illustrated in Figures 5 to 8. Results are promising for gain, noise figure and phase and magnitude mismatch. Stability is also insured ($K_f > 2.5$).

Figure 5 presents the simulations of phase and magnitude mismatch. Unbalance between the two branches is expressed from their gain magnitude and phase differences extracted from forward transmission. A broadband well balanced behavior was achieved, since the circuit exhibits phase and amplitude errors between the two output ports lower than 4º and 0.9dB, respectively, from 4.5GHz to 5.5GHz. These errors are better than 1º and 0.2dB in a 100MHz span centered at 5GHz.

In Figure 6, input/output match and transducer gain magnitude are expressed in terms of S-parameters. The circuit has a good input match (S_{11} = -18dB) and reasonable output mach at both output branches ($S_{22} = S_{33}$ = -9dB). The transducer gain, S_{31} and S_{21}, presents a maximum value of 20dB at 5GHz, leading to 23dB single-ended input to differential output gain. In a 1GHz span centered at 5GHz, the transducer gain is higher then 16dB (19dB differential). The noise performance is shown at the same graph. At 5GHz the noise figure (NF) is 3.6dB and the phase and magnitude errors are 0.1º and 0.06dB, respectively. In the 4.5GHz to 5.5GHz band, the circuit presents a NF lower then 5.1dB. Figures 7 and 8 demonstrate that the overall circuit is highly linear, since the input-referred 1dB compression point is -22dBm and the input-referred third-order intercept point is -8dBm.

IV. Conclusions

An LNA integrated with an active Balun was presented for WLAN applications. The total circuit is fully integrated in a low cost CMOS process with total area of 1mm^2. Simulations show that under a 1.8V power supply the circuit has a 23dB differential power gain at 5GHz with 8mA current consumption. The overall circuit presents a well balanced broadband behavior, since the Balun exhibits low differential phase and magnitude errors compared with the ones reported in [5] and [6]. It also achieves better performance in S_{21}, $1dB_{CP}$, IIP_3 and power consumption.

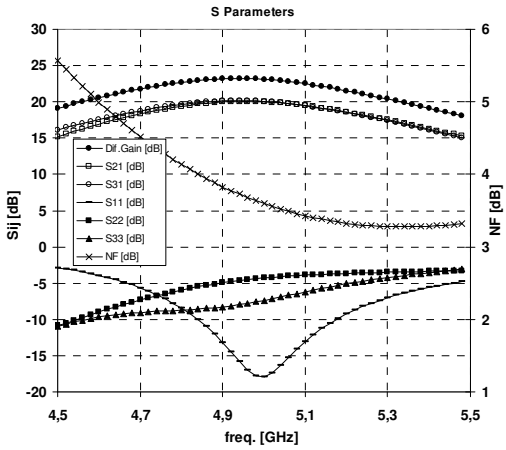

Fig. 6. S-Parameters and NF.

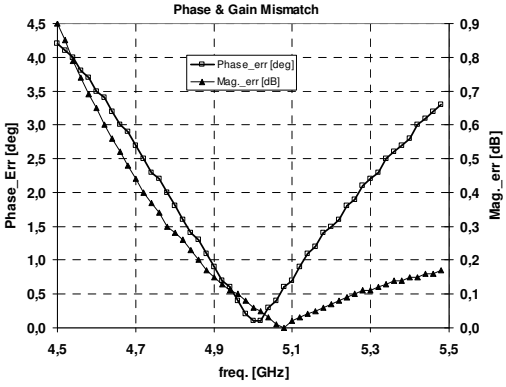

Fig. 5. Phase and mag. mismatch.

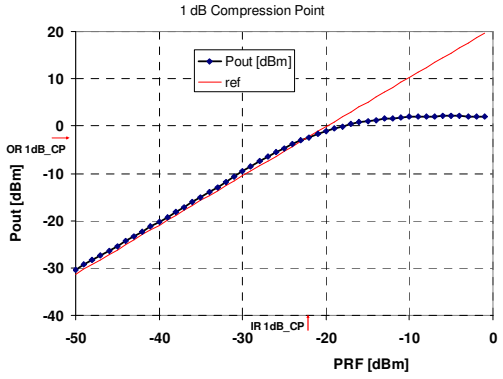

Fig. 7. P_{out} versus P_{in}.

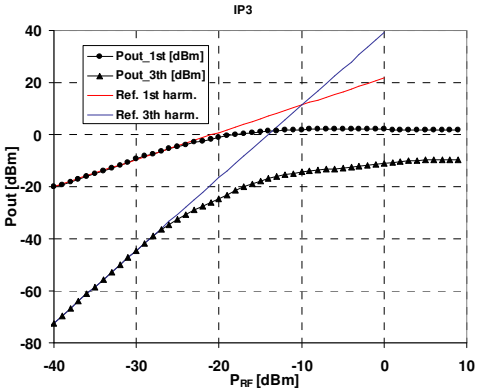

Fig. 8. Two-tone test IP3.

The prototype, whose die photograph is presented in Figure 9, is currently under experimental tests. The performance measurements are in progress and should be available for the presentation. To conclude, one must notice that the proposed circuit has been designed to match, in a near future work, the inputs of a double converter image-rejection mixer with integrated oscillator (to be reported soon).

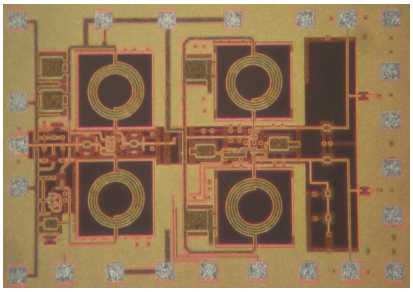

Fig. 9. LNA/Balun die photograph.

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