Single Stage Techniques for Power Factor Correction

Hugo Ribeiro[1], Beatriz Borges[2], Carlos Ferreira[3]
[1,3]Instituto de Telecomunicações, Instituto Politécnico de Tomar, Tomar, Portugal, hugo@ipt.pt; cferreira@ipt.pt
[2]Instituto de Telecomunicações, Instituto Superior Técnico, Lisboa, Portugal, mbvb@lx.it.pt

***Abstract* - Medium and high power switch mode power supplies SMPS (>500W) used in telecommunications stations are normally based on the full-bridge DC-DC converter with isolation transformer. According to the transistors states, the full-bridge converter allows four different switching sates which can be used to control the output voltage of the SMPS, and to perform the power factor corrector (PFC) function simultaneously. This paper presents the techniques and the control strategies used to guarantee the control of both conversion process, i.e., output voltage regulation and input current wave shaping to provide PFC, previously referred. Experimental results of two single-stage DC-DC full-bridge topologies with PFC are also presented, in order to verify their higher performance.**

***Key words* - Single stage power factor correctors, full-bridge converters, low distortion input current, input current shaping.**

I. INTRODUCTION

The full-bridge converter with isolation transformer is often used in telecommunications energy applications, namely in medium or high power SMPS. In order to comply with standards, the input current of a SMPS must present low distortion, i.e. it must be near sinusoidal. This requirement is achieved with an input converter, typically a boost converter [1]. Fig.1 presents a two stage SMPS with an input boost for PFC. As an example, if considered an efficiency of 90% in each conversion stage, the global system efficiency would be reduced to 81%.

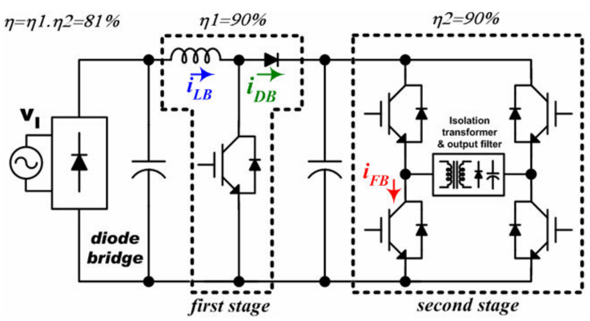

Fig.1. Two Stages SMPS with PFC.

Therefore, the association of the input boost with the full-bridge DC-DC converter, as presented in Fig.1 results in a two stages converter system with the inherent drawbacks: high cost and low efficiency. In order to solve this problem some authors introduced single stage (SS) topologies and important concepts, [2-3], based on the flyback or forward DC-DC single ended converters for low power applications, <250W.

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However, when considering high power applications, the voltage and current ratings of the power transistor and diodes increase considerably, turning this solution unsuitable for high power, due to the cost rise [4]. To overcome the referred power limitation of those topologies, SS full-bridge topologies, capable of power factor correction, galvanic isolation and regulation of the output variables have been proposed recently, [5-9]. Accordingly, the authors have recently developed new SS topologies that also present very good performance [10-11].

The proposed paper has the objective of describing the SS techniques used in the existing topologies and introduce a generalized control technique valid for full-bridge SS converters with sinusoidal input current. In order to verify the theoretical concepts, experimental results of a SS topology, derived from ones existing, is also presented.

II. SINGLE STAGE TECHNIQUES FOR FULL-BRIDGE TOPOLOGIES

In a full-bridge SS topology the unique transistors used are the bridge transistors, meaning that the input boost transistor function must be realized by one of the bridge transistors, i.e. it is necessary that the same transistor will realize both functions: the boost and the full-bridge functions. Fig.2 shows different switch cells where it is possible to share the boost current, i_{LB}, and the full-bridge current, i_{FB}.

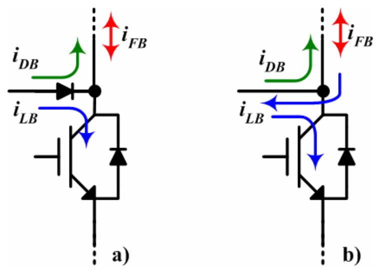

Fig.2. Switching cells: a) cell A - unidirectional current in the input inductor; b) cell B - bidirectional current in the input inductor.

In cell B the current, i_{LB} can flow in both directions, however in cell A, due to the presence of the diode, the current i_{LB} only can flow in one direction. As it will be seen further this characteristic allows obtaining a better regulation of the input current; however a lower efficiency is expected. Fig. 3 shows two SS topologies (***Top.I*** and ***Top.II***) that use the switching cells presented in Fig.2. Both topologies provide two input boost converters making use of the two low side transistors.

Each input inductor together with the lower side transistor and upper side diode (L_1, T_1, D_1 or L_2, T_2, D_2) may perform the function of a boost converter. Consequently, it is possible to control the conduction times of transistors T_1 and T_2, in order to maintain each inductor current proportional to the input voltage (rectified mains voltage). Each boost converter charges the storage capacitor C_F, at a voltage higher than the peak value of the rectified input voltage. The energy transfer from the storage capacitor C_F to the secondary of the transformer is performed by the simultaneous conduction of transistors T_1 and T_4, or T_2 and T_3.

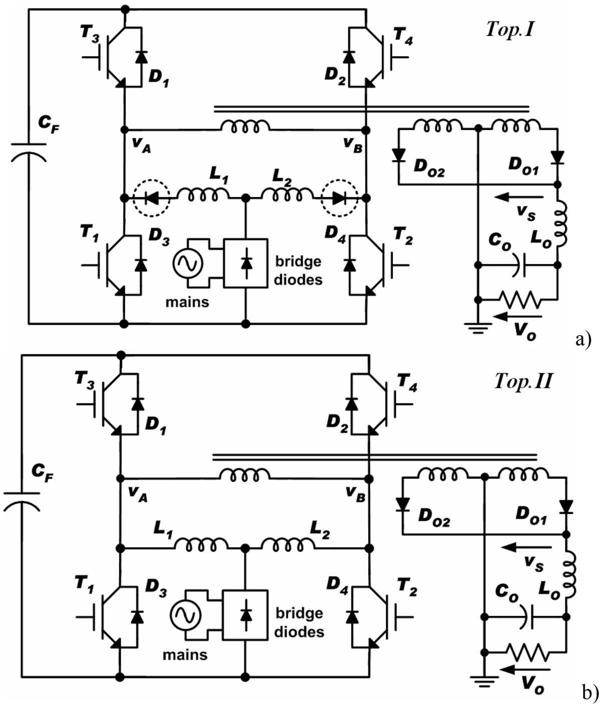

Fig. 3. SS topologies: a) with cell A; b) with cell B.

As any other full-bridge converter, the circuits have four states in each operating period accordingly to the conduction states of the two pairs of switches, as presented in Table I:

TABLE I
POWER TRANSISTORS' SWITCHING STATES

T_1 / T_3	T_2 / T_4	$v_P = v_A$-v_B	state/time	i_{L1}	i_{L2}
ON/OFF	ON/OFF	0	S_{00}/t_{00}	↑	↑
ON/OFF	OFF/ON	$-V_{CF}$	S_{01}/t_{01}	↑	↓
OFF/ON	OFF/ON	0	S_{11}/t_{11}	↓	↓
OFF/ON	ON/OFF	$+V_{CF}$	S_{10}/t_{10}	↓	↑

Where v_A and v_B are the collector voltages of transistors T_1 and T_2, v_P the voltage in the transformer primary and $t_{00} + t_{01} + t_{11} + t_{10} = T_S$, the switching period.

In continuous conduction mode (CCM), the full-bridge conversion transfers energy from storage capacitor C_F to the output, and the relation between voltages in CCM is:

$$V_O = V_{CF} \cdot D_O / n \tag{1}$$

where n is the transformer turns ratio. The duty ratio D_O for the conversion of the capacitor voltage to the output voltage is:

$$D_O = 2 \cdot t_{01}/T_S = 2 \cdot t_{10}/T_S \tag{2}$$

The control strategy for the input currents is to select between the states S_{00} and S_{11} during the time intervals where $v_P = 0$. By adopting S_{00} both inductor currents increase. On the contrary, if adopting S_{11} both currents will decrease. The conduction time t_{01} must be equal to t_{10} in order to avoid transformer saturation. Consequently, during a switching period the active time intervals t_{01} and t_{10} are imposed by the output voltage regulation, and cannot be changed in order to provide input current wave shaping.

The duty ratio for boost operation, D_I, increases with the state S_{00} and decreases with the state S_{11}, when $v_P = 0$, time interval t_C marked in Fig. 4. During a switching period, the total time interval where $v_P = 0$ is $(1 - D_O) \cdot T_S$ and is imposed by the regulation of the output voltage. Selecting the appropriate states (S_{00} or S_{11}) for those time intervals where $v_P = 0$, a discrete variation of the input-duty ratio is obtained:

$$D_{Imax} = \frac{2 \cdot t_{00} + t_{10}}{T_S} = \frac{2 \cdot t_{00} + t_{01}}{T_S} = 1 - \frac{D_O}{2} \tag{3}$$

$$D_{Imin} = \frac{t_{10}}{T_S} = \frac{t_{01}}{T_S} = \frac{D_O}{2} \tag{4}$$

The above equations show that D_I and D_O are independent variables, with the following restriction:

$$D_O / 2 \le D_I \le 1 - D_O / 2 \tag{5}$$

This condition is the unique restriction to the compatibility of the two independent control processes of the input current and of the output voltage. Fig. 4 show the most relevant waveforms that allow identifying the two duty ratios, D_I and D_O. The evolution of the current in the input inductances, L_1 and L_2 is also presented.

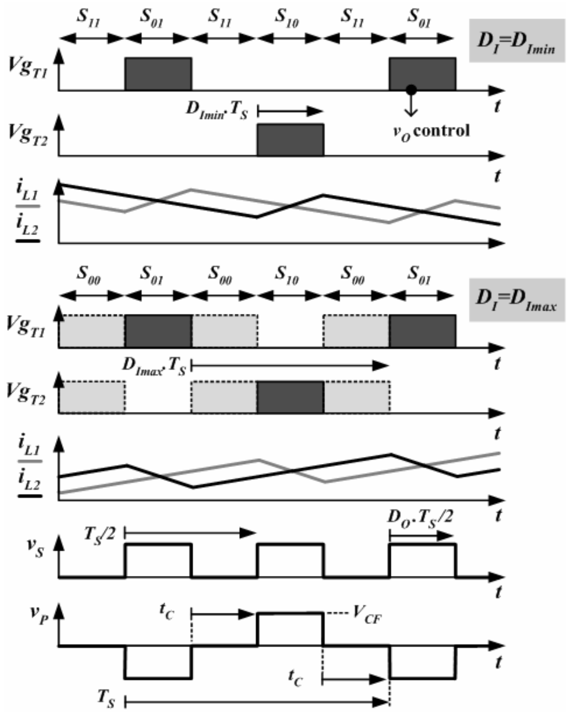

Fig. 4. Typical waveforms of the SS topology.

III. INPUT CURRENT EVOLUTION

When the mains voltage is low the input boosts cannot generate a sufficient value of *di/dt*, to follow the reference, which results in zero current cross distortion (Fig.5). It is possible to define an input current reference control angle, α (equal for the two topologies), that, for values of ωt higher then α, the two input boosts can generate high values of *di/dt* and can reach the reference current rapidly:

$$\alpha = \omega t = sin^{-1}\left(\frac{V_{CF}}{V_I}\cdot\frac{D_O}{2}\right) \tag{6}$$

For Topology I, during the angular interval $\omega t<\alpha$ the two input boosts operate in discontinuous conduction mode, DCM, and the input current presents a low value evolution. Eq.(7) represents the average input current evolution ($L=L_1=L_2$):

$$\langle i_I\rangle_{TS} = \frac{V_I\cdot sin(\omega t)\cdot D_O^{\ 2}\cdot T_S}{4\cdot L}\cdot\frac{V_{CF}}{V_{CF}-V_I\cdot sin(\omega t)} \tag{7}$$

Topology II, is very similar to the topology I, and is obtained from the last by eliminating the two boost series diodes with the objective of improving, the boost efficiency. The removal of the two diodes allows the current in each input inductor to flow in both directions. Due to this characteristic, the topology has input zero current, if $\omega t<\alpha$.

During the angular interval $\alpha<\omega t<\pi-\alpha$ the input current is controlled. For higher angles, $\omega t>\pi-\alpha$ the two boost converters cannot generate sufficient *di/dt* and the input current evolution starts to have an error, relatively to the reference current, Fig. 5.

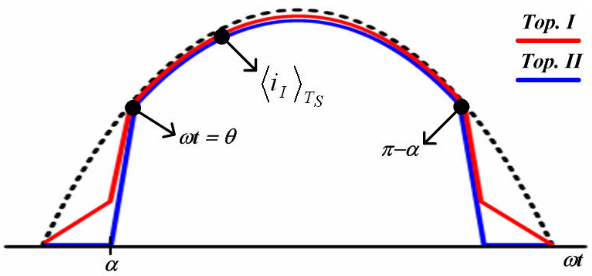

Fig. 5. Linearized input current evolution.

The angle $\omega t=\theta$ marked in Fig.5 corresponds to the angle where the input current reaches the reference. During the interval $\alpha<\omega t<\theta$ both boost converters will operate with $D_I=D_{Imax}$ constantly in order eliminate the current error. The influence of the L value in the angular interval $\alpha<\omega t<\theta$ is analyzed further.

IV. DESIGN CRITERIA AND OPERATING LIMITS

To guarantee the boost operation during all the mains period, the voltage on the C_F capacitor must verify the condition (8):

$$V_{CF}\geq V_{Imax}\cdot\frac{1}{1-D_{Imin}} \Leftrightarrow V_{CF}\geq V_{Imax}\cdot\frac{2}{2-D_O} \tag{8}$$

To guarantee low THD in the input current, the angle, α, must be small. The definition of maximum value of α, α_{max} and the ratio V_{Imax}/V_{Imin} introduces a D_O restriction (9). In (9) it is assumed $V_{CF}=V_{CF\,min}$, which also reduces α.

$$D_O\leq\frac{2\cdot sin(\alpha_{max})\cdot V_{Imin}}{V_{Imax}+sin(\alpha_{max})\cdot V_{Imin}} \tag{9}$$

Considering CCM operation of the output filter, the output duty ratio is constant. Therefore, the minimum input duty ratio, D_{Imin}, imposes a minimum input power, P_{Imin}. Neglecting the converter losses, this minimum input power must be absorbed by the load to guarantee the capacitor voltage, V_{CF}, control. The low load operation is guaranteed considering the operation of the output filter in DCM. When the DCM starts the output duty ratio reduces with the load reduction and the P_{Imin} reduces too. To avoid that, the output filter operates in DCM for large loads; the input inductances of the topologies are designed considering a minimum input power at which the output filter operates in CCM.

$$L\cong\frac{V_{Imax}^{\ 2}\cdot D_O\cdot T_S}{4\cdot P_{Imin}} \qquad \text{Topology I} \tag{10}$$

$$L\cong\frac{V_{Imax}^{\ 2}\cdot D_O\cdot T_S}{4\cdot P_{Imin}}\cdot\left(\frac{1-D_O}{2-D_O}\right) \qquad \text{Topology II} \tag{11}$$

Analyses of the input current during the angular interval, $\alpha<\omega t<\theta$ allows to demonstrate that if the L value is obtained considering $P_{Imin}>0{,}1\cdot P_{Imax}$, this angular interval, can be neglected.

To guarantee the V_{CF} control it is necessary to verify that $P_{Imin}<P_O/\eta$, condition that defines the L_O restriction:

$$L_O<L\cdot\frac{V_O^{\ 2}}{\eta\cdot V_{Imax}^{\ 2}}\cdot\left(\frac{1-D_O}{D_O}\right) \qquad \text{Topology I} \tag{12}$$

$$L_O<L\cdot\frac{V_O^{\ 2}}{\eta\cdot V_{Imax}^{\ 2}}\cdot\left(\frac{2-D_O}{D_O}\right) \qquad \text{Topology II} \tag{13}$$

The design of the capacitor C_F is obtained according to its voltage ripple, ΔV_{CF}, considering the maximum output power and the expected efficiency η:

$$C_F>\frac{P_{O\,max}}{V_{CF}\cdot\omega\cdot\Delta V_{CF}\cdot\eta} \tag{14}$$

The value for the output capacitor, C_O, is achieved by considering the output voltage ripple in CCM.

IV. INPUT CURRENT AND OUTPUT VOLTAGE CONTROLLER

For the input current control, a hysteretic comparator is used to compare the reference current with the input current, i_I, and to select the appropriate states S_{00} or S_{11} to achieve the input current wave shaping.

A low cost analogue multiplier, AD633, is used to define the current reference, which is proportional to the error in V_{CF} voltage capacitor. For the output voltage regulator a modulator in voltage mode is used. An additional logic circuit generates the gate signals, Fig. 6. The variable G_S marked in Fig. 6 corresponds to the Hall Effect sensor gain. In the experimental results, a hysteretic current of 0,3A was considered.

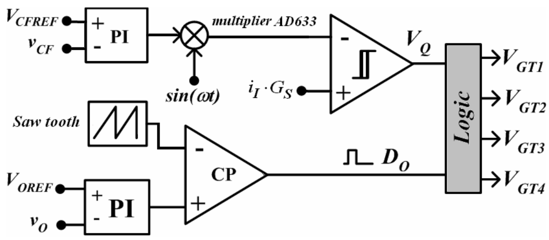

Fig. 6. Input current controller and output voltage controller.

V. EXPERIMENTAL RESULTS

To obtain experimental results of the two topologies a prototype has been developed with the following specifications: $L=5mH$; $P_O=400W$; $V_O=48V$; $T_S=40\mu s$; $n=3.75$; $V_I=230V_{ef}$-10% (worst case), $D_O=0.4$; $V_{CF}=450V$; $\alpha_{max}=20^o$; $C_F=500\mu F$; $\Delta v_{CF\,max}=10V$.

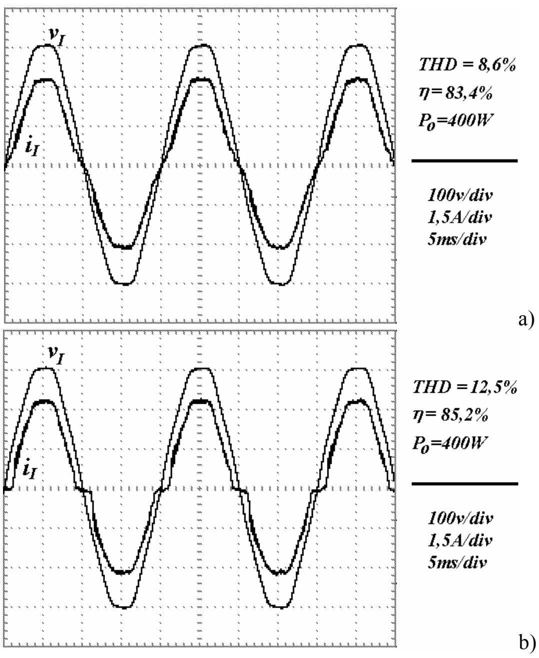

Fig. 7. Input current and voltage waveforms: a) Topology I; b) Topology II.

As expected, the Topology II presents a higher THD when compared with the Topology I; however, it still satisfies the standards by a wide margin. The higher THD observed in Topology II is the result of the bidirectional current in the two input inductors which results in zero cross current distortion. However the topology uses few components and presents high efficiency which makes it suitable for high power applications.

VI. CONCLUSIONS

The paper introduces and describes the characteristics of two switching cells used in SS, full-bridge topologies. The techniques used to provide the input current shaping and output voltage, are totally explained in the paper. This analysis includes the circuit limitations and the interdependence between the two conversion processes. The achieved design equations are also presented.

In order to verify the proposed techniques and the influence of the switching cells in the operation of SS topologies, illustrative experimental results are presented.

The SS topologies introduced in this paper are the most suitable to introduce the switching cells and the control techniques, however, further work that involves the research of new topologies in order to improve their performance is being carried out by the authors.

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