Effects of the Noise Spikes on the Digital Symbol Synchronizers

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Abstract

This work study the effects of the noise spikes on the digital symbol synchronizers.

In these synchronizers, we distinguish two types namely the combinational digital symbol synchronizers and the sequential digital symbol synchronizers.

The combinational type has a phase detector without intern memory whereas the sequential type has a phase detector with intern memory.

The objective is to study the various synchronizers output jitter UIRMS (Unit Interval Root Mean Square) versus the input SNR (Signal to Noise Ratio).

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

This work study the effects of the noise spikes on the digital symbol synchronizers.

To explain this issue, in the digital symbol synchronizers, we consider two types namely the combinational symbol synchronizers and the sequential symbol synchronizers. The first has a phase detector without intern memory whereas the second has a phase detector with intern memory [1, 2, 3, 4].

To explain better the issue, in the combinational type, we consider only the previous manual adjust version, but in the sequential type, we consider the previous manual adjust version and the automatic auto adjust version [5, 6, 7, 8, 9].

The combinational type output depends only of the input signal, but the sequential type output depends of the input signal and also of his state [10, 11, 12].

Fig.1 shows as a noise spike can be confounded with the one data conducting to the error state.

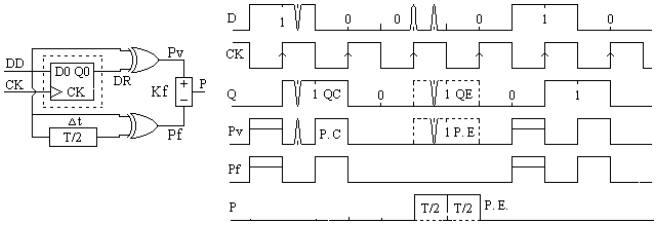

Fig.1 Contribution of the error state to the jitter increasing

The output Pv, that determines the jitter, is function of the input D (signal corrupted by noise) and also of the flip flop state Q which can be correct QC or erroneous QE.

The waveshapes show that the input signal is processed normally in the correct state QC and only during one period T is processed in the error state QE.

The sequential type output depends on the input signal and system state. Then, the error state QE changes incorrectly the pulse PV what causes a great jitter increment.

The fixed pulse Pf creates a DC component equal to the variable pulse PV in equilibrium synchronism.

Following, we present the combinational digital symbol synchronizers only in the manual version.

Next, we present the sequential digital symbol synchronizers in the manual and automatic versions.

After, we present the design and tests of the synchronizers.

Then, we present the results.

Finally, we present the conclusions.

II. COMBINATIONAL DIGITAL SYNCHRONIZERS

In this type, we consider only the manual combinational digital symbol synchronizer. Its output jitter depends only of the input signal with noise [1, 2, 3].

A. Combinational digital synchronizer - manual

The input noise spikes provokes gate commutations, what affects directly the output jitter (Fig.2).

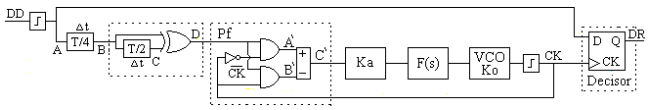

Fig.2 Manual combinational digital symbol synchronizer (cmb-m)

The phase comparator inputs (main input and VCO output) are both digital. The output is only function of the input.

Following waveshapes show the operation mode of the manual combinational digital synchronizer (Fig.3).

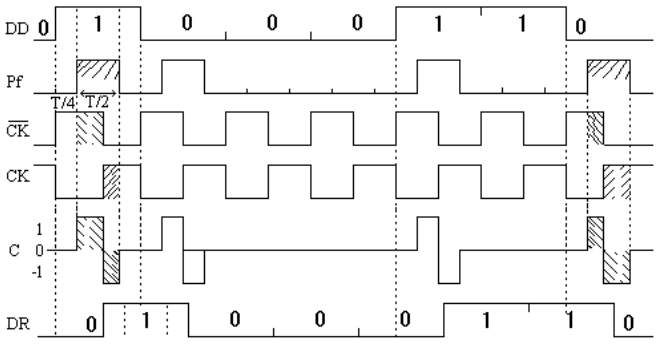

Fig.3 Waveshapes of the manual combinational synchronizer

When occurs a data transition is open a window pulse, that observes the clock phase, correcting it if necessary.

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III. SEQUENTIAL DIGITAL SYNCHRONIZERS

In this type, we present two versions namely the manual sequential digital symbol synchronizer and the automatic digital symbol synchronizer. Their output jitter depends on the input signal with noise and of the synchronizer state [4].

A. Sequential digital synchronizer - manual

The input noise spikes affects directly the output jitter and at same time causes the error state that contributes also to the output jitter increasing (Fig.4).

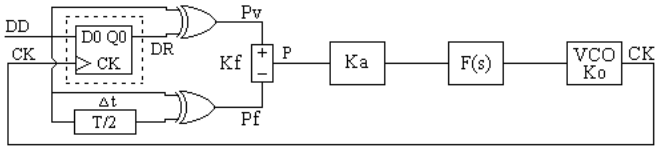

Fig.4 Manual sequential digital symbol synchronizer (seq-m)

The phase comparator inputs (main input and VCO output) are both digital. The output is function of the input and error state. Only one flip flop contributes to the error state.

Following waveshapes show the operation mode of the manual sequential digital synchronizer (Fig.5).

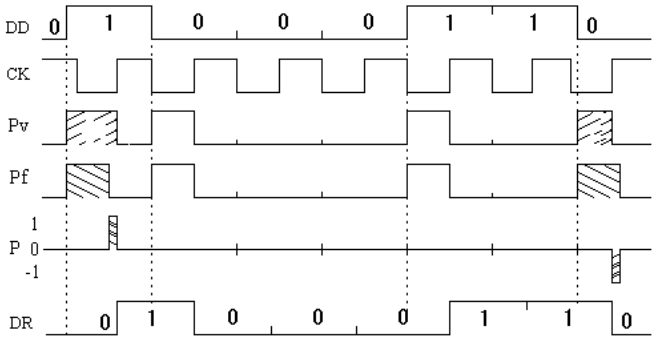

Fig.5 Waveshapes of the manual sequential synchronizer

When occurs a data transition is made a comparation, at the same time, between the variable pulse Pv and the fixed pulse Pf. The difference area is the error signal.

B. Sequential digital synchronizer - automatic

The input noise spikes affects directly the output jitter and also causes the error states that greatly contributes to the output jitter increasing (Fig.6).

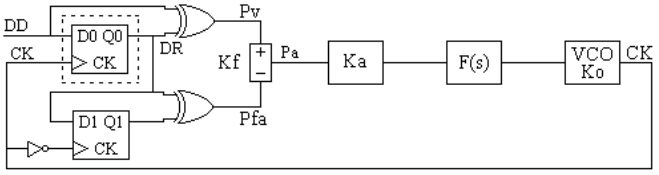

Fig.6 Automatic sequential digital symbol synchronizer (seq-a)

The phase comparator inputs (main input and VCO output) are both digital. The output is function of the input and error state. Two flip flops contribute to the error state.

Following waveshapes show the operation mode of the automatic sequential digital synchronizer (Fig.7).

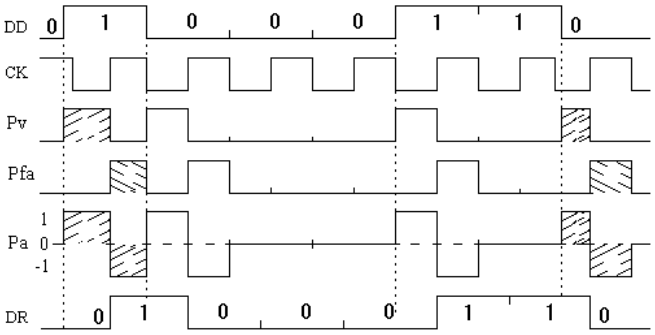

Fig.7 Waveshapes of the automatic sequential synchronizer

When occurs a data transition is made a comparation, at different time, between the variable pulse Pv and the fixed pulse Pf. The difference area is the error signal.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling $\Delta\tau=1/Samp$, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi$ (3)

For the hybrid synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi$ (4)

For the combinational synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)
$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5)

For the sequential synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)
$(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.
For analog PLL the jitter is
$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$
For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

The following figure (Fig.8) shows the setup that was used to test the various synchronizers.

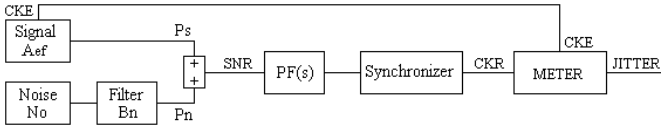

Fig.8 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.9).

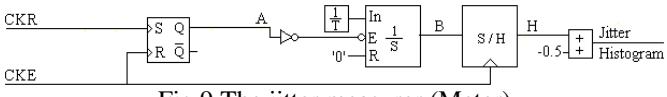

Fig.9 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter UIRMS - input SNR) for the three digital symbol synchronizers.

Fig.10 shows the jitter-SNR curves of the manual combinational digital synchronizer (cmb-m), manual sequential digital synchronizer (seq-m) and automatic sequential digital synchronizer (seq-a).

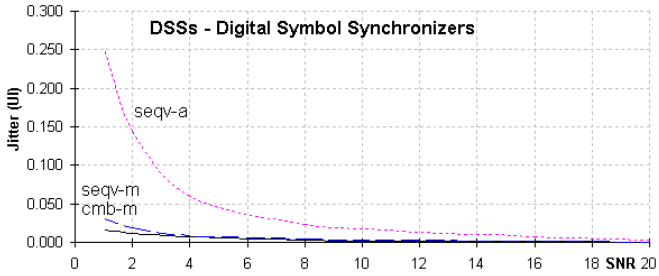

Fig.10 Jitter-SNR curves of the three synchronizers(c-m, s-m, s-a)

We verify, that generally the output jitter UIRMS diminishes exponentially with the input SNR increasing.

For high SNR, the three curves tend to be equals. However, for low SNR the manual combinational (cmb-m) is the best, followed of the manual sequential (seq-m) and the automatic sequential (seq-a) is the worst.

V. CONCLUSIONS

We studied three digital symbol synchronizers, namely the manual combinational, the manual sequential, and the automatic sequential.

After, we tested their output jitter UIRMS as function of the input SNR.

We observed that, generally, the jitter diminishes almost exponentially with the SNR increasing.

We verified that for high SNR, the jitter of the three digital synchronizers is similar. This is comprehensible because the noise is similarly ignored by the digital gates noise margin.

However, for low SNR, the manual combinational is the best, because only contributes to the jitter the input noise spikes. Following is the the manual sequential, because contributes to the jitter the input noise spikes and also the error state of one flip flop. The automatic sequential is the worst, because contributes to the jitter, the input noise spikes and also the error state of the first flip flop that is still propagated to the error state of the second flip flop.

So, the combinational type has only the contribution of the input, whereas the sequential type has the contribution of the input and also the error state that aggravates the jitter.

VI. ACKNOWLEDGMENTS

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