One Cycle Control Design for High Performance Two-Level Power Inverters

Carlos Ferreira[134], Beatriz Borges[24], Luís de Sá[34]
[1]Instituto Politécnico de Tomar, Estrada da Serra, Quinta do Contador, 2300-313 Tomar, Portugal
Phone: +351- 249328100, Fax: +351- 249 328 186, e-mail: cferreira@ipt.pt
[2]Instituto Superior Técnico, [3]Universidade de Coimbra, [4]Instituto de Telecomunicações

Abstract — **Constant frequency One Cycle Control (OCC), as proposed by Smedley [1], is a powerful method for controlling switching power converters. The dimensioning of this control method is not of common knowledge and as far as the authors know, has not yet been published for two level AC output converters. This paper describes OCC for two level switched power converters. Its instability problems and solutions are analysed and dimensioning equations are deducted. This technique allows the construction of stable high bandwidth power converters with low output THD and high PSRR. The obtained analytical expressions are compared with experimental results, showing good correlation.**

I. INTRODUCTION

Pulse Width Modulation (PWM) is traditionally used in constant frequency power supply's converters. The typical switched AC output converter consists in a modulator that converts the input signal into a PWM signal (by comparison to a saw tooth or triangular wave), a bridge or half bridge power converter configuration and a low pass filter to "demodulate" the output signal.

To achieve sufficient PSRR and low THD of the output signal a linear negative feedback loop is often used. In order to assure system stability, linearised models have to be studied and the system "tuned". This limits the improvements achieved on PSRR, output impedance, THD, gain flatness, bandwidth, etc. So it is highly desirable to have a general control method, like OCC, that allows the construction of stable high bandwidth power converters with low output THD and high PSRR [2].

II. ONE CYCLE CONTROL

A. Unipolar OCC

OCC principle is very simple. The aim of the control system is to attain an average output level proportional to the reference signal, OCC performs this control action in each switching period, T_s.

Let us consider the buck converter represented in Fig. 1.

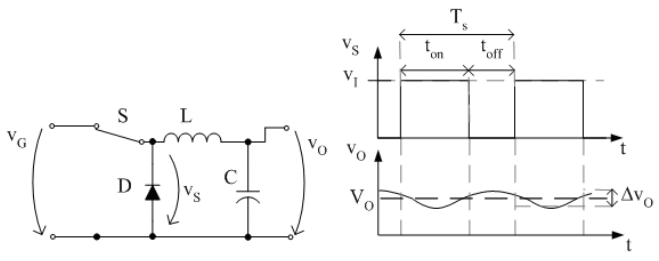

Fig. 1. Buck converter.

The input voltage is a DC voltage, v_G, the converter is formed by the switch, S and the diode, D. The inductor, L, composes an LC low pass filter in conjunction with capacitor C. Let us consider that the converter operates with a constant PWM frequency, in continuous conduction mode and with an output voltage v_O.

The output voltage is the sum of the switched voltage average and the ripple voltage at the switching frequency, f_s.

Considering the duty-cycle δ as the relation between the on time of the switch, t_{on}, and T_s, the switched voltage average in a switched cycle is:

$$\langle v_S \rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} v_S\,dt = \frac{1}{T_s}\int_0^{\delta T_s} v_G\,dt. \qquad (1)$$

To achieve the desired average output voltage, a circuit to control t_{on} is needed.

Considering that at the start of the analysis the switch is turned on, then the control system only has to provide the instant when the switch has to be turned off (t_{on}). The objective is to attain an average value proportional to the reference v_{REF}, as expressed in equation (2):

$$\frac{1}{T_s}\int_0^{t_{on}} v_G\,dt = v_{REF}\,. \qquad (2)$$

The OCC basic concept is to "force" the average value of v_S to be exactly equal to the reference value in each switching cycle; it does that by integrating the output voltage and comparing it to the reference voltage. Fig. 2 presents the OCC concept applied to a real implementation of the Fig. 1 converter (considering an integrator with unitary time constant) [1].

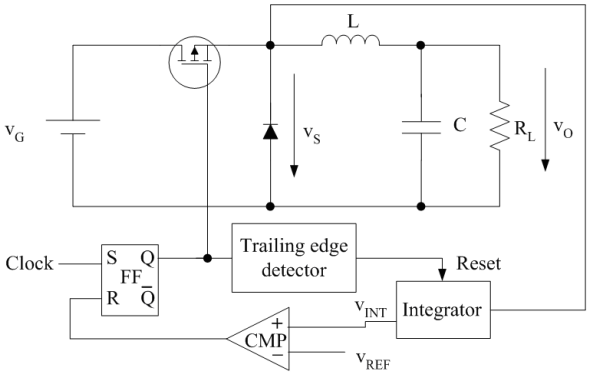

Fig. 2. Buck converter with OCC control.

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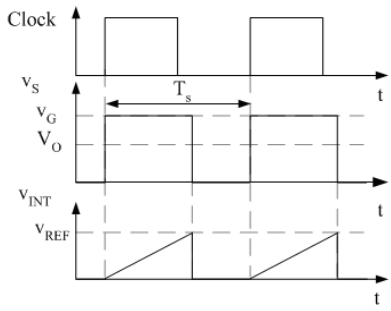

Fig. 3. OCC signals.

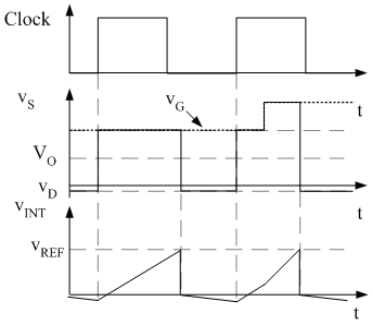

Fig. 4. OCC signals in a non-ideal system.

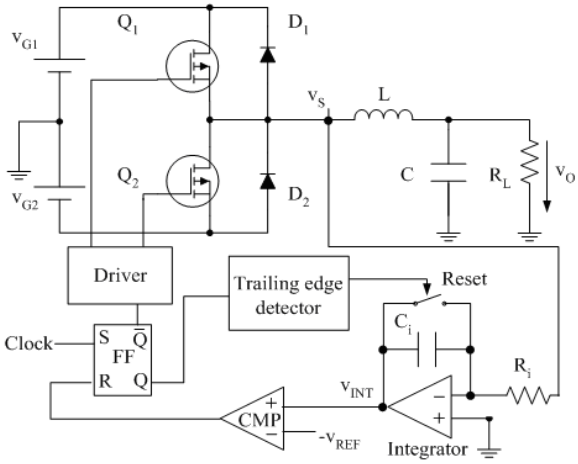

Fig. 5. OCC applied to a half-bridge converter.

The OCC signals are represented in Fig. 3. In order to assure constant frequency operation an external clock is needed. The leading edge of the clock signal initiates the system by setting (S) a Set-Reset Flip-Flop (FF) which forces the transistor to turn on.

The v_S voltage equals the v_G value and the integrator output voltage starts growing. When it reaches the reference voltage, the comparator (CMP) resets (R) the FF, turning off the switching transistor and resetting the integrator.

Turning off the transistor forces the diode to conduct, and v_S becomes zero (ideally) until a new clock pulse reinitiates the system. This type of control assures the law expressed in equation (2).

In practical non-ideal systems, voltage drops in the transistor and diode or v_G voltage variations are compensated by adjusting transistor's t_{on}, as represented in 4. This compensation is also valid for any other perturbations in the converter, namely switching times delays or transients.

An important characteristic of OCC derives from the fact that the integrator reset's at the beginning of each control cycle, preventing the transmission of information between consecutive cycles and leading to an inherently stable system [3]. In traditional linear negative feedback, information transmission between successive cycles provokes delays in the feedback path, leaving to possible oscillation which does not happen with OCC (when the output filter is not considered) [2].

B. Bipolar One Cycle Control

In the aforementioned circuit the output voltage is unipolar and could only take values between 0 and v_G.

The circuit represented in Fig. 5 is an extension of the OCC circuit to a half-bridge converter that allows bipolar output voltage swing [4]. The integrator with reset is made with an Operational Amplifier and a reset switch. The driver block commands the transistor's state based on the FF output. Table I describes the operating sequence of events and Fig. 6 the typical produced waveforms.

Table I
Bipolar OCC event sequence

Interval	Description
$[t_0, t_1]$	At the leading edge of the clock signal the FF is set. The FF output actuates the driver input, provoking Q_2 actuation (on) and Q_1 cut (off). v_S voltage is $-v_{G2}$, the output's integrator voltage starts growing.
$[t_1, t_2]$	Output's integrator voltage reaches $-v_{REF}$, provoking comparator's output transition to high logic level: "1". The comparator's output transition causes the FF to reset, making the driver to turn Q_1 on and Q_2 off. Simultaneously the integrator's output voltage is resetted. v_S voltage is v_{G1}, the output's integrator voltage starts decreasing.
$[t_2, t_3]$	In the leading edge of the clock the FF is set and the cycle continues…

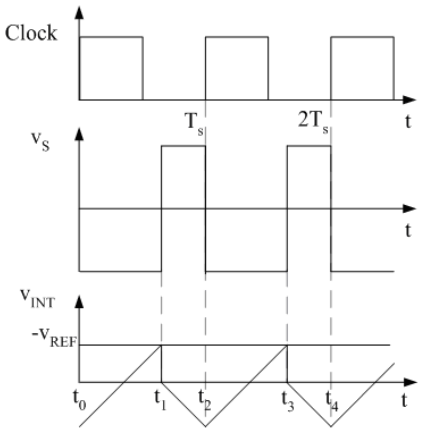

Fig. 6. Typical waveforms of the bipolar OCC circuit.

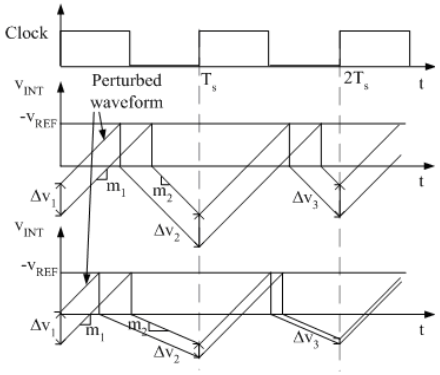

Fig.7. Integrator's error propagation.

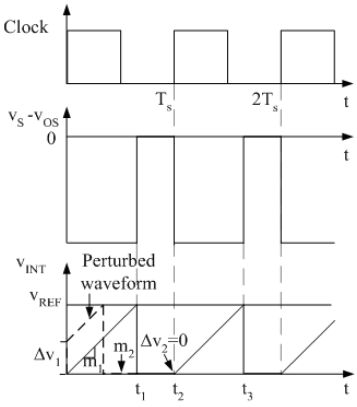

Fig. 8. Compensated waveforms.

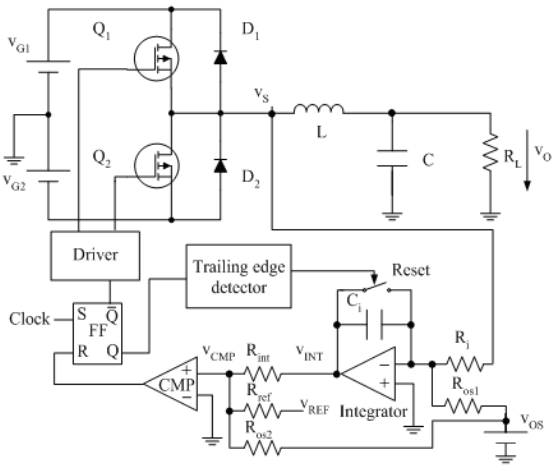

Fig. 9. Compensated OCC circuit.

The control law could be represented as:

$$\int_{t_1}^{t_3} \frac{v_S}{R_i C_i} dt = v_{REF}. \qquad (3)$$

If f_s is much higher than the maximum frequency of the signal to reproduce, v_{REF}, it could be concluded that between two successive switching periods the reference signal is almost constant, being similar in the intervals $[t_0, t_1]$ and $[t_2, t_3]$, and also in $[t_1, t_2]$ and $[t_3, t_4]$.

The v_S average in T_s, $\langle v_S \rangle_{T_s}$, could be represented by:

$$\langle v_S \rangle_{T_s} = \frac{1}{T_s}\int_{t_0}^{t_2} v_S dt = \frac{1}{T_s}\int_{0}^{T_s} v_S dt. \qquad (4)$$

The circuit gain, G, is the relation between $\langle v_S \rangle_{T_s}$ and v_{REF}, accordingly to equations (3) and (4) it will be:

$$\frac{\langle v_S \rangle_{T_s}}{v_{REF}} = \frac{\frac{1}{T_s}\int_0^{T_s} v_S dt}{\frac{1}{R_i C_i}\int_0^{T_s} v_S dt} = R_i C_i f_s = G. \qquad (5)$$

Although the OCC controlled unipolar circuit aforementioned in section *A* is inherently stable, the bipolar circuit has some stability issues.

Fig. 7 shows the time evolution of the integrator's voltage when it is exposed to a disturbing signal, Δv_1 [4]. Two distinct situations are analysed: in the first case v_{G1} e v_{G2} are equal, meaning that the integrators output voltage slope (m_1 and m_2) are equal (disregarding its signal); if $v_{G1}>v_{G2}$, then $m_1>m_2$.

By analysing Fig. 7 it could be seen that the error propagation depends on the integrator's voltage slope: m_1 and m_2 [4]. For $t=nT_s$, the propagated error due to Δv_1, Δv_n, is:

$$\Delta v_n = \left(-\frac{m_2}{m_1}\right)^{n-1} \Delta v_1. \qquad (6)$$

In the general half-bridge or full-bridge inverters v_{G1} and v_{G2} are equal, implying that $m_1=m_2$. Like this, the perturbation Δv_n will not disappear and there will be an oscillation at half the switching frequency.

If an offset voltage, v_{OS}, is added to the integrator's input to null m_2, the error propagation ends. To achieve this condition the added voltage has to be $-v_{G1}$. Fig 8 illustrates the obtained waveforms, showing that in this situation the Δv_1 perturbation disappears in one switching cycle [4].

The control law is now:

$$\int_{t_1}^{t_3} \left(\frac{v_S}{R_i C_i} - \frac{v_{OS}}{R_{os1} C_i} \right) dt = v_{REF}. \qquad (7)$$

In order to obtain an output switching average voltage proportional to v_{REF} a parcel has to be added to v_{REF} to null the v_{OS} contribution. Fig. 9 shows a way to do that by using a resistance network. We must now design the system such that v_{OS} disappears in equation (7).

C. Design

We consider the circuit represented in Fig. 9, where the voltages v_{G1} and v_{G2} are equal (being represented by v_G) and for the sake of simplicity, $v_G=-v_{OS}$. To avoid error transmission between successive cycles, R_i and R_{os1} values have to be equal.

By using the superposition theorem, the voltage at the input of the comparator, v_{CMP}, due to v_{INTt}, v_{REF} and v_{OS} can be calculated by summing its several contributions:

v_{INT} contribution:

$$v_{CMP1} = \frac{\frac{R_{ref} R_{os2}}{R_{ref} + R_{os2}} v_{INT}}{\frac{R_{ref} R_{os2}}{R_{ref} + R_{os2}} + R_{int}} \Leftrightarrow v_{COMP1} = \beta_1 v_{INT}; \qquad (8)$$

v_{REF} contribution:

$$v_{CMP2} = \frac{\frac{R_{int} R_{os2}}{R_{int} + R_{os2}} v_{REF}}{\frac{R_{int} R_{os2}}{R_{int} + R_{os2}} + R_{ref}} \Leftrightarrow v_{COMP2} = \beta_2 v_{REF}; \qquad (9)$$

v_{OS} contribution:

$$v_{CMP3} = \frac{\frac{R_{\text{int}} R_{ref}}{R_{\text{int}} + R_{ref}} v_{OS}}{\frac{R_{\text{int}} R_{ref}}{R_{\text{int}} + R_{ref}} + R_{os2}} \Leftrightarrow v_{COMP3} = \beta_3 v_{OS}; \qquad (10)$$

The sum of the three contributions gives:

$$v_{CMP} = \beta_1 v_{INT} + \beta_2 v_{REF} + \beta_3 v_{OS}. \qquad (11)$$

The OCC analysis is initiated at t=0. We designate t_{off} as the instant when v_S switches from v_G to $-v_G$, which coincides with time when the input voltage of the comparator reaches zero. Also, as referred before, $v_G = -v_{OS}$ and equation (7) becomes:

$$0 = \beta_1 v_{INT} + \beta_2 v_{REF} - \beta_3 v_G. \qquad (12)$$

Considering that v_{G2} is constant (with $v_{G2}=v_{G1}=v_G$) and disregarding the voltage drops in the transistor, the v_{INT} voltage at the t_{off} will be:

$$v_{INT} = \frac{1}{C_i} \int_0^{t_{off}} \frac{2v_G}{R_i} dt = \frac{2v_G}{R_i C_i} t_{off}. \qquad (13)$$

Representing t_{off} as a function of δ:

$$\begin{cases} t_{off} = T_s - t_{on} \\ \delta = \frac{t_{on}}{T_s} \end{cases} \Leftrightarrow t_{off} = T_s - \delta T_s = T_s(1-\delta). \qquad (14)$$

Equation (13) then becomes:

$$v_{INT} = \frac{2v_G}{R_i C_i f_s}(1-\delta). \qquad (15)$$

By substitution of this value in equation (12), we obtain:

$$0 = \frac{\beta_1 v_G}{R_i C_i f_s}(1+1-2\delta) + \beta_2 v_{REF} - \beta_3 v_G. \qquad (16)$$

For an half-bridge the relation between v_O and v_G is: $v_O=(2\delta-1)v_G$. Substituting this value in equation (16) gives:

$$0 = \left(\frac{\beta_1 v_G}{R_i C_i f_s} - \frac{\beta_1 v_O}{R_i C_i f_s} \right) + \beta_2 v_{REF} - \beta_3 v_G. \qquad (17)$$

To avoid a DC component in the output due to v_G, the following two solutions are possible:

$$v_G = 0 \vee \beta_1 = \beta_3 R_i C_i f_s. \qquad (18)$$

The $v_G=0$ solution is not relevant. The other solution is a circuit dimensioning equation.

Using (18) equation (17) becomes:

$$0 = \beta_2 v_{REF} - \frac{\beta_1 v_O}{R_i C_i f_s}. \qquad (19)$$

This conduces to another design equation, corresponding to the circuit gain, G:

$$\frac{v_O}{v_{REF}} = \frac{\beta_2 R_i C_i f_s}{\beta_1} = G. \qquad (20)$$

III. EXPERIMENTAL RESULTS

A switching converter in half bridge configuration was built using an IR2110 driver and IRFB41N15D transistors, $\pm v_G = \pm 32V$, $f_s=333kHz$ and a low pass filter at the output. The OCC components were designed by means of the deducted equations, giving a theoretical gain of 18.79 (due to the available component values).

Fig. 10 a) shows the measured experimental OCC signals. The experimental diagrams are referred (from top) to: clock signal, v_S, v_{INT} and v_O. Fig. 10 b) shows v_{REF} and v_O at 10kHz input frequency and allows us to calculate a practical gain of 18.9, very close to the predicted value. The measured THD is always lower then 0.5% (1W, 20-20kHz, 8Ω load).

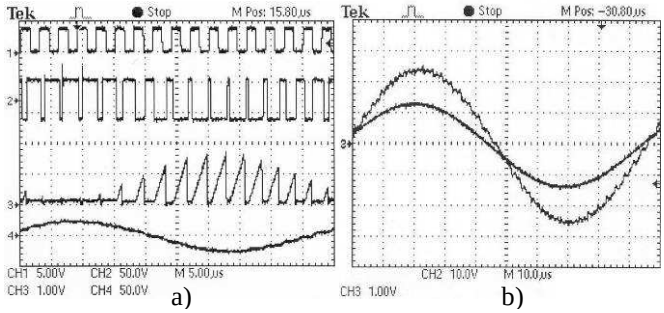

Fig. 10 a) OCC signals, b) Filtered output signal.

IV. CONCLUSIONS

This paper introduces the OCC control target at converters capable of producing unipolar and bipolar output voltages, operating with two level switching output. The design equations, for the bipolar case, have been deducted based on the superposition theorem applied to the OCC circuit. A prototype has been built using the design method developed in this paper. Experimental data is in accordance with the design, showing that this technique allows the construction of stable high performance converters. Also, the design procedure proved to be simpler then the linear feedback case.

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