

A 2.4GHz CMOS Integer-N Phase-Locked Loop

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Abstract — This paper presents the study, design and experimental characterization of a 2.4GHz Integer-N phase-locked loop. Several building blocks are studied, with more emphasis on the voltage controlled oscillator and frequency divider. Three circuits were tested, the isolated oscillator, the oscillator loaded with the frequency divider and the phase-locked loop. All the circuits were designed using the Austria Micro Systems CMOS 0.35 μ m 2P4M technology. The voltage supply is 2.6V. The circuits were tested using chip-on-board technique.

I. INTRODUCTION

With the *Global System for Mobile Communications* (GSM) and more recently with the *Wireless Local Area Network* (WLAN), the wireless communications at 2.4GHz and 5.2GHz have a big market slice comparing with the cable communications. The high working frequency demands that the project of these integrated circuits is made in short channel technologies, such as, the *Complementary Metal-Oxide Semiconductor* (CMOS) and *Bipolar CMOS* (BiCMOS).

Therefore, during the project it's mandatory to establish direct relations between concepts like Signal-to-Noise Ratio (SNR), *Bit Error Rate* (BER), *Error Vector Magnitude* (EVM) and the electrical parameters of the several devices that compose the circuits to improve phase noise, power and consumption [1].

The synthesizer has a major role in transceiver systems because it offers a stable signal whose frequency is integer or fractional related to a reference value. Because the synthesizer frequency can be changed, it is possible to select the wanted channel [1] [2].

This paper presents the design of an integer-N phase-locked loop (PLL) for 2.4GHz applications implemented with the 0.35 μ m 2P4M CMOS technology from *Austria Micro Systems* (AMS). The N has a fixed value of 32.

Section II presents the project of the building blocks used on the PLL such as the *Voltage Controlled Oscillator* (VCO), the frequency divider and the charge pump. In section III measurement results are shown and finally in section IV some conclusions are made.

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II. PLL BUILDING BLOCKS

The PLL reported in this paper has the topology shown in Figure 1.

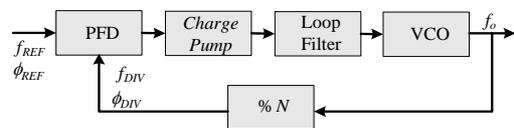


Fig. 1. Integer-N PLL topology.

These blocks are a VCO, a modulus N divider, a *Phase-Frequency Detector* (PFD), a *charge pump* and a loop filter. The output frequency is given by (1)

$$f_o = N \cdot f_{REF} \quad (1)$$

were f_{REF} is the reference frequency. The N factor is the division ratio which, in this particular circuit, has a fixed value of 32. Therefore for a 2.4GHz output frequency, f_{REF} is 75MHz. Following the design of the PLL building blocks will be described.

A. The 2.4GHz LC VCO

The VCO design is made with the technique described in [3], where a generic VCO circuit is decomposed in a passive circuit (LC tank) and an active circuit (cross coupled differential pair). At 2.4GHz the chosen tank inductor has a 5nH value, 18 Ω series resistance, and a 4.17 quality factor value [1].

The dimensions of the MOS varactors (M_1 , M_2) are obtained by simulation of the LC tank circuit and taking into account an excess capacitance from the active circuit. This excess capacitance was chosen to be equal to 300fF.

The cross-coupled transistors (M_3 , M_4) can compensate the resistive losses of the LC tank circuit, because its equivalent resistance is negative [1] [2] [4]. Their dimensions were obtained keeping in mind that their equivalent capacitance must be 300fF at 2.4GHz. So, the width for the MOS devices was 200 μ m [1]. For these dimensions, the minimum bias current for the on-set of the oscillations obtained by simulation was 500 μ A [1].

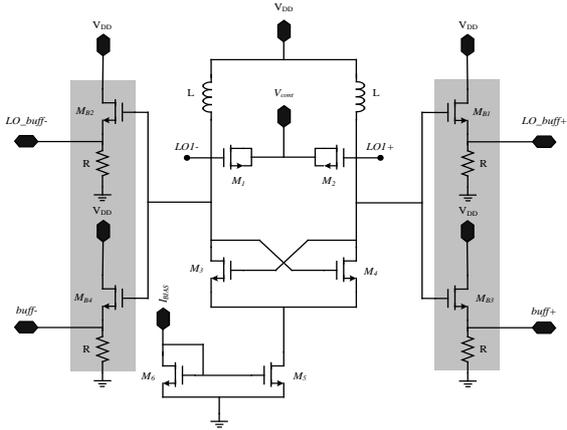


Fig. 2. LC VCO schematic.

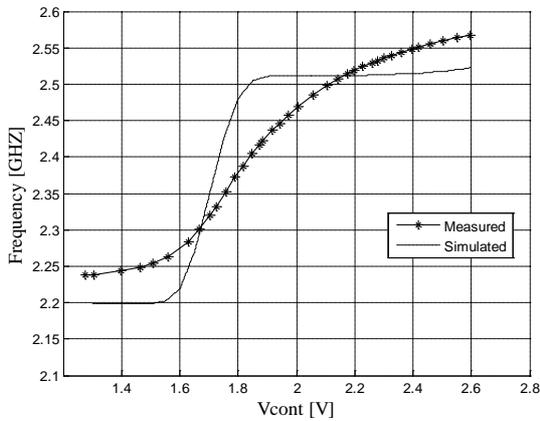


Fig. 3. Simulated and measured output frequency.

Figure 2 presents the LC VCO schematic. The buffers that allow connecting this circuit to a spectrum analyzer and to the frequency divider are represented in shadowed. The source resistance value (R) that composes the source followers (M_{B1} to M_{B4}) is 500Ω . These values establish a compromise between consumption, load effect and output power [1].

Comparisons between simulation and experimental results are shown in figure 3 for the VCO output frequency. The VCO is tunable in the required band, but the experimental gain (K_{VCO}) is lower than the simulated one, 558MHz/V and 1.58GHz/V , respectively. This difference is justified as explained in [5].

The output power is -25.12dBm and the phase noise $-75.09\text{dBc/Hz}@100\text{kHz}$ and $-115\text{dBc/Hz}@10\text{MHz}$, for a 2.4GHz output frequency.

B. Frequency Divider

The frequency divider is based on the *Source-Coupled Logic* (SCL) topology. This divider does a division by 2 of the VCO output frequency, and uses two type D flip-flops.

The circuit is shown in figure 4 [1].

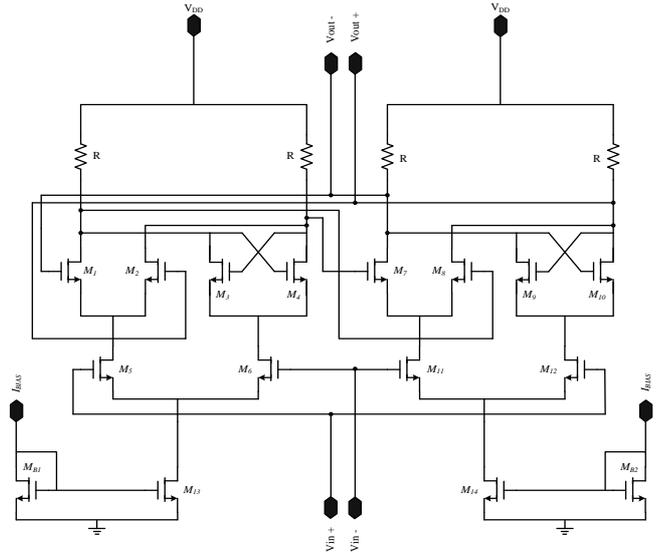


Fig. 4. SCL frequency divider by 2.

The drain resistance allows adjusting the DC value of the output signal, and at the same time with M_1 to M_4 and M_7 to M_{10} dimensions, obtain the correct value for the division. The bias current (I_{BIAS}) is 1mA .

After connecting the VCO with the frequency divider, the whole circuit simulation gives the results presented in figure 5. This way it is possible to see if the divider is working properly [1].

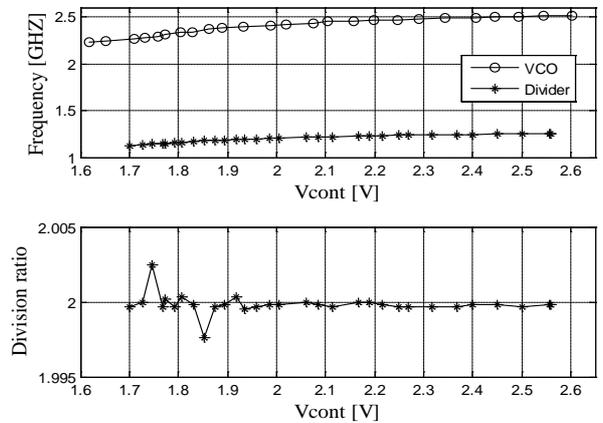


Fig. 5. Simulated VCO and divider output frequencies, and divider ratio.

The ratio error between 2.25GHz and 2.51GHz is less than 0.01% and is due to FFT numerical errors.

As said before the required total divider ratio is 32, therefore, five of these blocks in cascade were used.

C. Phase-Frequency Detector

A typical logical circuit of a PFD is shown in figure 6 [6].

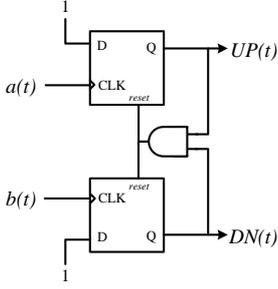


Fig. 6. PFD logic circuit.

This configuration allows comparisons between phase (ϕ_a and ϕ_b) and frequency (f_a and f_b) of the input signals $a(t)$ and $b(t)$. The flip-flops circuit is based on *True Single Phase Clock* (TSPC) topology [7].

This topology has great advantages such as reduced number of devices and low consumption. The main disadvantage is the high sensitivity to small variations of the supply voltage.

D. Charge Pump

The charge-pump circuit is shown in the figure 7 [8]. The main advantage of this circuit is that it uses only one current source instead of the typical two. This simplifies the external bias of the chip. Usually this source value is less than few hundreds of μA , however in this work 1mA was used due to the necessary voltage swing that must be applied to the VCO. The switches are made by MOS transistors M_3 and M_{10} [1] [8].

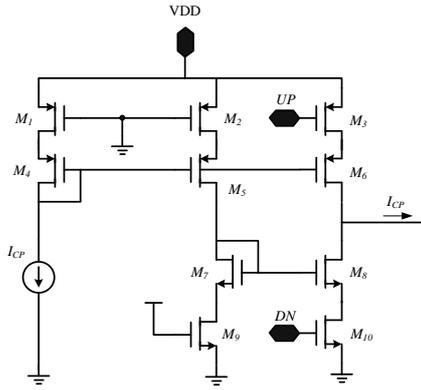


Fig. 7. Charge-pump circuit.

E. Loop Filter

In close loop, the PLL is an unstable system. Therefore it is necessary to introduce an additional zero [1] [2] [4]. So, besides charge pump capacitor C_P , a series capacitor resistor circuit is introduced, as shown in figure 8.

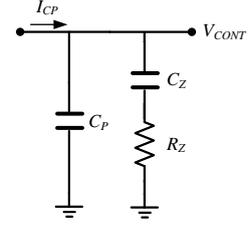


Fig. 8. Loop filter.

Capacitor C_P value is 16pF and C_Z is 270pF. The resistor value is 1.5k Ω . These elements are placed off-chip and their values were obtained by [1] [9].

F. PLL

Figure 9 shows the VCO control voltage (V_{CONT}) during PLL locking acquisition. This simulation was obtained for a reference frequency of 75MHz.

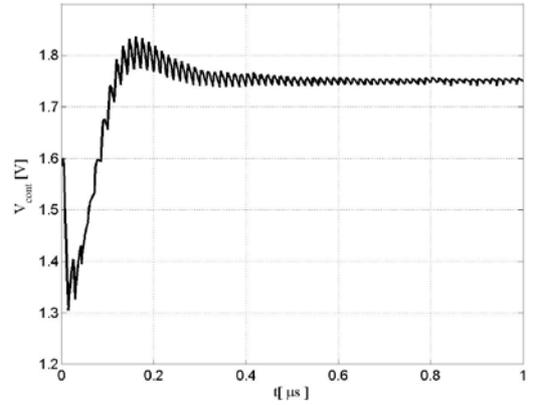


Fig. 9. PLL locking acquisition for $f_{REF} = 75\text{MHz}$.

III. EXPERIMENTAL RESULTS

In this section the experimental results of the PLL are presented. Figure 10 presents a photo of the chip mounted on a PCB test-board.

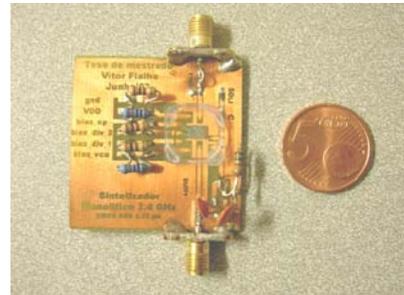


Fig. 10. Photo of the chip mounted on a PCB test-board.

First, the circuit was tested for a fixed reference frequency. This way it is possible to visualize the PLL output signal spectrum and check if the division is correct. Figure 11 shows

the PLL output spectrum at $f_o=2.4\text{GHz}$ for a reference frequency $f_{REF}=75\text{MHz}$.

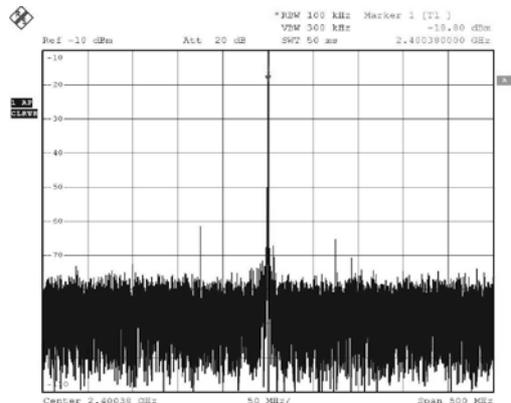


Fig. 11. PLL output spectrum for $f_{REF}=75\text{MHz}$.

It is also possible to measure the lock and the capture bands. The capture band is 282MHz and the lock band is 323MHz. The total consumption of this circuit is 34mA from a 2.6V supply voltage.

Simple output buffers were used which justifies the low oscillator output power.

IV. CONCLUSIONS

In this paper it was described the working prototype of a monolithic 2.4GHz Integer-N PLL, implemented on a CMOS $0.35\mu\text{m}$ 2P4M technology. The circuit area including pads is $995\mu\text{m} \times 545\mu\text{m}$. The loop filter defines the capture and lock bands, because in C_Z and R_Z absence, these bands reduce 150MHz. The *charge-pump* worked as expected. The load effect of the divider in the VCO originates a frequency decrease of 50MHz, but the output still covers the 2.4GHz standards.

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