Analog Circuits Optimization based on Evolutionary Computation Techniques

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Abstract — **This paper presents a new design automation tool based on a modified genetic algorithm kernel, in order to increase efficiency on the analog circuit and system design cycle. It combines a robust optimization with corners, machine learning modeling and distributed processing capability able to deal with multi-objective and highly constrained optimization problems. The resulting optimization tool, simulation capabilities, and extensible architecture are presented and the improvement in design productivity is demonstrated for the design of robust CMOS operational amplifiers.**

I. INTRODUCTION

The microelectronics market trends present an ever-increasing level of complexity with special emphasis on the production of complex mixed-signal systems-on-chip. Strict economic and design pressures have driven the development of new methods and tools for automating the analog design process. Despite the evolution verified in the past few years, most of the designer effort is still dedicated to automate the circuit sizing process because, like layout and topology generation tasks, circuit sizing is considered a very time-consuming process. Analog design problem is typically an over constrained problem with many degrees of freedom and many performance requirements and it is still characterized by the lack of a unique and structured design flow definition. The majority of the applied techniques and tools used to solve the analog problem, such as DELIGHT.SPICE [1], ANACONDA [2], AMGIE [3], and APE [4], among many others [5], are based on powerful numerical optimization engines (e.g. evolutionary algorithms, geometric programming,) conjugated with evaluation engines (e.g. circuit simulators), equation engines (e.g. based on symbolic analysis) which evaluate the merit of some developing analog circuit candidate. In these approaches the design problem is first mapped or modeled into an optimization problem and then solved by an appropriate optimization method. In general, optimization tools, for analog circuits design, composed by an optimization kernel and an evaluation engine based on electrical simulation are pointed out as the most flexible solution when compared with other methodologies (equation-based, knowledge-based) since it accommodates to any type of circuit topology and accuracy, only depending on the selected device models.

The work presented in this paper is partially supported by the PRODEP Program, under the action no.5.3 and the EVOLUTION Project (POSC/EEA-ESE/60225/2004) sponsored by FCT.

The work presented in this paper describes a new design automation approach to the problem of sizing analog ICs. The developed design optimization tool, GENOM, is based on a modified genetic algorithm (GA) kernel and incorporates heuristic knowledge in the control mechanism, allowing a significant reduction of the required number of generations and, therefore, iterations to reach the optimal solution. However, the optimization process, employing a simulation-based approach with a kernel based on stochastic optimization techniques, is clearly a computational intensive task typified by high dimension search spaces and high costly function evaluations. A step forward to enhance the efficiency of the implemented optimization tool corresponds to the introduction of modeling techniques. The model introduced in this paper follows a supervised learning strategy based on Support Vectors Machines [9] which, together with an evolutionary strategy, are used to create "feasibility" models to efficiently prune the design search space during the optimization process, therefore, reducing the overall number of required evaluations [6-8].

The paper is organized as follows: section II, gives an overview of the design automation tool and in section III, the improvement in algorithm performance is demonstrated. Finally, the conclusions are drawn in section IV.

II. EVOLUTIONARY ANALOG IC DESIGN OPTIMIZATION TOOL

A. Project Overview

The EVOLUTION project aims at exploring new design automation techniques by combining state-of-the-art modeling and searching techniques. GENOM is a design optimization tool, resulting from the EVOLUTION project, which combines a modified genetic algorithm kernel with SVM models. This approach also handles multi-objective multi-constraint problem formulation, deals with process variations, supports the interaction with both equation-based and simulation-based evaluation engines (HSPICE), and can be executed either in a single processor machine or distributed in a multiprocessor environment [10]. The GENOM optimization tool can be used as a standalone application, although it holds some functionalities which can only be fully accomplished when it is part of the in-house design automation environment called AIDA [11], illustrated in Fig.1.

B. GENOM Optimization Kernel

A new hybrid optimization algorithm has been developed combined with a design methodology, which increases the efficiency on the analog circuit and system design cycle. This new algorithm combines an enhanced GA kernel with an automatic learning machine based on SVM model which efficiently guides the selection operator of the GA algorithm avoiding time-consuming SPICE evaluations of non-promising solutions [12].

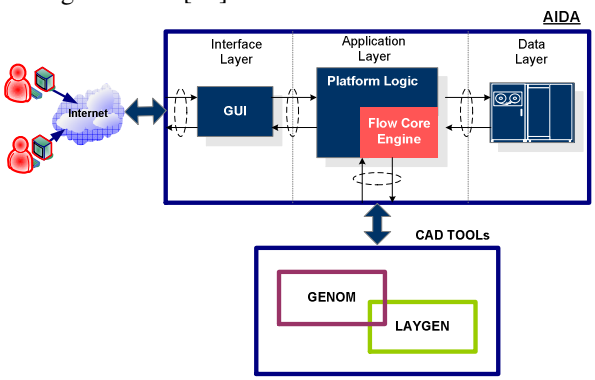

Fig.1 - Tool integration in an analog IC design flow automation environment (AIDA)

. The SVM model can be used as a feasibility or performance model. Whenever the model is built before optimization (off-line) and the topology remains the same, it can be reused for other optimization runs with different performance requirements. Although the optimization tool is able to deal with equation based optimization, (as long as design equation has already been defined by an expert designer), the primarily decision is oriented to a simulation based approach, since it can be applied to all types of design circuits, producing more accurate results and providing an extended layer of analysis, concerning the robust design required in the industrial environment. Parameter variation effects due to manufacturing tolerances or environment conditions have also been included in the optimization loop implemented as a two step optimization methodology. The final solution results in a more robust approach with respect to variations and mismatches. Additionally, the undesired sensitivity effects are attenuated automatically by robust design.

C. GENOM Tool

The result of design methodology and optimization strategy is materialized in a tool, GENOM. The proposed design optimization tool represents an automated alternative to the traditional design flow, automating some steps of the design methodology. It covers some of the most time consuming tasks of analog design process at the circuit or transistor level, like circuit sizing and design trade-offs identification. Like in many analog design environments, some time is spent in the set-up of the optimization system prior to synthesis runs. This includes the conformance test to the format of input files, configuration of optimization, definition of design and independent variables, definition of performances and respective measures, incorporation of technology models, corners, mismatches, designer rules and finally, the training of the learning model in case of optimization with offline model generation. All these tasks take advantage of the GUI interface developed for these effects as illustrated in Fig.2.

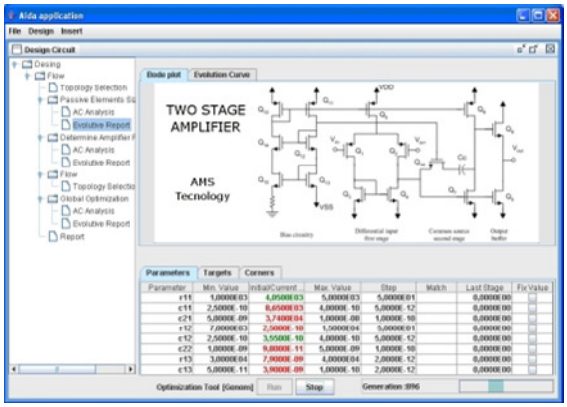

Fig. 2 – Two-stage amplifier

The GUI interface adds some reporting facilities as the designer is able to evaluate some dynamic parameters of the optimization process and to carry out some configuration steps (interactive design, and flexibility). This computational tool allows a designer to examine regions of feasibility with differing uncertainty models available to approximate multi-objective problems like uniform distribution, latin hyper sampling (LHS) and design of experiments. This tool also permits combining different algorithm approaches, like variations of standard operators and including several model approaches. A designer can quickly assess promising design space regions by entering the historical database used to build the SVM model or consulting the database of non-dominated solutions where all the detailed information associated with the current problem is maintained. The graphical representation of the evolution process updated on the fly depends on the specifications provided by the designer. A summary of statistics in the form of post-processing text reports completes the feedback of the process. The information gained in one experiment was useful to the understanding of the overall problem. Further optimizations could be followed after the changing of some design or optimization parameters. Embodying this tool in a design platform or using it as a standalone application can lead to the increase of design efficiency and the improvement of the circuit performance, as it is demonstrated on several examples where the convergence to the desired performance criteria has been attained. The computation cost for several experiments have shown that circuits of moderate complexity can be synthesized in a reasonable amount of time by the use of automatic learning models. This has been made possible by employing fast SVM models in the evolutionary cycle, avoiding expensive simulation iterations. The synthesized designs have also been simulated and verified with HSPICE using the industry standard transistor models.

III. TESTING THE GENOM PERFORMANCE

The benchmark circuit presented above, which was gently provided by the "Electrónica y Electromagnetismo" department from Sevilla University, allows the comparison between GENOM and one important reference tool for analog design, the FRIDGE [13] optimizer.

A. Fridge Benchmark Circuit Tests

The benchmark circuit of reference is a novel single ended folded cascode opamp tested with the Fridge synthesis tool [13] whose results are used to compare the performance and effectiveness of the final GENOM optimizer. This benchmark circuit includes all items necessary to the implementation and test, including the original netlist, testbench, device model, constraints, variables range and performance results obtained by the Fridge optimization tool. The schematic of the circuit is shown in Fig. 3 and tesbench defined in Fig. 4.

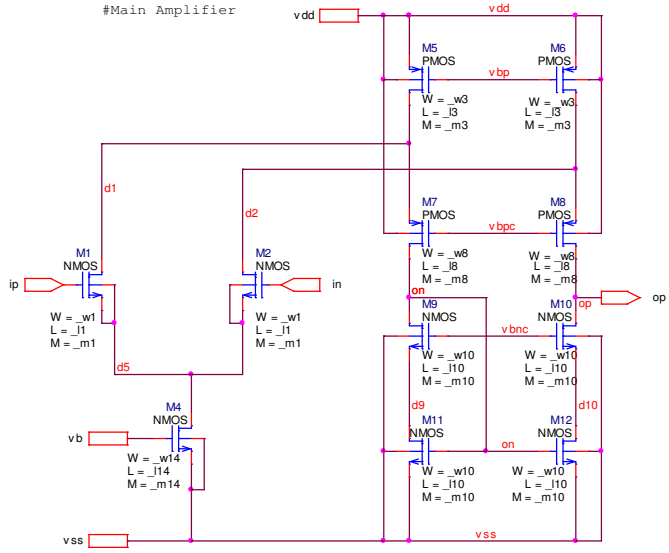

Fig. 3 - Two-stage amplifier

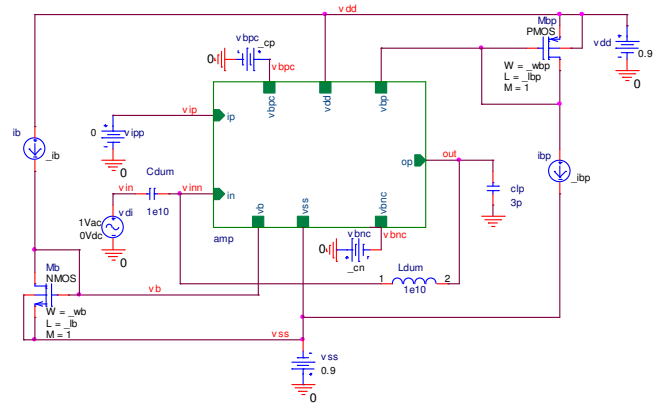

Fig. 4 – OpAmp testbench for DC and AC specifications

B. Optimization Test with FRIDGE Ampop

Following the original Fridge approach, this experiment does not optimize the bias circuit, only the main circuit. The experiments were synthesized with the UMC 0.18um Regular Vt 1.8V Mixed Mode process Spice Model and were executed on an AMD X64 2.8 GHz dual core machine and use HSPICE to simulate the circuit and extract performance parameters. The total of constraints (performance constraints and the constraints derived from designer's rules) result in 20 optimizations constraints that must be satisfied in the optimization process described in Table I. The design performances and final results achieved with both tools are depicted in Table II. Optimization process uses 15 independent variables whose ranges and respective final transistor dimensions are given in Table III.

Table I - Optimization algorithm parameters

Parameter	**value**	**Parameter**	**value**
Kernel	GA-MOD	Crossover	Two point
Strategy	Typical + Corner Optimization	Mutation	Dynamic
Sampling	LHS	Adaptive	No
Sort method	Priority to constraints then fitness	Elite	25% of population
Selection	Tournament by "feasibility"	Generations	150
Popsize	32	Search Space	4.7168e+53

Table II - Design performance and final results

Target	**FRIDGE**	**GENOM**
gbw > 1.20e+07	1.60e+07	**1.535e+07**
gain > 7.00e+01	7.00e+01	**7.061e+01**
pm > 5.50e+01	8.06e+01	**7.960e+01**
sr > 1.00e+07	1.53e+07	**1.536e+07**
dm2 > 1.20e+00	9.78e+00	**9.245e+00**
dm4 > 1.20e+00	5.20e+00	**1.568e+00**
dm5 > 1.20e+00	2.21e+00	**1.836e+00**
dm7 > 1.20e+00	1.05e+01	**8.171e+00**
dm9 > 1.20e+00	3.05e+00	**2.807e+00**
dm11 > 1.20e+00	1.95e+00	**1.653e+00**
onm2 > 1.00e-01	1.004e-01	**1.098e-01**
onm4 > 3.00e-02	3.02e-02	**3.240e-01**
onm5 > 3.00e-02	5.66e-02	**9.866e-02**
onm7 > 3.00e-02	4.25e-02	**8.761e-02**
onm9 > 3.00e-02	4.91e-02	**3.802e-02**
onm11 > 3.00e-02	1.78e-01	**2.451e-01**
osp > 5.00e-01	6.25e-01	**5.660e-01**
osn < -5.00e-01	-5.02e-01	**-5.057e-01**
Areas (min)	2.371e+01	**1.687e+01**
Power (min)	2.333e-04	**2.44e-04**
Cost value	-0.29258	**8.070e-02**
Iteration **Final/First** solution	2497/------	**2464 /1110**
Time (s) **Final/First** solution	----------	**53.68/25.08**

The main performance spec *gbw* stands for gainbandwith, *gains* means the dc gain, *pm* is the phase margin, *sr* is the slew rate and the goal is to minimize both the area (Areas) and power dissipation (power). The electrical constraints are illustrated in HPSICE style in expression (1):

```
.meas ac dm2 param='abs(lx3(x1.m1)/lv10(x1.m1))'
.meas ac onm2 param='vgs(x1.m1) - vth(x1.m1)'
.meas ac osp param='(_cp + abs(vth(x1.m8)))'
.meas ac osn param='(_cn - abs(vth(x1.m10)))'
```
(1)

Table III – Ranges and Final Transistor Dimensions

Optimization Var.	FRIDGE	GENOM
$cn = [-0.4,0];	$cn = -8.75e-02	**_cn = -4.49e-02**
$cp = [0.0,0.4];	$cp = 6.24e-02	**_cp = 1.00e-03**
$l1 = [0.18u,5u];	$l1 = 1.56e-06	**_l1 = 1.38e-06**
$l4 = [0.18u,5u];	$l4 = 4.70e-07	**_l4 = 1.94e-06**
$l5 = [0.18u,5u];	$l5 = 3.80e-07	**_l5 = 3.70e-07**
$l7 = [0.18u,5u];	$l7 = 7.60e-07	**_l7 = 9.10e-07**
$l9 = [0.18u,5u];	$l9 = 2.06e-06	**_l9 = 8.90e-07**
$l11 = [0.18u,5u];	$l11 = 6.00e-07	**_l11 = 2.19e-06**
$ib = [30u,400u];	$ib = 4.84e-05	**_ib = 4.85e-05**
$w1 = [0.24u,200u];	$w1 = 1.95e-05	**_w1 = 1.49e-05**
$w4 = [0.24u,200u];	$w4 = 3.03e-05	**_w4 = 6.99e-06**
$w5 = [0.24u,200u];	$w5 = 7.13e-05	**_w5 = 3.68e-05**
$w7 = [0.24u,200u];	$w7 = 1.04e-04	**_w7 = 6.30e-05**
$w9 = [0.24u,200u];	$w9 = 6.56e-05	**_w9 = 3.14e-05**
$w11 = [0.24u,200u];	$w11 = 3.08e-06	**_w11 = 7.32e-06**

C. Comparison results

Table IV shows the GENOM performance and depicts the run-time information in several optimizations points.

Table IV – GENOM benchmarks

Target	nEval	Power (min)	Areas (min)	Time (s)
Final results in FRIDGE	2497	2.333E-04	2.371E+01	-------
GENOM				
1st Solution	1110	4.0590e-04	2.9727e+01	25.08
GENOM similar to FRIDGE	1461	2.284e-04	2.377e+01	32.47
GENOM better than FRIDGE	2064	1.918e-04	2.009e+01	43.33
Final Results	2464	2.446e-04	1.6873e+01	53.68

GENOM achieved the first solution in 25s approx. using 1110 evaluations and reaches a similar performance to FRIDGE in 1461 evaluations, corresponding to an efficiency increase of 41%. The GENOM optimization produces 183 new feasible solutions. One of the best solutions improves simultaneously the power in 17% and 15% in the area as described in Table 6.53 with 2064 evaluations.

IV. CONCLUSIONS

The presented design automation work, GENOM, uses one of the most promising optimization techniques, evolutionary computation techniques, to face (handle) the challenges of the analog design industry. In order to ensure the design correctness and accuracy, GENOM employs a standard simulation tool in the loop of a modified genetic algorithm kernel. To increase the efficiency of the evolutionary algorithm, a machine learning algorithm based on SVM was introduced. The proposed approach results in a new GA-SVM learning scheme applied to analog circuit design composed by the interaction of two machine learning engines. Additionally, GENOM was designed to deal with statistical fluctuations (process variations) inherent to the fabrication process and varying operating conditions (supply voltage or temperature variations), a fundamental feature to obtain a robust design. A graphical user interface was also supplied in order to increase productivity. Finally, the performance and effectiveness of the GENOM optimizer was demonstrated taking into account a benchmark circuit and one important reference tool for analog design.

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