A Bandgap Voltage Reference With Only MOS Transistors

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***Abstract*— The bandgap voltage reference (BGR) circuit is an important component of Analog-to-Digital and Digital-to-Analog converters, which are broadly used in mixed-signal and radio-frequency systems. Most BGR use bipolar junction transistors (BJT) to easily reduce the temperature dependence, due to temperature coefficients, other common practice is the use of operational amplifiers (OP-AMP). The goal is to implement a BGR architecture without the use of an op-amp and using only one type of transistors, in this case, CMOS technology, and without the use of parasitic BJT. This must be accomplished without compromising the specified voltage variation requirements, BGR with 1% variation. An all CMOS BGR without BJT and without Op-Amp is proposed and simulated using Xfab 0.18-µm process. The bandgap works with 1.8-V supply voltage with ±10% variation. The circuit generates an output reference voltage of 605.865 mV with a variation of ±3.325 mV over a temperature range from -40 to 85ºC, which corresponds to 1.097% variation.**

I. INTRODUCTION

To convert a signal, digital to analog or analog to digital, a reference voltage is needed. Furthermore being considered an auxiliary circuit, their function makes bandgap voltage reference one of the most important circuits in all mixed-signal and radio-frequency systems. It is not possible to make a precise conversion if the voltage reference is not constant. Generic mixed-signal systems have more than one voltage reference as a result different voltage references are necessary. All of them need to have high-accuracy to grant high-resolution high-speed data conversions. The bandgap voltage reference output value is not important, but it must be constant and accurate. It must be as tolerant as possible to the inherent external non-ideal factors, such as: temperature, power supply variation, production process, etc. The most used bandgap voltage reference circuits use BJT or parasitic BJT in CMOS process [1] [2], as well as op-amp [2] [3] and also lateral bipolar transistors [4].

With the reduction of the transistors size, and the reduction of supply voltage, more precise BGR circuits are needed. With 5 V supply, a bandgap output voltage of 2 V with 20 mV variation is 1% error. With 2 V supply voltage, output of 1 V and the same 20 mV variation, the error is 2% error. The aim of this work is to realize an all CMOS Bandgap. The study of new bandgap circuit with CMOS technology, without BJT, is done throughout this paper. Another feature is the reduction of the circuit area since Operational-Amplifiers are not used.

II. BANDGAP VOLTAGE REFERENCES OVERVIEW

Voltage references are used in generally on all analog integrated circuits. Some IC needs more than one voltage reference in order to avoid signal degradation and to respect different requirements of voltage reference. Their outputs can be predicted and need to have high accuracy.

A. BGR

The purpose of a bandgap voltage reference is to eliminate all external factors and provide an output as constant and accurate as possible. There are several external factors like temperature, V_{DD} and process variations, something that after the IC production, the designer can not predict, so the BGR circuit must be able to withstand these sources of error. The working principle of a bandgap voltage references using BJT can easily be explained. When temperature increases, V_{be} decreases linearly and V_T increases linearly, which makes V_{out} approximately linear.

This conception can be elucidated by using the circuit in Figure 2.1 [5], using parasitic BJTs. V_A must be equal to V_B, which produces an equal current in each branch, current that is proportional-to-absolute-temperature (PTAT). ΔV_{BE} is the difference between V_{BE1} and V_{BE2}, and is equal to:

$$\Delta V_{BE} = V_T \ln N \quad (1)$$

V_T is the thermal voltage and N the emitter area ratio between the two BJT. The bandgap voltage reference is given by:

$$V_{OUT} = (I_1 + I_2) \cdot R_3 = \frac{R_3}{R_2}\left[\frac{R_2 \ln(N)}{R_1} V_T + V_{EB2}\right] \quad (2)$$

With an appropriate choice of the R_3/R_2 and R_2/R_1 ratios, the variation of V_{OUT} due to the variation of V_T and V_{EB}, with temperature, can be reduced.

Most of BGR architectures use BJT and operational amplifiers. With this type of circuit, it is easier to reduce the external error sources. Depending on the technology, BJT have normally linear temperature coefficients, this is one of the reasons to be usually used in BGR architectures. Current must be equal in all the three branches, the temperature compensation produces two currents that are mirrored to the output branch. One way to assure that is using an operational amplifier.

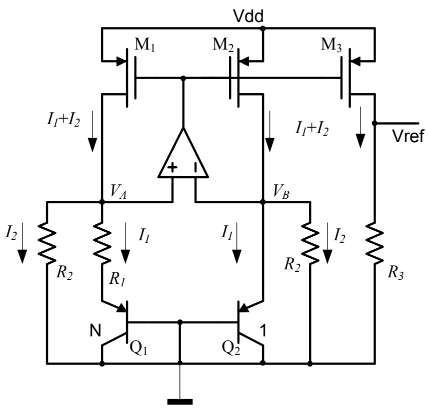

Figure 2.1 – Simple implementation of bandgap reference.

There are other similar architectures [6], but they all have the same goal, to reduce the temperature compensation in order to make V_{REF} as more precise as possible.

Trimming technique is made to improve the output voltage reference. It is used to guarantee that after corners simulation the target performance is achieved. Trim techniques have been studied for a long time. George Erdi [7] studied a precision trim technique for analog circuits. The correct resistor value choice is made with the proper selection of the right bit. The number of bits that are necessary to use, is proportional to the number of resistors needed.

In table 2.1 an overview about the works that were published about bandgap voltage references is done. Several BGR circuits with supply voltage around 1.8 V and with a 0.180 µm technology are analyzed. Table 2.1 shows the principle characteristics of each one. The main characteristics observed were Vref, Vref variation and the technology used. All of them use BJT, CMOS process with parasitic BJT or BiCMOS. BGR circuits are very sensitive to temperature and voltage supply variations. These two characteristics are more focused by the authors.

It is imperative to minimize the effects of this variation in the output voltage. During the last years the schematics have not changed their architecture, they used amp-op and BJT or parasitic BJT, because of its ability to reduce the temperature and V_{DD} variation. As regards to the number of branches, here the authors differ in their number, in order to obtain better temperature compensation. In this section the focus was the study of circuits with similar characteristics to what will be presented.

Table 2.1 – Comparison of BGR available in the literature.

Ref.	Year	Author	V_{DD} (V)	Technology	Vref (mV)	Variation (mV)	Error
[8]	2005	Mao Jingwen *et al*	1.8	0.18 µm - CMOS *	1116	N/A	0.296%
[9]	2006	Po-Hsuan Huang *et al*	0.9-2.5	0.18 µm - CMOS *	222	6	2.70%
[10]	2005	Ron-Min Weng *et al*	1.8	0.18 µm - CMOS *	615.1	1.4	0.23%
[11]	2006	Wang Xichuan *et al*	1.8	0.18 µm - CMOS *	712.73	0,357	0.05%
[12]	2007	Keith Sanborn *et al*	1	0.5 µm - BiCMOS	190.91	2.166	1.13%
[13]	2006	Vadim Ivanov *et al*	1	N/A - BiCMOS	~200	N/A	~1%
[14]	2003	Yang Li *et al*	1.8	N/A - BiCMOS	721.64	0.24	0.03%

Technology with a * refers to CMOS process with parasitic BJT.

III. Proposed Bandgap Voltage Reference

A new bandgap voltage reference topology is proposed. An all CMOS BGR without BJT and without Op-Amp is proposed and simulated using Xfab 0.18-µm process. The bandgap works with 1.8-V supply voltage with ±10% variation. In this section the architecture and circuit operation is presented.

A. *Proposed architecture*

The proposed bandgap voltage reference architecture is presented in Figure 3.1. The circuit is a modification of a common architecture using Bipolar transistors [15]. Here only standard MOS transistors are used. The objective is to only use one type of transistors in the BGR circuit. Despite most of BJT being parasitic MOS transistors, the proposed architecture has only pure MOS transistors. From the circuit it is possible to extract the following equations:

$$V_{DD} = V_{DS_{M1}} + V_{SD_{M4}} + V_{R1} + V_{DS_{M6}} \quad (3)$$

$$V_{DD} = V_{DS_{M2}} + V_{DS_{M5}} + V_{DS_{M7}} \quad (4)$$

$$V_{DD} = V_{DS_{M3}} + V_{R2} + V_{DS_{M8}} \quad (5)$$

$$V_A = V_B \Leftrightarrow V_{R1} + V_{DS_{M6}} = V_{DS_{M7}} \quad (6)$$

Transistors M1-M3 are current mirrors, M4-M5 force A node voltage to be equal to B node voltage, in order to stabilize the circuit behavior with corner and V_{DD} variation. Resistors R_1 and R_2 implement the temperature compensation. Transistors M6 and M7 produce the circuit current and make possible to transistor M8 to be stable and preserve the voltage with V_{DD} variation.

The output voltage is given by:

$$V_{REF} = V_{GS_{M8}} + R_2 \cdot I \approx \frac{R_2}{R_1} \quad (7)$$

The resistors value varies from corner to corner, as well as R_2/R_1 ratio. The trimming is done with the correct R_2/R_1 ratio calibration. The output voltage value is not important, can be any value. Output voltage will be used to produce a voltage reference of any value in another circuit before being used in ADC, DAC or in other mixed-signal systems.

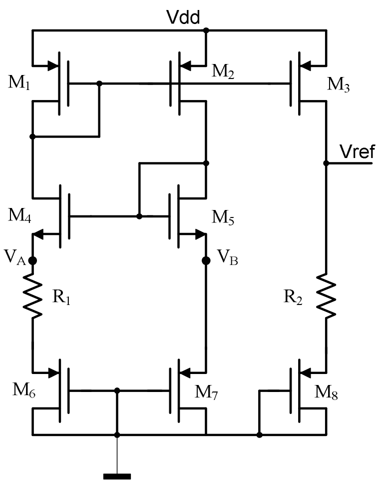

Figure 3.1 - Proposed BGR Architecture.

B. Temperature Correction

The temperature correction can be done, with the correct adjustment of the R_2/R_1 ratio. Different corners may have different ratios. With this type of circuit, with only MOS transistors, it is necessary to have higher resistor values. With MOS transistors, the temperature correction control is more difficult to assure than with BJT, is more difficult to characterize the behavior of BJT with temperature variation. With BJT the temperature produces a lower dependence in current. In MOS transistors, temperature will affect both V_{DS} and V_{GS}, which, in turn, influence the transistor current. The resistors used in different corners produce different ratios R_2/R_1.

C. Voltage Supply Correction

The voltage supply variation is ±10%, so it is indispensable to correct the Vref value with such variation of 360 mV, 1.62 V to 1.98 V. Like in temperature correction, with MOS transistors, variation of V_{DD} will change V_{DS} and V_{GS} of the transistors, which in turn also varies the current and finally Vref. This issue was overcome by the trimming technique, which implied changing the resistors values. In different corners with the same V_{DD} variation, the resistors ratio increase can be different.

D. Trim technique

Trimming technique is used to overcome the output variation in the different corners that are simulated. Corners create a virtual demonstration from which kind of conditions the BGR will find in their operation, like temperature and power supply variation. There are a few trim techniques for analog circuits [7]. The trimming technique used in the BGR is presented in Figure 3.2.

At each time only one bit is chosen. Different bits have associated different values of resistors. The bit N+1 selects all the resistors before, so bit N+1 have higher resistor value than bit N. The resistor value increment does not need to be constant.

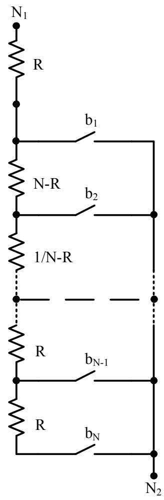

Figure 3.2 – Trimming technique.

The resistors value of R_1 and R_2, have the contribution of two different type of resistances, one with positive TC and the other with negative TC. In the trimming technique there are several combinations of resistors. Any resistor value can be achieved with this technique.

E. Design considerations

Other characteristics are also important to consider, such as Power Supply Rejection (PSR), the circuit noise and the need of a start-up circuit. All of these are analyzed. The start-up circuit is not used, since with simulations it was possible to confirm that the circuit starts to work without need the start-up circuit. With this achievement of non-use of start-up circuit, the area is reduced. PSR must be as higher as possible. As the circuit was being designed, there was always a concern to make sure that transistors matching were reached. The ratio between resistances R1 and R2 should also be equal, this to achieve better results in corners simulation.

IV. Simulation Results

To validate that the results presented in this section are the best that can be found with this circuit, hundreds of simulations were realized with different combinations of resistors, in all the corners. Only the final circuit simulations are presented in this section, the other results, while important to achieve the final results are not presented in theory, because they were improved.

In order to achieve the resistors values, 56 different corners were simulated. There were simulated 7 different values of V_{DD}, 4 transistors corners and 2 resistors. These 56 different corners not only prove that proposed bandgap are able to work in different conditions (temperature) and can support different types of production processes, but also show the resistors that must be applied to the circuit, in order to get it operational.

Temperature correction, as power supply, was done with resistors trimming. To reach the circuit resistors simulations were performed. To overcome the power supply variation the resistors value were increased, in order to produce the circuit current, and consequently the output voltage. The temperature correction with the power supply fixed, was more difficult to ensure. The resistors values were changed in order to obtain minimum and maximum output voltages, between the previous simulated corner limits.

In addition to corners simulation, also the circuit noise and the PSR testing was realized. The worst PSR result from all corners is about 22.5 dB in the 35 kHz bandwidth. The circuit noise is 4.4 µV rms. With this value of noise, the bandgap should only be used in voice applications.

All the maximum and minimum Vref values are presented in Figure 4.1.

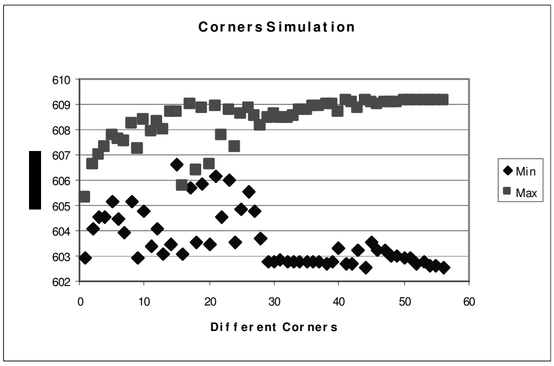

Figure 4.1 – All maximum and minimum values.

It can be seen that minimum values are near 603 and 604 mV and the maximum values near 608 and 609 mV. Some corners have minimum values higher than the maximum values of other corners, but what matter is the absolute minimum and absolute maximum to find the bandgap error. After the 56 corners were simulated, the minimum and maximum values for Vref are among 602.54 mV and 609.19 mV. The variation is 6.65 mV and the error is 1.097 %.

V. CONCLUSIONS

A new topology for a bandgap voltage reference is proposed. The variation of V_{REF} is 6.65 mV, with minimum of 602.54 mV and the maximum of 609.19 mV. This bandgap should be used in voice applications due to circuit noise, which is 4.4 µV rms, to reduce the circuit noise the size of transistors should be increased. The bandgap PSR is 22.5 db in 35 kHz. One way to increase the PSR is to use an external capacitor.

Comparing the results of the proposed BGR and the BGR presented in table 2.1, it can be concluded that the proposed BGR does not have the best, and not the worst, performance of the analyzed bandgaps. The proposed bandgap error is in the middle values. However, the proposed BGR only use one type of technology, pure MOS transistors. With this the process fabrication is reduced to one type of transistors. The circuit does not use amp-op and capacitor, which can reduce the overall circuit area.

ACKNOWLEDGMENT

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT/MCTES) SPEED (PTDC/EEA-ELC/66857/2006).

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