An Improved Design Method for Monolithic CMOS Quasi-Square-Wave DC-DC Converters

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Abstract — **This paper presents a study of resonant converter topologies targeted for CMOS integration. An improved new method to design efficient monolithic Quasi-Square-Wave converters is proposed. A power loss model of the power stage including the driver circuits used on the design method permits to optimize the design parameters for the power stage and conclude about the technology limitations. Based on this method and taking as reference the 0.35µm CMOS technology from AMS a buck converter operating at 70MHz is designed. Simulation results of the buck converter design are presented.**

I. INTRODUCTION

The constant growing of portable electronic equipment, in diverse applications, powered by batteries and the growing demand for increased power autonomy, create the needs of new solutions with better efficiency for power management circuits. The great advance that the concept of SoC (System on a Chip) has reached associated to the continuous decreased of the supply voltage [1] as a form of reducing the power consumption causes a diversification of the supply voltages due to the different circuits inside the chip. Some times with substantial difference between the battery voltage and the circuit voltage. For this kind of applications these are inherent advantages on the use of Power Electronics switching topologies, in the conception of integrated DC-DC converters used in power management circuits, in order to achieved good performances on efficiency.

When the defining a DC-DC converter it is usual to consider as design parameters the ratio between the input and output voltages, the output power or output current and the voltage ripple of the output voltage. These parameters are not sufficient to define all the elements of a switching DC-DC converter. It is necessary to consider additional variables such as the switching frequency and the inductor current ripple. For the definition of these variables one considers the occupation area and the efficiency, optimizing the ratio between them.

The inclusion of power management blocks inside of SoC assumes particular importance as a form of reducing the losses [2]. Due to its availability and cost CMOS technology becomes the key technology on the fabrication of these circuits. The integration of a switching DC-DC converter in CMOS technology brings new challenges. The inductor and capacitance integration is restrictive to low values, when compared with discrete components, due to the occupied area. The low value integrated capacitors present reasonable behaviour and are normally used on mixed-signal. The integrated inductors on CMOS process, present poor parasitic impedance characteristics degrading the efficiency of the converter. However, the physical dimension and the parasitic impedances of these components are greatly reduced as the switching frequency increases [3]. More recently a new technology on micro inductors, which uses magnetic materials, permitted the integration of these devices with low parasitic impedances and working with high frequencies (up to 3GHz) [4].

The key parameter to a switching DC-DC converter full integration is the high switching frequency. For these values of switching frequency the power transistors and respective drivers power losses, dominate the losses on the converter [5], mainly due to the increase of the switching losses. So, maintaining high efficiency at high switching frequency is a major challenge. Among the Power Electronics DC-DC converters circuit topologies, the soft-switching topologies [6] are distinguished by their efficiency and low Electromagnetic Interference (EMI). Thus, the use of soft switching techniques appears attractive to minimize noise and switching losses [7].

Taking these considerations into account, two ZVS resonant topologies are investigated in this paper, for integration purposes: A Quasi Resonant Converter and a Quasi-Square-Wave Converter. As it will be shown in section II, the use of ZVS Quasi-Resonant topologies is restrictive due to the voltage stress imposed on switching devices, and also because of the same order values of the resonant components and of the parasitic components. On the other hand, the inductor current in Quasi-Square-Wave topologies presents higher variation, which implies enlarged silicon area for the switching devices.

On section III an improved design method for the Quasi-Square-Wave converter is presented. Several simulation results based on a mixed mode 0,35 µm CMOS process are shown in section IV, in order to verify the

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viability of the theoretical approach. Preliminary conclusions are presented in section V.

II. QUASI-RESONANT TOPOLOGIES

A. Quasi-Resonant Converters

Quasi-Resonant Converters are obtained from conventional PWM (Pulse Width Modulation) converters by using resonant switches. The difference between these switches and the conventional PWM switches is the inclusion of an inductor and a capacitor, as in the buck converter showed in Figure 1, in order to allow ZCS (zero current switch) (a), or ZVS (zero voltage switch) (b).

As a consequence, switching frequency can be increased, with reduced switching losses and higher power density for integration purpose.

Quasi-Resonant converters control is achieved by switching frequency (f_S) variation, leading to a more complex control when compared with conventional PWM converters.

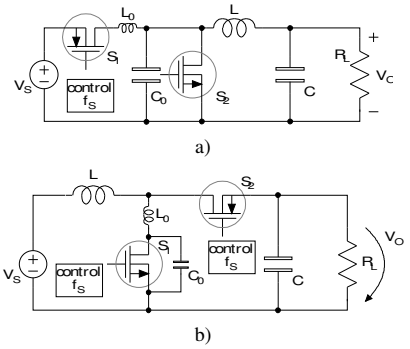

Fig. 1. a) Buck ZCS QR converter; b) Boost ZVS QR converter.

Consider $M_{min}=V_O/V_{Smax}$ and $M_{max}=V_O/V_{Smin}$. The approximate relation between maximum and minimum switching frequencies, for the ZVS boost converter in Figure 1 b), is given by:

$$\frac{f_{S_{\max}}}{f_{S_{\min}}} = \frac{M_{\max}}{M_{\min}} \cdot \frac{\left(\frac{R_{L_{\min}} \cdot M_{\min}}{2 \cdot R_{L_{\max}} \cdot M_{\max}} + \alpha_{\min} + \frac{R_{L_{\max}} \cdot M_{\max}}{R_{L_{\min}} \cdot M_{\min}} \cdot (1 - \cos\alpha) \right)}{\frac{3}{2} \cdot (1 + \pi)} \qquad (1.a)$$

with:

$$\alpha_{\min} = \pi + \operatorname{arcsen}\left(\frac{R_{L_{\min}} \cdot M_{\min}}{R_{L_{\max}} \cdot M_{\max}} \right) \qquad (1.b)$$

where $R_{L_{máx}}$ and $R_{L_{\min}}$ represent the maximum and minimum load resistances. The resonant frequency can be obtained as an approximate function of the maximum switching frequency:

$$\frac{f_{S_{\max}}}{f_0} = \frac{4 \cdot \pi}{M_{\min} \cdot 3 \cdot (1 + \pi)} \cong \frac{1}{M_{\min}} \qquad (2)$$

The critical condition for zero voltage switching occurs for input voltage and highest load resistance ($V_{S_{máx}}$, $R_{L_{máx}}$). Since the condition for ZVS is $I_O Z_0 \geq V_S$, the characteristic impedance Z_0 will be given by:

$$Z_0 = \frac{R_{L_{\max}}}{M_{\min}} \qquad (3)$$

corresponding to the boundary condition.

The converter resonant inductor and capacitor are given by:

$$L_0 = \frac{Z_0}{2 \cdot \pi \cdot f_0} \qquad (4.a) \qquad C_0 = \frac{1}{2 \cdot \pi \cdot f_0 \cdot Z_0} \qquad (4.b)$$

The current and voltage on the active switch, S_1, considering that $M_{\max} = M_{\min}$, will be:

$$V_{DS_{máx}} = \left(1 + \frac{R_{L_{máx}}}{R_{L_{\min}}} \right) V_O \qquad (5.a) \qquad I_{D_{máx}} = I_{O_{máx}} \qquad (5.b)$$

and the current and voltage on the passive switch, S_2, are:

$$V_{R_{máx}} \cong -V_O \qquad (6.a) \qquad I_{R_{máx}} = 2 I_{O_{máx}} \qquad (6.b)$$

Considering equations (5) and (6) and a fixed load, it can be concluded that the maximum voltage on the active switch is twice the maximum voltage at the converter input. This will represent a problem if the input voltages are near the maximum CMOS process voltage, or for high load variations, especially if the switching frequency rises to tens or even hundred of MHz (although there is the possibility of producing high-voltage CMOS compatible transistors [8], these transistors operate at lower frequencies). This could become a limitation for the integration purpose. Although that, using the last equations and an extension of the design method for hard-switching converters presented on [9], a boost converter was simulated showing some drawbacks on the use of this kind of converters for integration propose.

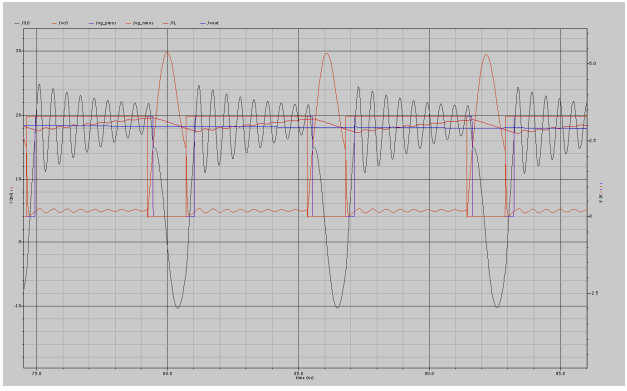

Fig. 2. Transient Analysis detailed Waveforms of output voltage (vout), inductors currents (IL and IL0), power transistors control signals (vg_nmos and vg_pmos) and resonant capacitor voltage (vc0) of the boost QR converter.

On Figure 2 is possible to see that the current on the resonant inductor and the voltage on the resonant capacitor oscillate on the last interval of the switching period. This should happen but with lower values that are near invisible, has it happens in the discrete QR ZVS converters. In our case this is not possible because the characteristic impedance of the regular resonance is of the same order of the not desired

one, between the parasitic capacitor of S_2 and the resonant inductor, in the last interval. This will be a significant drawback in the use of QR ZVS topologies for CMOS integration, unless the CMOS technology used have parasitic capacitances associated to the power transistors smaller than de resonant capacitor, at least one order.

B. Quasi-Square-Wave Converters

ZVS QSW converters present lower voltage and higher current stress on the switching devices. On the other hand ZCS QSW converters have lower current and higher voltage stress [10]. Thus, ZVS QSW topologies appear as an alternative to the use of high-voltage transistors in ZVS QR topologies. Another advantage is that the parasitic capacitors associated to the two power transistors are in parallel and contribute both to the resonant capacitor and only one resonant frequency. However, it is necessary to take into account that there is a price to pay: the higher variation of the inductor current, which leads to an increase on the Electromagnetic Interference (EMI) when compared with the Quasi-Resonant topologies.

To obtain a QSW converter it is necessary to manipulate the low-frequency storage elements in the correspondent PWM topology, followed by the insertion of resonant tank elements. Certain PWM converters cannot be transformed into their corresponding ZVS or ZCS QSW topologies unless new low frequency storage elements are added to the original PWM converter (e.g. the ZCS buck converter) [10]. This solution is only attractive for the topologies that do not need the additional low-frequency elements as the ZVS buck converter, presented in Figure 3.

In this converter the output filter inductor is also used as the resonant inductor. Therefore, this solution appears more attractive then the correspondent QR topology presented in Figure 1. b), because the resonant inductor is not present.

After the steady state analysis of the ZVS-QSW buck converter is possible to obtain a set of five equations which resolution is not trivial. In order to solve this problem, a semi-closed method to obtain the conversion-ratio for the design of a buck ZVS QSW converter was developed in [11]. Using the result obtained in [11] the frequency conversion ratio is given by:

$$\frac{f_{S_{\max}}}{f_0} = \frac{4 \cdot \pi \cdot M^2 \cdot (1-M)}{Q \cdot \left[\frac{M^2}{Q^2} \cdot \frac{i_L(t_0)^2}{I_L^{\,2}} - (2 \cdot M - 1) \right]} \qquad (7)$$

Assuming that M is known and that the parameter Q is function of the load and of L_0, the only unknown variable is $i_L(t_0)$ (this value of current corresponds to the maximum current in the active switch, S_1). The relation between the maximum current in the active switch and the average output current, α_{IL}, can be obtain from the solution of (8):

$$a \cdot \alpha_{IL}^{\,3} + b \cdot \alpha_{IL}^{\,2} + c \cdot \alpha_{IL} + d = 0 \qquad (8)$$

with $\alpha_{IL} = i_L(t_0)/I_L$, and:

$$a = -\frac{1}{2 \cdot Q \cdot (1-M)} \qquad (8.a) \qquad b = \left[\frac{1}{Q} + \frac{M}{Q \cdot (1-M)} \right] \qquad (8.b)$$

$$c = \left[\arccos\left(\frac{M-1}{M} \right) + \frac{1}{1-M} \cdot \sqrt{2 \cdot M - 1} + \frac{(2 \cdot M - 1) \cdot Q}{2 \cdot M^2 \cdot (1-M)} \right] \qquad (8.c)$$

$$d = M \cdot Q \qquad (8.d)$$

Substituting α_{IL} in (7), the ratio between the switch frequency and the resonant frequency is obtained.

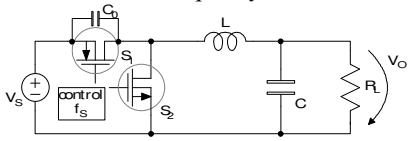

Fig. 3. Buck ZVS QSW converter.

III. DESIGN METHOD FOR QUASI-SQUARE-WAVE CONVERTERS

Some authors have proposed design methods for QSW ZVS converters, [12, 13], however these methods are not appropriated for CMOS integration. A new proposal was initial proposed in [11], but without the design procedure for the power stage. In this way a more detailed and improved method is proposed in this paper.

The CMOS monolithic integration of ZVS QSW converter implies a careful attention over the definition of circuit parameters. As a matter of fact the linear approximations made to obtain equation (7), are only valid if the ratio between the switching frequency and the resonant frequency is small [11]. This implies that Q should have the smallest value as possible. However the choice of Q depends on load and characteristic impedance Z_0. Since C_0 is the intrinsic power transistors capacitances plus an external capacitance, it depends directly on the transistors dimensions, which is defined by the load current, switching frequency and technologic parameters of CMOS process. This implies that the value of L_0 defines Q and the resonant frequency, and therefore, this is a critical value. Taking this into account, the following design method is proposed:

1. Define the normalized load, Q, that with the conversion relation, M, of the converter to be designed, corresponds to a small ratio between the switching frequency and the resonant frequency.
2. With the Q value defined, obtain the characteristic impedance, Z_0, considering the maximum load resistance, $R_{L_{\max}}$, corresponding to the boundary condition. Obtain the ratio between $i_L(t_0)$ and I_L using equation (8). Determine the ratio between the maximum switching frequency, $f_{S_{\max}}$, and the resonant frequency using equation (7).
3. Design the power transistors and associated drivers using an extension of the method used in [10], function of the load current, I_O, and the maximum

switching frequency, $f_{S_{max}}$, which is defined considering the compromise between the occupied area and the converter efficiency, taking into account the technology limitations of the CMOS process used. Obtain the resonant frequency with the information of step 2.

4. Obtain the intrinsic parasitic capacitors of the power transistors that contributes to the resonant capacitor, C_0. The sum of these capacitances must be smaller than the resonant capacitor determined after steps 2 and 3. If not, return to step 1 and relax the specification of Q.

With this method it is possible to guarantee a normal behaviour of the converter in the worst case, defining as in the case of the QR ZVS converters, ranges of variation for the input voltage and output load.

IV. Simulation Results

Using the described design method, a ZVS QSW buck converter was designed with the following characteristics: V_S=4.8…5.2V, V_O=3.3V, R_L=110Ω, L_0=249nH, C_0=1.3pF, $f_{S_{max}} = 70\text{MHz}$.

The waveforms presented in Fig. 4. are in good agreement with the expected results. After the transient, the converter tends to stabilize on the desired values for output voltage and average inductor current. The efficiency of this converter is approximately 75% theoretically considering only the losses of the power transistors. By simulation it was obtained a value about 8% inferior.

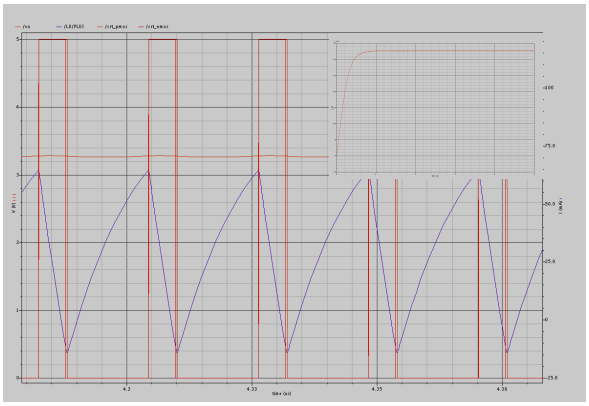

Fig. 4. Transient Analysis detailed Waveforms of inductor current, L0, output voltage, vo and PMOS and NMOS control signals. The complete simulation waveform of the output voltage.

V. Conclusions and Future Work

A QSW ZVS buck converter was conceived using the proposed design method. The good results obtained encourage the experimental test of the converter and the extension of this design method to the boost topology.

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