Electronic Equalization of PMD – Numerical Results

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Abstract — **The capabilities of Electronic Dispersion Compensation (EDC) for Polarization Mode Dispersion (PMD) mitigation are assessed in the context of high-speed optical communication systems. Numerical results are presented for a Feed Forward Equalizer (FFE) for systems operating at 10 and 40 Gbit/s.**

I. INTRODUCTION

Electronic equalization is a well-established technique largely used in automatic phone line equalization [1]. These same principles can also be applied to high-speed lightwave transmission systems. Electronic Dispersion Compensation (EDC) has been reported to overcome fiber dispersion in metro links [2]. Electrical filter based devices are now under deep study and are expected to have a significant impact at the high bit rate optical link receiving edge. These devices are in general based on analog domain transversal filters that are able to operate at high bit rates signals (10Gbit/s - 40Gbit/s and potentially above) [3][4]. A major advantage of EDC is the possibility of electronic adjustment, making possible to compensate changes in non-ideal receiver response or other distortions due to ageing and/or temperature variations.

Inter Symbol Interference (ISI) due to Chromatic Dispersion (CD) and Polarization Mode Dispersion (PMD) is the main impairment that affects pulse shape in high-speed systems and should be mitigated. Monolithic Microwave Integrated Circuit (MMIC) techniques allow the realization of high-performance, reliable microwave circuits and are thus suitable for implementing such circuits as filters in nowadays, high bit rate electro-optical transceivers. The introduction of electrical noise can be stated as the main counter back when using EDC in optical channel equalization.

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Simple electrical equalizer model is presented in section II where Feed Forward Equalizer (FFE) comes up as the nuclear device in the EDC process. Section III introduces transversal filters practical implementation considerations while section IV resumes the Decision Feedback Equalizer (DFE) as EDC performance improvement module as fast technology becomes available. Fiber CD and PMD modeling comes out in section V where numerical simulation set up is also presented. EDC simulation results for 10-40 Gbit/s optical channels are also discussed within this section. A final conclusion comes in section VI.

II. SIMPLE ELECTRICAL EQUALIZER MODEL

Figure 1 shows a simple Transversal Filter (TF) model where the incoming signal is delayed, by one bit period per stage in the Synchronously Spaced Equalizer (SSE) or by less then one bit period in the Fractionally Spaced Equalizer (FSE). For high-speed systems the FSE is best choice in order to avoid aliasing in the equalized signal [5]. Both configurations are known as Feed Forward Equalizers (FFEs).

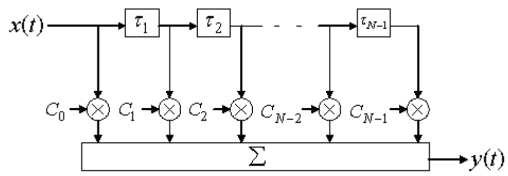


Figure 1 – Simple Transversal Filter (TF) Model

The incoming signal is tapped and weighted by stage coefficients - C_n - that can adaptively be changed so that the resulting filter response equals as much as possible the inverse of the channel response.

A 10Gbps SiGe IC FFE comprising eight taps, aiming to compensate over 95km of standard Single Mode Fiber (SMF) was already tested [6]. Full differential group delay (DGD) compensation was reported for DGD values up to 65ps whilst 3.4dB of gain penalty reduction were measured for DGD of 100ps.

III. Transversal Filters (TF) Practical Implementation Considerations

Transversal filters for 10Gbit/s and 40Gbit/s have been designed using high speed GaAs MMIC technology [3][4]. A distributed configuration was used and is well suited to implementing a high-bandwidth delay line as the feed-forward topology requires. Artificial Transmission Line (ATL) sections implemented with microstrip inductances, making use of the active device capacitance, provide the necessary delays. Gilbert cell or cascode variable transconductance based configurations are used to implement the multiplying blocks [3][7]. In distributed electronic circuits, a tradeoff exists that relates bandwidth and delay similarly to the gain-bandwidth product seen in lumped designs. Therefore the way the ATL sections are implemented is fundamental to guarantee constant delay values between taps. Of most importance is phase linearity, which depends strongly on the behavior of series and shunt elements that compose the ATL sections. The Heaviside condition LG = RC (where L and R are series inductance and resistance, respectively and C and G are shunt capacitance and conductance, respectively) relates incremental elements in a transmission line section for maximum phase linearity and should be enforced within the desired filter bandwidth.

Additional considerations related with stability, input and output matching, input dynamic range and noise require careful circuit design and layout.

IV. ADVANCED ELECTRICAL EQUALIZATION TOPICS

Recent study on this topic shows that some other filter structures derived from the TF, namely the Decision Feedback Equalizer (DFE), are capable of improving EDC circuit performances.

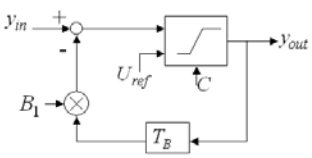


Figure 2 – Step Decision Feedback Equalizer (DFE) Model.

The DFE is a nonlinear filter that is able to cope with severe signal distortions. This device gathers its knowledge from the previously detected bits and adjusts the level on the decision block by subtracting the previous ISI from the decision to be made. One stage DFE is presented in Figure 2, where the reference (U_{ref}) is kept halfway the bit decision by subtracting previous signal level weighted by B_1 at the filter input within a time bit (T_B) interval. By using knowledge from previous bit decisions, DFE can only compensate for post ISI while FFE may do it for post and pre ISI. The basic idea behind DFE is that once a decision has been made to set information symbol to a '1' or '0', the ISI that is present on future symbols can be subtracted out before the decision is made about subsequent symbols. Series combination of FFE-DFE structures outperforms single FFE and DFE electrical blocks, leading to an optimized operation [8].

For a 40 Gbit/s systems, *Nakamura* [9] has recently reported for a 3 tap FFE-DFE IC using InP/InGaAs HBT technology, 20 ps of DGD mitigation.

For the iterative change of the filter coefficients, Zero-Forcing (ZF), Least Mean Square (LMS) as other annealing techniques can be fast enough to set coefficients value while monitoring received pulse shape. They are effective with FFE, DFE or even FFE-DFE structures.

Other digital equalizing processes like Maximum Likelihood Sequence (MLS) analyzers are very robust for low data rate processing equalization [10]. Simplified versions of its analog implementation are beginning to be used in high bit rates systems [8][11].

V. PMD mitigation in terms of Eye Open Penalty (EOP)

Polarization Mode Dispersion arises in fibers when the fiber cylindrical symmetry is broken due to noncircular core or noncircular symmetric stress. The loss of circular symmetry degrades the degeneracy of the two orthogonal polarized modes in the fiber, which causes different group velocities for these modes. PMD varies from fiber to fiber and moreover, in the same fiber varies randomly with respect to wavelength and position.

In this study we will only account for wavelength nondependent PMD, usually called first order PMD and normally expressed by the Differential Group Delay (DGD) that quantifies for polarization misalignment between slow and fast axis in terms of time delay.

Looking forward to establish the EDC capabilities on PMD compensation, a numerical simulation set up was developed where a FFE device with 5 coefficients and a tap delay equal to one third of the incoming bit rate was considered after the photo-detector in the optical receiver. For coefficients updating, a simplex algorithm with the eye opening height as state variable was enforced [12].

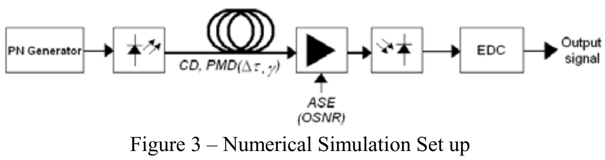
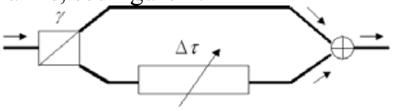


Figure 3 – Numerical Simulation Set up

In this work we numerically studied systems at two different bit rates, 10 and 40 Gbit/s. In order to numerically considerer the DGD, the signal is split and forced to follow two distinct paths. The propagation time difference between the paths is given by $\Delta\tau$, which models the time difference between the fast and slow polarization axis. Due to the random nature of the birefringence along the fiber, $\Delta\tau$

increases proportionally to the fiber length square root. The γ parameter governs the splitting process of the optical power between both arms, see figure 4.



$$\Delta\tau = D_p.\sqrt{Z} \text{ ps}, \; 0 \le \gamma \le 1$$

Figure 4 – 1st Order Fiber PMD Emulation

The fiber transfer function, (1), was implemented in both arms of the emulator of figure 4. In (1) the product $D{\cdot}Z$ states for the CD in ps/nm, being D the dispersion and Z the total length of the system. We considered several distances and in all cases we assumed D=17 ps/nm/km.

$$H_{fibre}(f) = \ell^{j\frac{\pi DZ\lambda^2 f^2}{c}} \qquad (1)$$

The output optical signal is then amplified to completely compensate the optical losses, overall Amplification Spontaneous Emission noise (ASE) is added to the signal in order to have an Optical Signal to Noise Ratio (OSNR) at the receiver input of 13dB measured over 0.1nm of optical bandwidth. After photo detection, modeled as a square law device, adaptively EDC is finally performed. A noise factor of 10dB for the EDC filter was considered.

The SMF was assumed with mean DGD ($\Delta\tau$) proportional to fiber length square root ($\sqrt{Z}$), being D_p the PMD fiber intrinsic parameter in $ps/\sqrt{km}$, see figure 4. Note also that the splitting ratio, γ, is the relative power traveling in the fast axis while slow axis optical signal is delayed by $\Delta\tau$ (ps). When γ equals “1” we say to have all optical power traveling through the fast axis. By the opposite way, when γ equals “0”, all optical power is considered to travel through the slow axis. A ratio for fast to slow axis relative power of 0.7/0.3 or even 0.5/0.5 are usually stated as standard, giving this last ratio the worse overall power penalty.

Since conventional signal quality evaluation methods are not so reliable when strong ISI is present, an Eye-Opening Penalty (EOP) ratio was defined where H_{ref} states for the eye opening in a back to back configuration and H is the eye opening measured after the signal had crossed the link.

$$EOP = -10.\log\left(\frac{H}{H_{ref}}\right) \text{ (dB)} \qquad (2)$$

A. Numerical Simulation Results

Simulations were carried out for three different scenarios and two distances, see figures 5 and 7. The first scenario, “without PMD” means considering only the CD in the link. In the second scenario, ”with PMD”, CD and PMD were both considered. In the last scenario, “after EDC”, CD and PMD were considered in the link and electrical equalization was performed at the receiver. Systems operating at 10 Gbit/s and 40 Gbit/s were simulated and the results hereafter presented.

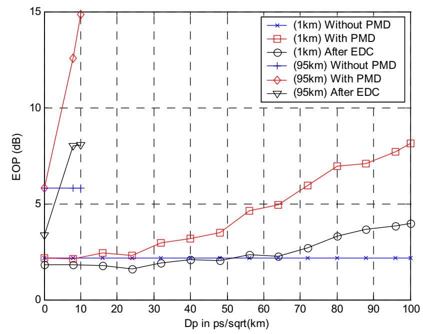


Figure 5 – EDC numerical results for 10Gbit/s NRZ 512bits sequence over a SMF link. γ =0.7

By looking at Figure 5 we see that FFE is able to fully compensate for roughly 65ps of DGD for a 10Gbit/s SMF link while showing an EOP improvement of 4dB at 100ps of DGD. These results are quite similar to those reported by *F. Cariali* [6]. We may take notice that an eight tap FFE was used in [6] instead of our 5 taps filter. The FFE performance is proportional to the number of taps although after 95km of SMF the signal CD induced distortion is already so significant that the overall CD+PMD channel equalization should not change too much when using lower filter orders corresponding to FFE tap numbers from 4 to 8 taps. This explains the similar results obtained.

In figure 6-a is presented the eye diagram considering only the CD in a 95km link. This signal can be improved by means of electrical equalization, as it is shown in figure 6-b. In figure 6-c is presented an eye diagram obtained in the same systems, adding now the effect of PMD. It is noticeable the eye open closure due to the PMD. It is also evident in figure 6-d the improvement in the signal achieved by using electrical equalization.

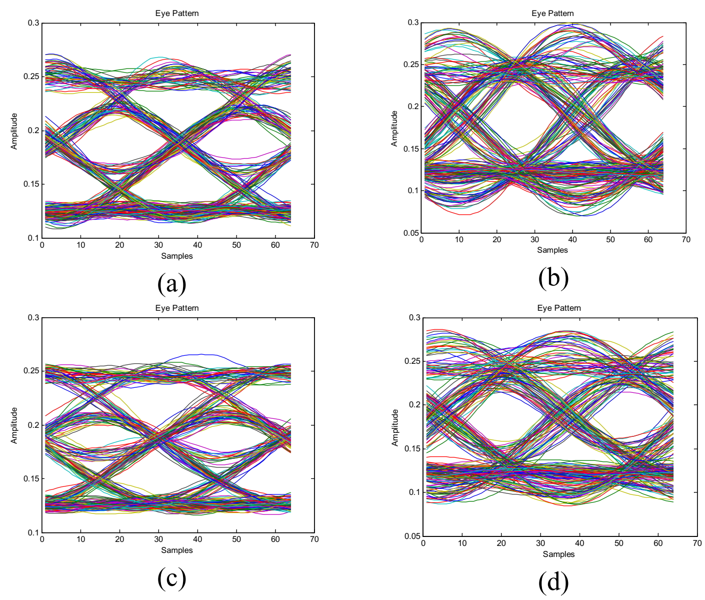


Figure 6 – 10Gbit/s Eye Patterns (a) Unequalized channel without PMD - 95km of SMF (b) Equalized channel without PMD - 95km of SMF (c)

Unequalized channel with PMD - 95km of SMF and 65ps of DGD (d) Equalized channel with PMD - 95km of SMF and 65ps of DGD

At 40Gbit/s, we can observe from figure 7 and 8 that 16 ps of DGD is fully compensated while achieving 4dB of improvement in the EOP for 24 ps DGD after 1 km of SMF. In extreme signal detection conditions - after 7 km of SMF - we may also see that an EOP improvement of 16 dB is theoretically possible for a 21 ps DGD, nevertheless in practice difficult signal detection may be experienced with such high level of impairment.

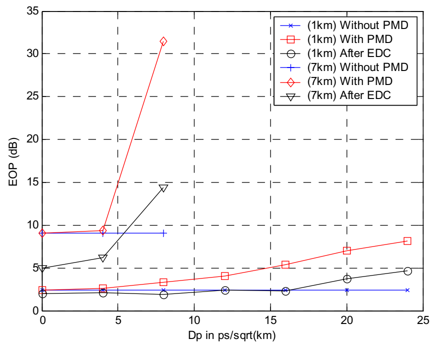
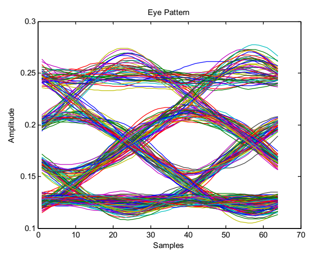
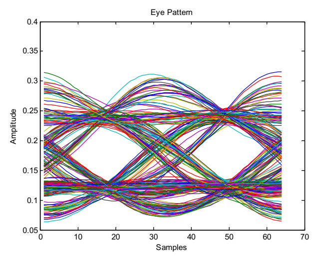


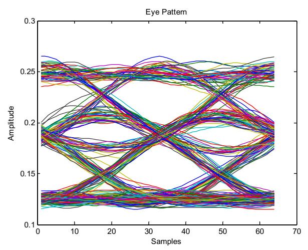
Figure 7 – EDC numerical results for a 40Gbit/s NRZ 512bits sequence over a SMF link. γ =0.7



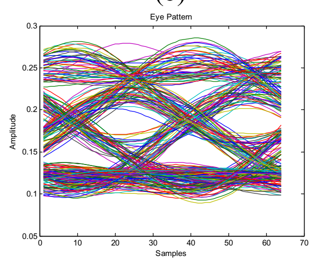
(a)



(b)



(c)



(d)

Figure 8 – 40Gbit/s Eye Patterns (a) Unequalized channel without PMD - 7km of SMF (b) Equalized channel without PMD - 7km of SMF (c) Unequalized channel with PMD - 7km of SMF and 20ps of DGD (d) Equalized channel with PMD - 7km of SMF and 20ps of DGD

Comparing figure 8-a with 6-a is visible that we obtain almost the same eye opening degradation in a 95km at 10Gbit/s or in a 7km system operating at 40Gbit/s, confirming the rule of thumb used in practice that degradation due to CD increases quadratically with the bit rate increase. In figures 8-c and 8-d is visible the difficulty of the electrical equalizer in improving the signal after a strong degradation and it is also evident the increasing of importance of PMD when the bit rates goes from 10 to 40Gbit/s.

VI. CONCLUSIONS

The FFE is a viable building block for EDC in multigigabit optical link. It is able to adaptively compensate for <65ps and <16ps of DGD at 10Gbit/s and 40Gbit/s, respectively. Improved performances may be expected as advanced high-speed electronic processing techniques become available.

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