

XTP056

ML605 Built-In Self Test Flash Application

May 2010



Overview

- Xilinx ML605 Board
- Software Requirements
- ML605 Setup
- ML605 BIST (Built-In Self Test)
- Run ML605 BIST Ready for Download Files
- Compile ML605 BIST Design
- Generate ML605 BIST Design CompactFlash

References

ML605 BIST Design Description

Description

 The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

Reference Design IP

- EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_sysmon_adc, xps_iic, xps_mch_emc, xps_sysace, util_io_mux, util_bus_split, util_vector_logic, xps_ll_temac, xps_tft, xps_epc
 - Embedded System Tools Reference Guide (UG111)
 - http://www.xilinx.com/ise/embedded/edk_ip.htm

Reference Design Source

- rdf0017.zip
- Available through http://www.xilinx.com/ml605

Xilinx ML605 Board





ISE Software Requirements

Xilinx ISE 12.1 software





EDK Software Requirement

Xilinx EDK 12.1 software



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Hardware Setup

- Set S2 to 011010 (1 = on, Position $6 \rightarrow$ Position 1)
- Set S1 to 1000 (Position $4 \rightarrow$ Position 1)
 - This enables JTAG configuration from the Compact Flash



- Power on the ML605 board for UART Drivers Installation
- Connect a USB Type-A to Mini-B cable to the USB UART connector on the ML605 board
 - Connect this cable to your PC



Install USB UART Drivers

 <u>https://www.silabs.com/Support Documents/Software/</u> <u>CP210x_VCP_Win2K_XP_S2K3.zip</u>

👰 WinZip - CP210x_VCP_Win2K_XP_	S2K3.zip		_ 🗆 🗙
File Actions Options Help			
🎋 📰 🗞 🚱 🖗 🌾			
Name	Path		Modified
CP210x_VCP_Win2K_XP_S2K3.exe			10/25/2009 4:59 PM
Selected 0 files, 0 bytes	Total 1 fil	e, 5,352KB	🖯 🗘 //.



Right-click on My Computer and select Properties

- Select the Hardware tab
- Click on Device Manager

Sys	stem Prop	erties	<u>? ×</u>
	System General	Restore Automatic Updates Remote Computer Name Hardware Advance	d
	Device M	lanager The Device Manager lists all the hardware devices installed on your computer. Use the Device Manager to change the properties of any device. <u>D</u> evice Manager	
	Drivers -	Driver Signing lets you make sure that installed drivers are compatible with Windows. Windows Update lets you set up how Windows connects to Windows Update for drivers. Driver <u>Signing W</u> indows Update	
	Hardware	Profiles Hardware profiles provide a way for you to set up and store different hardware configurations.	
		Hardware <u>P</u> rofiles	
_		OK Cancel App	ly

- Expand the Ports Hardware
 - Right-click on Silicon Labs
 CP210x USB to UART
 Bridge and select Properties



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 Under Port Settings tab Click Advanced Set the COM Port to an open Com Port setting from COM1 to COM4 	icon Labs CP210x US General Port Settings	B to UART Bridge (COM2) Properties ? × Driver Details Bits per second: 9600 Data bits: 8 Parity: None Stop bits: 1
Advanced Settings for COM2 Image: Use FIFO buffers (requires 16550 compatible UART) Select lower settings to correct connection problems. Select higher settings for faster performance. Receive Buffer: Low (1) Image: Image	○K Cancel Defaults	Elow control: None Advanced Restore Defaults OK Cancel

ML605 BIST Setup

- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your USB Com Port
 - Set the baud to 9600

💆 COM2:9600baud - Te	era Term VT			
File Edit Setup Contro	ol Window Resize Help			
	Tera Term: Serial port s	etup	×	-
	Port:	СОМ2 -	ОК	
	<u>B</u> aud rate:	9600 💌		
	<u>D</u> ata:	8 bit 💌	Cancel	
	P <u>a</u> rity:	none 💌		
	<u>S</u> top:	1 bit 💌	Help	
	Elow control:	none 💌		
	Transmit dela	ry c/ <u>c</u> har 0 ms	sec/ <u>l</u> ine	_

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Note: Tera Term may need to be restarted if board power is cycled

- Insert ML605 Evaluation Kit CompactFlash into the ML605
- Push SysACE Reset and view initial BIST screen
 - Type "1" to start the UART Test



COM2:9600baud - Tera Term VT	
e Edit Setup Control Window Resize Help	
***************************************	1
* Xilinx Virtex-6 FPGA ML605 Evaluation Kit **	

llart Test	
LED Test	
Timer Test	
FLASH Test	
IIC lest Ethouset Leashack Test	
Switch Test	
External Memory Test	
System Monitor Test	
PushButton Test	
LGD lest Suptom ACE CE Toot	
DUL/UGA Test	

UART Test completed

– Type 2 to begin LED Test

💯 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
18726 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)0000012c S-records Executing program starting at address: 00000000	

1: UART Test 2: LED Test 3: Timer Test	-

• View Walking 1's pattern on GPIO LEDs

- Sequence repeats six times
- LED Test completed
 - Type 3 to begin Timer Test

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
24198 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)000001f4 S-records Executing program starting at address: 00000000	

Watch the LEDs	

** Xilinx Virtex-6 FPGA ML605 Evaluation Kit **	

Choose Feature to Test:	
2: LED Test	
3: Timer Test	
4: FLHSH lest 5: IIC Test	_
6: Ethernet Loopback Test	
7: Switch Test	<u> </u>

Timer Test completed

- Type 4 to begin Flash test

💯 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
36766 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x>000002bc S-records Executing program starting at address: 00000000	

Choose Feature to Test: 1: UART Test 2: LED Test 3: Timer Test 4: FLASH Test	
5: IIC Test 6: Ethernet Loopback Test	-

Flash Test completed

– Type **5** to begin IIC EEPROM Test

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
54094 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)0000044c S-records Executing program starting at address: 00000000	

<pre>************************************</pre>	321 349 371 399 3C1 3E9
***************************************	-

IIC EEPROM Test completed

- Type 6 to begin Ethernet Loopback Test
 - PHY is put into internal loopback mode

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
43414 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)0000384 S-records Executing program starting at address: 00000000	

2: LED Test 3: Timer Test	-

Ethernet Loopback Test completed

- Set 8-position GPIO DIP Switch (SW1)
- Type 7 to begin GPIO Switch Test
 - Reads switch settings

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
113650 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)000008fc S-records Executing program starting at address: 00000000	

Transmitted Packet!	
Received Packet!	

Choose Feature to Test: 1: UART Test 2: LED Test	•

GPIO Switch Test completed

– Type 8 to begin External Memory Test

💹 COM2:9600baud - Tera Term VT	_ _ _ _ ×
File Edit Setup Control Window Resize Help	
24526 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)000001f4 S-records Executing program starting at address: 00000000	

${2}$	

Data read from Griv input is 0x0	

Choose Feature to Test:	
1: UAKI lest 2. LED Test	
3: Timer Test	
4: FLASH Test	
5: IIC Test	
6: Ethernet Loopback Test	-
Jr. Switch lest	

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	🖳 COM2:9	9600baud - Tera Term VT	
	File Edit	Setup Control Window Resize Help	
	40334 b Bootloa Executi	ytes read from file. SRECORDS at: 0x50100000 der: Processed (0x)00000320 S-records ng program starting at address: 00000000	^
ŀ	******	***************************************	
	******	**************************************	
ŀ	******	********	
	~~~~~~	~~~~~~~~~	
	Multi-Po Testing	ort Memory Controller Memory Test address range 0x50200000-0x5FFFFFF. or 1 of 1	
þ	Pass A)	ICache: On, DCache: On	
		TESTO: Write all memory to 0x00000000 and check Writing Reading	
I		Test Complete Status = SUCCESS	
		TEST1: Write all memory to ØxFFFFFFFF and check Writing Reading	
I		Test Complete Status = SUCCESS	
		TEST2: Testing for stuck together bank/row/col bits Clearing memory to zeros	
I		Test Complete Status = SUCCESS	
		TEST3: Testing for maximum ba/row/col noise This test performs 16 word writes followed by 16 word reads Each 64 bytes inverts the ba/row/col address Initializing Memory to ØxA5A5A5A5 Writing and Baading	
		Test Complete Status = SUCCESS TEST4: Testing for Inverse Data at Address Writing Reading	
		Test Complete Štatus = SUCCESS	
		Number of errors in this pass = Ø	-1

 External Memory Test running with caches on

Note: External Memory Test takes about 20 minutes

- Second part of External Memory test (caches off)
  - Type 9 to begin System Monitor Test

```
- 🗆 ×
  COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
Pass B) ICache: Off, DCache: Off
                                                                                     ٠
        TESTO: Write all memory to 0x00000000 and check
                 Writing...
                Reading...
        Test Complete Štatus = SUCCESS
        TEST1: Write all memory to 0xFFFFFFFF and check
                 Writing...
                 Reading...
        Test Complete Status = SUCCESS
        TEST2: Testing for stuck together bank/row/col bits
                Clearing memory to zeros...
                Writing and Reading...
        Test Complete Štatus = SUCČESS
        TEST3: Testing for maximum ba/row/col noise
                This test performs 16 word writes followed by 16 word reads
                Each 64 bytes inverts the ba/row/col address
                 Initializing Memory to 0xA5A5A5A5...
        Writing and Reading...
Test Complete Status = SUCCESS
        TEST4: Testing for Inverse Data at Address
                 Writing...
                 Reading...
        Test Complete Status = SUCCESS
                 Number of errors in this pass = 0
MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
```

#### System Monitor Test completed

- Type **A** to begin PushButton Test

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
75254 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)000005dc S-records Executing program starting at address: 00000000	<b>_</b>
***************************************	
**************************************	
***************************************	
***************************************	
Entering the SysMon Polled Example.	
The Present Temperature is 53.547 Centigrades.	
The Maximum Temperature is 53.955 Centigrades.	
The Minimum Temperature is 50.102 Centigrades.	
The Present VCCINT is 1.007 Volts.	
The Maximum VCCINT is 1.009 Volts.	
The Minimum VGGINI is 1.006 Volts.	
The Present VCCAUX is 2.495 Volts.	
The Maximum VCCAUX is 2.499 Volts.	
The Minimum VCCAUX is 2.494 Volts.	
The VCCINT Current is 3.964 Amps.	
The UCCINT Power is 3.995 Watts.	
The ML605 12V Voltage is 12.410 Volts. The ML605 12u Current is 1.584 Amus.	
Exiting the SysMon Polled Example.	

#### PushButton Test completed

- Type **B** to begin LCD Test



#### LCD Test completed

– Type **C** to begin System ACE CF Test

💹 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
26254 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)000001f4 S-records Executing program starting at address: 00000000	<b></b>
**************************************	
** MLbU5 - LCU lest ** **********************************	
Watch the LCD screen for text:	
**************************************	
**************************************	
1: UART Test 2: LED Test	
3: limer lest 4: FLASH Test 5: LIC Test	
6: Ethernet Loopback Test 7: Switch Test	-

**EXILINX**.

COM2:9600	baud - 1	Tera Term VI

File Edit Setup Control Window Resize Help

77430 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)00000640 S-records Executing program starting at address: 00000000

This program attempts to access the CF card's file system to perform file I/O operations.

Please insert a CF card with the contents of the directory <ref design install dir>/sw/standalone/testfatfs/required_files/ copied into a directory named test on that CF card.

```
Warning: This program will attempt to create a file and directory on the CF card.
```

File I/O Test Program running. Reading file : a:\test\test.txt This is a test file. 0123456789

abcdefghijklmnopqrstuvwxyz

Total bytes read = 60

```
Reading file : a:\test\xflow.log
dummy log file
```

Total bytes read = 16 Reading file : a:\test\xilfatfs.pdf Total bytes read = 59885 Failed to open a:\test\noexist.c: check if file present Total bytes read = 0

read done Writing file contents.

# of bytes written: 38 write done executing mkdir talica.. mkdir success

### System ACE CF Test completed

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- Connect a DVI
   Monitor to the
   ML605 board
- Type **D** to begin
   DVI/VGA Test

#### DVI/VGA Test completed

🖳 COM2:9600baud - Tera Term VT	
File Edit Setup Control Window Resize Help	
47062 bytes read from file. SRECORDS at: 0x50100000 Bootloader: Processed (0x)00000384 S-records Executing program starting at address: 00000000	•
***********	
×× ML605 - TFT Test ××	
***************************************	
Display color Painting Screen RED Painting Screen GREEN Painting Screen BLUE Writing Color Bar Pattern TFT test completed! You should see vertical color and grayscale bars	
across your VGA Output Monitor	
**************************************	•

#### Unzip the rdf0017.zip file

Available through http://www.xilinx.com/ml605

🗐 WinZip Pro - rdf0017.zip					
File Actions View Jobs Options He					
🏷 🥸 🚱 🚱 🖻 🖻 🏄					
Name	Path	Modified 🔺			
bootloader_linker_script.ld	ml605_bist\bootloader\	7/28/2009 12:25 PM			
executable.elf	ml605_bist\bootloader\	5/18/2010 11:52 AM			
🗐 blconfig.h	ml605_bist\bootloader\src\	7/15/2009 1:26 PM			
🗐 bootloader.c	ml605_bist\bootloader\src\	1/21/2010 1:47 PM			
🗐 errors.h	ml605_bist\bootloader\src\	11/15/2005 2:29 PM			
🗐 portab.h	ml605_bist\bootloader\src\	11/15/2005 2:29 PM			
🗐 srec.c	ml605_bist\bootloader\src\	7/28/2009 2:45 PM			
🗐 srec.h	ml605_bist\bootloader\src\	6/8/2009 10:47 AM			
bootloader_linker_script.ld	ml605_bist\bootloader_p30t\	7/28/2009 1:25 PM			
🔊 executable.elf	ml605_bist\bootloader_p30t\	5/18/2010 11:52 AM			
🗐 blconfig.h	ml605_bist\bootloader_p30t\src\	1/13/2010 5:19 PM			
Selected 0 files, 0 bytes Total 222 files, 98, 138KB					

**EXILINX**.



- Add a second USB Type-A to Mini-B cables to the USB JTAG connector on the ML605 board
  - Connect this cable to your PC





- Open XPS project <design path>\ system.xmp
- Launch XMD
  - Select Debug →
     Launch XMD... (1)



#### Download the bitstream with xmd:

#### fpga -f ready_for_download/download.bit

C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe	
Did not find timing summary in SysACE_CompactFlash's synthesis log file Did not find device sumary in Hard_Ethernet_MAC's synthesis log file Did not find timing summary in Hard_Ethernet_MAC's synthesis log file Did not find device sumary in LCD_GPIO's synthesis log file Did not find timing summary in LCD_GPIO's synthesis log file Did not find device sumary in Display_Cntlr's synthesis log file Did not find timing summary in Display_Cntlr's synthesis log file Did not find device sumary in Display_Cntlr's synthesis log file Did not find device sumary in xps_epc_0's synthesis log file Did not find device sumary in xps_epc_0's synthesis log file Did not find device sumary in util_vector_logic_2's synthesis log file Did not find timing summary in util_vector_logic_0's synthesis log file Did not find device sumary in util_vector_logic_0's synthesis log file Did not find device sumary in util_vector_logic_0's synthesis log file Did not find device sumary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file Did not find device sumary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file Did not find timing summary in util_vector_logic_1's synthesis log file	
JIAG chain configuration	
Device ID Code IR Length Part Name 1 0a001093 8 System_ACE_CF 2 24250093 10 XC6VLX240T XMD% fpga -f ready_for_download/download.bit_	<b>-</b>

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#### Connect XMD to the MicroBlaze:

#### connect mb mdm

C:\Xilinx\12	.1\ISE_DS\EDK\bin\	nt\xbash.exe		
Did not fin Did not fin Did not fin Did not fin Conversion	nd device sumar nd timing summa nd device sumar nd timing summa to XML complet	y in util_ve ry in util_v y in util_ve ry in util_v re.	ector_logic_0's synthesis log file vector_logic_0's synthesis log file ector_logic_1's synthesis log file vector_logic_1's synthesis log file	
XMD%				
JTAG chain	configuration			
Device II 1 Øa 2 24 XMD% fpga - Fpga Progra Ø40.Don JTAG chain	D Code I a001093 4250093 -f ready_for_do amming Progress ne configuration	R Length 8 10 wnload/down] 10	Part Name System_ACE_CF XC6ULX240T load.bit 20304050 01020	3
Device ID 1 Øa 2 24	D Code I a001093 4250093	R Length 8 10	Part Name System_ACE_CF XC6VLX240T	
Successfull XMD% connec	ly downloaded b ct mb mdm	oit file.		-

**EXILINX**.

#### Download the bootloader with xmd:

#### dow ready_for_download/executable.elf

con

C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe	
XMD% dow ready_for_download/executable.elf	
System Reset DONE	
Downloading Program ready_for_download/executable_elf	
section, .vectors.reset: 0x0000000_0x0000000?	
section, .vectors.sw_exception: 0x0000008-0x00000004	
section, .vectors.interrupt: 0x00000010-0x00000017	
section, vectors.hw_exception: 0x00000020-0x00000027	
section, text: 0x41a00000-0x41a143db	
Section, init: $0X41a1430C = 0X41a14403$	
Section, $v_{0,1}$ and $v_{0,1}$ and $v_{0,1}$ and $v_{1,1}$	
section sdata?: 0x41a15134-0x41a15135	
section, data: 0x41a15138-0x41a156c3	
sectionctors: 0x41a156c4-0x41a156cb	
section, .dtors: 0x41a156cc-0x41a156d3	
section, .eh_frame: 0x41a156d4-0x41a156d7	
section, .jcr: 0x41a156d8-0x41a156db	
section, .bss: 0x41a156e0-0x41a18a23	
section, heap: 0x0000050-0x0000044f	
section, .stack: 0x0000450-0x0000144f	
Setting PC with Program Start Hddress 0x00000000	
YMDy cost	
RUNNING> XMD%	-

Bootloader runs in the terminal window







- The BIST Design is compiled with EDK
- Generate the libraries needed to create the bitstream
  - Select Software →
     Generate Libraries
     and BSPs (1)

📀 Xilinx Platform Studio - C:\ml60	5_bist\system.xmp	
File Edit View Project Hardware	Software Device Configuration Debug Simulation	Window Help
Project	Software Platform Settings	
Platform	Assign Default <u>D</u> rivers	
Project Files     MHS File: system.mhs     MSS File: system.mss     UCF File: data/system.ucf     iMPACT Command File: etc/dow     Implementation Options File: et     Bitgen Options File: etc/bitgen.     Project Options     Device: xc6vlx240tff1156-1     Netlist: TopLevel     Implementation: XPS (Xflow)     HDL: Verilog     Sim Model: BEHAVIORAL     Design Summary     Project Applications      Generate Libraries and Drivers	LIPG       Generate Libraries and BSPs         Image: Add Software Application Project         Image: Build All User Applications         Get Program Size         Image: Generate Linker Script         Image: Clean Libraries         Image: Clean Software         Image: Clean Software	1

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- Compile the Software Applications and create the application ELF files
  - Select Software →
     Build All User
     Applications (1)

🧇 Xilinx Platform Studio - C:\ml60	5_bist\sy	stem.xmp				
File Edit View Project Hardware	S <u>o</u> ftware	Device Configuration	Debug	Simulation	Window	Help
Project Platform	Softw Assign	are Platform Settings… n Default <u>D</u> rivers				
<ul> <li>Project Files</li> <li>MHS File: system.mhs</li> <li>MSS File: system.mss</li> <li>UCF File: data/system.ucf</li> <li>iMPACT Command File: etc/dow</li> <li>Implementation Options File: etc</li> <li>Bitgen Options File: etc/bitgen.ut</li> <li>Project Options</li> <li>Device: xc6vlx240tff1156-1</li> <li>Netlist: TopLevel</li> <li>Implementation: XPS (Xflow)</li> <li>HDL: Verilog</li> <li>Sim Model: BEHAVIORAL</li> <li>Design Summary</li> </ul>	LibG Gener Carlos Add S Add S Build A Get P Clean Clean Clean Clean Clean IP Catalog	ate Libraries and BSPs oftware Application Pro All User Applications rogram Size rate Linker Script Libraries Programs Software	ject		1	

**EXILINX** 

- Create the hardware design, system.bit, located in
   <project directory> /implementation
  - Select Hardware →
     Generate Bitstream (1)

File       Edit       View       Project       Hardware       Software       Device Configuration       Debug       Simulation       Window       Help         Project       Btg       Generate       Netlist       Image: Configuration       Image: Configuration	📀 Xilinx Platform Studi	o - C:\ml605_bist\system.xmp	
Project     Big Generate Netlist       Platform     Generate Bitstream       Project Files     Create or Import Peripheral       MHS File: system.m:     Create or Import Peripheral       UCF File: data/syste     Configure Coprocessor	File Edit View Project	Hardware Software Device Configuration Debug Simu	lation Window Help
Platform     Generate Bitstream     1       Image: Project Files     Image: System.m.     Image: System.m.       Image: MHS File: system.m.     Image: System.m.     Image: System.m.	Project	路명 Generate <u>N</u> etlist	
Project Files     MHS File: system.m     MSS File: system.m     Oreate or Import Peripheral     MSS File: system.m     Oreate or Import Peripheral     Oreate or Import Peripheral     Oreate or Import Peripheral     Oreate or Import Peripheral	Platform	🔛 Generate Bitstream 🗧 🗧 🚺	
Implementation Options File:       Launch Clock Wizard         Project Options       Check and View Core Licenses         Device: xc6vlx240t       Clean Netlist         Netlist: TopLevel       Clean Bits         Implementation: XP       Clean Hardware         Sim Model: BEHAVIORAL       Clean Hardware         Design Summary       Clean Hardware         Project Applications       Implementation: XP         Project Applications       Project         Project Applications       Implementation: XP         Project Applications       Project         Project Applications       Project	Project Files     MHS File: system.m     MSS File: system.m     UCF File: data/syst     iMPACT Command F     Implementation Op     Bitgen Options File:     Project Options     Device: xc6vlx240t     Netlist: TopLevel     Implementation: XP     HDL: Verilog     Sim Model: BEHAVIO     Design Summary      Project    Applica     Generate Bitstream	Create or Import Peripheral Configure Coprocessor Launch Clock Wizard Check and View Core Licenses Clean Netlist Clean Bits Clean Hardware Clean Hardware RAL	

**EXILINX**.

- Init memory with the Bootloader Application ELF
  - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
  - Select Device
     Configuration →
     Update Bitstream (1)



# **Generate ML605 BIST Design CompactFlash**

- Convert the ELF files to S-record format and create ACE file
  - Select Project →
     Launch Xilinx Bash
     Shell (1)

📀 Xilinx Platfor	rm Studio - C:\ml605_bist\system.xmp	
File Edit View	Project Hardware Software Device Configuration Debug Simulation Window He	lelp
Project	Project Options	
Platform  Platform  Project Files  MHS File:  UCF File:  MPACT C  Implemen  Bitgen Op  Project Opti Device: xi  Netlist: To Implemen HDL: Verili Sim Model Design Sum  Project	<ul> <li>Export Hardware Design to SDK</li> <li>Archive Project</li> <li>Generate Block Diagram Image</li> <li>Generate and View Design Report</li> <li>View Design Summary</li> <li>Rescan User Repositories</li> <li>Launch Xlimx Bash Shell</li> <li>Qustomize Buttons</li> <li>Clean All Generated Files</li> <li>Terminate Running Process</li> </ul>	
Launch Xilinx Bash Shell		

## Generate ML605 BIST Design CompactFlash

### Generate the S Records and ACE file

cd ready_for_download

./genace_all.sh

Copy the contents of ready_for_download/cf_image to your CompactFlash







### References

### EDK Documentation

- Embedded System Tools Reference Guide

http://www.xilinx.com/support/documentation/sw manuals/xilinx12 1/est rm.pdf

#### System ACE CF

System ACE CompactFlash Solution

http://www.xilinx.com/support/documentation/boards and kits/ug080.pdf

#### Virtex-6 Configuration

Virtex-6 FPGA Configuration User Guide

http://www.xilinx.com/support/documentation/user_guides/ug360.pdf







### **Documentation**

#### Virtex-6

- Virtex-6 FPGA Family

http://www.xilinx.com/products/virtex6/index.htm

#### ML605 Documentation

- Virtex-6 FPGA ML605 Evaluation Kit

http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards and kits/ug535.pdf

