ML605 Built-In Self Test Flash Application

May 2010

XTP056

Overview

- Xilinx ML605 Board
- Software Requirements
- ML605 Setup
- ML605 BIST (Built-In Self Test)
- Run ML605 BIST Ready for Download Files
- Compile ML605 BIST Design
- Generate ML605 BIST Design CompactFlash
- References

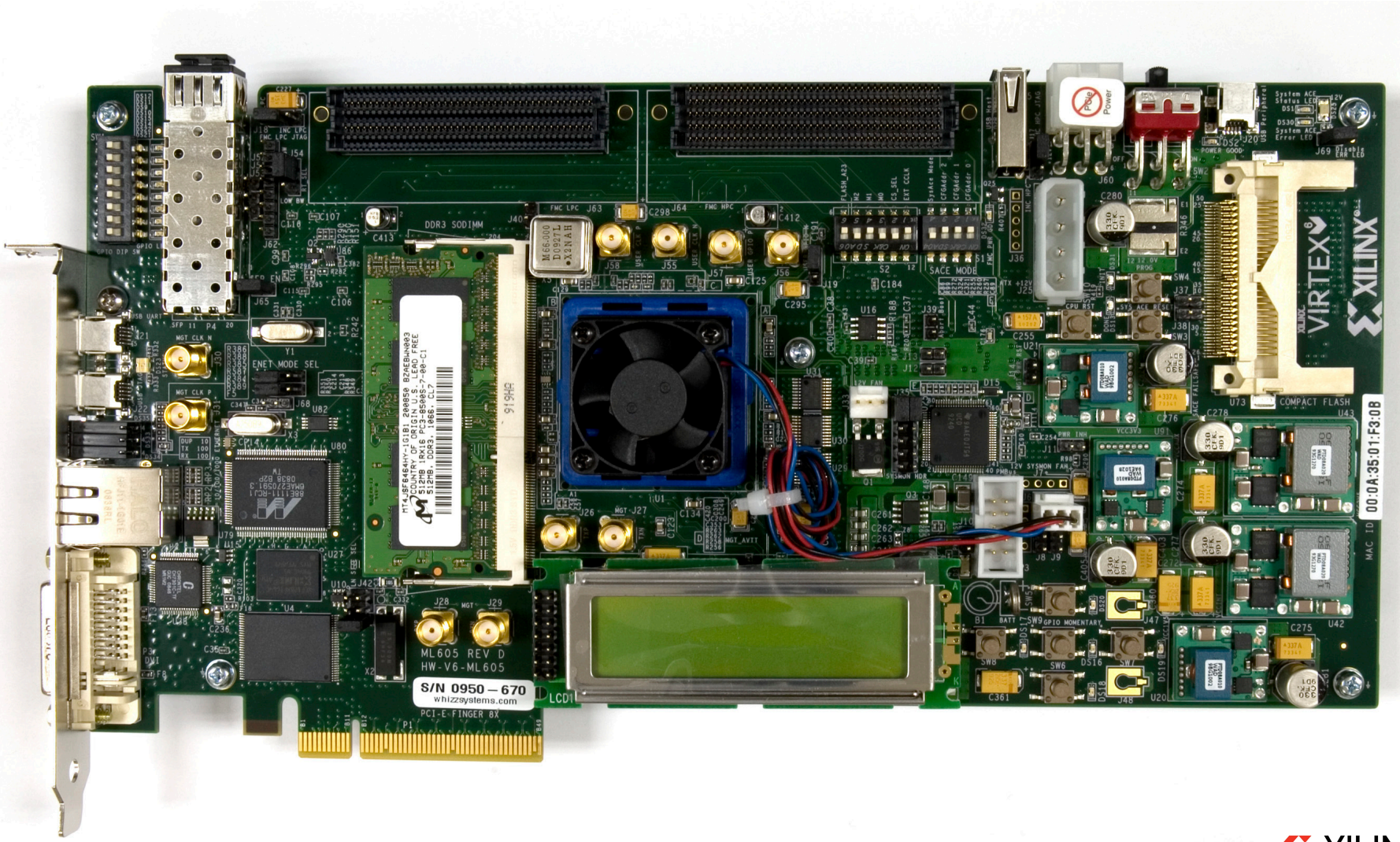
Note: This presentation applies to the ML605

ML605 BIST Design Description

- **Description**
  - The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.
- **Reference Design IP**
  - EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_sysmon_adc, xps_iic, xps_mch_emc, xps_sysace, util_io_mux, util_bus_split, util_vector_logic, xps_ll_temac, xps_tft, xps_epc
    - Embedded System Tools Reference Guide (UG111)
    - http://www.xilinx.com/ise/embedded/edk_ip.htm
- **Reference Design Source**
  - rdf0017.zip
  - Available through http://www.xilinx.com/ml605

Note: Presentation applies to the ML605

Xilinx ML605 Board



Note: Presentation applies to the ML605

ISE Software Requirements

- Xilinx ISE 12.1 software

Note: Presentation applies to the ML605

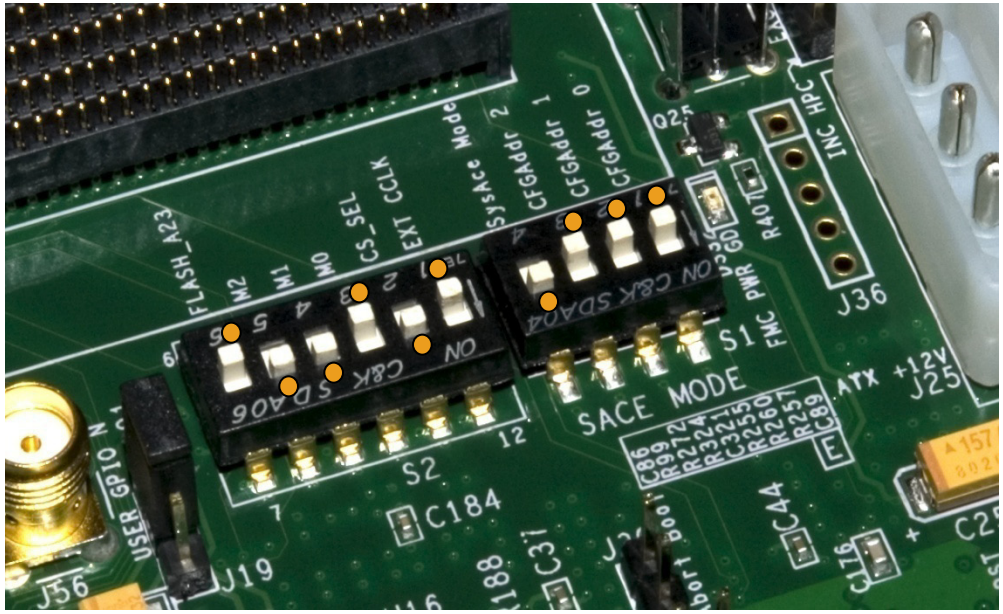
EDK Software Requirement

- Xilinx EDK 12.1 software

Note: Presentation applies to the ML605

Hardware Setup

- **Set S2 to 011010 (1 = on, Position 6 → Position 1)**
- **Set S1 to 1000 (Position 4 → Position 1)**
  - This enables JTAG configuration from the Compact Flash



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ML605 Setup

- **Power on the ML605 board for UART Drivers Installation**
- **Connect a USB Type-A to Mini-B cable to the USB UART connector on the ML605 board**
  - Connect this cable to your PC

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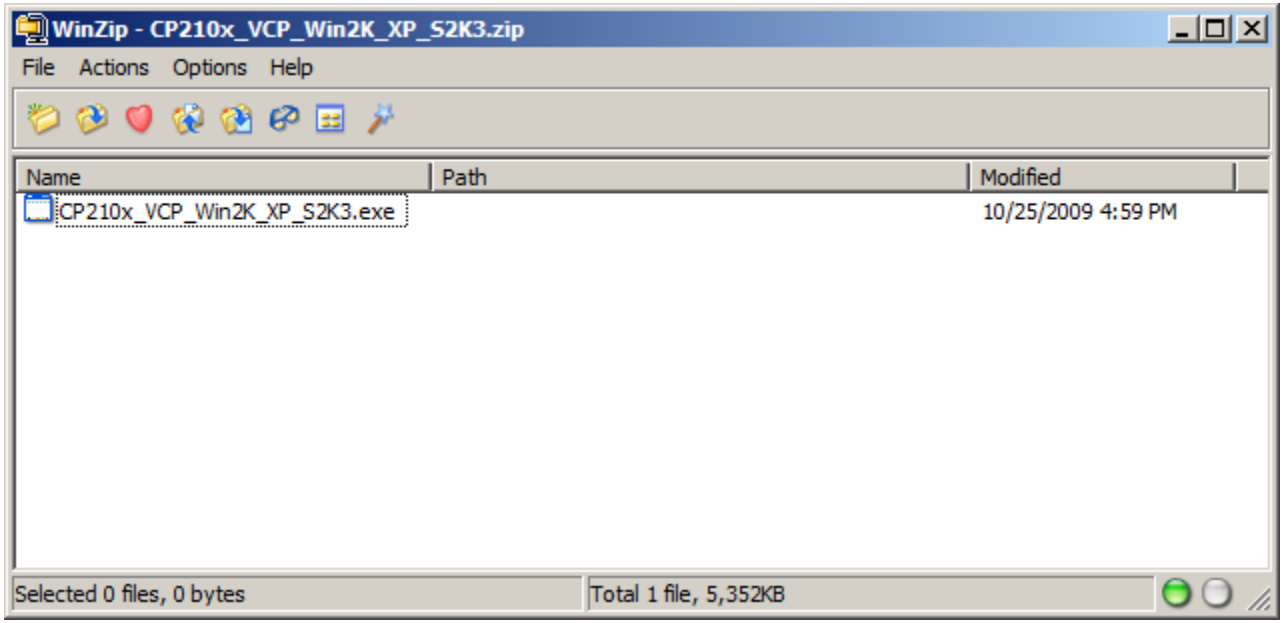
ML605 Setup

- **Install USB UART Drivers**
  - https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip



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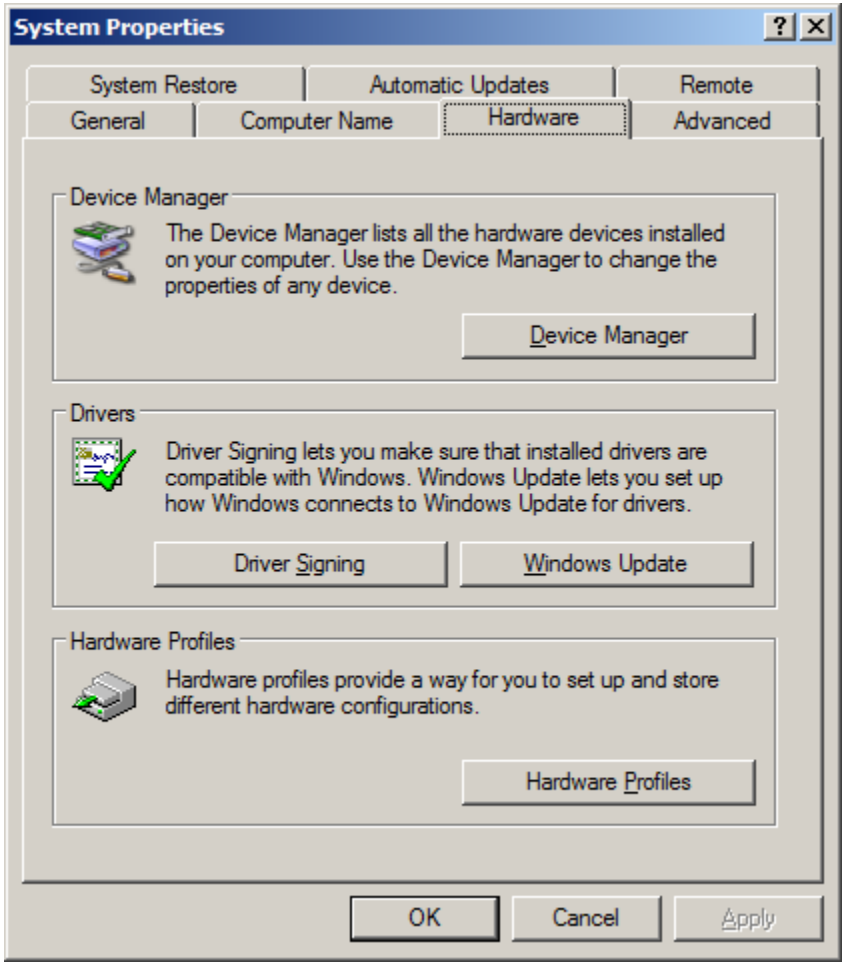
ML605 Setup

- **Right-click on My Computer and select Properties**
  - Select the Hardware tab
  - Click on Device Manager



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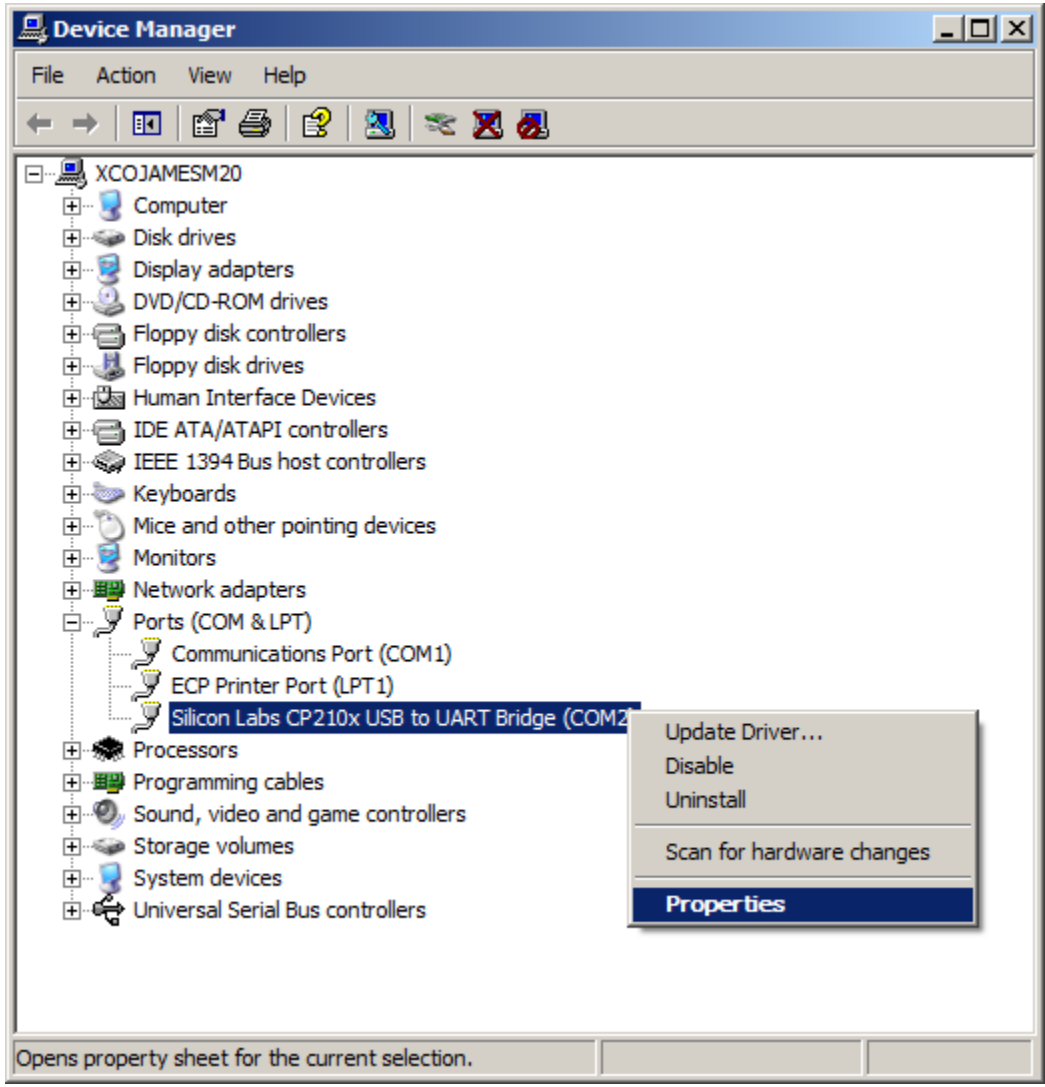
ML605 Setup

- **Expand the Ports Hardware**
  - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties



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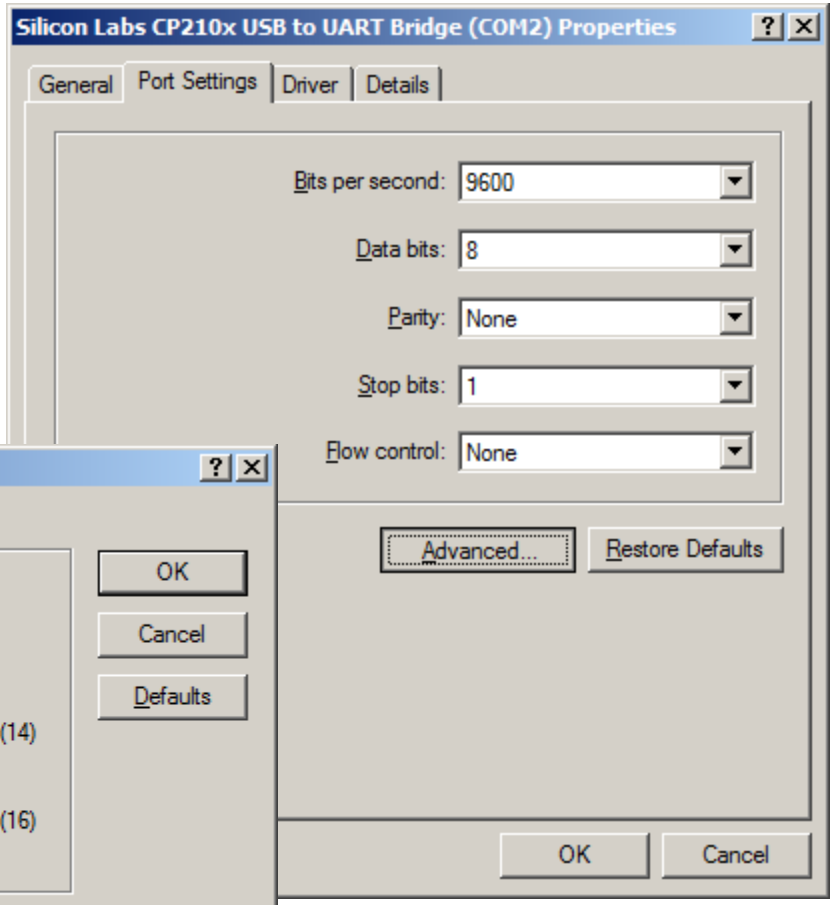
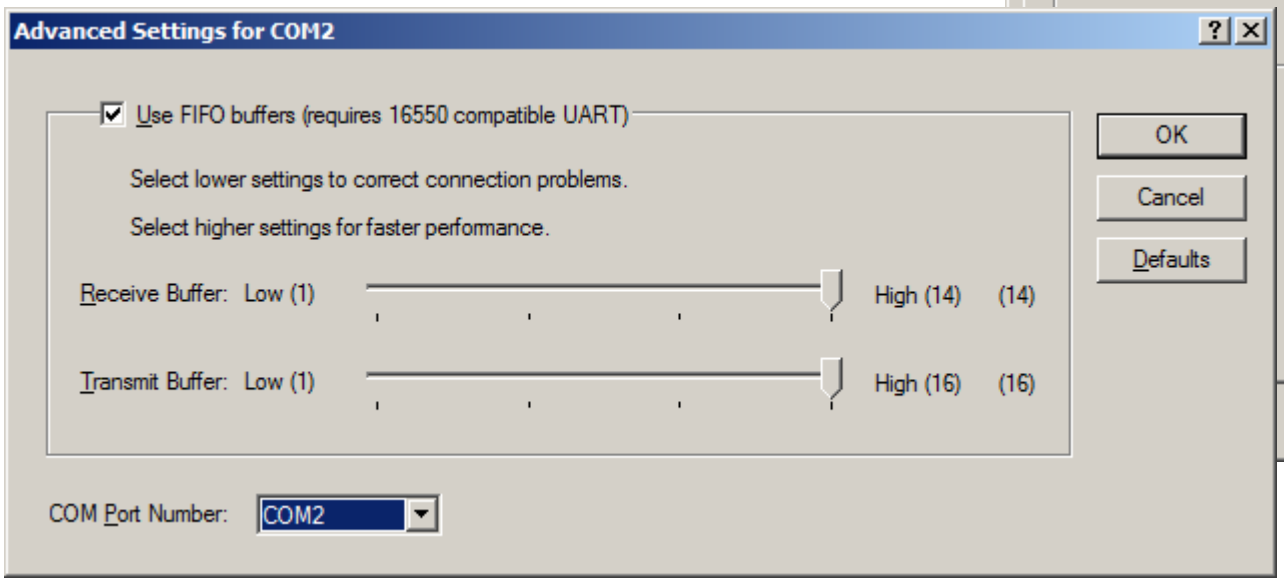
ML605 Setup

- **Under Port Settings tab**
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4





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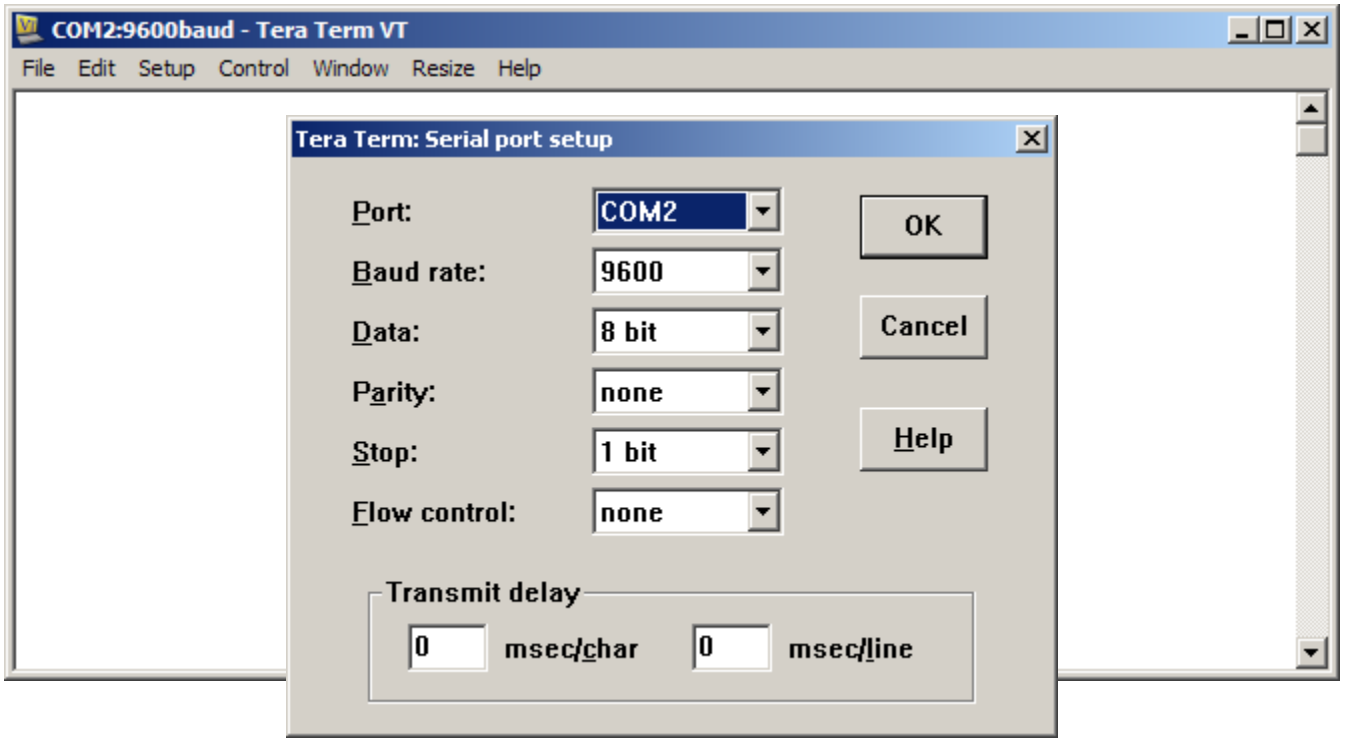
ML605 BIST Setup

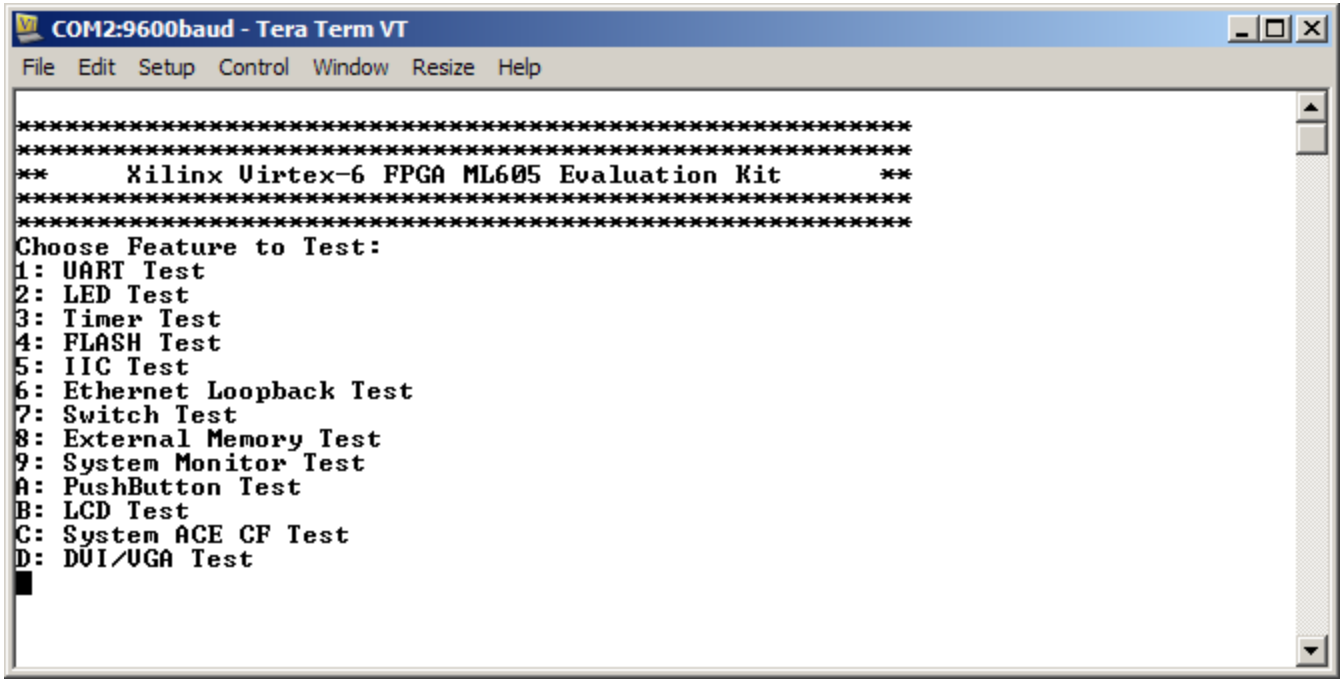
- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
  - Select your USB Com Port
  - Set the baud to 9600



Note: Tera Term may need to be restarted if board power is cycled

ML605 BIST

- **Insert ML605 Evaluation Kit CompactFlash into the ML605**
- **Push SysACE Reset and view initial BIST screen**
  - Type "**1**" to start the UART Test



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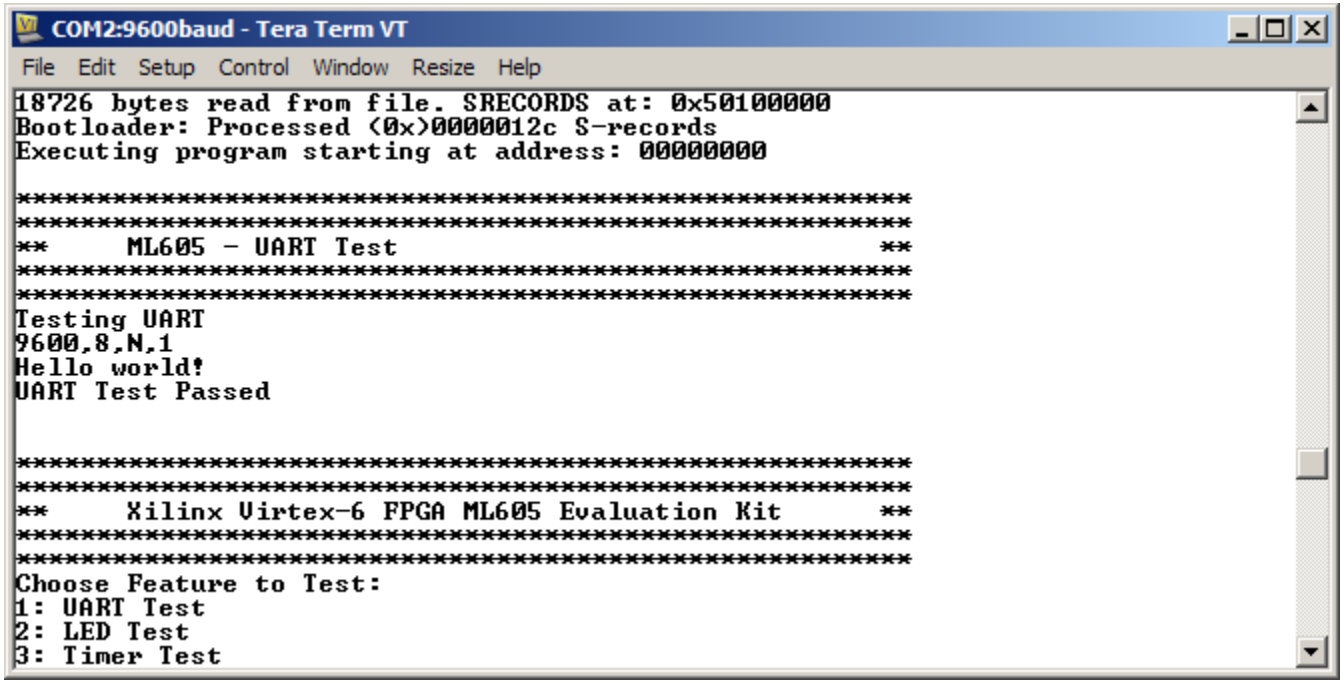
ML605 BIST

- **UART Test completed**
  - Type **2** to begin LED Test



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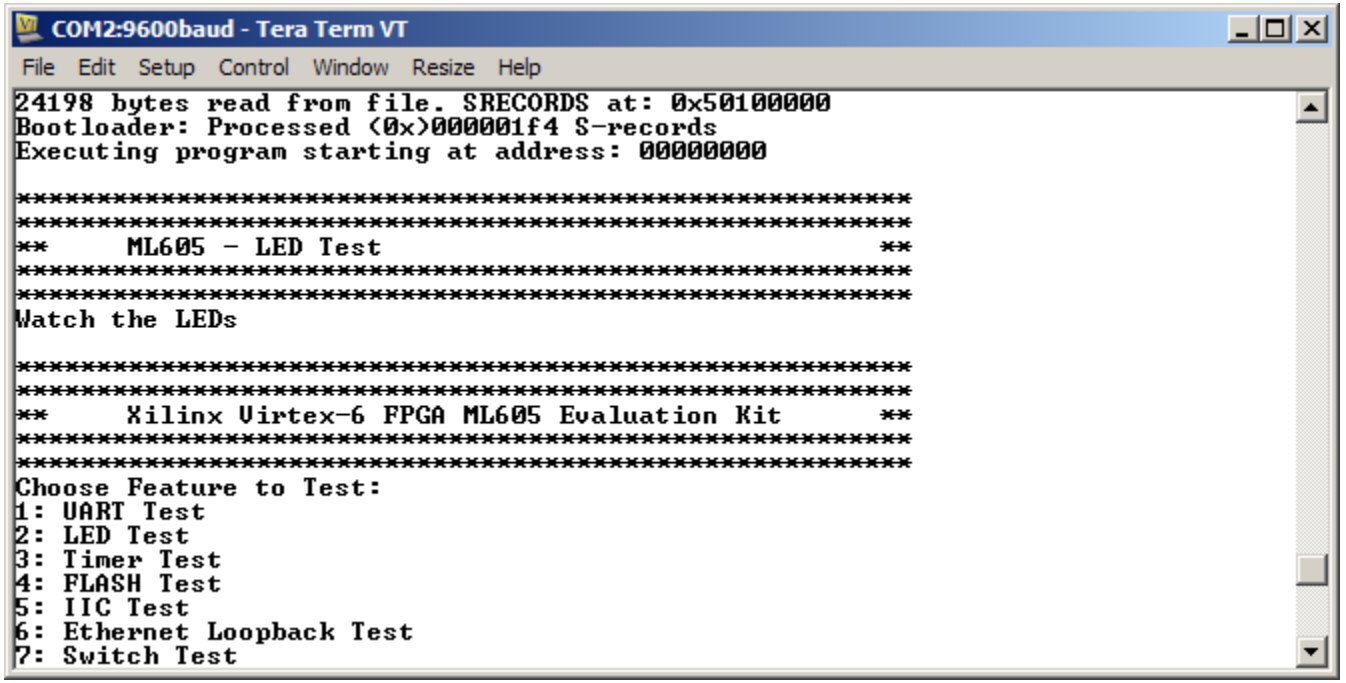
ML605 BIST

- **View Walking 1's pattern on GPIO LEDs**
  - Sequence repeats six times
- **LED Test completed**
  - Type **3** to begin Timer Test



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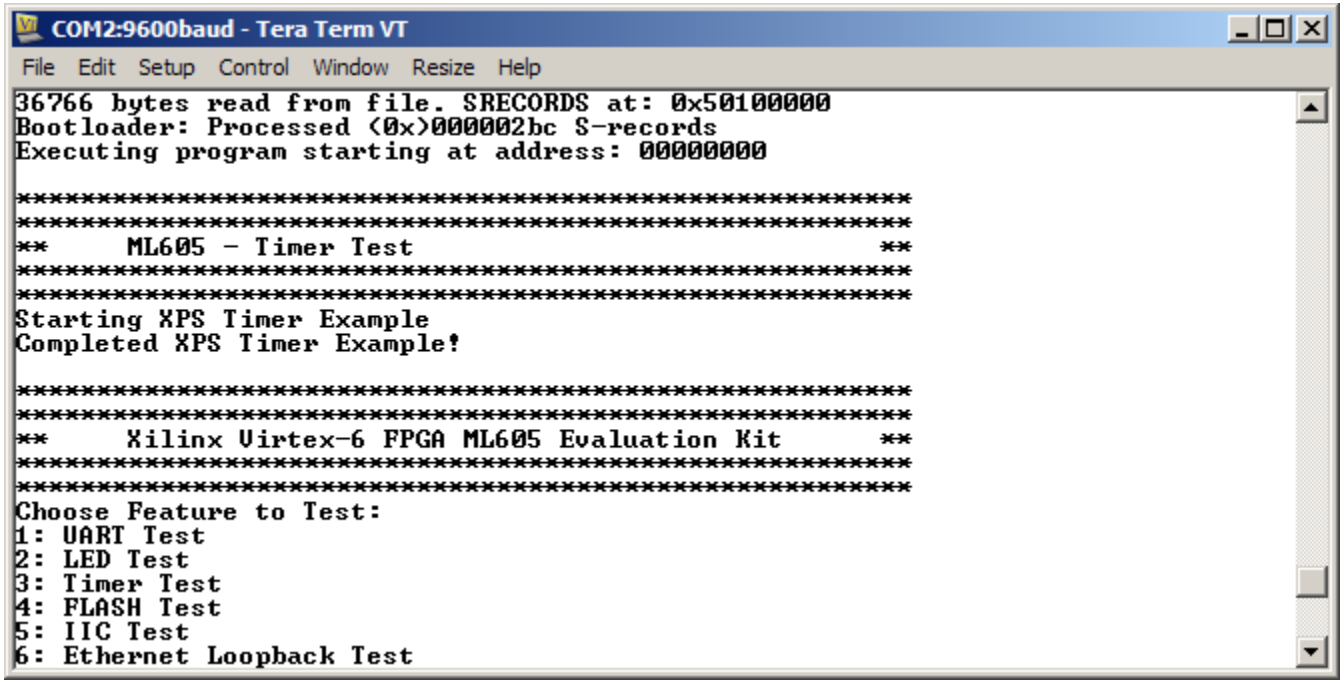
- **Timer Test completed**
  - Type **4** to begin Flash test



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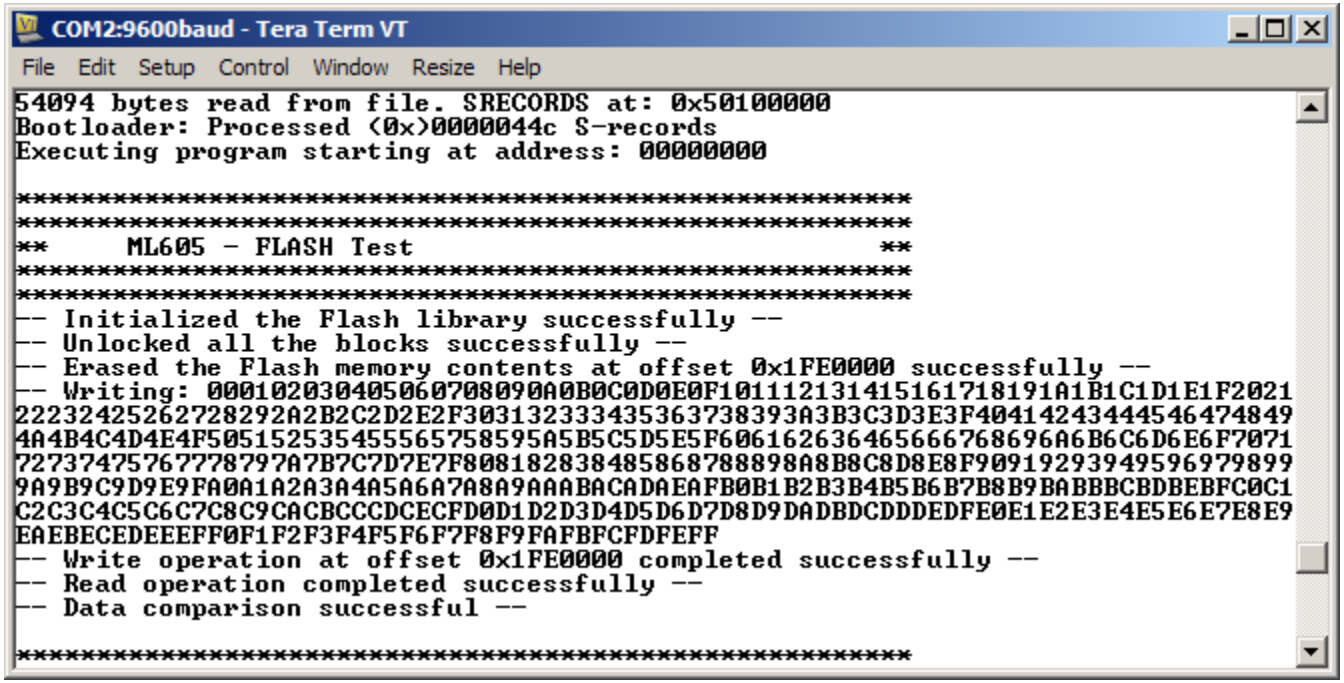
ML605 BIST

- **Flash Test completed**
  - Type **5** to begin IIC EEPROM Test



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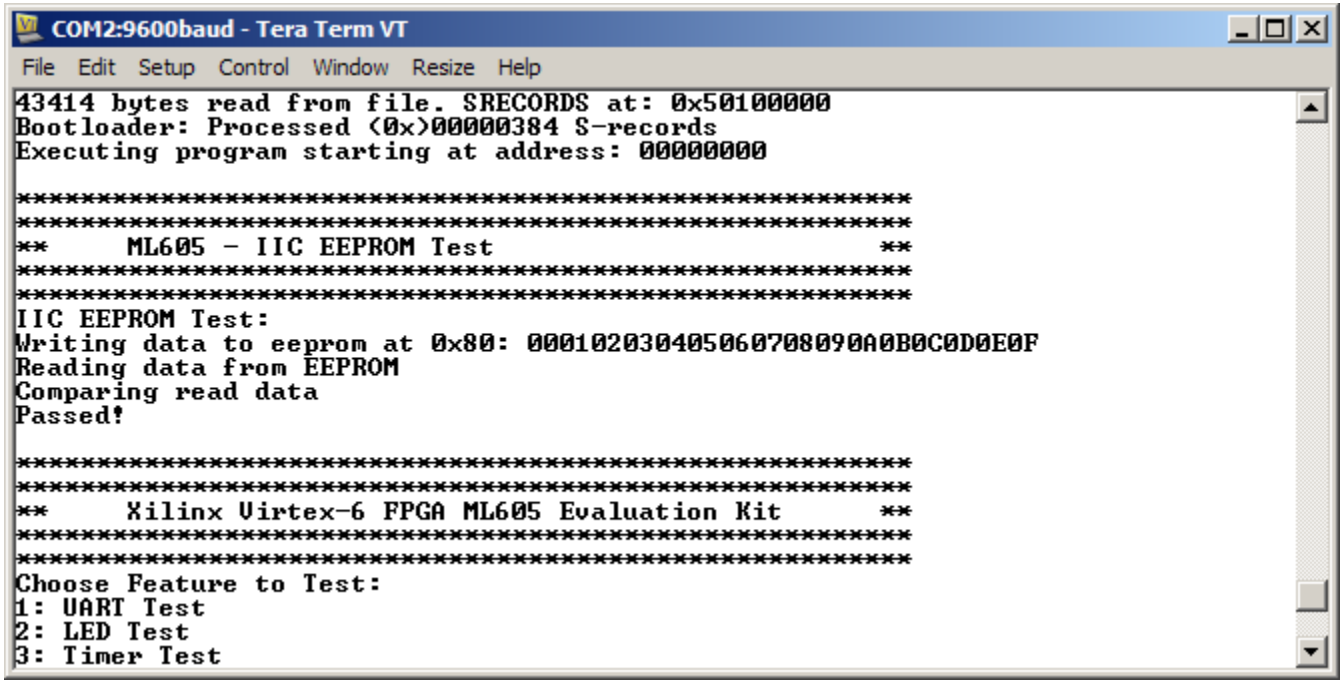
ML605 BIST

- **IIC EEPROM Test completed**
  - Type **6** to begin Ethernet Loopback Test
    - PHY is put into internal loopback mode



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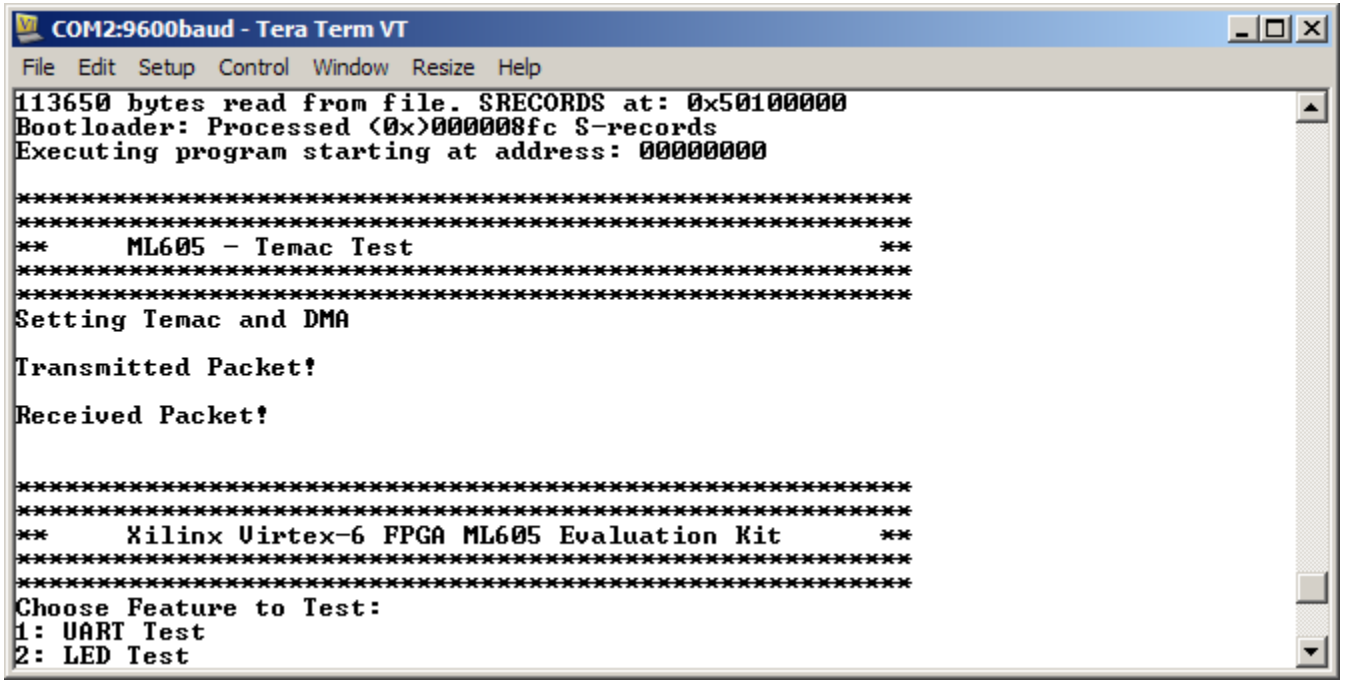
- **Ethernet Loopback Test completed**
  - Set 8-position GPIO DIP Switch (SW1)
  - Type **7** to begin GPIO Switch Test
    - Reads switch settings



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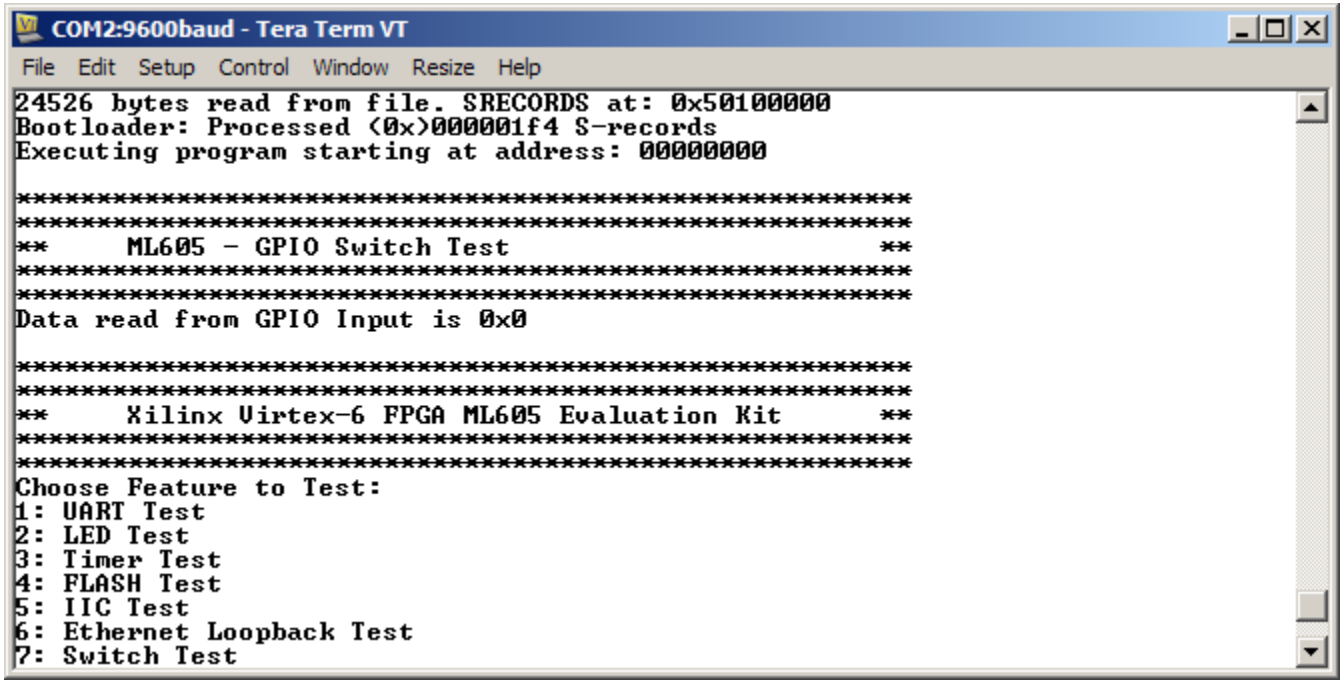
- **GPIO Switch Test completed**
  - Type **8** to begin External Memory Test



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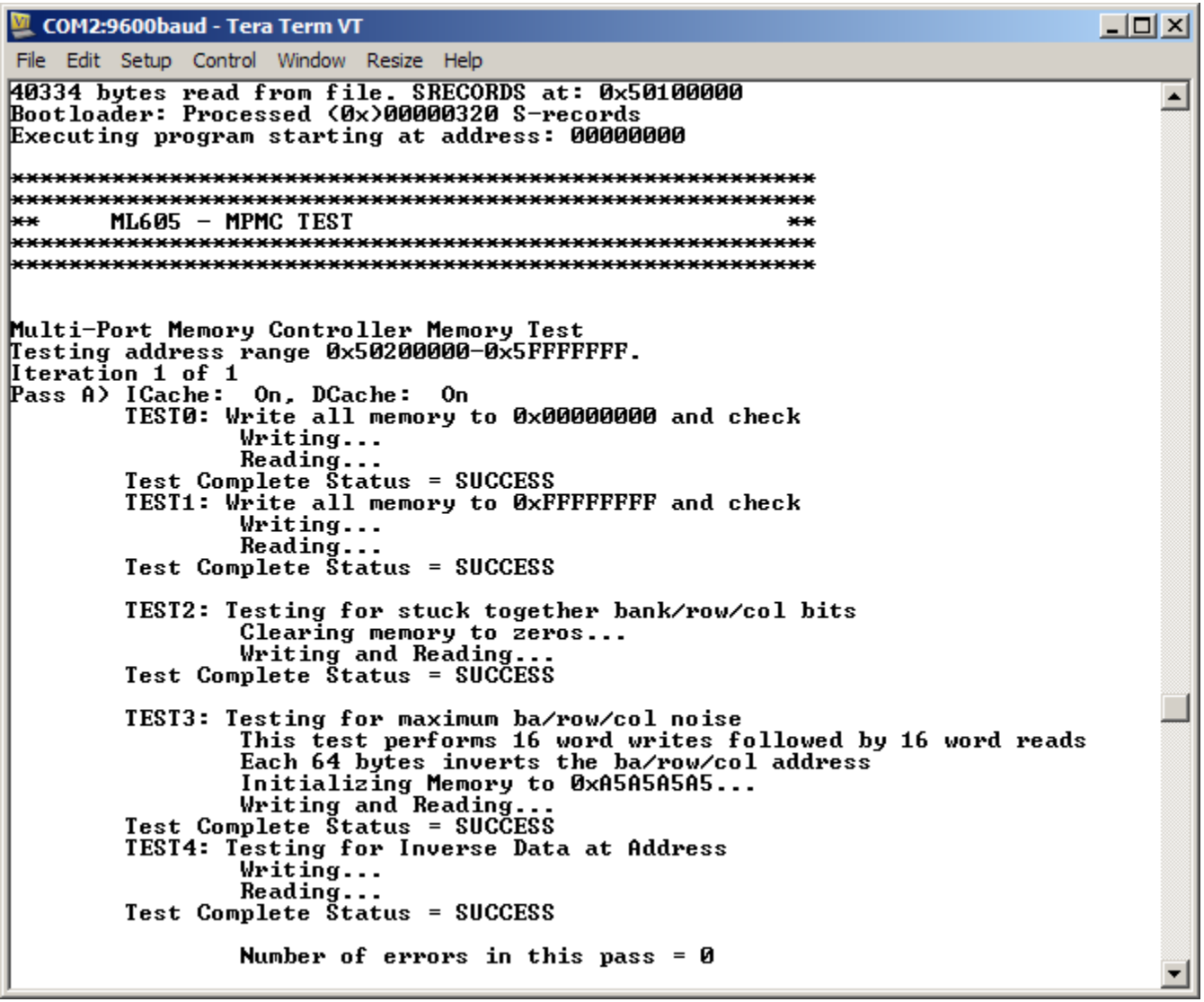
ML605 BIST



- External Memory Test running with caches on

Note: External Memory Test takes about 20 minutes

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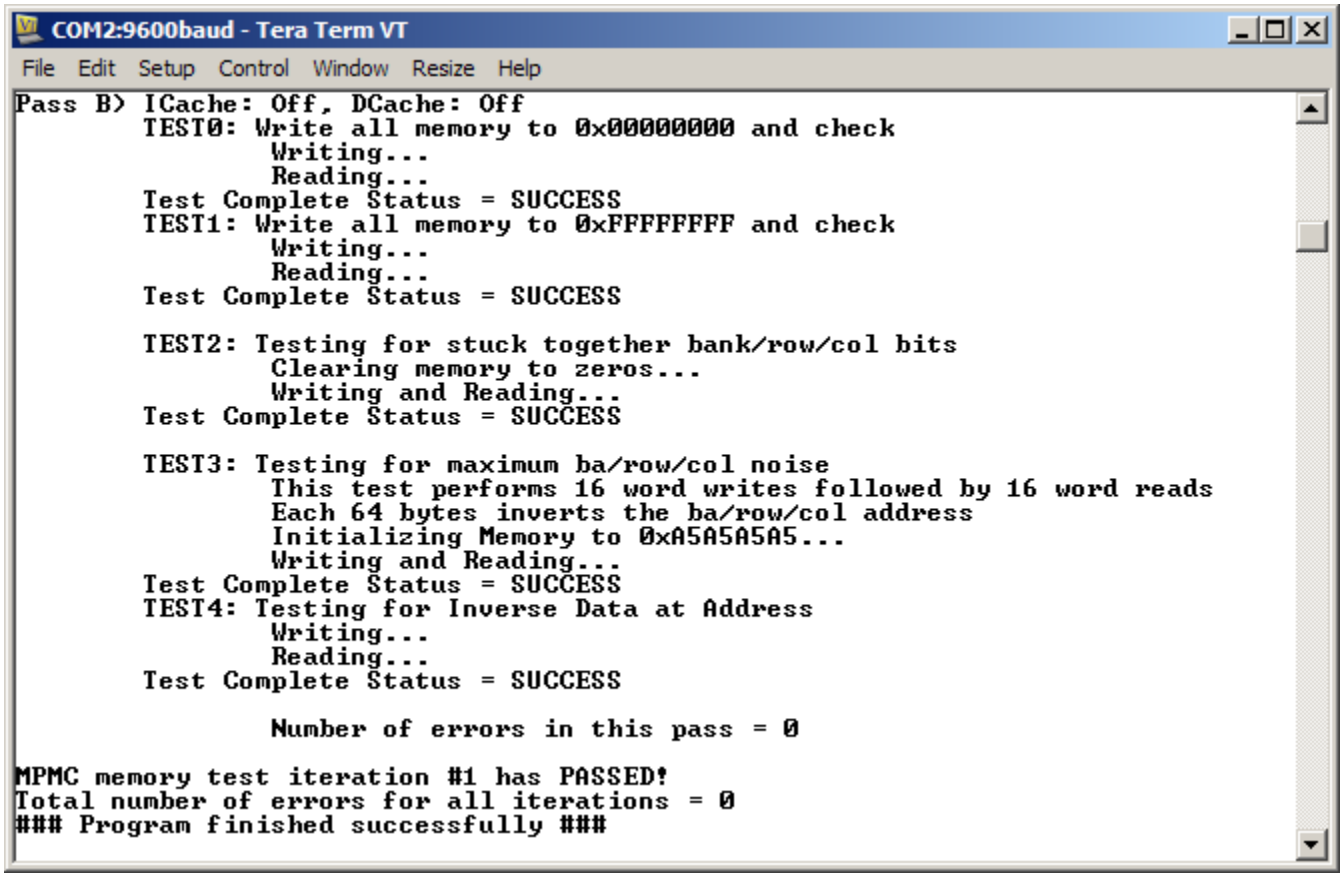
- **Second part of External Memory test (caches off)**
  - Type **9** to begin System Monitor Test



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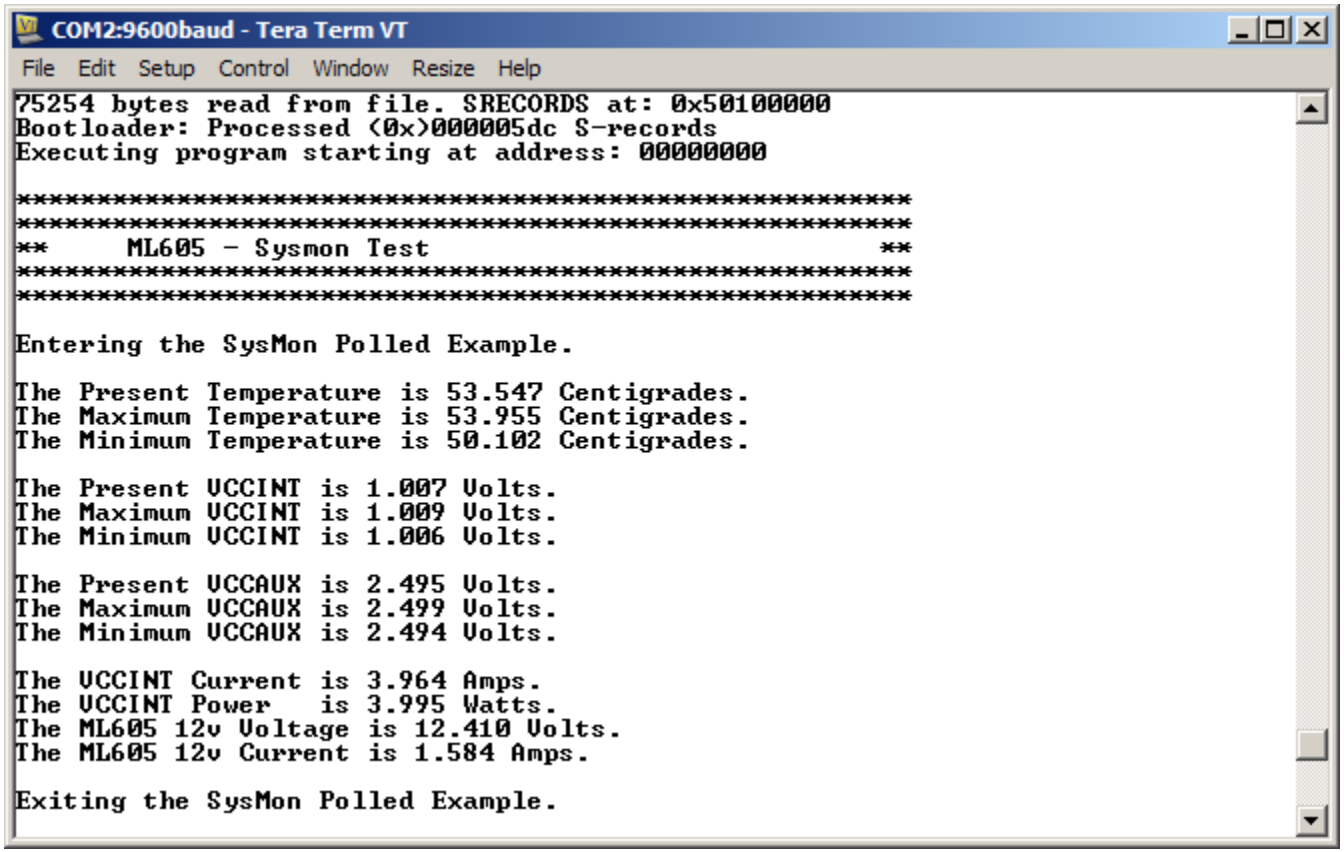
- **System Monitor Test completed**
  - Type **A** to begin PushButton Test



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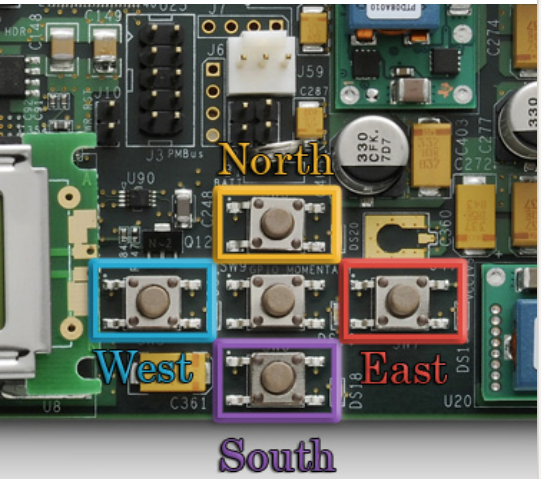
ML605 BIST

- **PushButton Test completed**
  - Type **B** to begin LCD Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Resize Help

```
18870 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000012c S-records
Executing program starting at address: 00000000

**************************************************************
**************************************************************
**      ML605 - Button Test                                 **
**************************************************************
**************************************************************
Press West Button & see if LED 0 glows

Press South Button & see if LED 1 glows

Press East Button & see if LED 2 glows

Press North Button & see if LED 3 glows

Press Center Button & see if all the 4 LEDs  glow


**************************************************************
**************************************************************
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit           **
**************************************************************
```

Note: Presentation applies to the ML605

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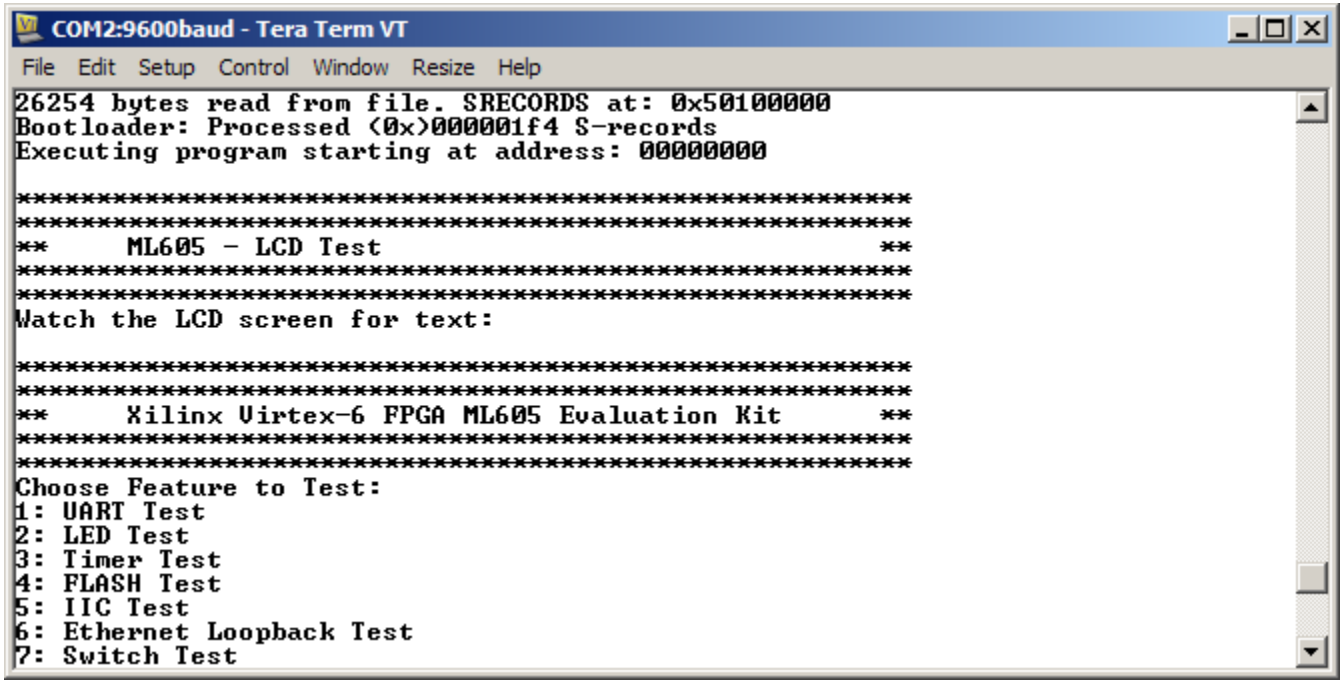
- **LCD Test completed**
  - Type **C** to begin System ACE CF Test



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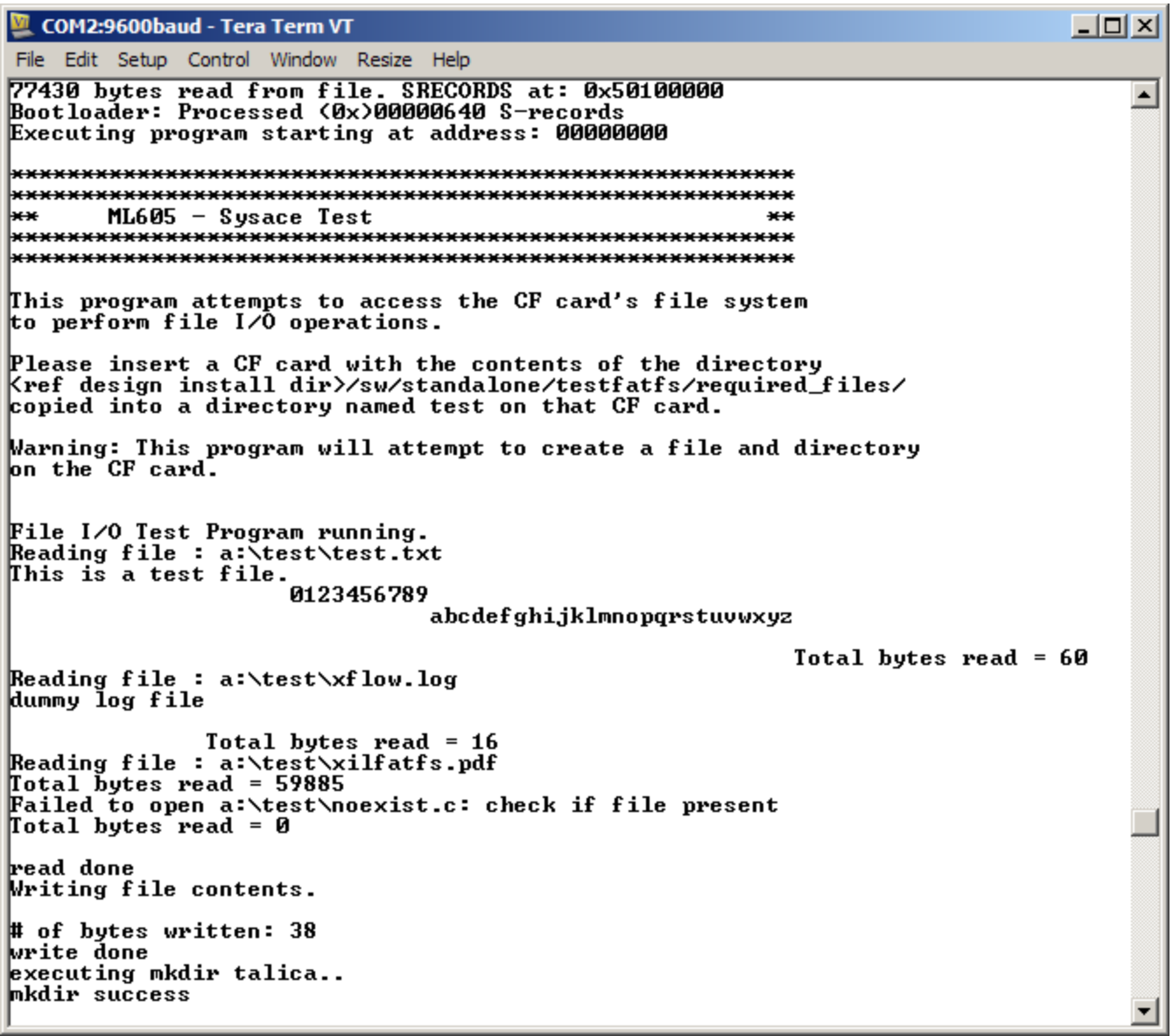

- **System ACE CF Test completed**
  - Connect a DVI Monitor to the ML605 board
  - Type **D** to begin DVI/VGA Test

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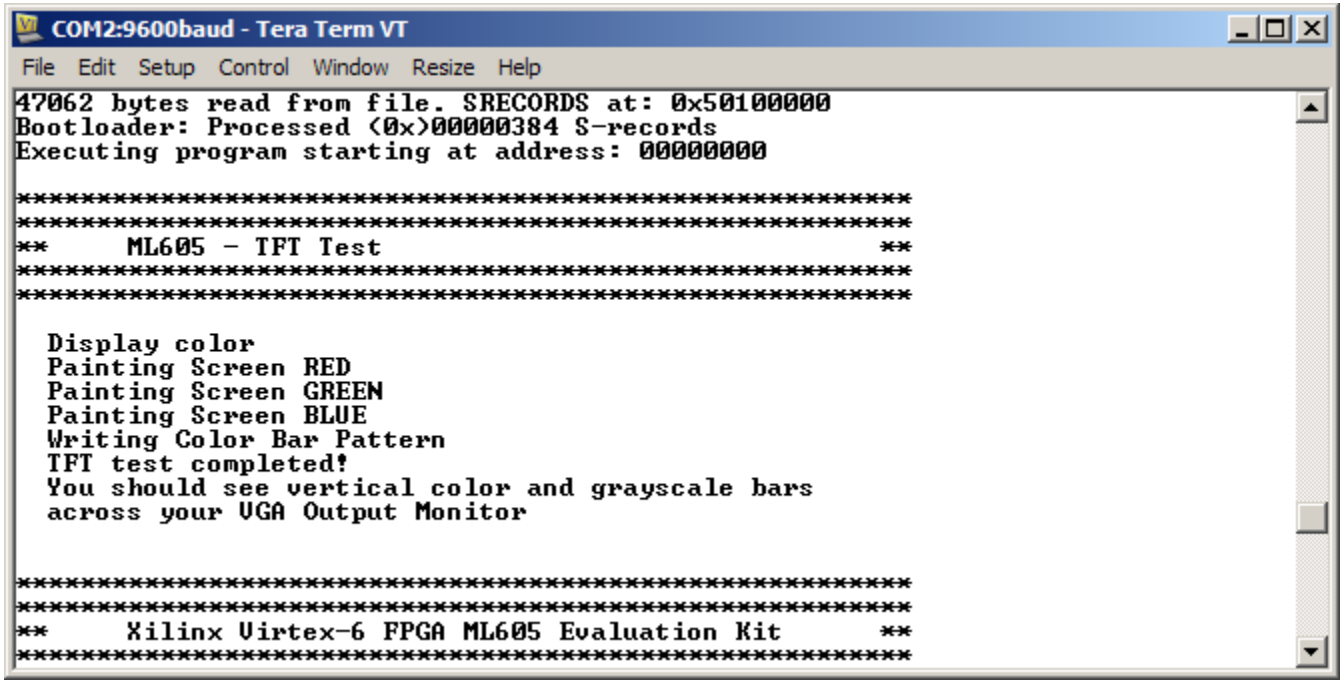
- DVI/VGA Test completed



Note: Presentation applies to the ML605

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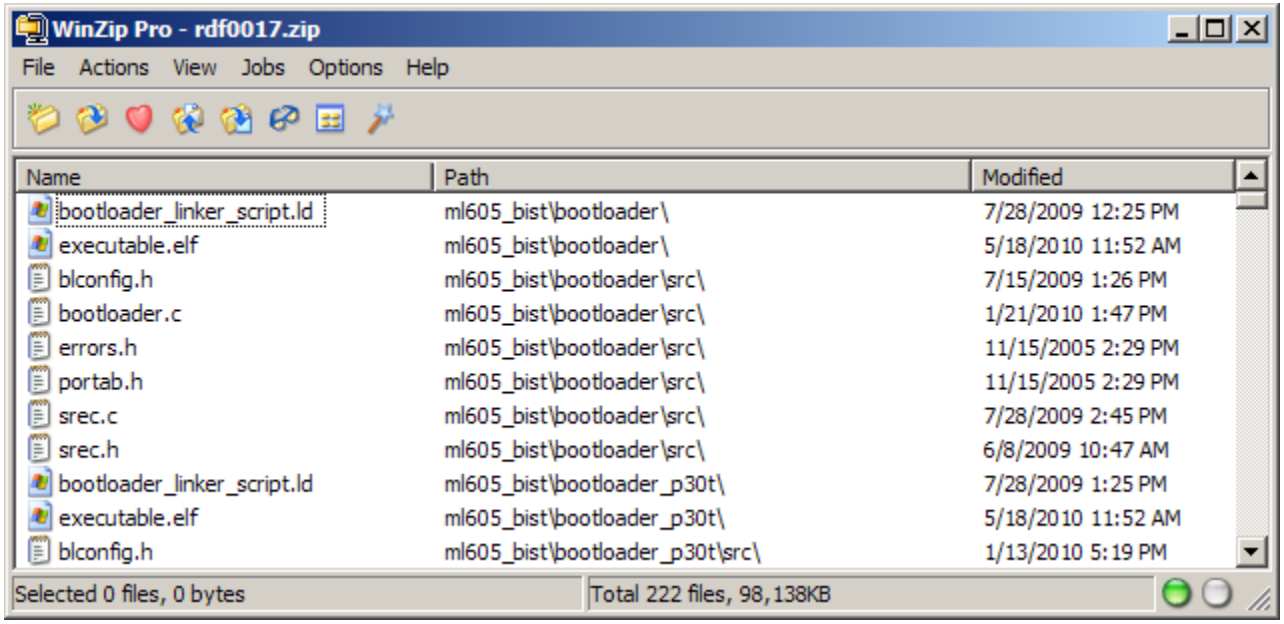
Compile ML605 BIST Design

- **Unzip the rdf0017.zip file**
  - Available through http://www.xilinx.com/ml605



Note: Presentation applies to the ML605

Run ML605 BIST Ready for Download Files

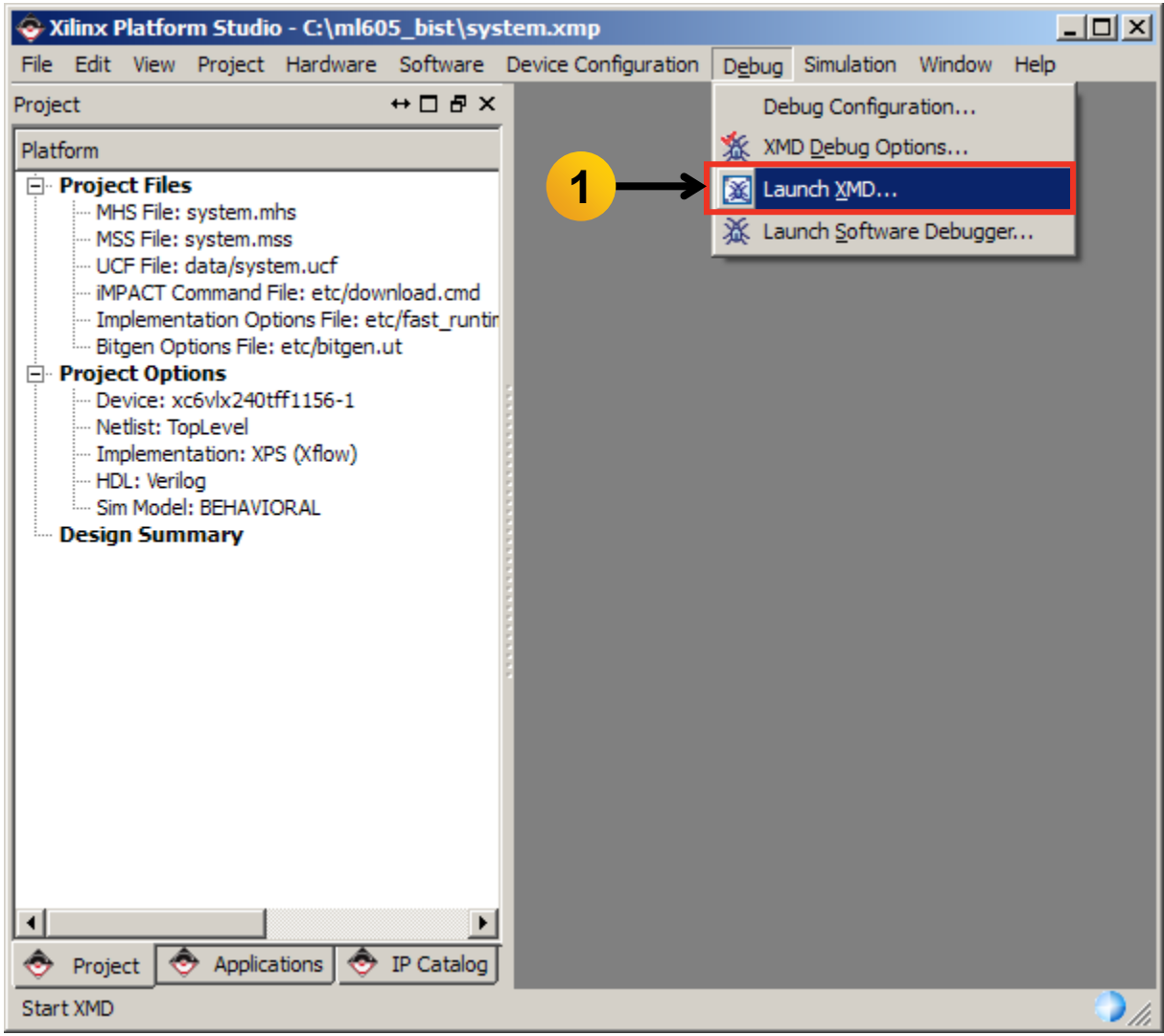
Run ML605 BIST Ready for Download Files

- **Add a second USB Type-A to Mini-B cables to the USB JTAG connector on the ML605 board**
  - Connect this cable to your PC

Note: Presentation applies to the ML605

Run ML605 BIST Ready for Download Files

- **Open XPS project <design path>\ system.xmp**
- **Launch XMD**
  - Select **Debug → Launch XMD…** (1)



Note: Presentation applies to the ML605

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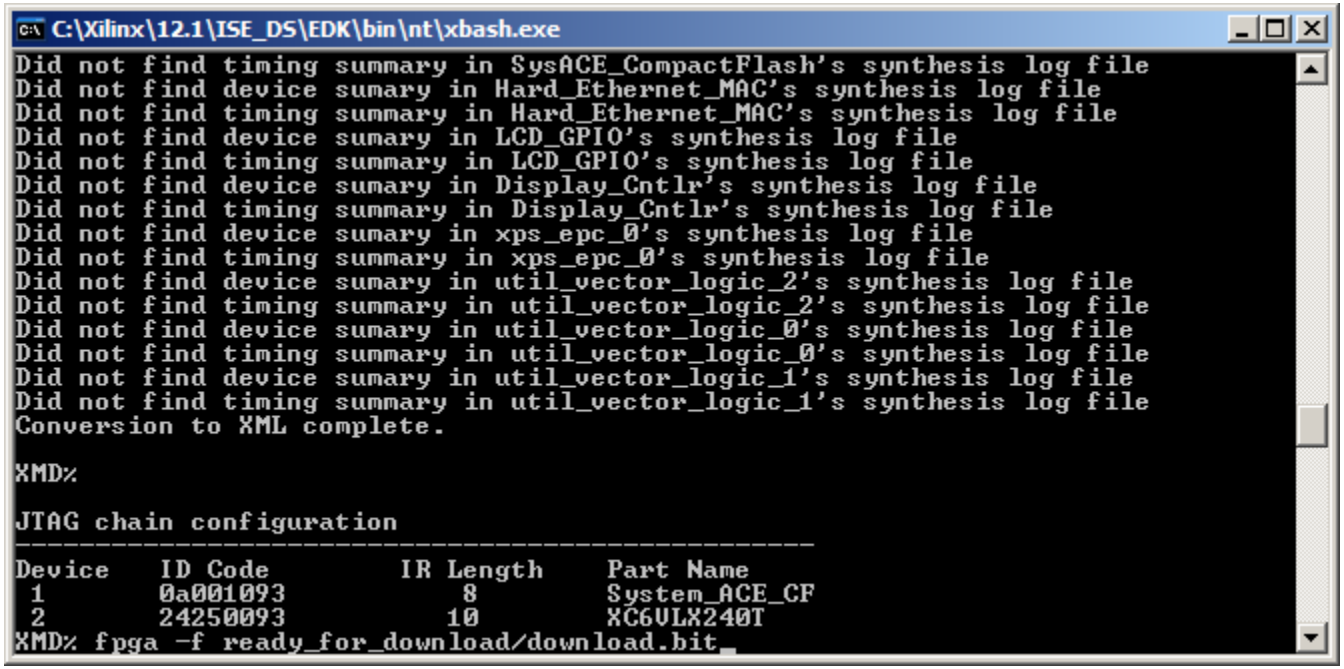
Run ML605 BIST Ready for Download Files

- **Download the bitstream with xmd:**

  fpga -f ready_for_download/download.bit



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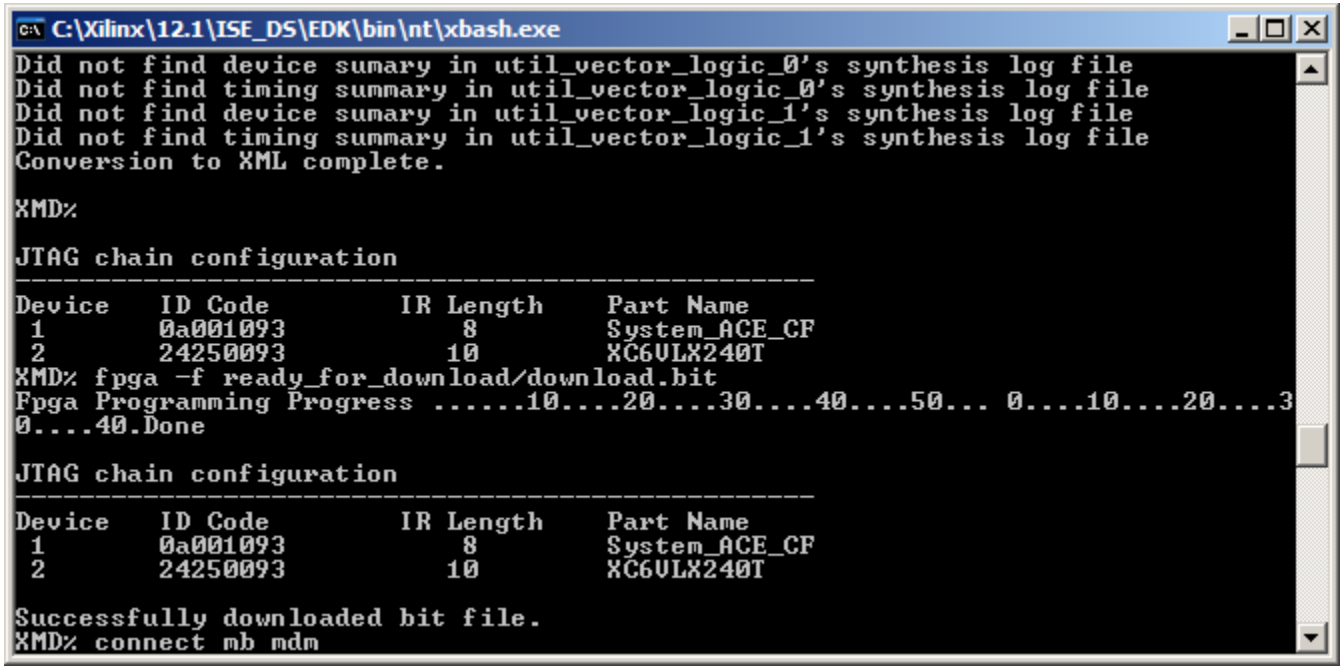
Run ML605 BIST Ready for Download Files

- **Connect XMD to the MicroBlaze:**

  connect mb mdm



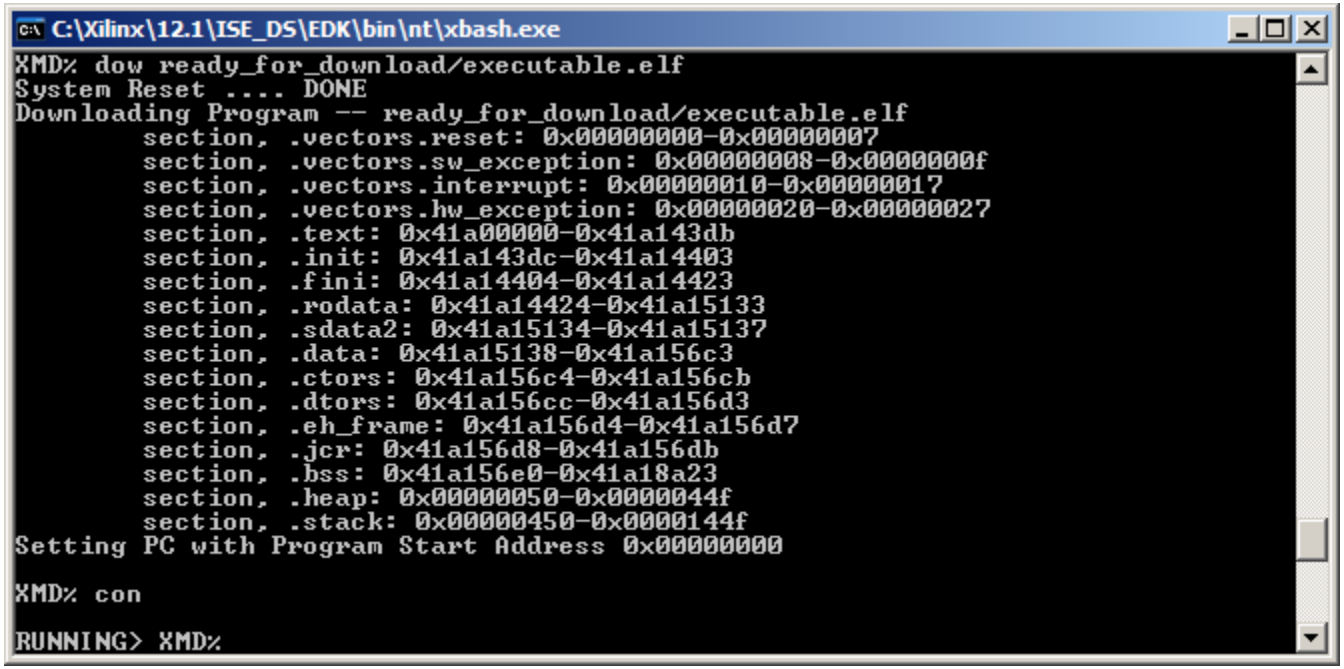
Note: Presentation applies to the ML605

Run ML605 BIST Ready for Download Files

- **Download the bootloader with xmd:**

  dow ready_for_download/executable.elf

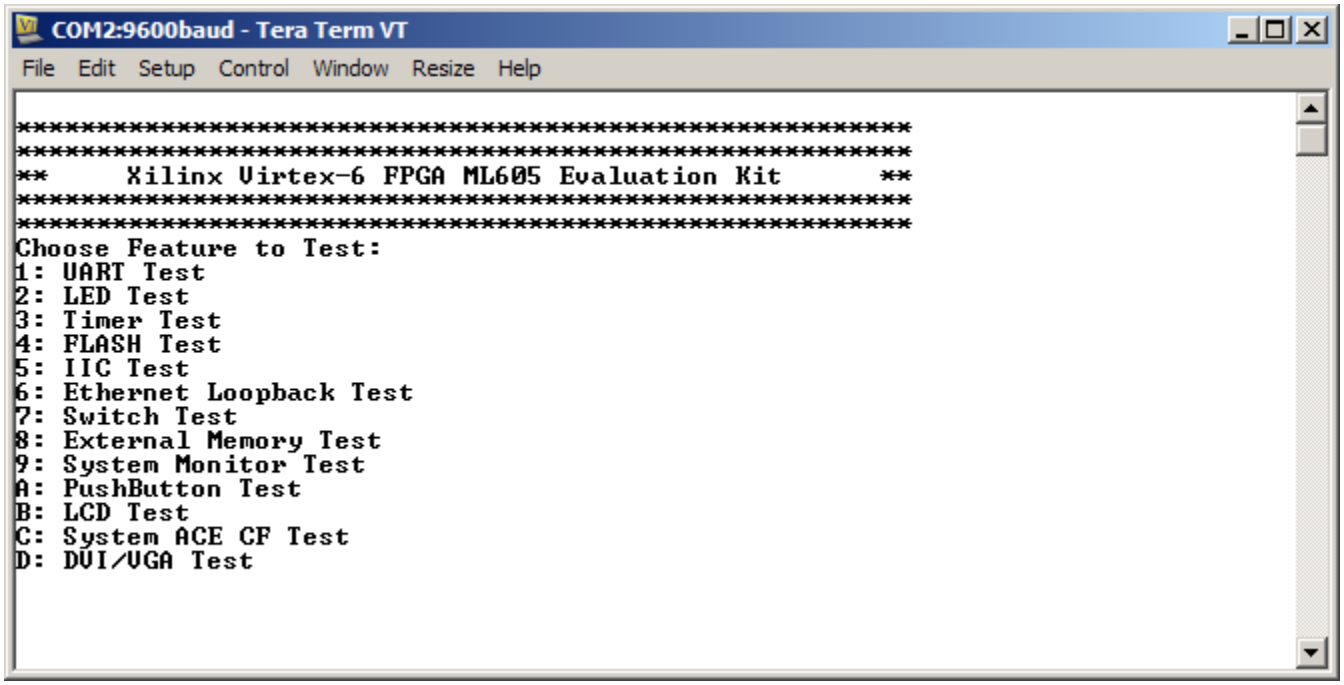
  con



Note: Presentation applies to the ML605

Run ML605 BIST Ready for Download Files

- Bootloader runs in the terminal window

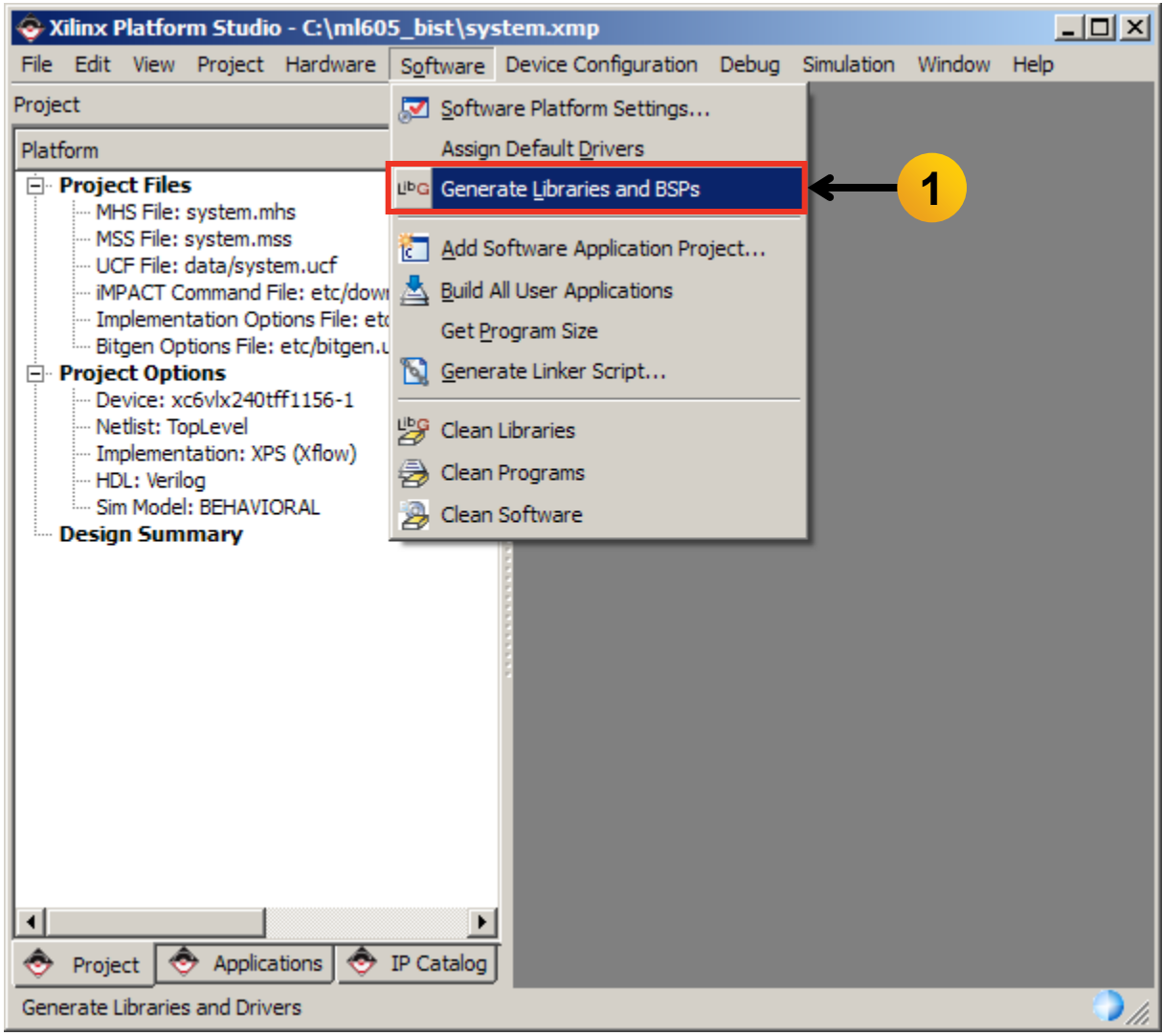


Note: CompactFlash must be inserted to launch applications

Compile ML605 BIST Design

Compile ML605 BIST Design

- The BIST Design is compiled with EDK
- Generate the libraries needed to create the bitstream
  - Select **Software → Generate Libraries and BSPs** (1)



Note: Presentation applies to the ML605

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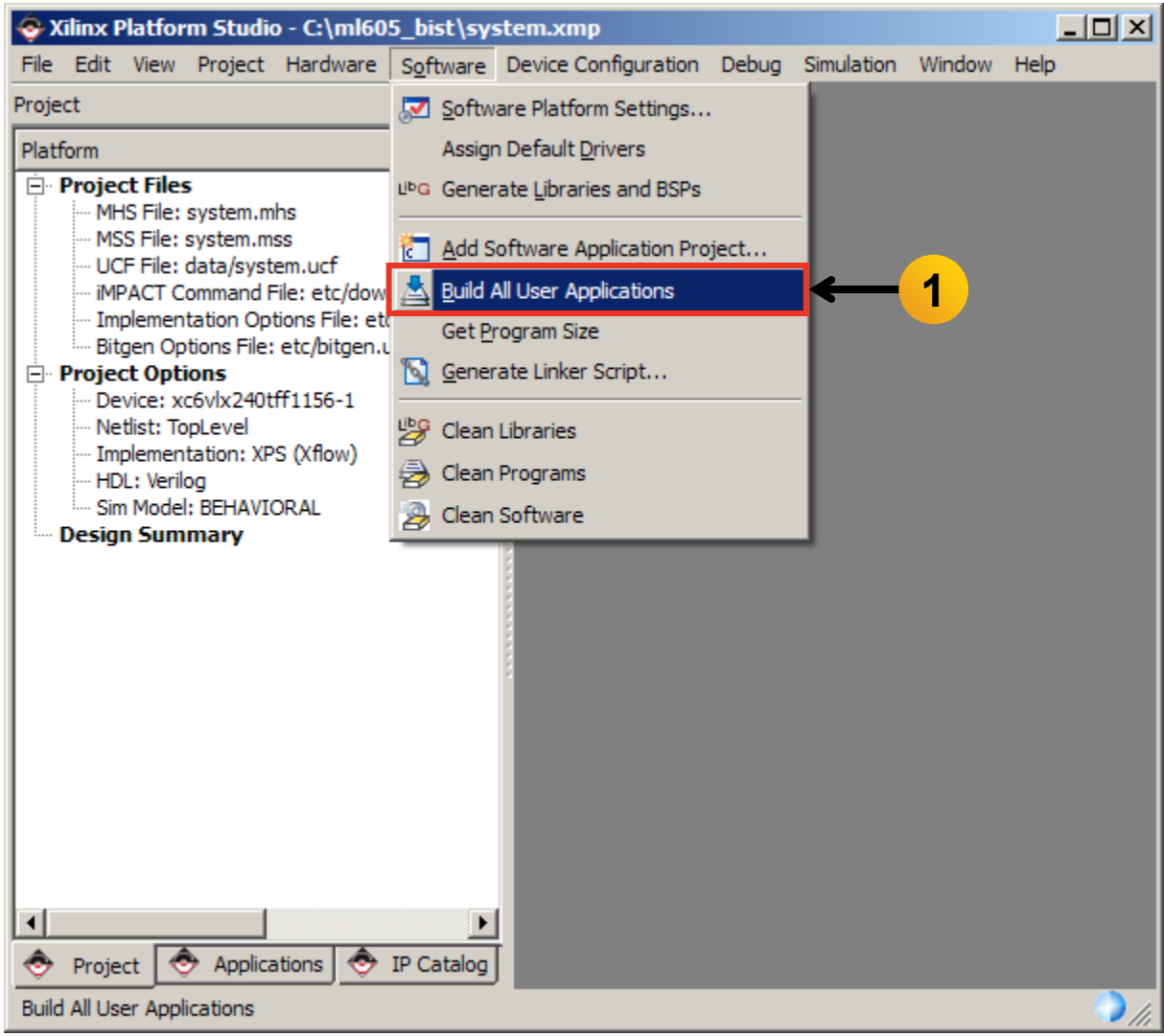
Compile ML605 BIST Design

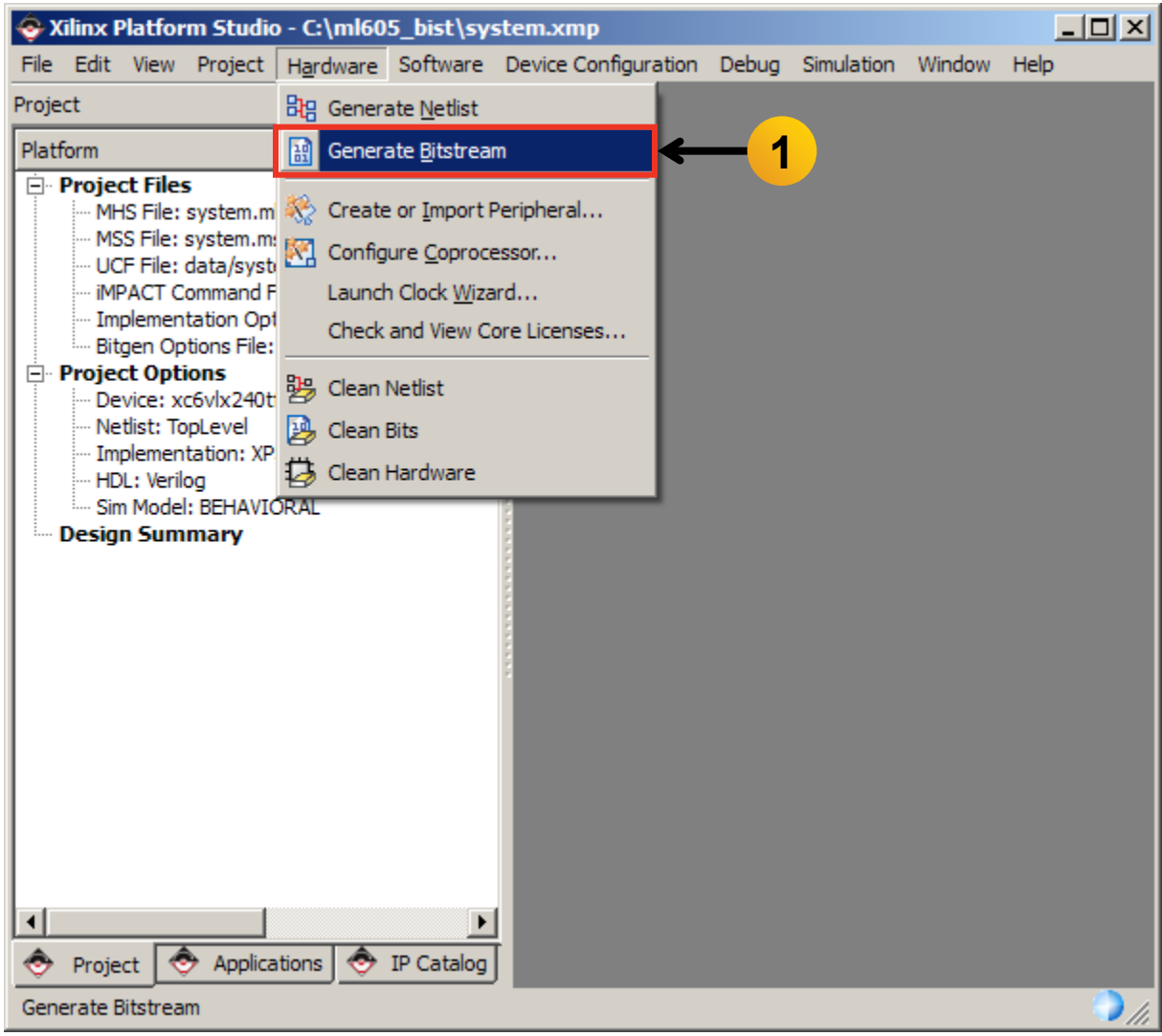
- **Compile the Software Applications and create the application ELF files**
  - Select **Software → Build All User Applications** (1)



Note: Presentation applies to the ML605

Compile ML605 BIST Design

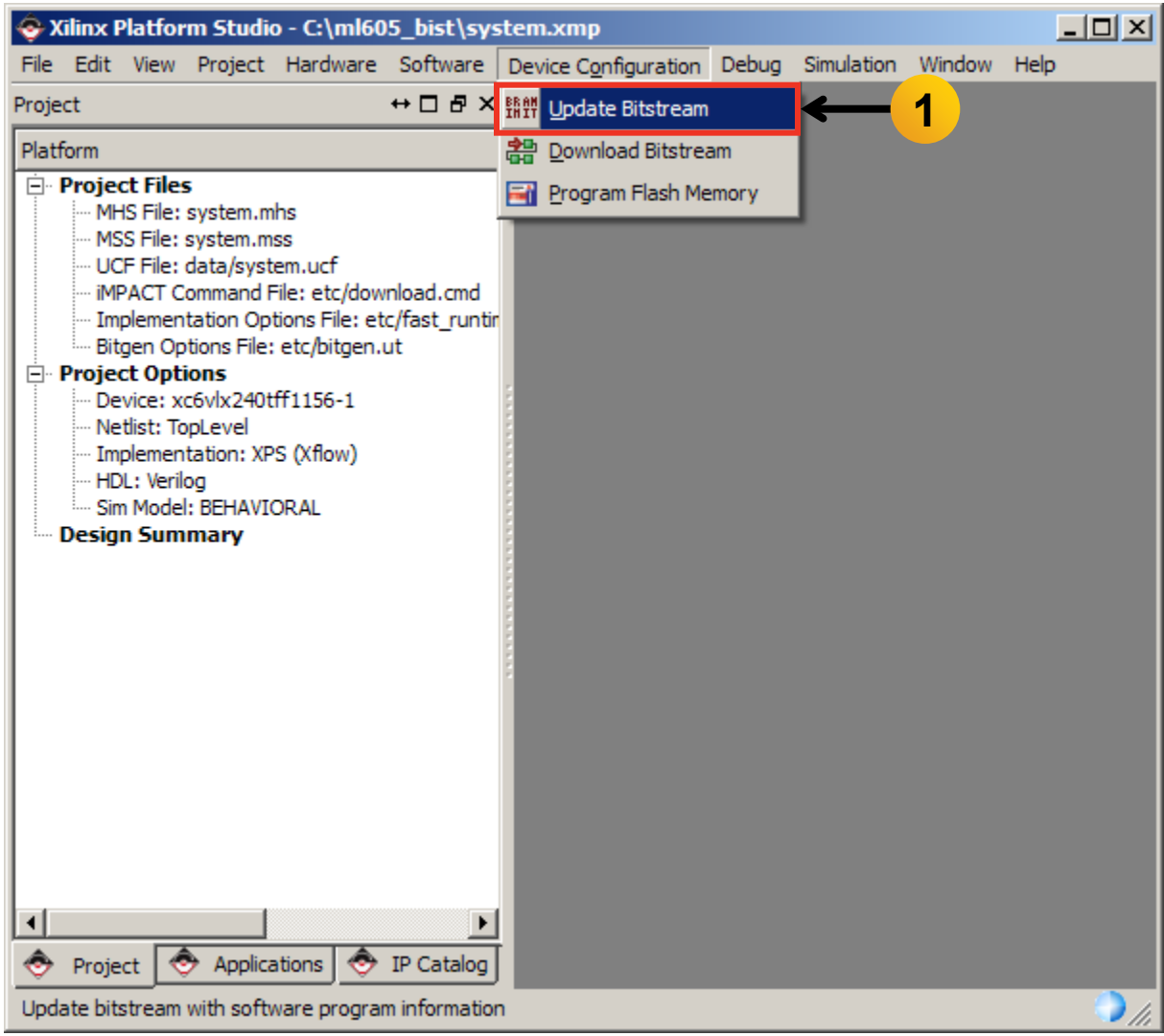
- **Create the hardware design, system.bit, located in <project directory> /implementation**
  - Select **Hardware → Generate Bitstream** (1)



Note: Presentation applies to the ML605

Compile ML605 BIST Design

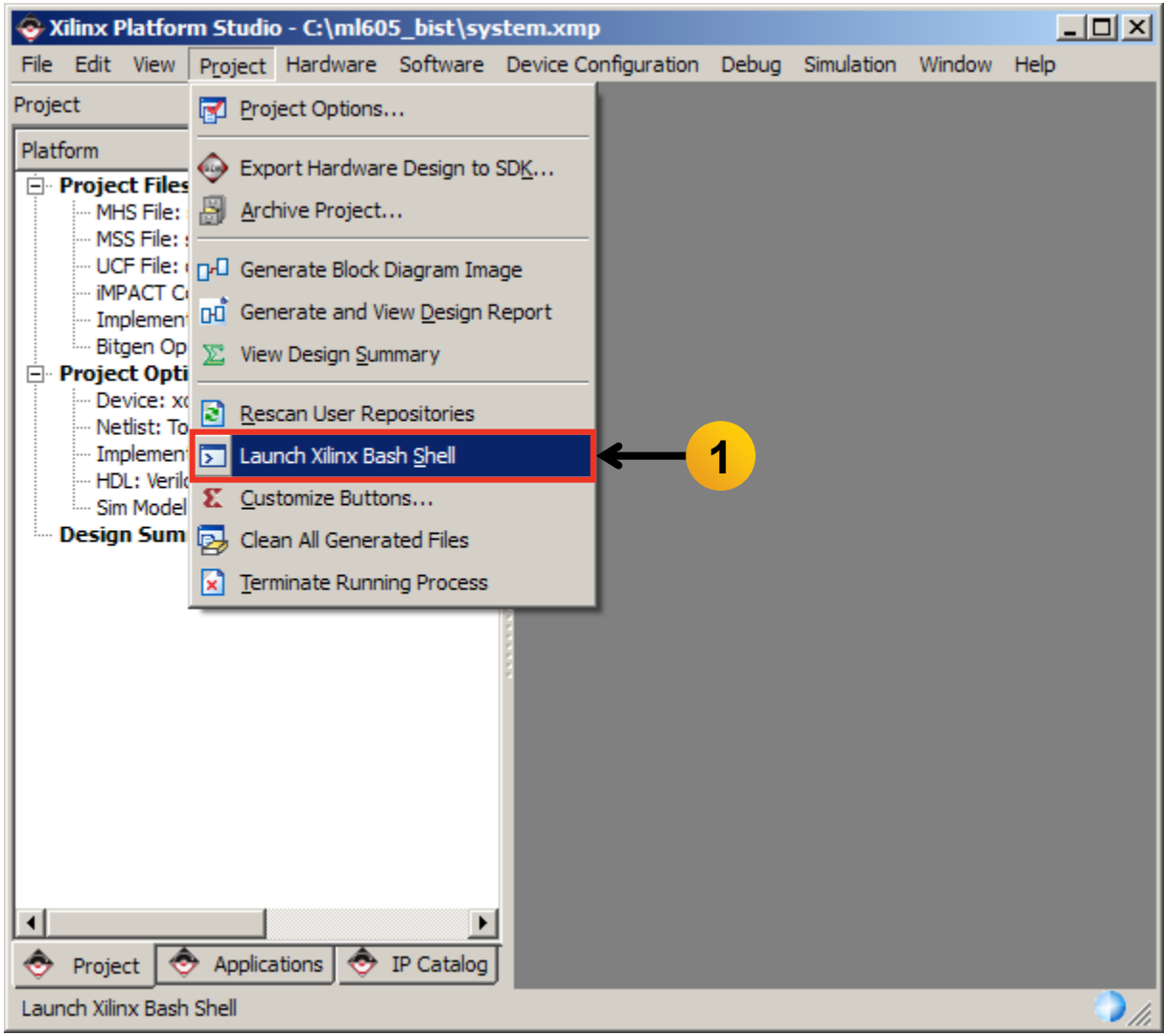
- **Init memory with the Bootloader Application ELF**
  - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
  - Select **Device Configuration → Update Bitstream** (1)



Note: Presentation applies to the ML605

Generate ML605 BIST Design CompactFlash

- **Convert the ELF files to S-record format and create ACE file**
  - Select **Project → Launch Xilinx Bash Shell** (1)



Note: Presentation applies to the ML605

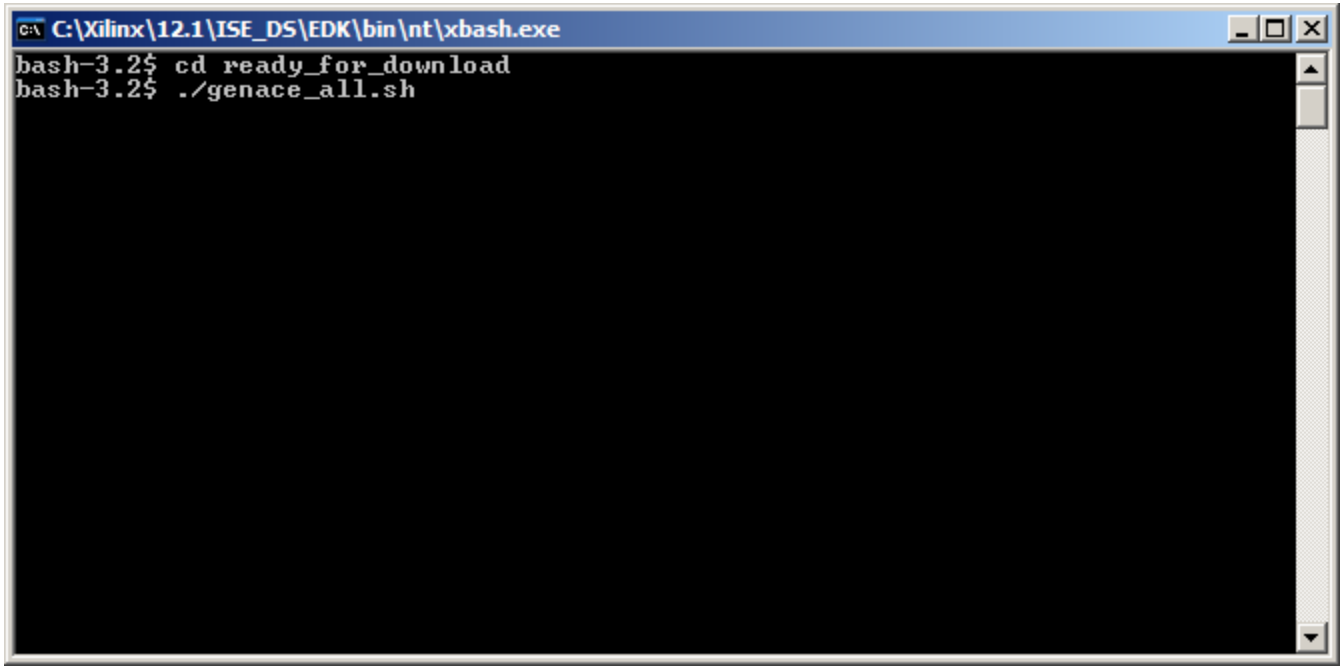
Generate ML605 BIST Design CompactFlash

- **Generate the S Records and ACE file**

  cd ready_for_download

  ./genace_all.sh

  – Copy the contents of ready_for_download/cf_image to your CompactFlash



Note: Presentation applies to the ML605

References

References

- **EDK Documentation**
  - Embedded System Tools Reference Guide
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/est_rm.pdf
- **System ACE CF**
  - System ACE CompactFlash Solution
    http://www.xilinx.com/support/documentation/boards_and_kits/ug080.pdf
- **Virtex-6 Configuration**
  - Virtex-6 FPGA Configuration User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug360.pdf

Documentation

Documentation

- **Virtex-6**
  - Virtex-6 FPGA Family
    http://www.xilinx.com/products/virtex6/index.htm
- **ML605 Documentation**
  - Virtex-6 FPGA ML605 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm
  - ML605 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf
  - ML605 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf