

ML605 Built-In Self Test Flash Application

May 2010

Overview

- **Xilinx ML605 Board**
- **Software Requirements**
- **ML605 Setup**
- **ML605 BIST (Built-In Self Test)**
- **Run ML605 BIST Ready for Download Files**
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- **Generate ML605 BIST Design CompactFlash**
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ML605 BIST Design Description

▪ Description

- The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

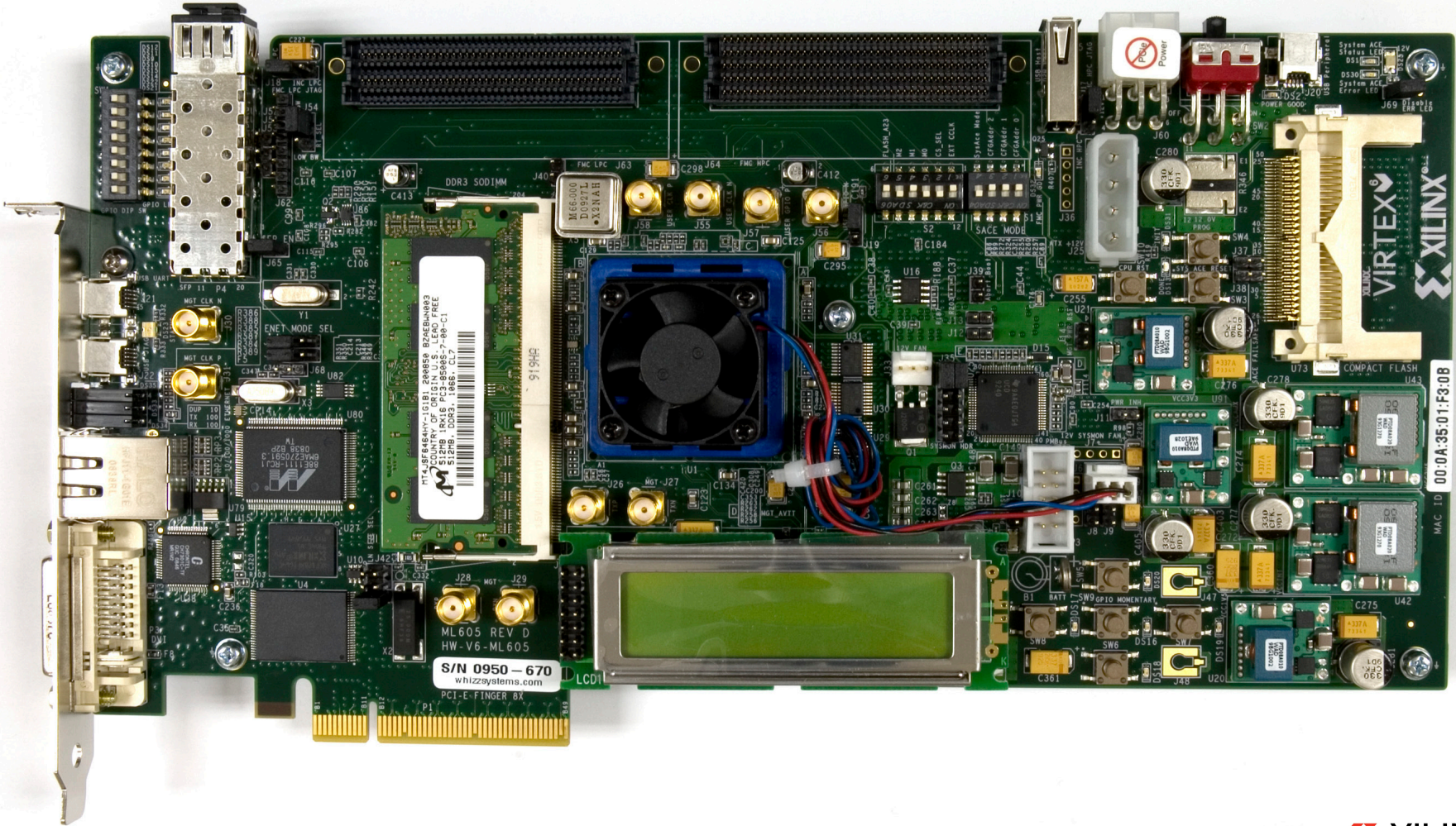
▪ Reference Design IP

- EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_sysmon_adc, xps_iic, xps_mch_emc, xps_sysace, util_io_mux, util_bus_split, util_vector_logic, xps_ll_temac, xps_tft, xps_epc
 - [Embedded System Tools Reference Guide](#) (UG111)
 - http://www.xilinx.com/ise/embedded/edk_ip.htm

▪ Reference Design Source

- rdf0017.zip
- Available through <http://www.xilinx.com/ml605>

Xilinx ML605 Board



Note: Presentation applies to the ML605



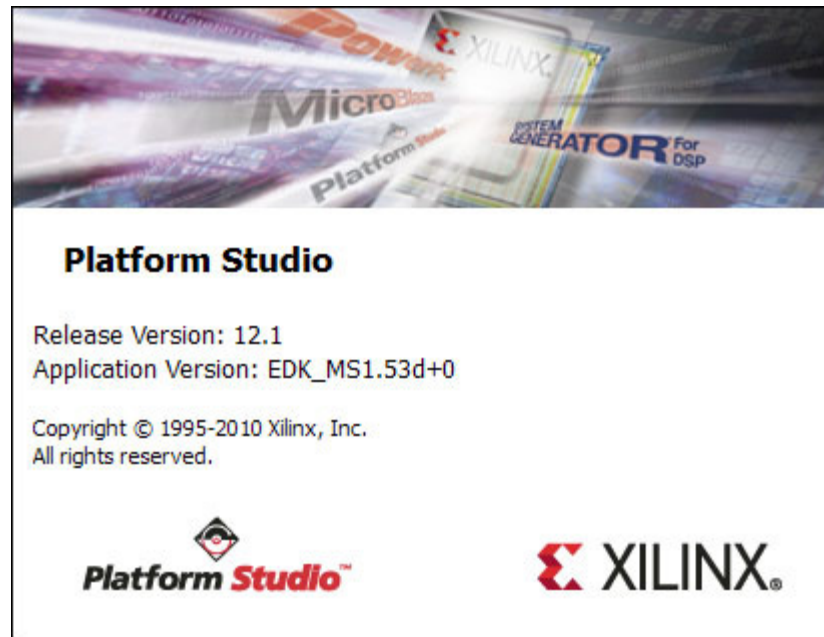
ISE Software Requirements

- **Xilinx ISE 12.1 software**



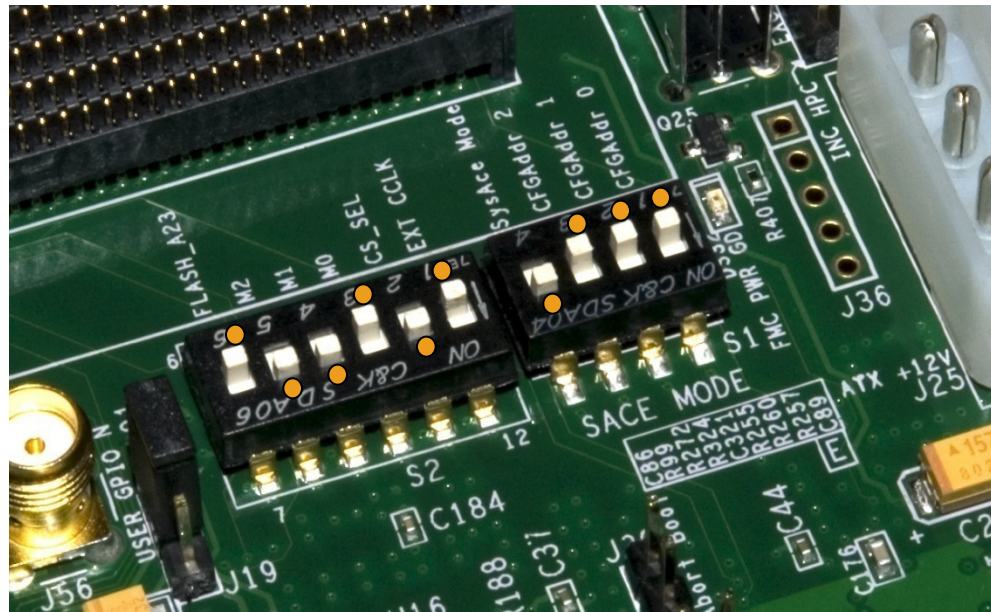
EDK Software Requirement

- **Xilinx EDK 12.1 software**



Hardware Setup

- **Set S2 to 011010 (1 = on, Position 6 → Position 1)**
- **Set S1 to 1000 (Position 4 → Position 1)**
 - This enables JTAG configuration from the Compact Flash



ML605 Setup

- Power on the ML605 board for UART Drivers Installation
- Connect a USB Type-A to Mini-B cable to the USB UART connector on the ML605 board
 - Connect this cable to your PC

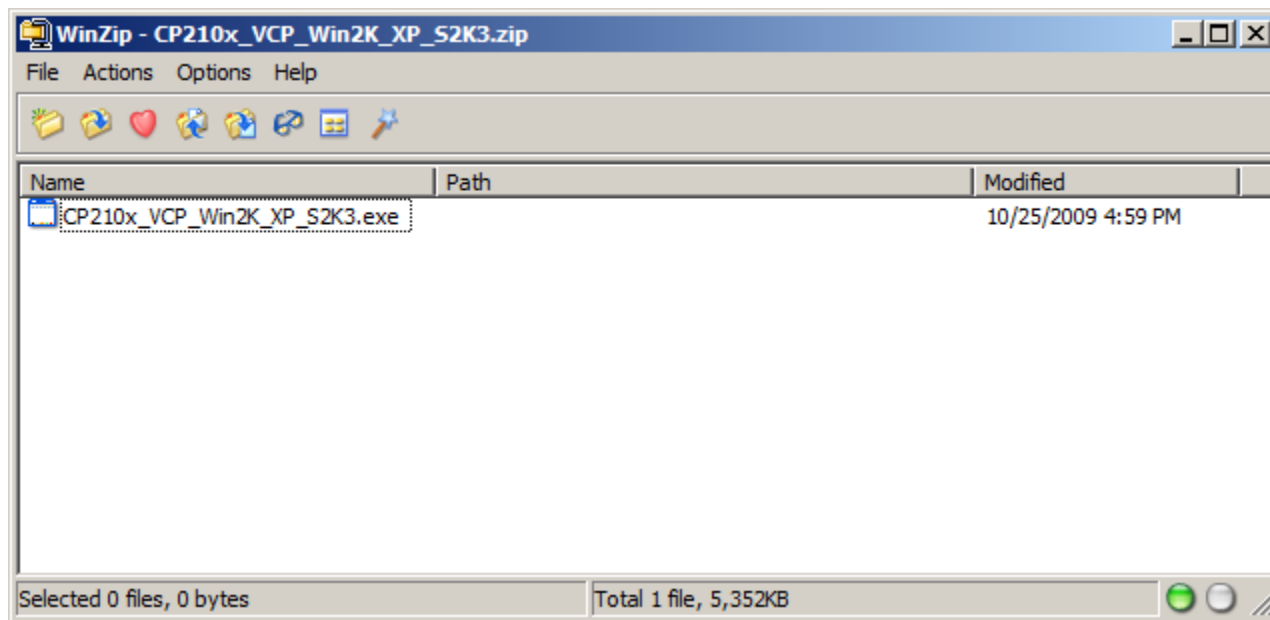


Note: Presentation applies to the ML605

ML605 Setup

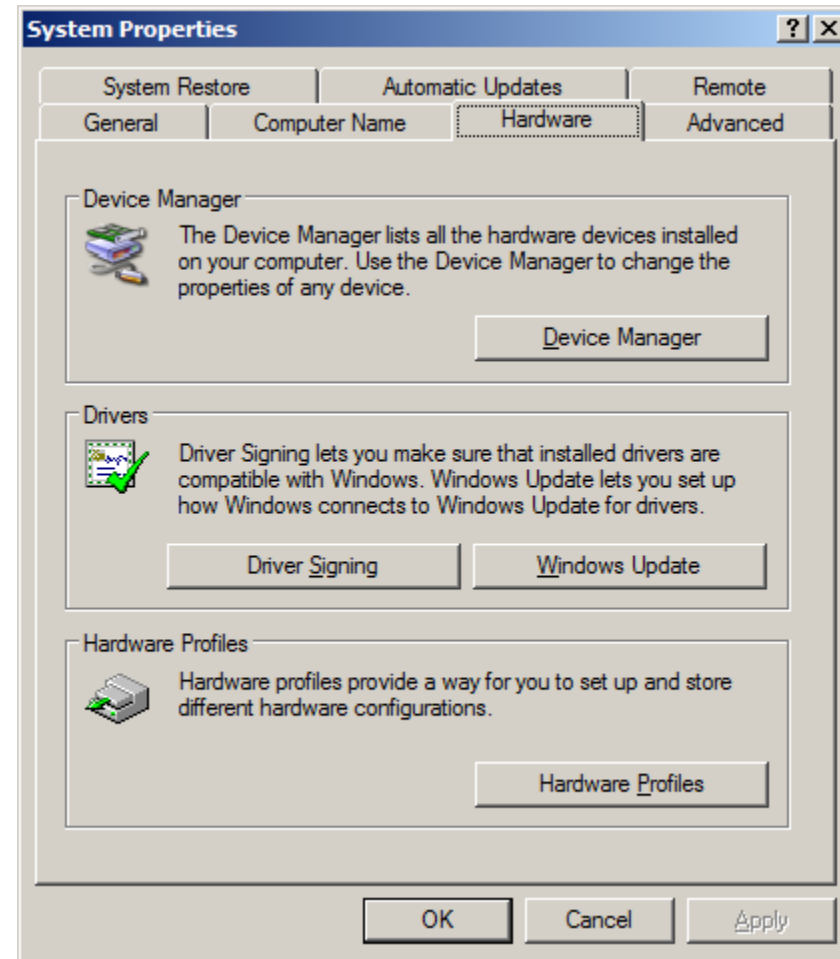
▪ Install USB UART Drivers

- https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip



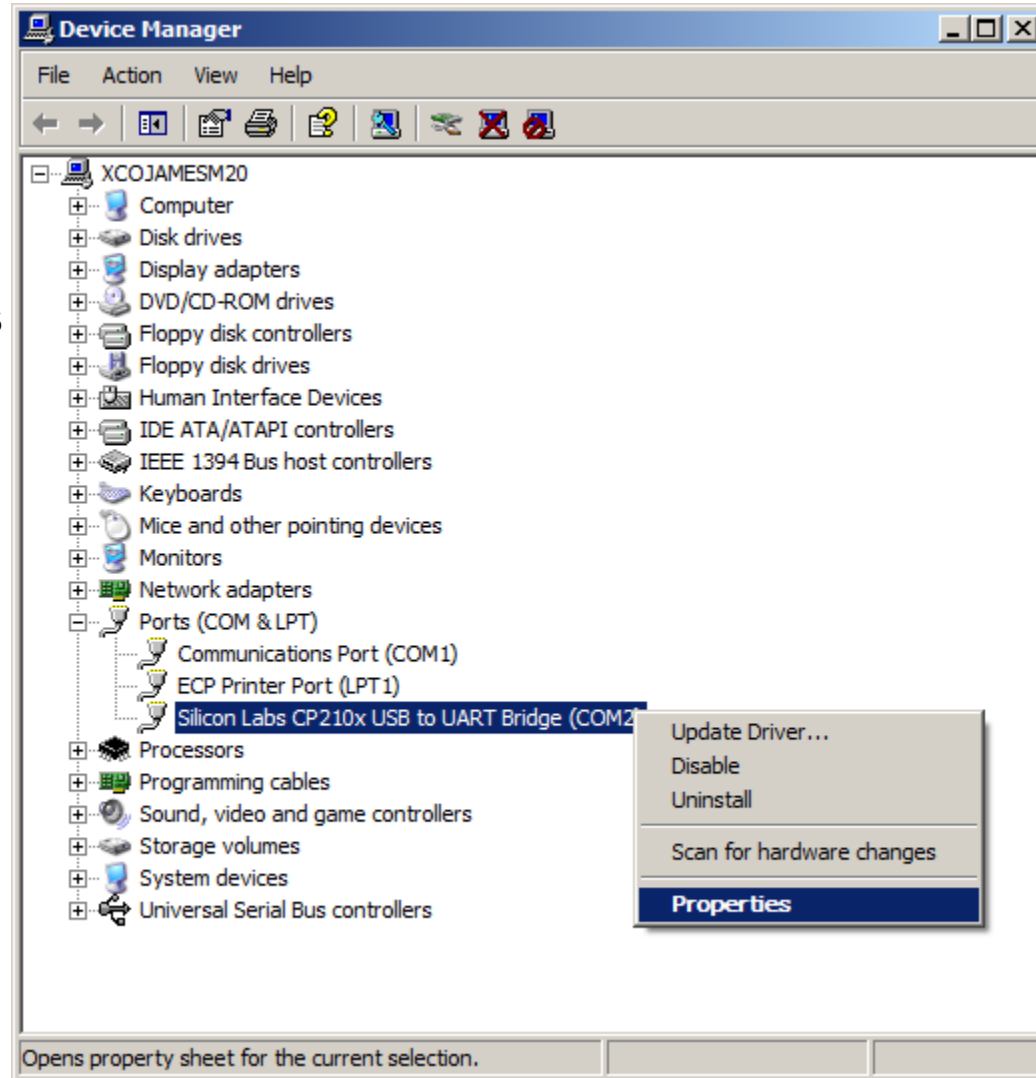
ML605 Setup

- **Right-click on My Computer and select Properties**
 - Select the Hardware tab
 - Click on Device Manager



ML605 Setup

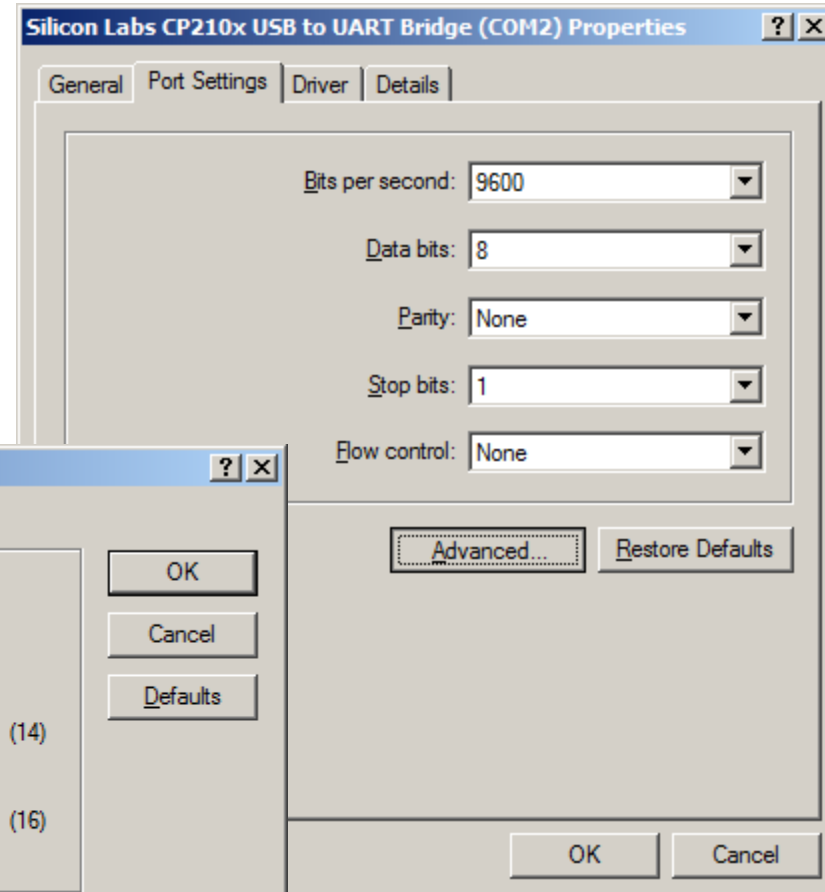
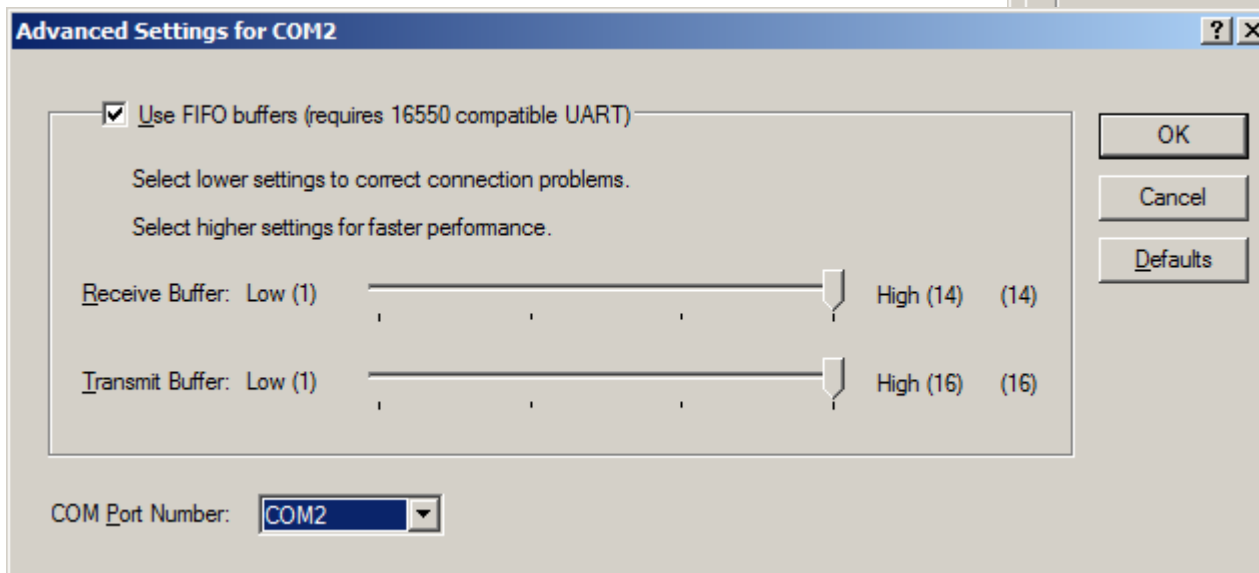
- **Expand the Ports Hardware**
 - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties



ML605 Setup

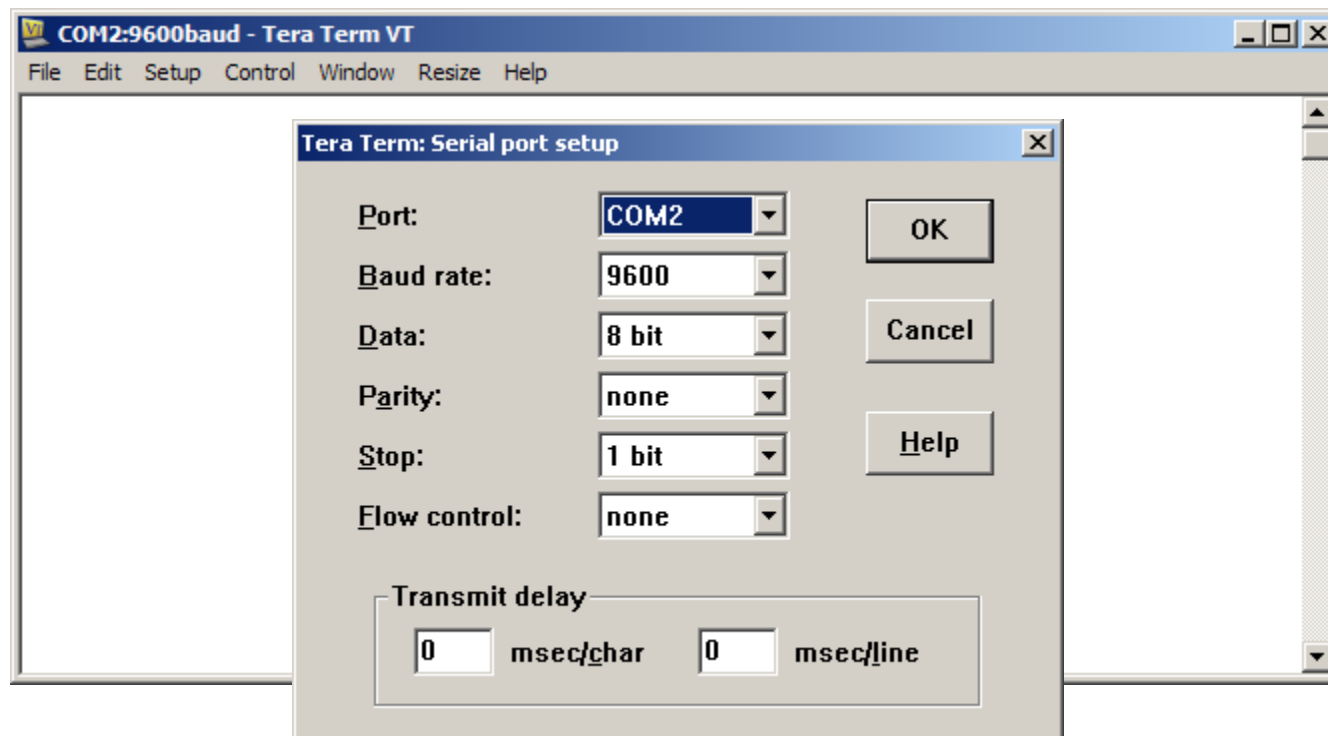
■ Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



ML605 BIST Setup

- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
 - Select your USB Com Port
 - Set the baud to 9600



Note: Tera Term may need to be restarted if board power is cycled

ML605 BIST

- Insert ML605 Evaluation Kit CompactFlash into the ML605
- Push SysACE Reset and view initial BIST screen
 - Type “1” to start the UART Test

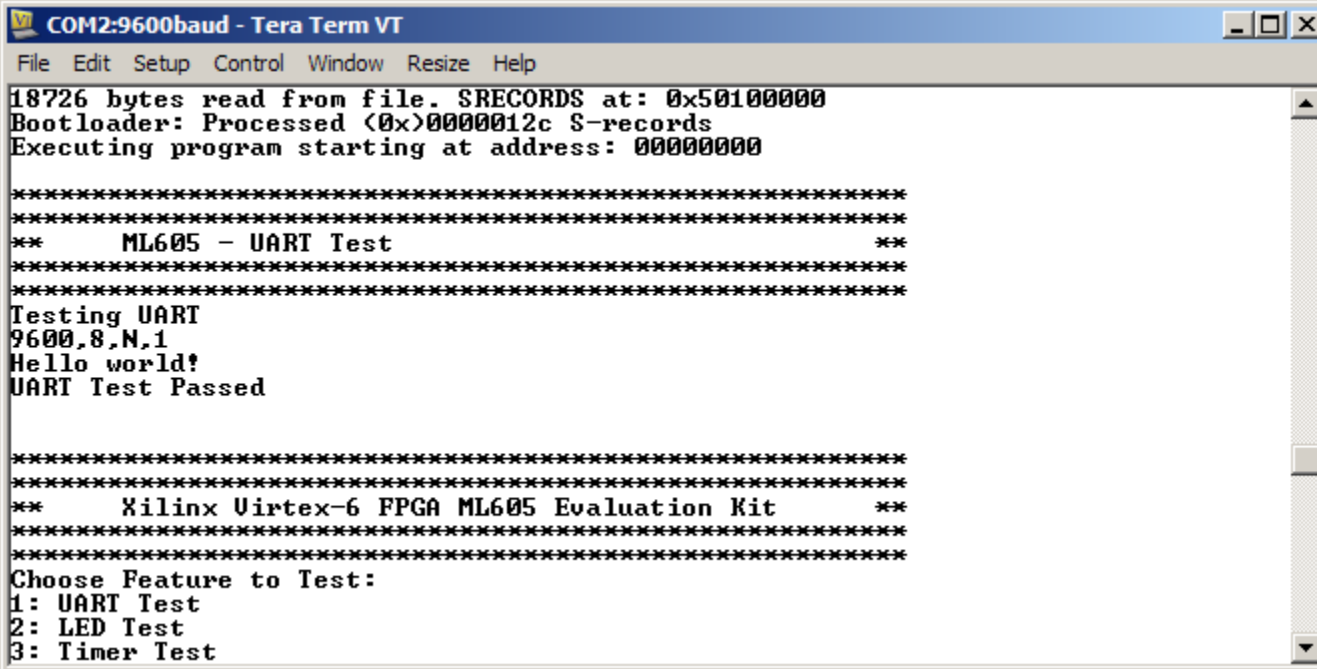


```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help

*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: System Monitor Test
A: PushButton Test
B: LCD Test
C: System ACE CF Test
D: DVI/UGA Test
█
```

ML605 BIST

- **UART Test completed**
 - Type **2** to begin LED Test



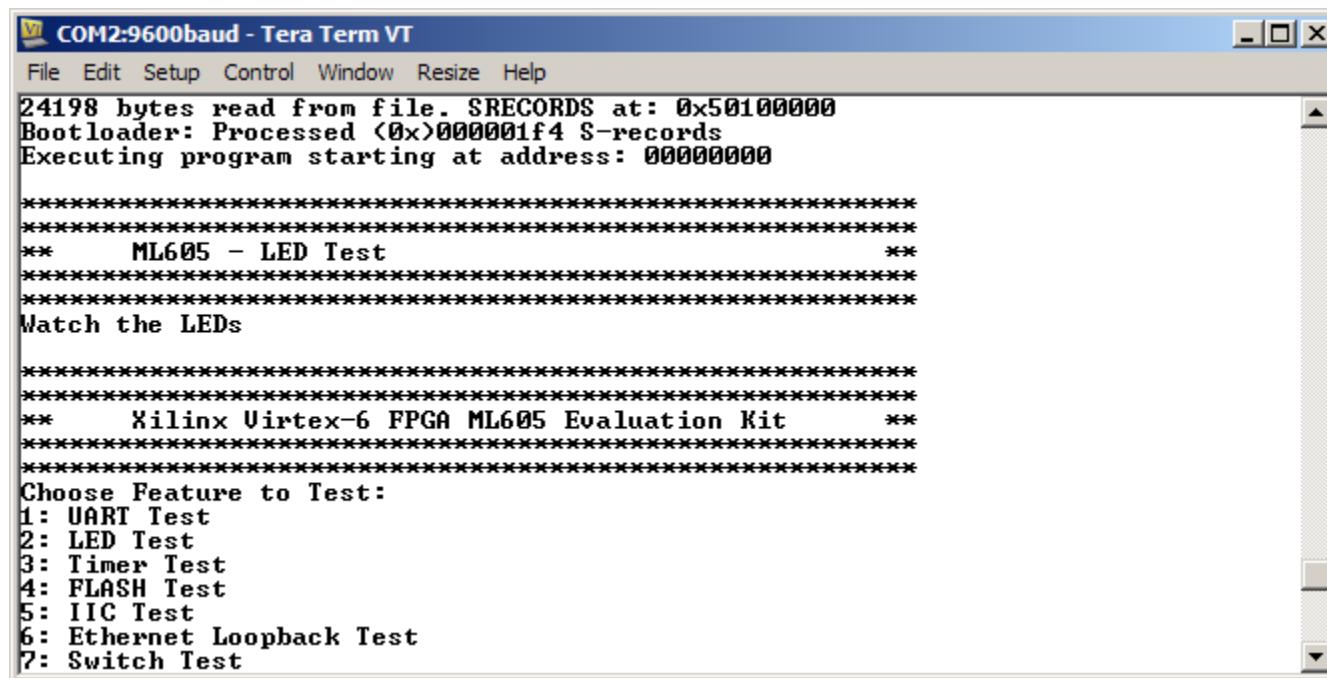
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
18726 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000012c S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - UART Test      **
*****
*****
Testing UART
9600,8,N,1
Hello world!
UART Test Passed

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
```

ML605 BIST

- **View Walking 1's pattern on GPIO LEDs**
 - Sequence repeats six times
- **LED Test completed**
 - Type **3** to begin Timer Test



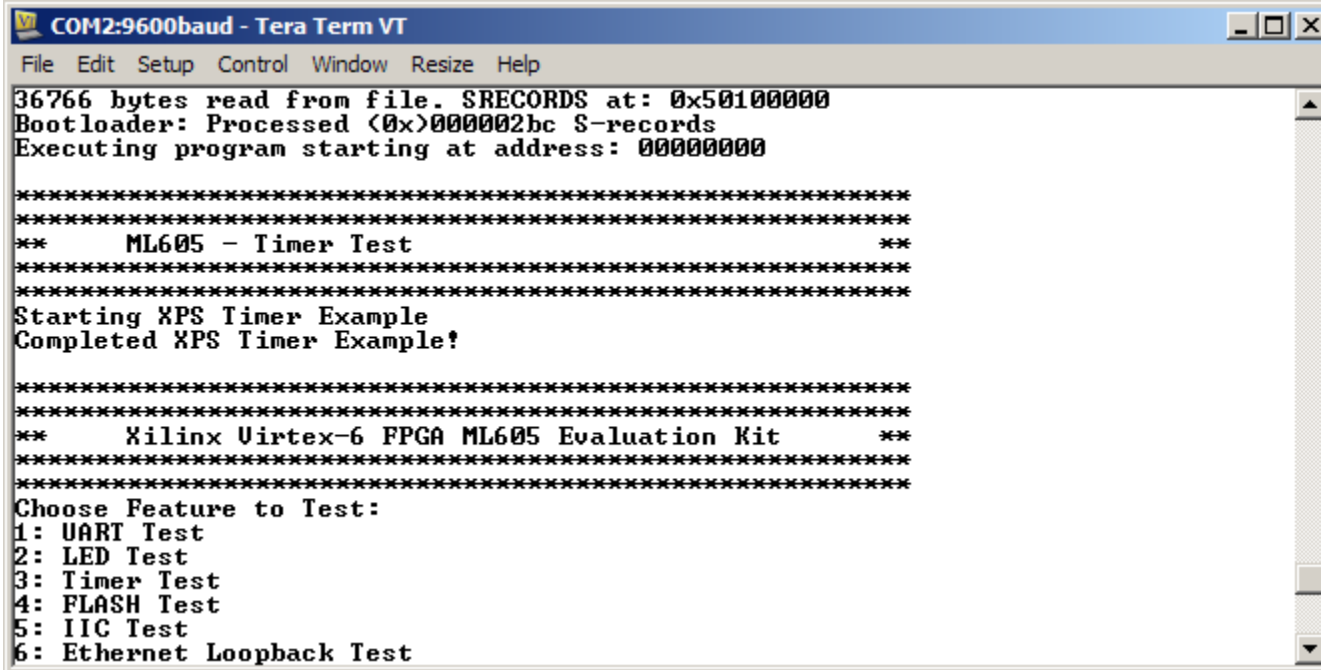
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
24198 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000001f4 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - LED Test      **
*****
*****
Match the LEDs

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
```


ML605 BIST

- **Timer Test completed**
 - Type 4 to begin Flash test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
36766 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000002bc S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - Timer Test      **
*****
*****
Starting XPS Timer Example
Completed XPS Timer Example!

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
```

ML605 BIST

Flash Test completed

- Type **5** to begin IIC EEPROM Test

```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
54094 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000044c S-records
Executing program starting at address: 00000000

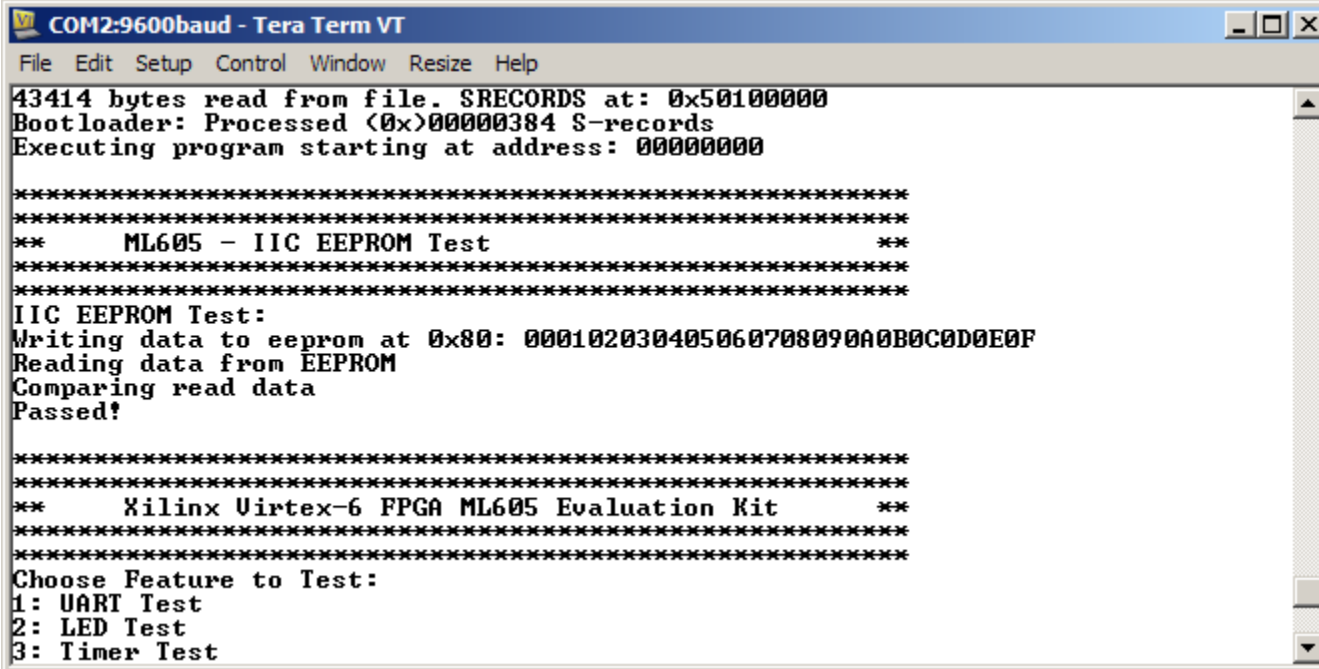
*****
*****
**      ML605 - FLASH Test      **
*****
*****
-- Initialized the Flash library successfully --
-- Unlocked all the blocks successfully --
-- Erased the Flash memory contents at offset 0x1FE0000 successfully --
-- Writing: 000102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F2021
22232425262728292A2B2C2D2E2F303132333435363738393A3B3C3D3E3F40414243444546474849
4A4B4C4D4E4F505152535455565758595A5B5C5D5E5F606162636465666768696A6B6C6D6E6F7071
72737475767778797A7B7C7D7E7F808182838485868788898A8B8C8D8E8F90919293949596979899
9A9B9C9D9E9FA0A1A2A3A4A5A6A7A8A9AAABACADAEAFB0B1B2B3B4B5B6B7B8B9BABBCBDBEBFC0C1
C2C3C4C5C6C7C8C9CACBCCDCECFD0D1D2D3D4D5D6D7D8D9DADBDCDDDEDFE0E1E2E3E4E5E6E7E8E9
EAEBECEDEEEFF0F1F2F3F4F5F6F7F8F9FAFBFCFDFF
-- Write operation at offset 0x1FE0000 completed successfully --
-- Read operation completed successfully --
-- Data comparison successful --

*****
```

ML605 BIST

▪ IIC EEPROM Test completed

- Type **6** to begin Ethernet Loopback Test
 - PHY is put into internal loopback mode



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
43414 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000000384 S-records
Executing program starting at address: 00000000

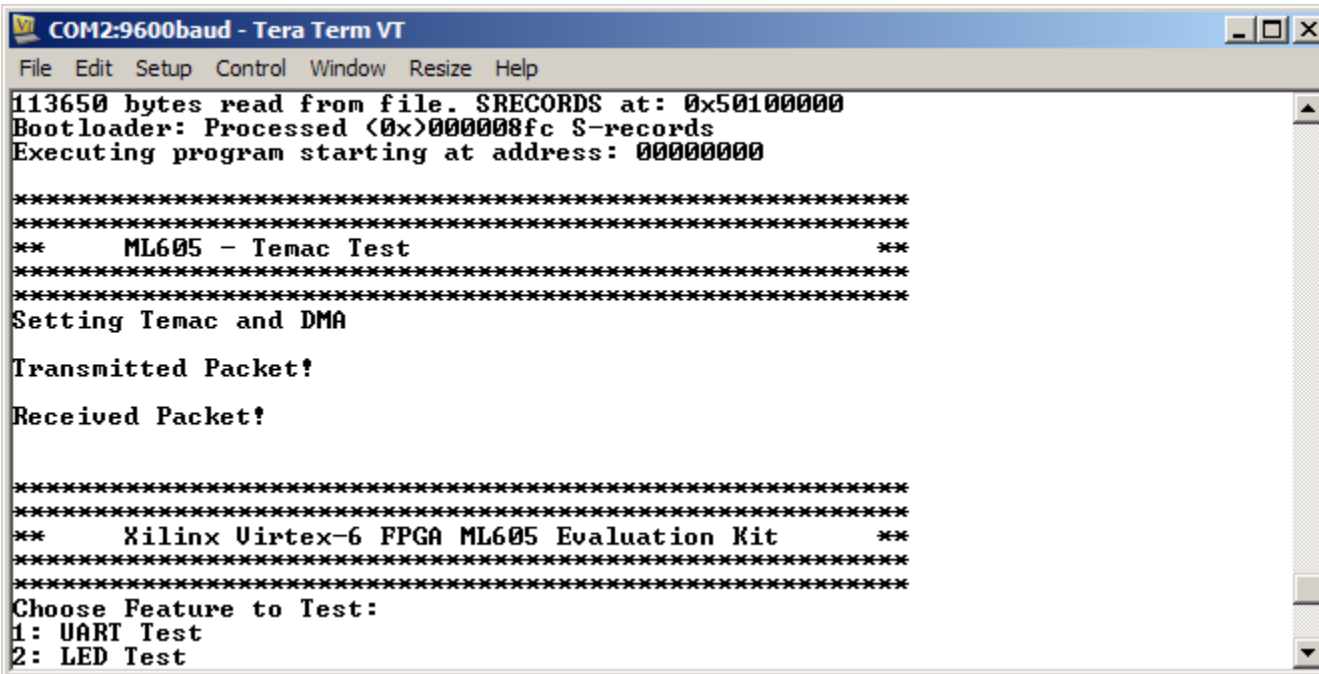
*****
*****
**      ML605 - IIC EEPROM Test      **
*****
*****
IIC EEPROM Test:
Writing data to eeprom at 0x80: 000102030405060708090A0B0C0D0E0F
Reading data from EEPROM
Comparing read data
Passed!

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
```

ML605 BIST

▪ Ethernet Loopback Test completed

- Set 8-position GPIO DIP Switch (SW1)
- Type 7 to begin GPIO Switch Test
 - Reads switch settings



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
113650 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000008fc S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - Temac Test      **
*****
*****
Setting Temac and DMA

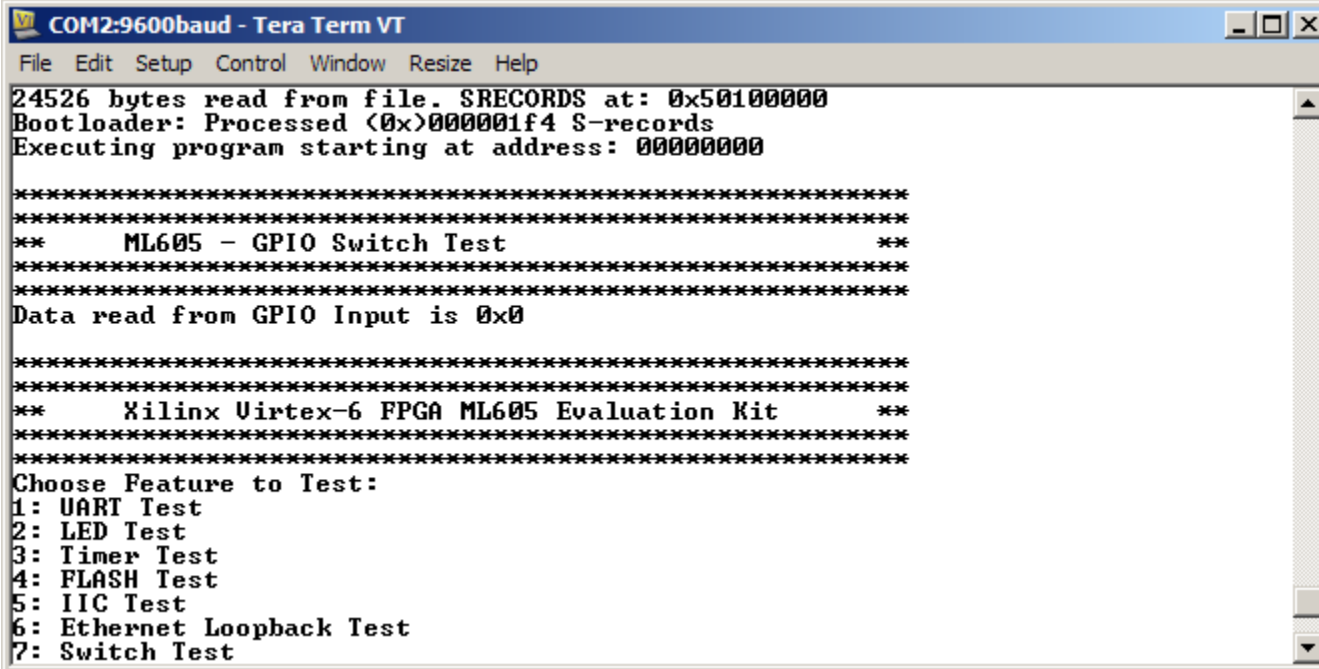
Transmitted Packet?

Received Packet?

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
```

ML605 BIST

- **GPIO Switch Test completed**
 - Type **8** to begin External Memory Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
24526 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000001f4 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - GPIO Switch Test      **
*****
*****
Data read from GPIO Input is 0x0

*****
*****
**      Xilinx Uirtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
```

ML605 BIST

```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
40334 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - MPMC TEST      **
*****
*****

Multi-Port Memory Controller Memory Test
Testing address range 0x50200000-0x5FFFFFFF.
Iteration 1 of 1
Pass A) ICache: On, DCache: On
  TEST0: Write all memory to 0x00000000 and check
        Writing...
        Reading...
        Test Complete Status = SUCCESS
  TEST1: Write all memory to 0xFFFFFFFF and check
        Writing...
        Reading...
        Test Complete Status = SUCCESS

  TEST2: Testing for stuck together bank/row/col bits
        Clearing memory to zeros...
        Writing and Reading...
        Test Complete Status = SUCCESS

  TEST3: Testing for maximum ba/row/col noise
        This test performs 16 word writes followed by 16 word reads
        Each 64 bytes inverts the ba/row/col address
        Initializing Memory to 0xA5A5A5A5...
        Writing and Reading...
        Test Complete Status = SUCCESS
  TEST4: Testing for Inverse Data at Address
        Writing...
        Reading...
        Test Complete Status = SUCCESS

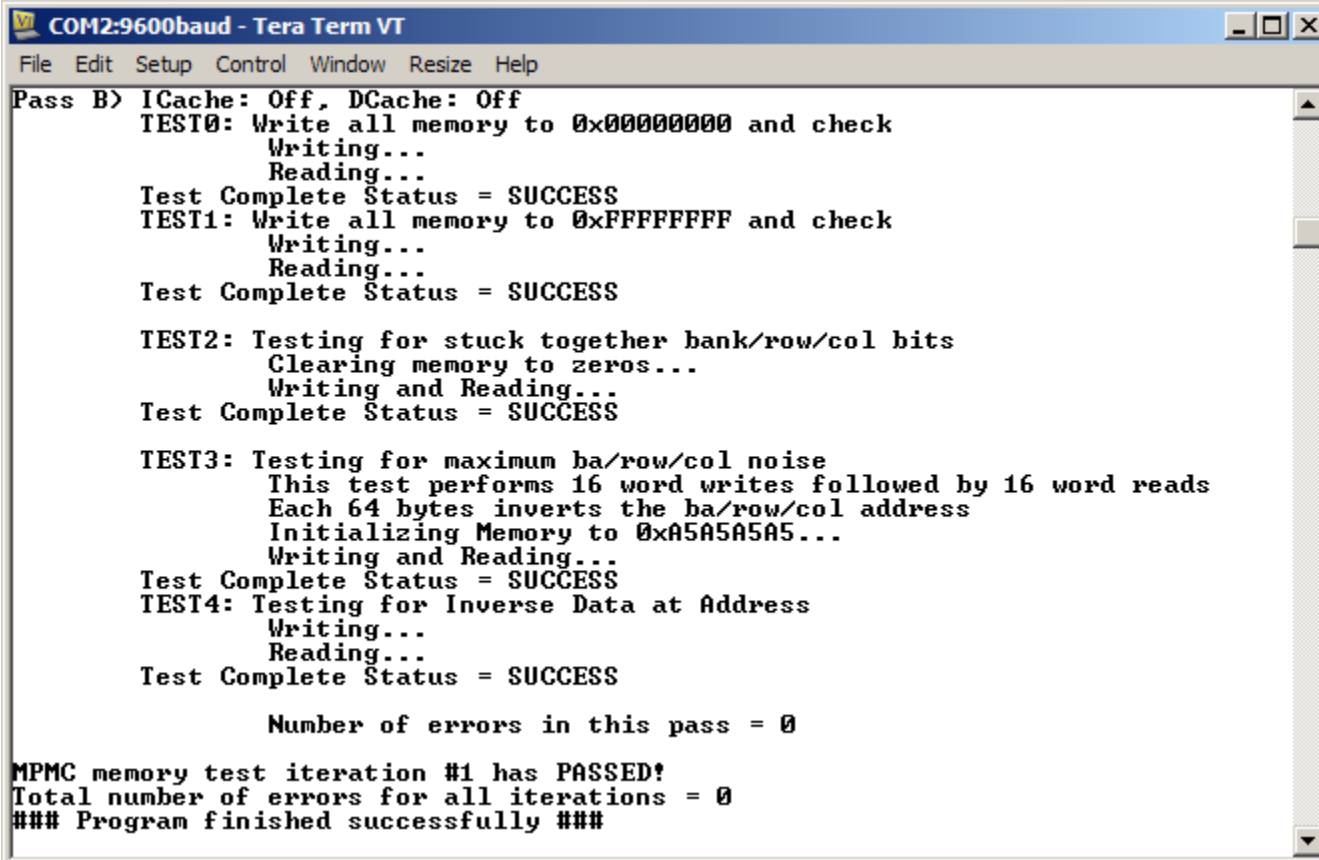
        Number of errors in this pass = 0
```

- External Memory Test running with caches on

Note: External Memory Test takes about 20 minutes

ML605 BIST

- **Second part of External Memory test (caches off)**
 - Type **9** to begin System Monitor Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
Pass B> ICache: Off, DCache: Off
TEST0: Write all memory to 0x00000000 and check
      Writing...
      Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
      Writing...
      Reading...
Test Complete Status = SUCCESS
TEST2: Testing for stuck together bank/row/col bits
      Clearing memory to zeros...
      Writing and Reading...
Test Complete Status = SUCCESS
TEST3: Testing for maximum ba/row/col noise
      This test performs 16 word writes followed by 16 word reads
      Each 64 bytes inverts the ba/row/col address
      Initializing Memory to 0xA5A5A5A5...
      Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
      Writing...
      Reading...
Test Complete Status = SUCCESS

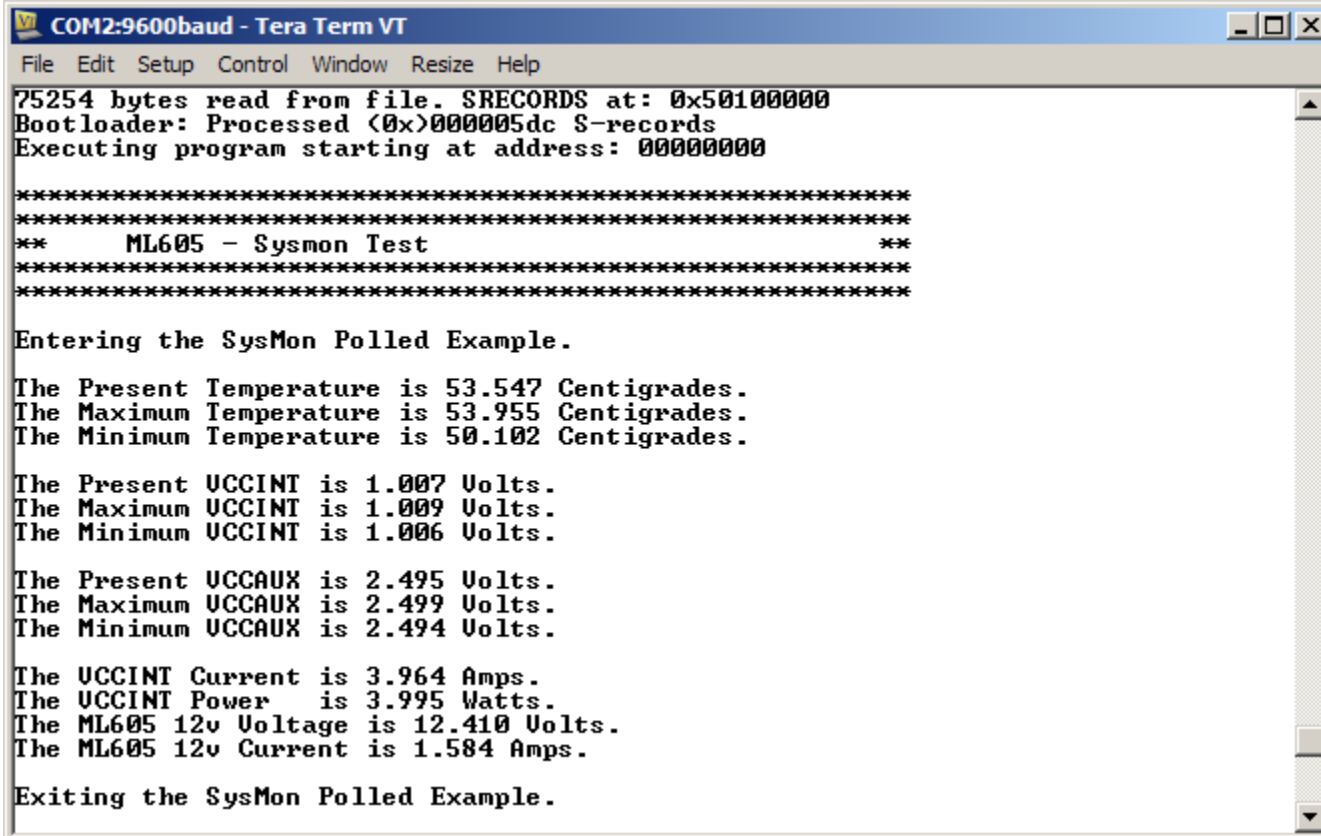
      Number of errors in this pass = 0

MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
```

ML605 BIST

- **System Monitor Test completed**

- Type **A** to begin PushButton Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
75254 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000005dc S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - Sysmon Test      **
*****
*****

Entering the SysMon Polled Example.

The Present Temperature is 53.547 Centigrades.
The Maximum Temperature is 53.955 Centigrades.
The Minimum Temperature is 50.102 Centigrades.

The Present UCCINT is 1.007 Volts.
The Maximum UCCINT is 1.009 Volts.
The Minimum UCCINT is 1.006 Volts.

The Present UCCAUX is 2.495 Volts.
The Maximum UCCAUX is 2.499 Volts.
The Minimum UCCAUX is 2.494 Volts.

The UCCINT Current is 3.964 Amps.
The UCCINT Power is 3.995 Watts.
The ML605 12v Voltage is 12.410 Volts.
The ML605 12v Current is 1.584 Amps.

Exiting the SysMon Polled Example.
```


ML605 BIST

- **PushButton Test completed**

- Type **B** to begin LCD Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
18870 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000012c S-records
Executing program starting at address: 00000000

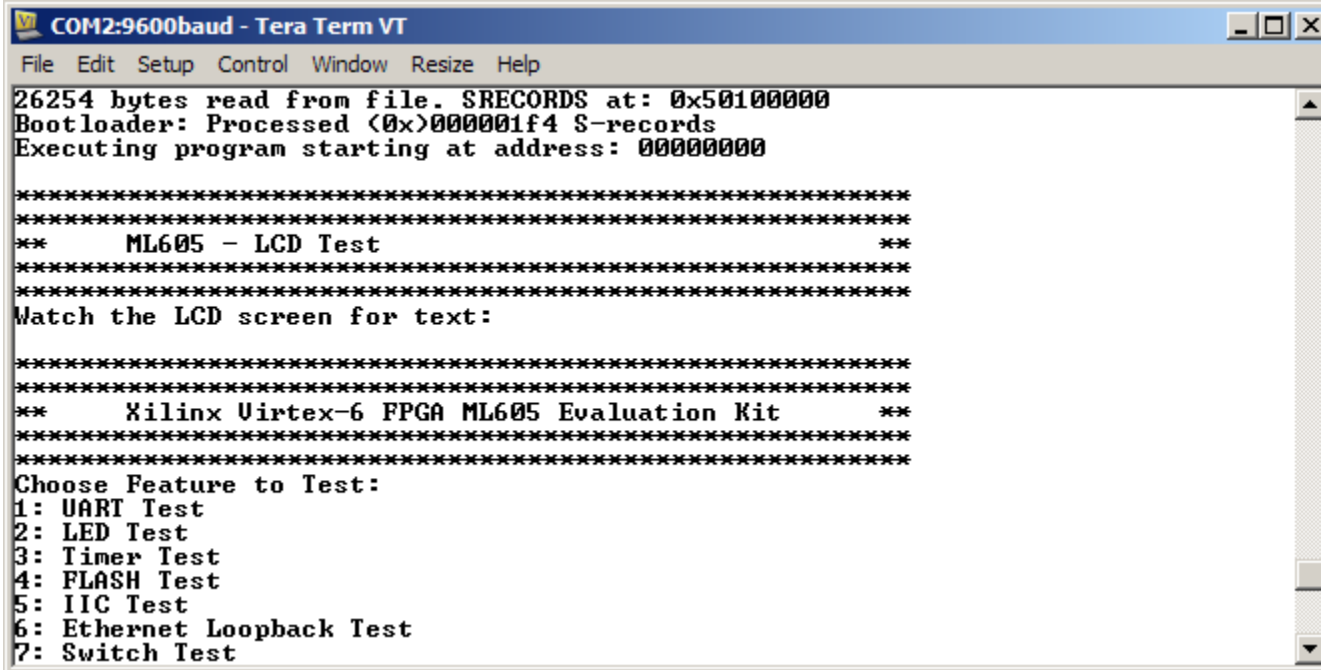
*****
*****
**      ML605 - Button Test      **
*****
*****
Press West Button & see if LED 0 glows
Press South Button & see if LED 1 glows
Press East Button & see if LED 2 glows
Press North Button & see if LED 3 glows
Press Center Button & see if all the 4 LEDs glow

*****
*****
**      Xilinx Uirtex-6 FPGA ML605 Evaluation Kit      **
*****
```

ML605 BIST

- **LCD Test completed**

- Type **C** to begin System ACE CF Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
26254 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000001f4 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - LCD Test      **
*****
*****
Match the LCD screen for text:

*****
*****
**      Xilinx Uirtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
```

ML605 BIST

```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
77430 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000640 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - Sysace Test      **
*****
*****

This program attempts to access the CF card's file system
to perform file I/O operations.

Please insert a CF card with the contents of the directory
<ref design install dir>/sw/standalone/testfatfs/required_files/
copied into a directory named test on that CF card.

Warning: This program will attempt to create a file and directory
on the CF card.

File I/O Test Program running.
Reading file : a:\test\test.txt
This is a test file.
          0123456789
          abcdefghijklmnopqrstuvwxyz

Total bytes read = 60

Reading file : a:\test\xflow.log
dummy log file

Total bytes read = 16
Reading file : a:\test\xilfatfs.pdf
Total bytes read = 59885
Failed to open a:\test\noexist.c: check if file present
Total bytes read = 0

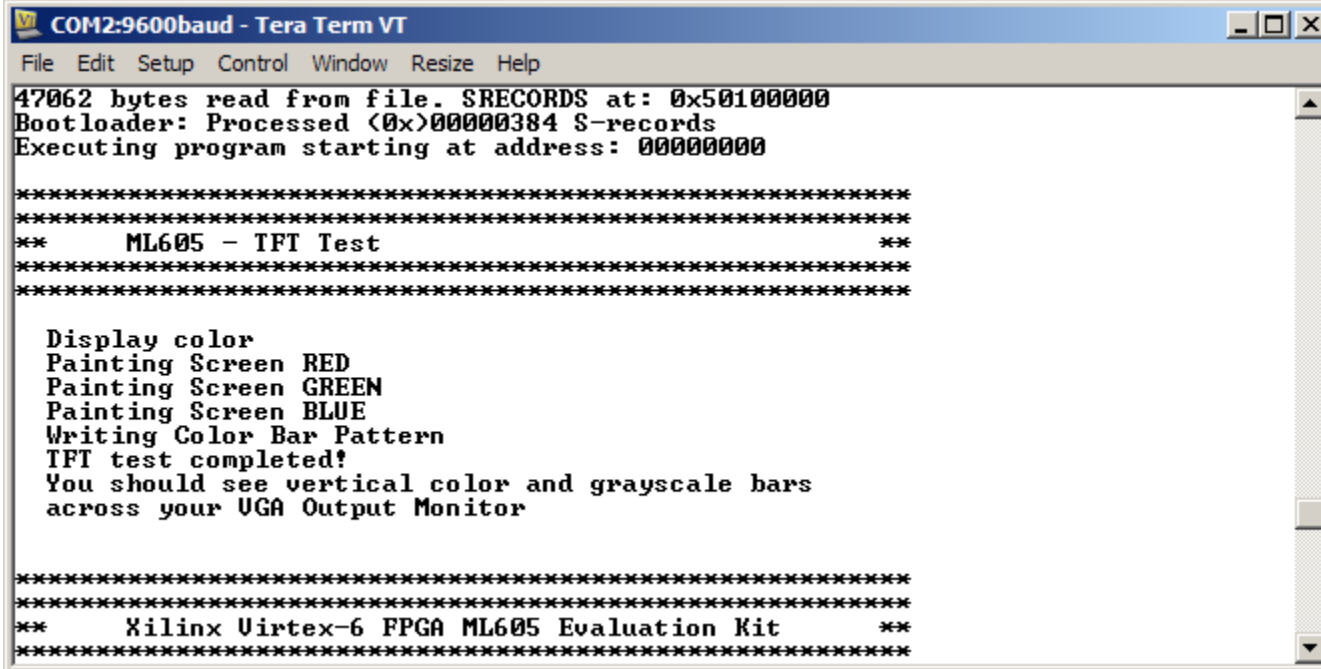
read done
Writing file contents.

# of bytes written: 38
write done
executing mkdir talica..
mkdir success
```

- **System ACE CF Test completed**
 - Connect a DVI Monitor to the ML605 board
 - Type **D** to begin DVI/VGA Test

ML605 BIST

- DVI/VGA Test completed



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
47062 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000384 S-records
Executing program starting at address: 00000000

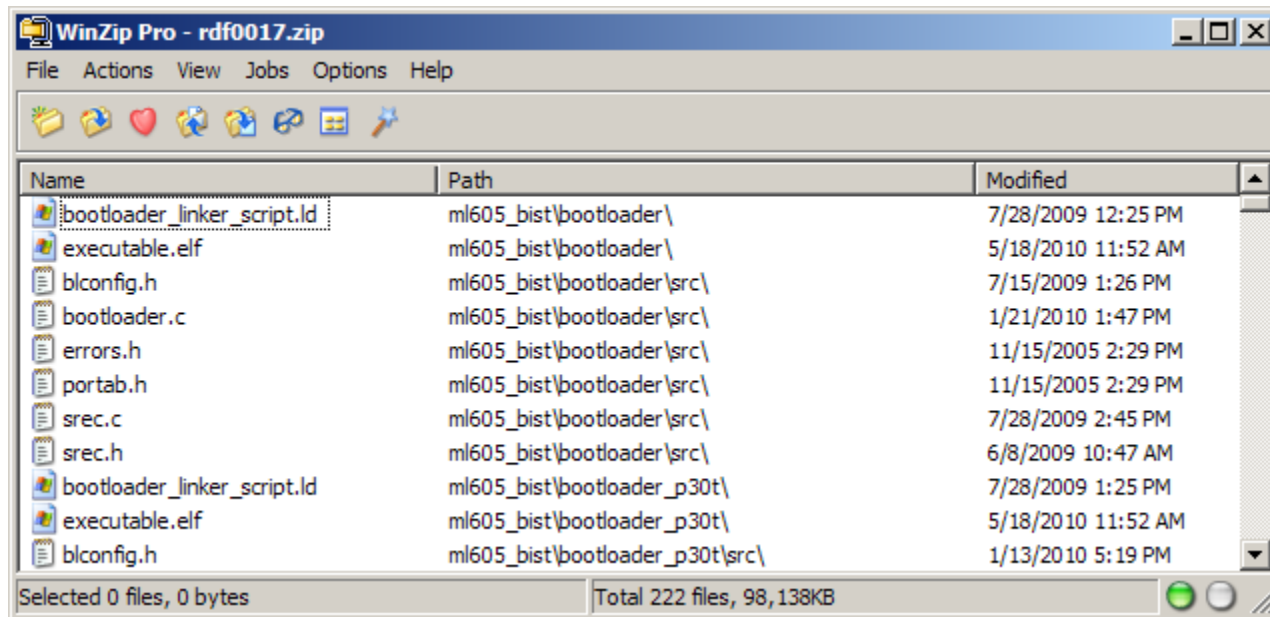
*****
*****
**      ML605 - TFT Test      **
*****
*****

Display color
Painting Screen RED
Painting Screen GREEN
Painting Screen BLUE
Writing Color Bar Pattern
TFT test completed!
You should see vertical color and grayscale bars
across your UGA Output Monitor

*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
```

Compile ML605 BIST Design

- **Unzip the rdf0017.zip file**
 - Available through <http://www.xilinx.com/ml605>



Run ML605 BIST Ready for Download Files

Run ML605 BIST Ready for Download Files

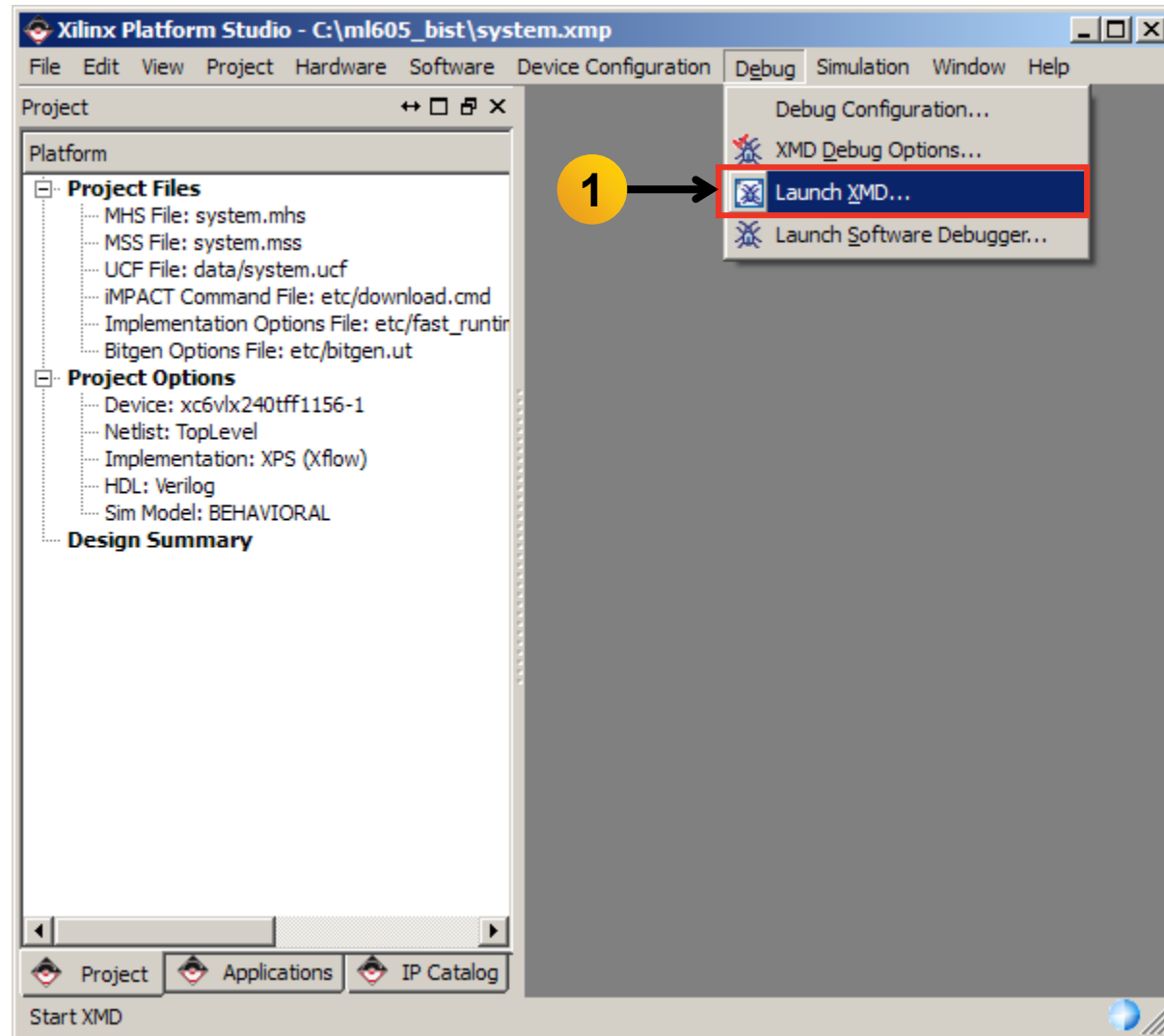
- Add a second USB Type-A to Mini-B cables to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC



Note: Presentation applies to the ML605

Run ML605 BIST Ready for Download Files

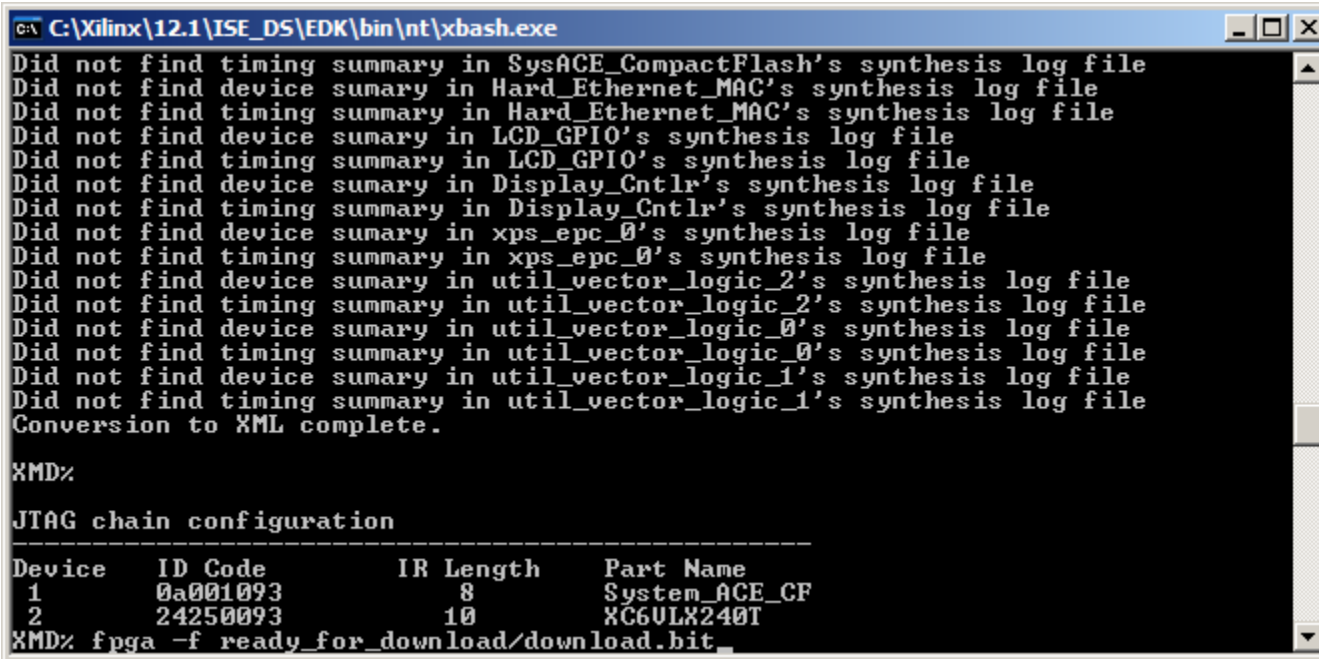
- Open XPS project
<design path>\
system.xmp
- Launch XMD
 - Select **Debug** →
Launch XMD... (1)



Run ML605 BIST Ready for Download Files

- Download the bitstream with xmd:

```
fpga -f ready_for_download/download.bit
```



```
C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe
Did not find timing summary in SysACE_CompactFlash's synthesis log file
Did not find device summary in Hard_Ethernet_MAC's synthesis log file
Did not find timing summary in Hard_Ethernet_MAC's synthesis log file
Did not find device summary in LCD_GPIO's synthesis log file
Did not find timing summary in LCD_GPIO's synthesis log file
Did not find device summary in Display_Cntlr's synthesis log file
Did not find timing summary in Display_Cntlr's synthesis log file
Did not find device summary in xps_epc_0's synthesis log file
Did not find timing summary in xps_epc_0's synthesis log file
Did not find device summary in util_vector_logic_2's synthesis log file
Did not find timing summary in util_vector_logic_2's synthesis log file
Did not find device summary in util_vector_logic_0's synthesis log file
Did not find timing summary in util_vector_logic_0's synthesis log file
Did not find device summary in util_vector_logic_1's synthesis log file
Did not find timing summary in util_vector_logic_1's synthesis log file
Conversion to XML complete.
XMD%
JTAG chain configuration
-----
Device   ID Code      IR Length   Part Name
  1      0a001093      8          System_ACE_CF
  2      24250093     10         XC6VLX240T
XMD% fpga -f ready_for_download/download.bit
```

Run ML605 BIST Ready for Download Files

- **Connect XMD to the MicroBlaze:**
connect mb mdm

```
C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe
Did not find device summary in util_vector_logic_0's synthesis log file
Did not find timing summary in util_vector_logic_0's synthesis log file
Did not find device summary in util_vector_logic_1's synthesis log file
Did not find timing summary in util_vector_logic_1's synthesis log file
Conversion to XML complete.

XMD%

JTAG chain configuration
-----
Device   ID Code      IR Length   Part Name
  1      0a001093      8          System_ACE_CF
  2      24250093     10         XC6VLX240T
XMD% fpga -f ready_for_download/download.bit
Fpga Programming Progress .....10....20....30....40....50... 0....10....20....3
0....40.Done

JTAG chain configuration
-----
Device   ID Code      IR Length   Part Name
  1      0a001093      8          System_ACE_CF
  2      24250093     10         XC6VLX240T

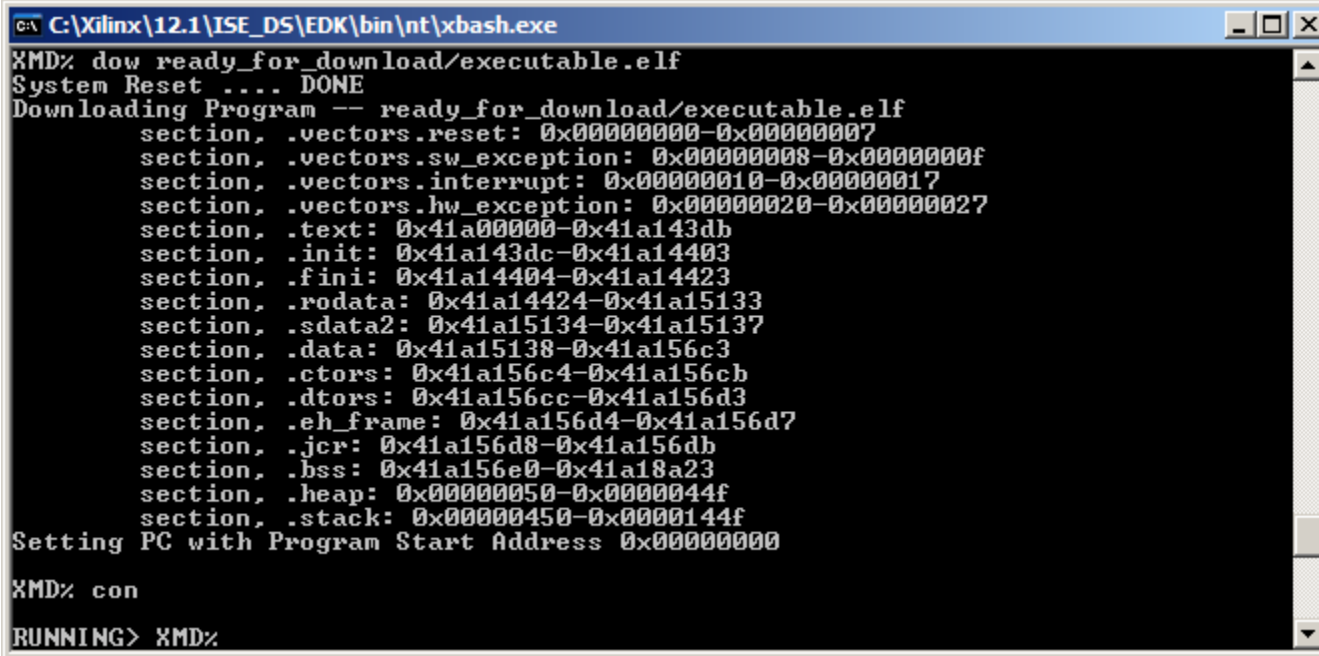
Successfully downloaded bit file.
XMD% connect mb mdm
```

Run ML605 BIST Ready for Download Files

- Download the bootloader with xmd:

dow ready_for_download/executable.elf

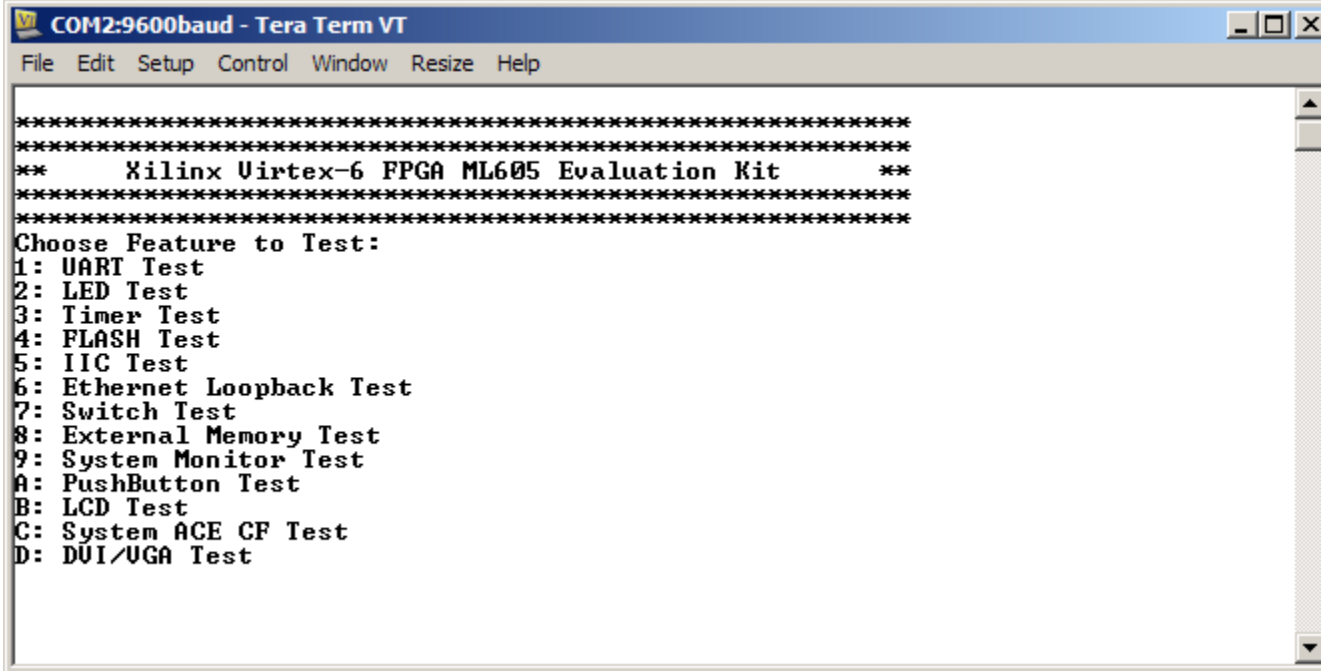
con



```
C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe
XMD% dow ready_for_download/executable.elf
System Reset .... DONE
Downloading Program -- ready_for_download/executable.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw_exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw_exception: 0x00000020-0x00000027
section, .text: 0x41a00000-0x41a143db
section, .init: 0x41a143dc-0x41a14403
section, .fini: 0x41a14404-0x41a14423
section, .rodata: 0x41a14424-0x41a15133
section, .sdata2: 0x41a15134-0x41a15137
section, .data: 0x41a15138-0x41a156c3
section, .ctors: 0x41a156c4-0x41a156cb
section, .dtors: 0x41a156cc-0x41a156d3
section, .eh_frame: 0x41a156d4-0x41a156d7
section, .jcr: 0x41a156d8-0x41a156db
section, .bss: 0x41a156e0-0x41a18a23
section, .heap: 0x00000050-0x0000044f
section, .stack: 0x00000450-0x0000144f
Setting PC with Program Start Address 0x00000000
XMD% con
RUNNING> XMD%
```

Run ML605 BIST Ready for Download Files

- Bootloader runs in the terminal window



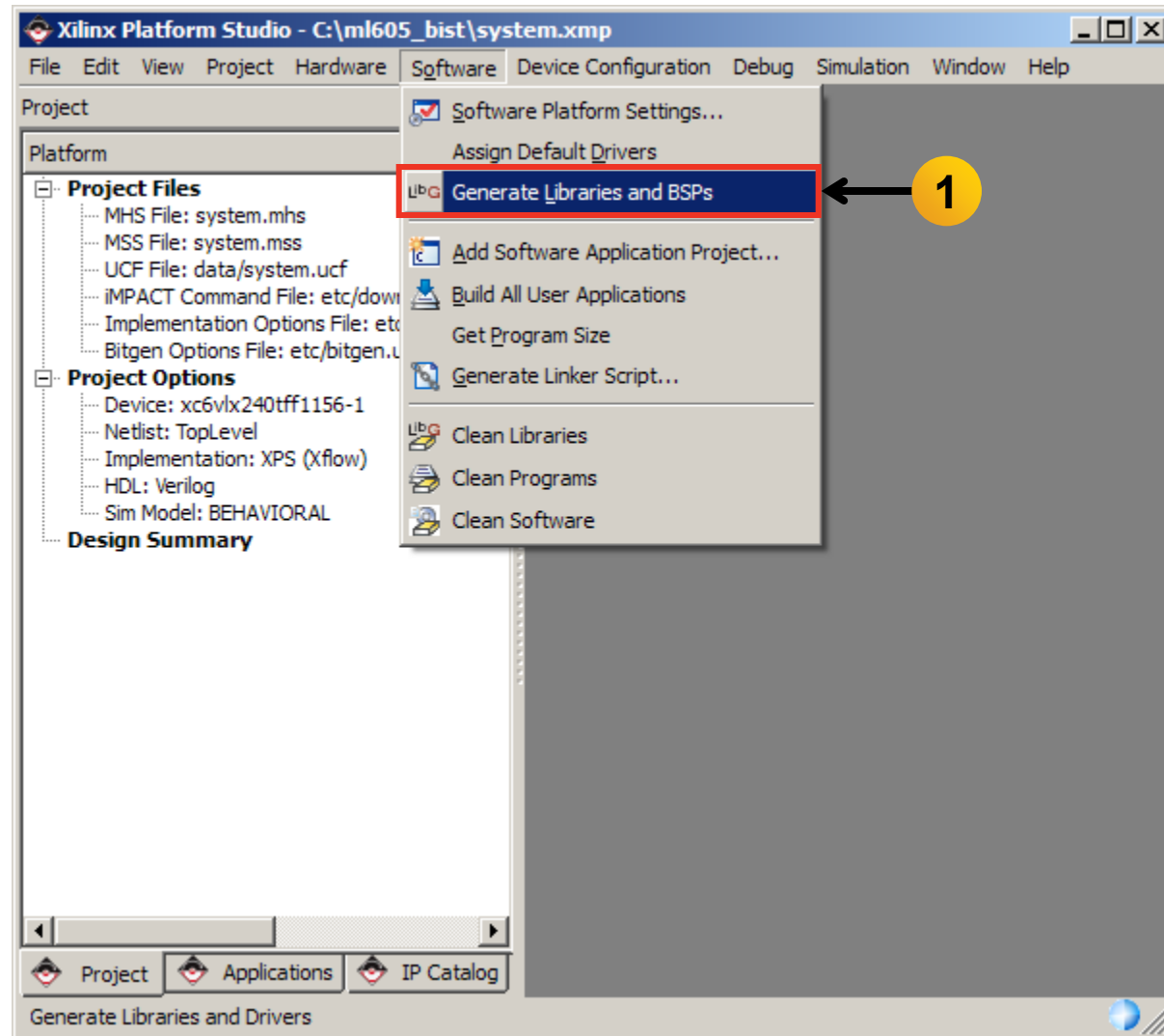
```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Resize Help
*****
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: System Monitor Test
A: PushButton Test
B: LCD Test
C: System ACE CF Test
D: DVI/UGA Test
```

Note: CompactFlash must be inserted to launch applications

Compile ML605 BIST Design

Compile ML605 BIST Design

- The BIST Design is compiled with EDK
- Generate the libraries needed to create the bitstream
 - Select **Software** → **Generate Libraries and BSPs** (1)

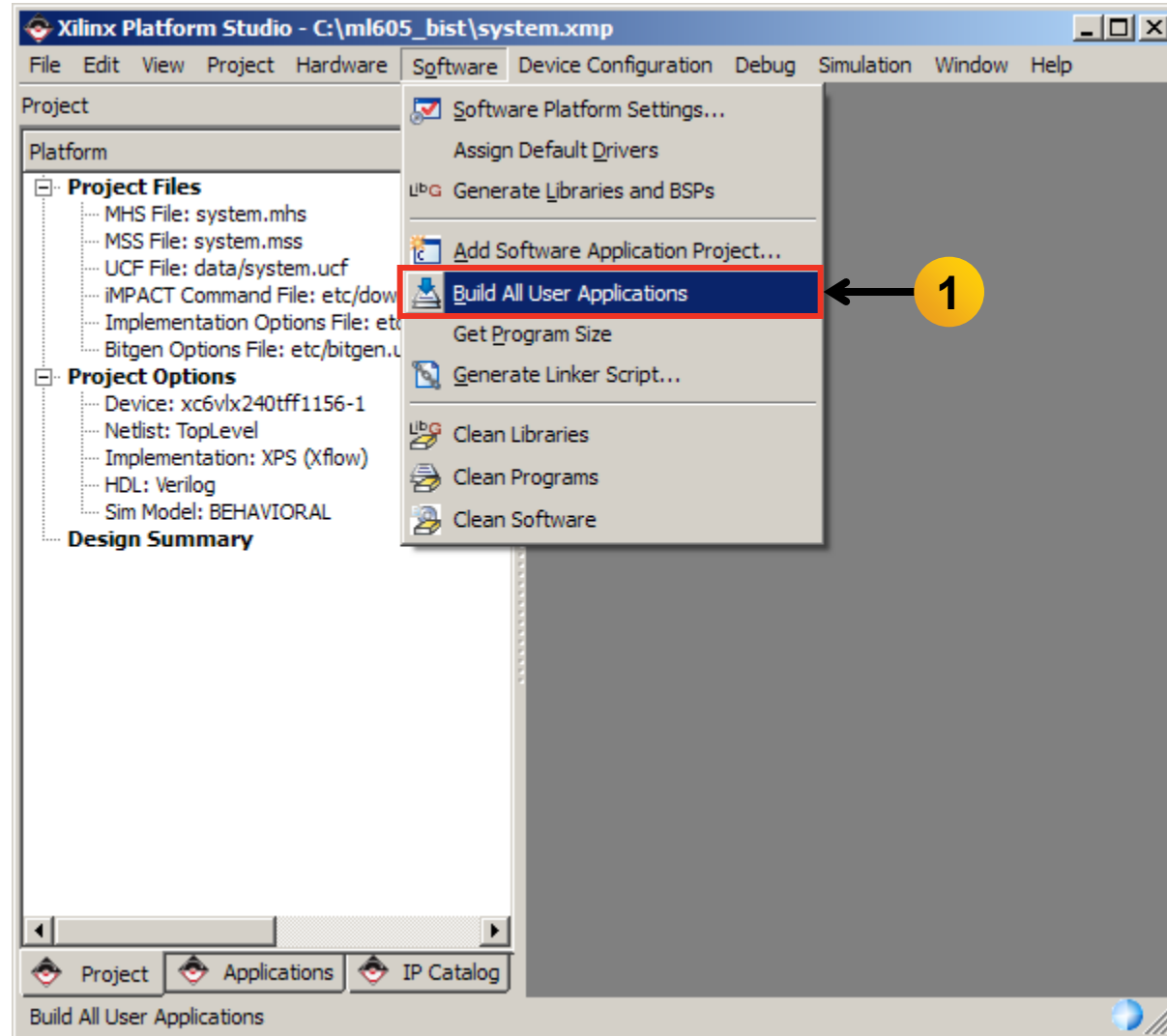


Note: Presentation applies to the ML605

Compile ML605 BIST Design

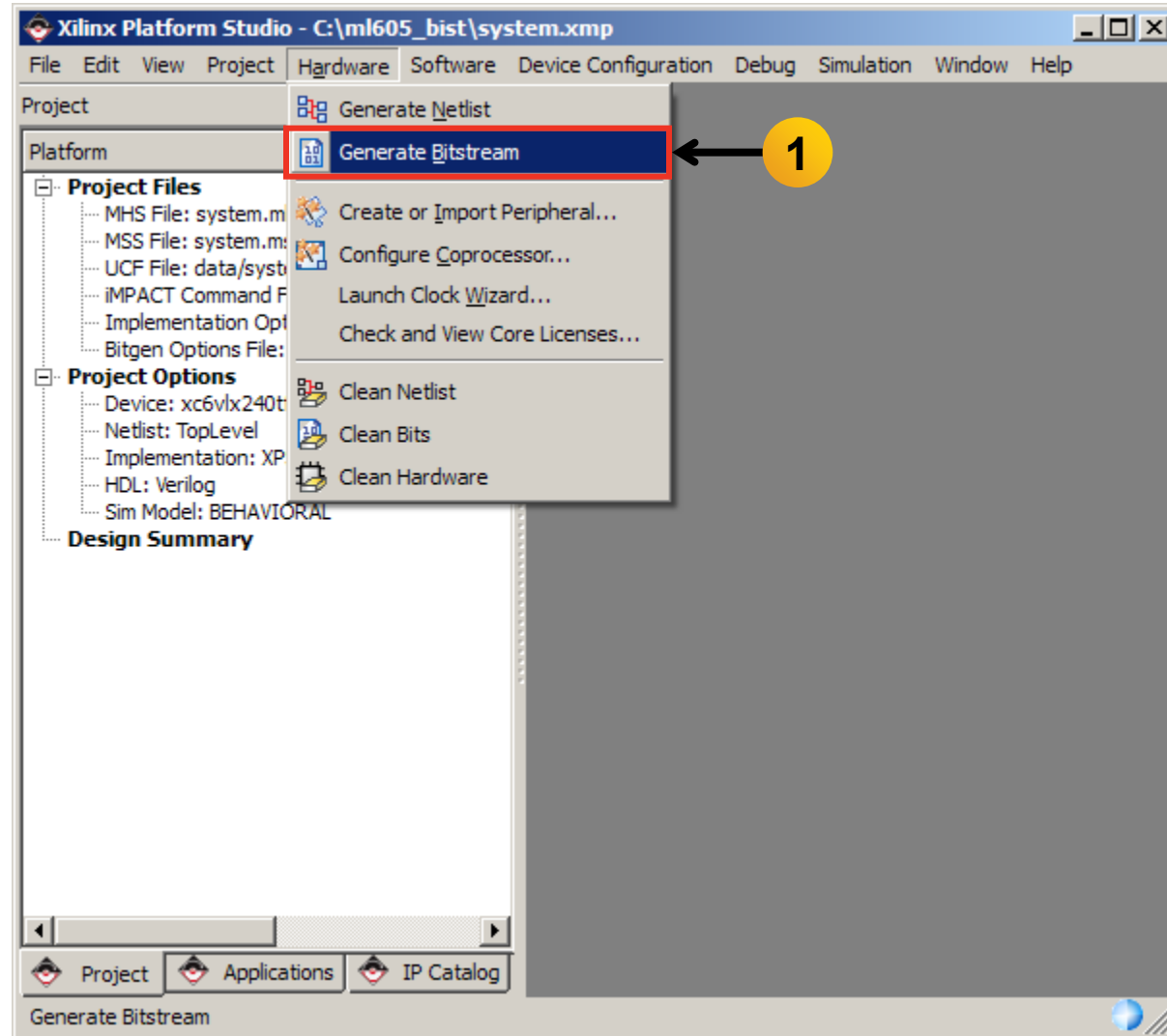
- **Compile the Software Applications and create the application ELF files**

- Select **Software** → **Build All User Applications** (1)



Compile ML605 BIST Design

- Create the hardware design, system.bit, located in <project directory>/implementation
 - Select Hardware → Generate Bitstream (1)

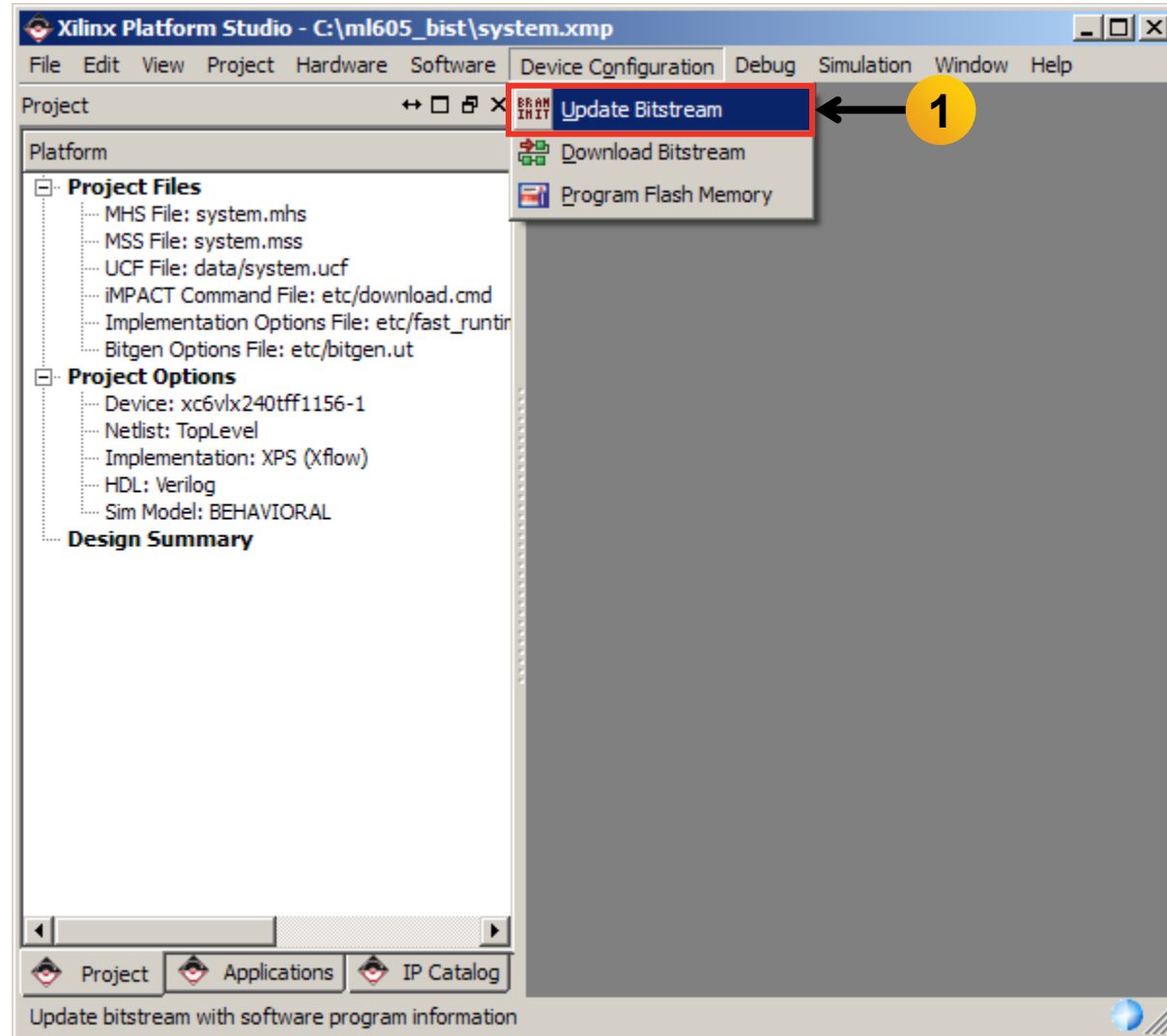


Note: Presentation applies to the ML605

Compile ML605 BIST Design

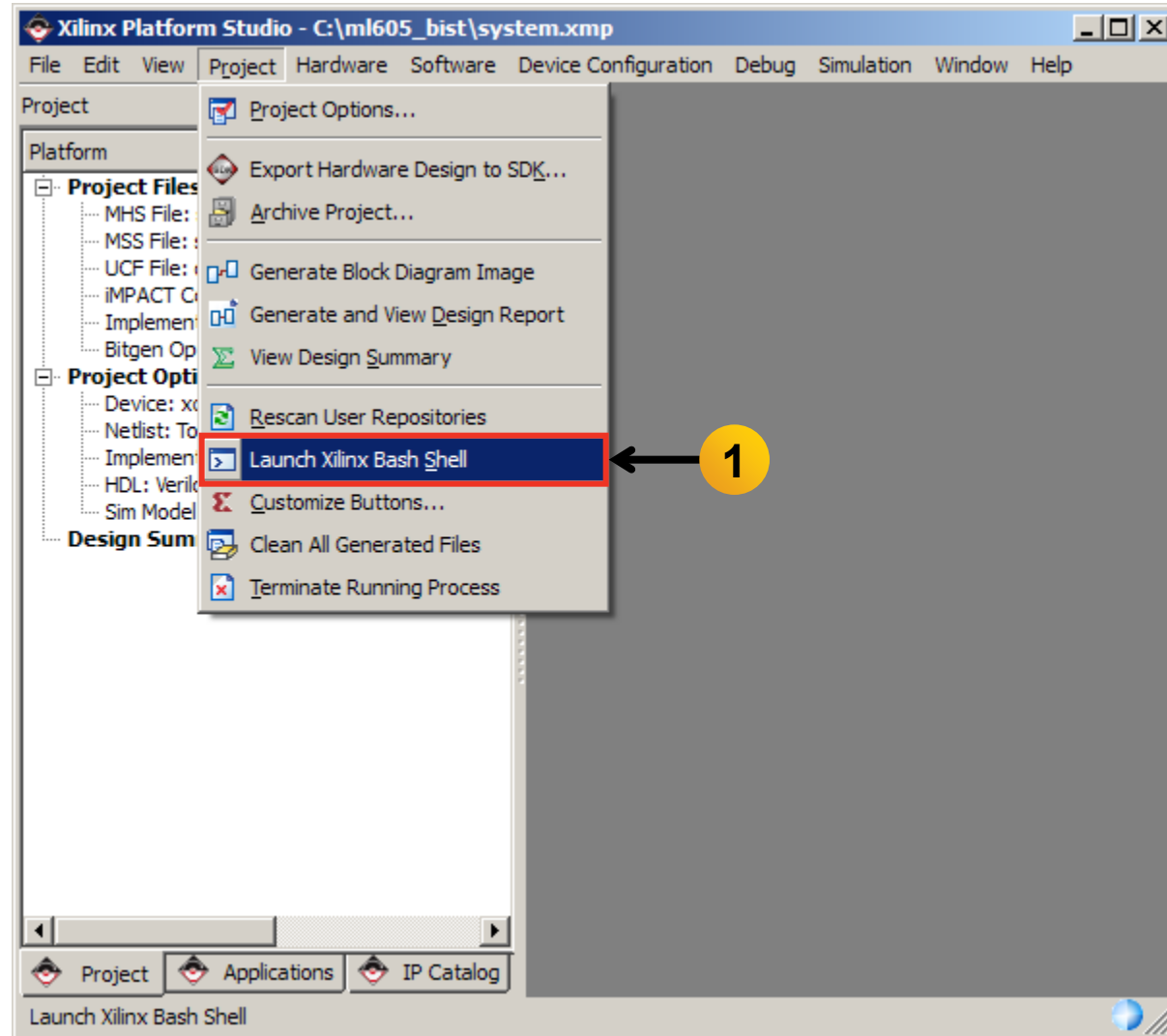
■ Init memory with the Bootloader Application ELF

- Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
- Select **Device Configuration** → **Update Bitstream** (1)



Generate ML605 BIST Design CompactFlash

- **Convert the ELF files to S-record format and create ACE file**
 - **Select Project → Launch Xilinx Bash Shell (1)**



Note: Presentation applies to the ML605

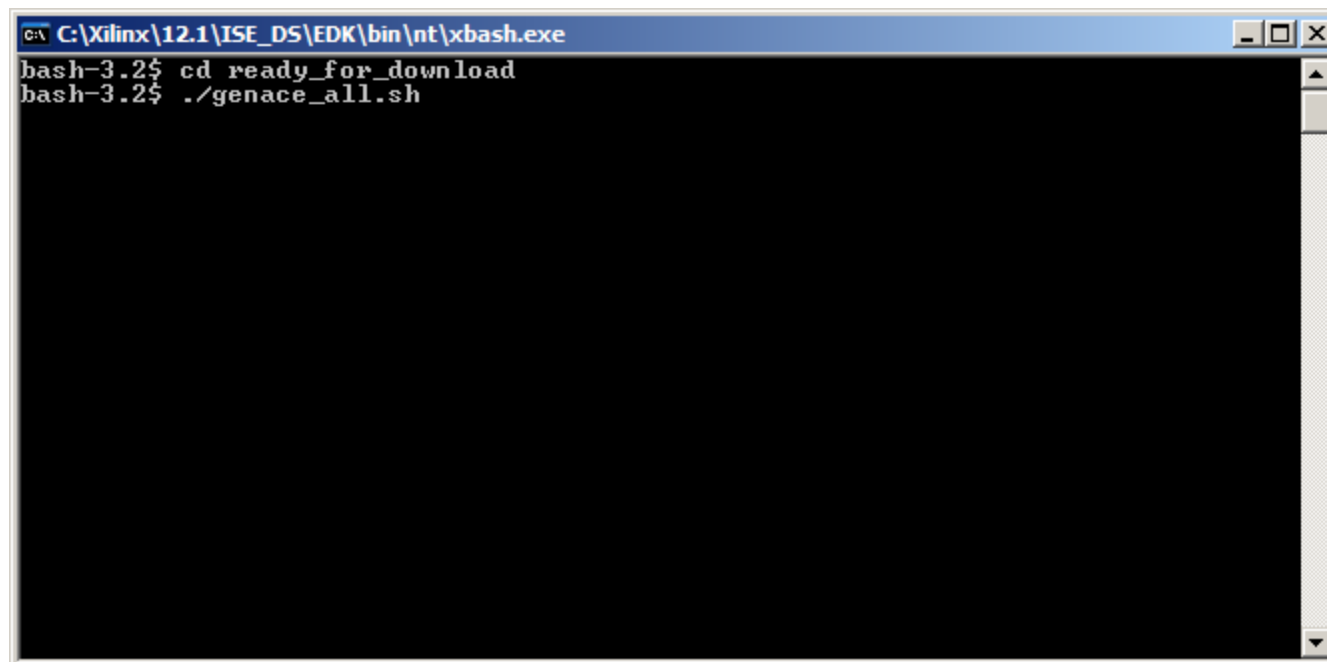
Generate ML605 BIST Design CompactFlash

- **Generate the S Records and ACE file**

 - `cd ready_for_download`

 - `./genace_all.sh`

 - Copy the contents of ready_for_download/cf_image to your CompactFlash



```
C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe
bash-3.2$ cd ready_for_download
bash-3.2$ ./genace_all.sh
```

References

References

- **EDK Documentation**

- Embedded System Tools Reference Guide

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/est_rm.pdf

- **System ACE CF**

- System ACE CompactFlash Solution

http://www.xilinx.com/support/documentation/boards_and_kits/ug080.pdf

- **Virtex-6 Configuration**

- Virtex-6 FPGA Configuration User Guide

http://www.xilinx.com/support/documentation/user_guides/ug360.pdf

Documentation

Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

<http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

<http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf