

**XTP048** 

# **ML605 System Monitor**

May 2010



### **Overview**

- Virtex-6 System Monitor Capability
- Xilinx ML605 Board
- ML605 Setup
- Running the System Monitor
- ML605 System Monitor Measurements
- Download ML605 System Monitor Design

- Compile ML605 System Monitor Design
- References

# **Virtex-6 System Monitor Capability**

- Available in all Virtex-6 Devices
- On-Chip Temperature Measurement (± 4°C)
- On-Chip Power Supply Measurement (± 1%)
- JTAG Accessible
  - Usable before, during, and after configuration
- Accessible from User Logic
- Programmable Alarms
- User Accessible Analog-to-Digital Converter

- 10-bit resolution
- 200 kSPS (kilo-samples per second)
- Digital Averaging

# Xilinx ML605 Board





# **ISE Software Requirements**

Xilinx ISE 12.1 software





- Power on the ML605 board for UART Drivers Installation
- Connect two USB Type-A to Mini-B cables to the USB JTAG and USB UART connectors on the ML605 board
  - Connect these cables to your PC



#### Install USB UART Drivers

 <u>https://www.silabs.com/Support Documents/Software/</u> <u>CP210x\_VCP\_Win2K\_XP\_S2K3.zip</u>

👰 WinZip - CP210x_VCP_Win2K_XP_	S2K3.zip		_ 🗆 🗙
File Actions Options Help			
🎋 📰 🗞 🚱 🖗 🌾			
Name	Path		Modified
CP210x_VCP_Win2K_XP_S2K3.exe			10/25/2009 4:59 PM
Selected 0 files, 0 bytes	Total 1 fil	e, 5,352KB	🖯 🗘 //.



### Right-click on My Computer and select Properties

- Select the Hardware tab
- Click on Device Manager

Sys	stem Prop	erties	<u>? ×</u>						
	System General	Restore Automatic Updates Remote Computer Name Hardware Advance	d						
	Device M	lanager The Device Manager lists all the hardware devices installed on your computer. Use the Device Manager to change the properties of any device. <u>D</u> evice Manager							
	Drivers Driver Signing lets you make sure that installed drivers are compatible with Windows. Windows Update lets you set up how Windows connects to Windows Update for drivers. Driver Signing								
	Hardware	Profiles Hardware profiles provide a way for you to set up and store different hardware configurations.							
		Hardware <u>P</u> rofiles							
_		OK Cancel App	ly						

- Expand the Ports Hardware
  - Right-click on USB to UART
     Bridge and select Properties



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<ul> <li>Under Port Settings tab         <ul> <li>Click Advanced</li> <li>Set the COM Port to an open Com Port setting from COM1 to COM4</li> </ul> </li> </ul>	icon Labs CP210x US General Port Settings	B to UART Bridge (COM2) Properties       ? ×         Driver       Details         Bits per second:       9600         Data bits:       8         Parity:       None         Stop bits:       1
Advanced Settings for COM2         Image: Use FIFO buffers (requires 16550 compatible UART)         Select lower settings to correct connection problems.         Select higher settings for faster performance.         Receive Buffer: Low (1)         Image: Image	○K       Cancel       Defaults	Elow control:     None       Advanced     Restore Defaults       OK     Cancel

#### Unzip the rdf0012.zip file to your C:\ drive

Available through http://www.xilinx.com/ml605

🖳 WinZip Pro - rdf0012.zip		
File Actions View Jobs Options He	łp	
🏷 🔁 🔇 🐼 🐼 🛡 🗮 🥕		
Name	Path	Modified 🔺
microblaze_0.elf	ml605_system_monitor\bootloops\	4/26/2010 3:15 PM
microblaze_0.elf	ml605_system_monitor\ces_grade_silicon\bootloops\	4/26/2010 3:15 PM
🔊 system.ucf	ml605_system_monitor\ces_grade_silicon\data\	4/23/2010 11:57 AM
🔊 bitgen.ut	ml605_system_monitor\ces_grade_silicon\etc\	2/18/2009 3:36 PM
S download.cmd	ml605_system_monitor\ces_grade_silicon\etc\	5/13/2009 11:12 AM
🔊 fast_runtime.opt	ml605_system_monitor\ces_grade_silicon\etc\	9/10/2009 9:04 AM
🔊 download.bit	ml605_system_monitor\ces_grade_silicon\impleme	4/26/2010 3:15 PM
🔊 system.bit	ml605_system_monitor\ces_grade_silicon\impleme	4/23/2010 1:46 PM
🔊 system.bmm	ml605_system_monitor\ces_grade_silicon\impleme	4/23/2010 1:12 PM
🛠 system.ncd	ml605_system_monitor\ces_grade_silicon\impleme	4/23/2010 1:42 PM
🔊 system.pad	ml605_system_monitor\ces_grade_silicon\impleme	4/23/2010 1:42 PM
Selected 0 files, 0 bytes	Total 84 files, 92,581KB	🖯 🛈 /i.

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Download the System Monitor bitstream:

# cd ml605\_system\_monitor\ready\_for\_download xmd





#### Start the Terminal Program

- Select your USB Com Port
- Set the baud to **115200**
- Start after bitstream is loaded

🛄 Tera	a Term - (	OM2 VT							
File Ed	dit Setup	Control	Window	Help					
			Tera Tern	n: Serial port	: setup			×	-
			<u>P</u> ort	t:	COM2	•	ОК		
			<u>B</u> au	id rate:	115200	-			
			<u>D</u> ata	a:	8 bit	•	Cancel		
			P <u>a</u> ri	ity:	none	•			
			<u>S</u> top	<b>p:</b>	1 bit	•	<u>H</u> elp		
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The System Monitor display will appear in the Terminal window

🖳 C	OM2:	115200	baud - T	era Term	VT			×
File	Edit	Setup	Control	Window	Resize	Help		
*** * *	****	****	*****	*****	****	<del>(xxxx</del> Sysl	**************************************	-
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* * * *					====	=== B 12V S 12V C	pard Sensors ====== upply: 12.079 U urrent: 1.723 A	
* * *				=== P	== Vco l lccint int =	cint ) Jshuni t = V: Icci	Power Measurement ===== t : 16.4 mU shunt/5mOhm : 3.289 A nt * Vccint : 3.320 W	
*						I	Alarms: OK	
* **	****	****	*****	() ******	Press *****	any I «××××	Key for Menu Options) ************************************	•

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# **ML605 System Monitor Measurements**

### 12V Supply

- Voltage, VAUXP[13], VAUXN[13] External Channel
- Current, VAUXP[12], VAUXN[12] External Channel

#### VCCINT

- Voltage Internal Channel
- Current, VP, VN External Channel

#### VCCAUX

- Voltage - Internal Channel

#### Temperature

- Internal Channel



- The System Monitor Design can be compiled with EDK
- Open XPS project
   <design path>\
   system.xmp
- Generate the libraries needed to create the bitstream
  - Select Software →
     Generate Libraries
     and BSPs (1)



- Compile the Software Applications and create the application ELF files
  - Select Software →
     Build All User
     Applications (1)

🚭 Xilinx Platform Studio - C:\ml60	5_system	_monitor\system.x	mp			
File Edit View Project Hardware	S <u>o</u> ftware	Device Configuration	Debug	Simulation	Window	Help
Project	Softw Softw	are Platform Settings				
Platform	Assigr	n Default <u>D</u> rivers				
Project Files     MHS File: system mbs	L <sup>ID</sup> G Gener	ate <u>L</u> ibraries and BSPs				
MSS File: system.mss	Add S	oftware Application Pro	ject			
····· UCF File: data/system.ucf ····· iMPACT Command File: etc/dow	📥 <u>B</u> uild /	All User Applications		<b>←</b>	1	
···· Implementation Options File: etc	Get P	rogram Size				
Project Options	🛐 <u>G</u> ener	ate Linker Script				
Device: xc6vlx240tff1156-1     Netlist: TopLevel	Libe Clean	Libraries				
Implementation: XPS (Xflow)	Clean	Programs				
Sim Model: BEHAVIORAL	Clean	Software				
Project Or Applications	IP Catalog					
build All User Applications						<b>v</b> //,

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- Create the hardware design, system.bit, located in
   <project directory> /implementation
  - Select Hardware →
     Generate Bitstream (1)

٠	Kilinx F	Platfo	rm Studio	o - C:\	,ml60	5_system	_monitor\syst	em.xı	mp			
File	Edit	View	Project	Hard	ware	Software	Device Configura	ation	Debug	Simulation	Window	Help
Proj	ect			<b>お</b> 名(	Genera	ate <u>N</u> etlist						
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												✓ //i

### Init memory with the bootloop ELF

- Update the bitstream (download.bit) with the bootloop ELF (microblaze\_0.elf)
- Select Device
   Configuration →
   Update Bitstream (1)



# Generate System Monitor ACE File (Optional)

- Convert the ELF files to S-record format and create ACE file
  - Select Project →
     Launch Xilinx Bash
     Shell (1)

📀 Xilinx Platfor	rm Studio - C:\ml605_system_monitor\system.xmp	_ 🗆 🗵
File Edit View	Project Hardware Software Device Configuration Debug Simulation Window He	lelp
Project	Project Options	
Platform  Platform  Platform  Project Files  MSS File:  UCF File:  MSS File:  VCF File:  Project Opti Device: xx Netlist: To Device: xx Netlist: To MIDL: Verik Sim Model Design Sum  Project Opti Project Verik Sim Model Verik Ver	Export Hardware Design to SDK Archive Project Archive Project Archive Project Archive Project Archive Project Generate Block Diagram Image Generate and View Design Report View Design Summary View Design Summary View Design Summary Nescan User Repositories Launch Xilinx Bash Shell Clean All Generated Files Terminate Running Process Applications P Catalog	
Launch Xilinx Bash	n Shell	🤍 (h

# **Generate System Monitor ACE File (Optional)**

- Generate the ACE file
- Open

cd ready\_for\_download ./genace\_all.sh

C:\Xiinx\12.1\ISE\_DS\EDK\bin\nt\xbash.exe
 bash=3.2\$ cd ready\_for\_download
 bash=3.2\$ ./genace\_all.sh



#### Download Bitstream

Select Device
 Configuration →
 Download Bitstream
 (1)



- Download the System Monitor ELF with XMD
  - Select Debug →
     Launch XMD (1)



 The first time XMD runs on a project, the XMD Debug options must be set

Please set the XMD Debug Options in Debug->XMD Debug Options before running >

OK

	ፍ XMD Debug Options Deprecated	×
	Processor: microblaze_0 Architecture: MicroBlaze	
	Connection Type	
	C Simulator C Hardware C Stub	
	JTAG Properties Advanced Options	
	Read-Only Memory Addr: Size (in Hex):	
×		
md		
	OK Cancel Help	

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📀 Platform Studio

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XMD opens and connects to the processor, using the default options

C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe	- D ×
Version	
OptimizationPerformance	
MMIL Tune	
No of PC Breakvoints	
No of Read Addr/Data Watchpoints0	
No of Write Addr/Data Watchpoints0	
Instruction Cache Supporton	
Instruction Cache Base Address0x50000000	
Instruction Cache High Huuress0x3fffffff	
Data Cache Base Address	
Data Cache High Address0x5fffffff	
Exceptions Supportoff	
FPU Supportoff	
Hard Divider Support	
Raywel Shiftey Support	
MSR clr/set Instruction Supporton	
Compare Instruction Supporton	
Data Cache Write-back Supportoff	
Connected to "MD" target. 1d = 0 Stanting CDP conversion for "mb" target (id = 0) at TCP ment po 1224	
XMDx	-
Pure a second seco	

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To execute a memory read, type

mrd 0x0000000

This will read the memory address at the reset vector; the value should be 0xB0005000 as shown below

<pre>C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe</pre>	
MMU TypeNo_MMU	<b>_</b>
No of PC Breakpoints	
No of White Addm/Data Watchpoints0	
Instruction Cache Supporton	
Instruction Cache Base Address0x50000000	
Instruction Cache High AddressØx5fffffff	
Data Cache Supporton Data Cache Baco Adducco AvE000000	
Data Cache High Address	
Exceptions Supportoff	
FPU Supportoff	
Hard Divider Supportoff	
Barvel Shifter Support	
MSR clr/set Instruction Supporton	
Compare Instruction Supporton	
Data Cache Write-back Supportoff	
Connected to "mb" tanget $id = 0$	
Starting GDB server for "mb" target (id = 0) at TCP port no 1234	
XMD% mrd 0x0000000	
0: B8000000	
XMD%	-

#### Download and run the System Monitor ELF file:

#### dow system\_monitor/system\_monitor.elf

con

C:\Xilinx\12.1\ISE_DS\EDK\bin\nt\xbash.exe	
VMDy day sustan ansitan (sustan ansitan alf	<b>_</b>
AND/ UOW System_monitor/system_monitor.eif Sustam Basat DONE	
oystem neset Done Nounloading Pwognam sustem monitov/sustem monitov elf	
section vectors reset: 0x0000000-0x0000007	
section. vectors.sw exception: 0x0000008-0x0000000f	
sectionvectors.interrupt: 0x0000010-0x00000017	
section, .vectors.hw_exception: 0x00000020-0x00000027	
section, .text: 0x41a00000-0x41a071f3	
section, .init: 0x41a071f4-0x41a07217	
section, .fini: 0x41a07218-0x41a07233	
section, .ctors: 0x41a07234-0x41a0723b	
section, .dtors: 0x41a0?23c-0x41a0?243	
section, .rodata: 0x41a0/244-0x41a0/af1	
section, .data: $0\times41a07at8-0\times41a07c73$	
section, .en_trame: 0x41a0/c/4-0x41a0/c//	
Section, .jcr $0.341a07c70^{-0}2341a07c70$	
section, stack: $0 \times 41 = 0 \otimes 10^{-1} \otimes 10^{-$	
Setting PC with Program Start Address Ax0000000	
XMD% con	
RUNNING> XMDz	<b>~</b>

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The System Monitor display will appear in the Terminal window

🖳 C	🚇 COM2:115200baud - Tera Term VT							
File	Edit	Setup	Control	Window	Resize	Help		
*** * *	****	<del>* * * * *</del>	*****	*****	*****	<del>(xxxx</del> SysM		•
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× × ×					==== [ [	=== Bo 2V Su 2V Cu	ard Sensors ====== pply: 12.079 V rrent: 1.723 A	
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# References

- Virtex-6 System Monitor
  - Virtex-6 FPGA System Monitor UG370

http://www.xilinx.com/support/documentation/user\_guides/ug370.pdf

- ChipScope Pro Software and Cores User Guide

http://www.xilinx.com/support/documentation/sw manuals/ xilinx12 1/chipscope pro sw cores ug029.pdf

#### EDK Documentation

- Embedded System Tools Reference Guide

http://www.xilinx.com/support/documentation/sw\_manuals/xilinx12\_1/est\_rm.pdf







# **Documentation**

#### Virtex-6

- Virtex-6 FPGA Family

http://www.xilinx.com/products/virtex6/index.htm

#### ML605 Documentation

- Virtex-6 FPGA ML605 Evaluation Kit

http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards\_and\_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards and kits/ug535.pdf

