

XTP047

ML605 MIG Design Creation

May 2010



Overview

- Virtex-6 DDR3 Memory Interface
- ML605 Board
- ML605 Setup
- Generate MIG Example Design
- Modifications to Example Design
- Compile Example Design
- Run MIG Example Design
- Adjust Data Pattern using VIO Console

- Example Design VIO Consoles
- References

Virtex-6 DDR3 Memory Interface

- Pre-Engineered Controller and Physical Layer (PHY) memory interface
- 300-533 MHz (600-1066 Mb/s) Performance
 - Center Column Interfaces
 - 400 MHz in a -1 speed device
 - 533 MHz in -2, -3 devices
- I Gb density memory device support
- X4, x8, x16 device support
- Configurable data bus widths
 - Multiples of 8 bits, up to 72 bits



Virtex-6 Memory Controller and Interfaces

Improved performance

- Higher data rates
 - Faster circuitry (40 nm)
 - Enhanced I/O (50 ps IODELAY)
 - Dedicated clocking paths
 - Real-time calibration
- Higher effective bandwidth
 - Reordering controller (DDR3/DDR2)

Improved functionality

- DDR3 DIMM write leveling

Easy to use

- MIG for ISE design flow
- MPMC for EDK design flow

Xilinx makes it easier and faster to design with Virtex-6

ML605 provides DDR3 SO-DIMM



DDR3 User Interfaces

Virtex-6 FPGA user interface similar to Virtex-5 architecture

- Native interface option available for the advanced users to achieve lower latency



Reordering for Higher Effective Bandwidth

- Half-frequency DDR2/DDR3 controller
 - Control state machine runs at half the memory clock rate

Reorder READs to avoid precharge time penalty

 Example : Execute out-of-order READs to a different bank while performing precharge for the current bank

Regroup READs and WRITEs to minimize bus turnaround

- Example : Read A Write B Read C Write D
- Reordered to: Read A Read C Write B Write D
- Reordering controller looks ahead several commands
 - Efficiency is dependent on applications (address / command patterns)

Reordering can more than double the throughput



Xilinx ML605 Board





ISE Software Requirements

Xilinx ISE 12.1 software





ChipScope Pro Software Requirement

Xilinx ChipScope Pro 12.1 software



Release Version: 12.1 Application Version: M.53d (Build 12100.10.99.1220) Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.





Open the CORE Generator

Start \rightarrow All Programs \rightarrow Xilinx ISE Design Suite 12.1 \rightarrow

 $\mathsf{ISE} \to \mathsf{Accessories} \to \mathsf{CORE}$ Generator

■ Create a new project; select File → New Project

🂐 Xilinx CORE Gen	Xilinx CORE Generator - No Project						
<u>File</u> View Help							
New Project	Ctrl+N			₽×			
ờ Open Project	Ctrl+O	ame			Vilinx CORE Generator		
<u>C</u> lose Project	Ctrl+W	△ Version	n Status	License	Logicit		
Recent Projects	•						
Save	Ctrl+S				There is no project open.		
Save <u>A</u> s,		king			You may browse the IP Catalog but you will not be able to generate any cores until you		
Preferences					open or create a project.		
		յո					
E <u>x</u> it	Ctrl+Q	onto.			Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.		
E Standard Bus	s Interfaces	ients					
🗄 🦻 Video & Imag	ge Processing	g					
Security TD Controls on U				Class			
Search IP Catalog:				Clear			
All IP versions		Coly IP co	mpatible wit	h chosen part			
New Project					Part: Unset Design Entry: Unset	et 🌔 //	

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🂐 Project Options				? ×
Part	-Part			
Generation Advanced	Select the part for	your project:		
	Fa <u>m</u> ily	Virtex6	•	·
	De <u>v</u> ice	xc6vlx240t	•	-
	P <u>a</u> ckage	ff1156	•	-
	Speed Grade	-1	•	
I	OK	Cancel	Apply	Help
			Apply	

Note: Presentation applies to the ML605

- Create a project directory: ml605_mig_design
- Name the project: ml605_mig_design. cgp
- Set the Part (as shipped on the ML605):
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1

🂐 Project Options		<u>? ×</u>
Part Generation Advanced	Flow © Design Entry © Custom Output Products Please refer to the online help for in models using compxlib and using .VE Flow Settings Vendor	Verilog formation about compiling behavioral (O (Verilog) templates.
	Netlist <u>B</u> us Format	B <n:m></n:m>
	Simulation Files Preferred Simulation Model Behavio <u>r</u> al C Str <u>u</u> ctural C <u>N</u> one	Preferred Language C VHDL VHDL Verjlog
	Other Output Products	
1	<u>O</u> K <u>C</u> ance	I <u>A</u> pply <u>H</u> elp

Select Generation

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- Set the Design Entry to Verilog
- Click OK

Right click on MIG Version 3.4

- Select Customize and Generate

🕻 Xilinx CORE Generator - C:\ml605_mig_design\ml605_mig_design.cgp						
File Project View Help						
I 🖓 🖻						
IP Catalog	₽×					
View by Function View by Name		REFERENCE	MIG	O		
Name 🛆 Version Status License		DESIGN		Show Project		
Digital Signal Processing FPGA Features and Design Math Functions Memories & Storage Elements FIFOs Memory Interface Generators Memory Interface Generators Memory Interfaces Math Sk ROMs Standard Bus Interfaces View Data Sheet View Version Information Search IP Catalog: Only IP compatible with chosen	▼ ar n part	This core is supported in this core is supported in the support of the support of the summary: Core Summary:	rted at status Pre-Production by your chosen part. ON MIG 3.4 This Memory Interface Generator is a simple menu driven tool to generate advanced memory interfaces. This tool generates HDL ar pin placement constraints that will help you design your application Spartan-3 family supports DDR & DDR2 SDRAM. Spartan-6 suppor LPDDR, DDR, DDR2 & DDR3 SDRAM. Virtex-4 supports DDR & DDR SDRAM and QDRII & DDRII SRAM and RLDRAM II. Virtex-5 suppor DDR & DDR2 SDRAM, QDRII SRAM and DDRII SRAM. Virtex-6 supports DDR2 & DDR3 SDRAM. RLDRAM II and ODRII + SRAM.	nd ts .2 ts		
			Part: xc6vlx240t-1ff1156 Design Ent	ry: Verilog 🌍 🎵		

Xilinx Memory Interface Generator					
REFERENCE DESIGN 🖽	Memory Interface Generator The Memory Interface Genera creates complete customized constraints for the FPGA selec	ator (MIG) creates memory controllers for Xilinx FPGAs. MIG Verilog or VHDL RTL source code, pin-out and design cted, and script files for implementation and simulation.			
	CORE Generator Options This GUI includes all configurable options along with explanations to aid in generation of the required controller. Please note that some of the options selected in the CORE Generator Project Options will be used in generation of the controller. It is very important that the correct CORE Generator Project Options are selected. These options are listed below.				
	Selected CORE Generator Pro	iject Opuons:			
	FPGA Family	Virtex-6			
Memory	FPGA Part	xc6vlx240t-ff1156			
	Speed Grade	-1			
	Synthesis Tool	XST			
Interface	Design Entry	VERILOG			
Generator	If any of these options ar CORE Generator Project O	re incorrect, please click on "Cancel", change the Options, and restart MIG.			
EXILINX					
Version Info User Guide View Dat	a Sheet	<u>N</u> ext> <u>C</u> ancel			

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Xilinx Memory Interface Generator			
REFERENCE DESIGN 🔛	MIG Output Options Create Design Select this option to generate a new memory controller. Generating a memory		
	controller will create RTL, design constraints (UCF), implementation and simulation files. C Xilinx Reference Boards Select this option for information on specific designs for Xilinx reference boards. Verify UCF and Update Design and UCF Selection this feature workfact the medified UCE for a design already concerted.		
Memory	through MIG. It updates the input UCF file to be compatible with the current version of MIG. While updating the UCF it preserves the pin outs of the input UCF. This option will also generate the new design with the Component Name you selected in this page.		
Interface	Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design", "user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.		
Generator	Component Name mig_v3_4 Multi-Controller Up to 8 DDR3 SDRAM controllers or 8 QDRII+ SRAM controllers or a combination of both can be generated. DDR2 and RLDRAM II are not supported for more than 1 controller. The number of controllers that can be accommodated may be limited by		
	the data width and the number of banks utilized. Number of Controllers 1		
Version Info User Guide View Data	Sheet < <u>B</u> ack <u>N</u> ext> <u>C</u> ancel		

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💐 Xilinx Memory Interface Generator

REFERENCE DESIGN E Pin Compatible FPGAs Memory Selection Controller Options Memory Options FPGA Options	Pin Compatible FPGAs Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If you change the target part, use the appropriate UCF in the compatible_ucf folder. If you do not choose a Pin Compatible FPGA now and need to use a different FPGA later, the generated UCF may not work for the new device and a board spin may be required. A device is considered compatible only if the package and speed grade matches to the target part. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process. Blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped. Target FPGA <u>xc6vlx240t-ff1156</u> -1
Extended FPGA Options	Pin Compatible FPGAs
Bank Selection	
Summary Memory Model	
PCB Information	□ ·····□ xc6vlx365t-ff1156 □ ··· sx
Design Notes	
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Version Info User Guide View Data	Sheet < <u>B</u> ack <u>N</u> ext> <u>C</u> ancel

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- Click Next

💐 Xilinx Memory Interface Generator					
REFERENCE DESIGN 🖽	Memory Selection Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA and speed grade chosen.				
Pin Compatible FPGAs 🛛 🚩	Select the Controller Type:				
Memory Selection	DDR3 SDRAM				
Controller Options	C DDR2 SDRAM				
Memory Options	C QDRII+ SRAM				
FPGA Options	C RLDRAM II				
Extended FPGA Options					
Bank Selection					
Summary					
Memory Model					
PCB Information					
Design Notes					
Version Info User Guide View Dat	a Sheet <u><u>R</u>ack <u>N</u>ext> <u>C</u>ancel</u>				

Select Memory Type

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tions for Controller 0 - DDR3 SDRAM		
Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade, and memory controller type. Choose the dock period for the desired frequency. Refer to User Guide for supported frequency range.	2500 ps 400.00 MHz frequency range shown here is iminary value. Final range will be ermined after characterization.	
Memory Type: Select the memory type. Parts marked with a warning symbol are not compatible with the frequency selection above. Based on the FPGA package, DIMMs selection is not allowed due to the unavailability of required number of pins. For RLDRAM II only CIO parts are supported.	SODIMMs	
Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. If the exact part that you will be using is not available here, you may be able to find an equivalent part. Alternately, you can create a part using the "Create Custom Part" selection at the bottom of this drop box. Refer to User Guide for complete list of memory devices supported.	MT4JSF6464HY-1G1	
Data Width: MIG supports multiples of 64 for components up to 64 bits. Note that the selection is dependent upon the previously selected parameters.	64	
ECC: MIG supports ECC for 72 bit and 144 bit data width configurations. To be able to select ECC, you will need to select a data width that has ECC supported.	Disabled	
Data Mask: You will be able to enable/disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part you have selected has DM pins. Uncheck this box if you would like to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs will not use Data Mask.		
ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received	Strict	
mory Details: 512MB, x16, row:13, col:10, bank:3, unbuffered, data bits per s	trobe:8, with data mask, single rank	
t	< <u>B</u> ack <u>N</u> ext> <u>C</u> ar	ncel

Select

- Type: SODIMMs
- Part: MT4JSF6464HY-1G1

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- Ordering: Strict

Memory Options for Controller 0 - DDR3 SDRAM		
Choose the Memory Options for the memory device. Memory Option selections are restricted to t controller. Consult the memory vendor data sheet for more information.	hose supported by the	
Burst Length Determines the maximum number of column locations that can be accessed for a given READ or WRITE command.	8 - Fixed	•
Read Burst Type		
The ordering of accesses with in a burst is determined the burst type.	Sequential	•
Write Recovery		
Delays the internal auto precharge operation by WR clocks from the last data burst.	5	•
Output Driver Impedance Control		
Programmable impedance for the output buffer.	RZQ/7	•
RTT (nominal) - On Die Termination (ODT) Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the DIMM. This value will be used for the unwritten slot during a write in 2 slot configurations. The value will also be used for the unselected slot during a read in 2 slot configurations. Use board level simulation to choose the optimum value. The default is the value listed at the JEDEC 2007 DDR3 Workshop (<u>http://www.jedecddr3.org/Todd Farreell ODT And Dynamic ODT.pdf</u>).	RZQ/4	T
Sheet < <u>B</u> ack	<u>N</u> ext> <u>C</u>	ancel

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💐 Xilinx Memory Interface Generator REFERENCE System Clock DESIGN 🔠 Choose the desired input clock configuration. Both Design clock and Idelay Control clock will be affected. Either both the clocks can be Differential or both can be Single-Ended. System Clock Differential Ŧ **Pin Compatible FPGAs** -Debug Signals Control Memory Selection This allows the debug signals to be monitored on the ChipScope tool. Selecting this Controller Options option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based on the selected design data width. If the design data width is greater than 72 bit and/or the number of Memory Options DQS/DQS# pins of the design is greater than 18, then the debug signals width is calibrated only for first 72 bits of data. Debug Signals for Memory Controller ON Ŧ Extended FPGA Options IODELAY Power Versus Performance Bank Selection Choose High Performance Mode for lowest IODELAY jitter and maximum interface Summary performance. Choose Normal Performance Mode to reduce power by approximately "(TBD)" per pin when interface performance requirements are less stringent. Memory Model Performance Mode HIGH • PCB Information -Internal Vref Design Notes Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This can free 2 pins per bank where inputs are used. In some topologies these 2 additional free pins will improve bank utilization. This setting has no effect on banks with only outputs. Internal Vref Version Info User Guide View Data Sheet < Back Next> Cancel

Select

– Debug: ON

💐 Xilinx Memory Interface Generator	
Xilinx Memory Interface Generator REFERENCE DESIGN [] Pin Compatible FPGAs Memory Selection ✓ Controller Options ✓ Memory Options ✓ FPGA Options ✓ Extended FPGA Options Summary Memory Model PCB Information Design Notes	DDR3 SDRAM Digitally Controlled Impedance (DCI) The DCI (Digitally Controlled Impedance) I/O Standard is applied only for certain applied on any signals. In Data group bank, only DQ and DQS/DQS# signals have DCI Standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). If VRN/NPP pins in any of Address/Control group or Data group banks are utilized, then DCI Cascading have to be applied. In such scenario, you have to select a Master Bank from the drop down box in the bank selection page. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.
	New Design: Pick the optimum banks for a new design Eixed Bin Out: Bre existing his out is known and fixed
	Tixed Pill Out Pre-existing pill out is known and fixed
Version Info User Guide View Data	Sheet < <u>B</u> ack <u>N</u> ext> <u>C</u> ancel

Select New Design

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Bank Selections Description	1		
Bank Selection For Controller	0 - DDR3 SDRAM		
Address/Control: 25/25 📀	Data: 96/96 🧿 System C	llock: 9/9 ⊘	
Master Bank	Master Bank	Master Bank	
Left Column	Inner Left Column	Inner Right Column	
Bank: 16 Available IOs: 40 Data	Bank:26 Available IOs: 2 Address/Control ✓ Data System Clock	MMCM MMCM MMCM MMCM MMCM MMCM MMCM MMC	<u> </u>
Bank: 15 Available IOs: 40 Data	Bank:25 Available IOs: 14 Address/Control Data System Clock	MMCM MMCM	
Bank: 14 Available IOs: 40 Data	Bank: 24 Available IOs: 2 Address/Control Data	Available IOs: 40 Address/Control Data MMCM	.
Press "Next" to proceed.		Deselect Banks Restore	Defaults
Sheet		< <u>B</u> ack <u>N</u> ext>	<u>C</u> ancel

- On this screen select the banks as used on the ML605 SODIMM interface
- Click Deselect Banks



Bank Selections Description	1		
Bank Selection For Controlle	er 0 - DDR3 SDRAM		
Address/Control: 0/25 📀	Data: 0/96 📀 System Clo	ck: 0/9 🔇	
Master Bank	Master Bank 📃	Master Bank	
Left Column	Inner Left Column	Inner Right Column	
Bank: 16 Available IOs: 40 Data	Bank:26 Available IOs: 40 Address/Control Data System Clock	MMCM MMCM MMCM MMCM MMCM MMCM MMCM MMC	
Bank: 15 Available IOs: 40 Data	Bank:25 Available IOs: 40 Address/Control Data System Clock	MMCM MMCM MMCM Bank: 35 Available IOs: 40 Data Data System Clock	
Bank: 14 Available IOs: 40	Bank:24 Available IOs: 40 Address/Control Data	Bank:34 Available IOs: 40 Address/Control Data MMCM	T
Step 1 of 4: Only center column banks are a selection. Select the "Restore I	allowed for Address/Control group Defaults" for recommended bank	Deselect Banks Restore D	Defaults
heet		< Back Next>	<u>ancel</u>

• All Banks Deselected



			<u>_ ×</u>
Bank Selections Description	1		
Bank Selection For Controller	0 - DDR3 SDRAM		
Address (Sector) as fas			
Address/Control: 25/25	pata: 0/96 🧿 System Cl	ock: 0/9 🧕	
Master Bank	Master Bank 📃 💌	Master Bank	
Left Column	Inner Left Column	Inner Right Column	
Available IOs: 40	Bank: 26 Available IOs: 40 Address/Control Data System Clock	MMCM MMCM MMCM MMCM MMCM Bank: 36 Available IOs: 14 Address/Control Data System Clock	-
Bank: 15 Available IOs: 40 Data	Bank: 25 Available IOs: 40 Address/Control Data System Clock	MMCM MMCM MMCM MMCM MMCM MMCM MMCM MMC	
Bank: 14 Available IOs: 40 Data	Bank:24 Available IOs: 40 Address/Control Data	MMCM Bank: 34 Available IOs: 40 Address/Control Data Suptom Clock	
Step 2 of 4: Banks inside the box are allowed column banks are recommended	for Data group selection. Centr for Data group selection for bes	er Deselect Banks Restore I	Defaults
heet		< Back	<u>C</u> ancel

Select

- Bank 36: Address/Control

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Address/Control: 25/25 📀	Data: 96/96 System Clo	ick: 0/9 📀	
.eft Column	Inner Left Column		
Available IOs: 40	Bank:26 Available IOs: 1 Address/Control Data System Clock	MMCM Bank: 36 Available IOs: 14 Address/Control Data System Clock	
Bank: 15 Available IOs: 40 Data	Bank:25 Available IOs: 2 Address/Control ✓ Data System Clock	MMCM MMCM MMCM MMCM Bank: 35 Available IOs: 14 Address/Control Data System Clock	
Bank: 14 Available IOs: 40	Bank:24 Available IOs: 40 Address/Control Data	Available IOs: 40 Address/Control Data	V
t ep 3 of 4: lect System Clock groups from	the enabled banks. Banks outside	the Deselect Banks Restore	Defaults

Select

- Bank 26: Data
- Bank 25: Data
- Bank 35: Data

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Address/Control: 25/25 📀	Data: 96/96 Ø System Cloc Master Bank	<: 9/9 ⊘ Master Bank 🗾 🔽	
eft Column	Inner Left Column	Inner Right Column	
Data	Address/Control	Address/Control Data	
Bank: 15 Available IOs: 40 Data	Bank:25 Available IOs: 2 ☐ Address/Control ☑ Data ☑ System Clock	MCM MCM MCM MCM MCM MCM MCM MCM MCM MCM	
Bank: 14 Available IOs: 40	Bank:24 Available IOs: 40 Address/Control Data System Clock	MCM System Clock	Ţ
ep 4 of 4:			

Select

– Bank 34: System Clock



Bank Selections Description	1		
Bank Selection For Controller	0 - DDR3 SDRAM		
Address/Control: 25/25	Data: 06/06 O System (lock: 9/9 Ø	
Madress/Condoi: 23/23	Masta Bark 25 -		
Left Column	Inner Left Column	Inner Right Column	
Bank: 16 Available IOs: 40 Data	Bank: 26 Available IOs: 1 Address/Control Data System Clock	MMCM MMCM MMCM Bata System Clock	
Bank: 15 Available IOs: 40 Data	Bank:25 Available IOs: 2 Address/Control ✓ Data System Clock	MMCM MMCM MMCM Bank: 35 Available IOs: 14 Address/Control Data System Clock	
Bank: 14 Available IOs: 40 Data	Bank: 24 Available IOs: 40 Address/Control Data	MMCM Available IOs: 31 Address/Control Data MMCM Available IOs: 31	-
Notes: Press "Next" to proceed.		Deselect Banks Restore	Defaults
Sheet		< Back Next>	<u>C</u> ancel

Select

- Master Bank: 25

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🂐 Xilinx Memory Interface Generator		
REFERENCE DESIGN 🖽		<u> </u>
	CORE Generator Options:	
	Target Device	: xc6vlx240t-ff1156
	Speed Grade	: -1
Rin Compatible ERCAc	HDL	: verilog
Fill Compatible Froas	Synthesis Tool	: XST
Memory Selection		
	If any of the above options as	re incorrect, please
Controller Options	click on "Cancel", change the	CORE Generator Project
Memory Options	Options, and restart MIG.	
	MIG Output Options:	
FPGA Options	Module Name	: mig v3 4
Extended EPGA Options	No of Controllers	: 1
	Selected Compatible Device	(3) :
Bank Selection 🖌		
Summary	FPGA Options:	
Memory Model	Clock Type	: Differential
richiory rioder	Debug Port	: OFF
PCB Information	Internal Vref	: disabled
Design Notes	Extended FPGA Options:	
g	DCI for DQ, DQS/DQS#, DM	: enabled
	DCI for Address/Control	: enabled
	/******	*****
	/* Controlle:	r 0
	*/	_
	/*********	*******
👗 XILIINX.)	Print
Version Info User Guide View Da	ta Sheet <	Back Next> Cancel

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🖁 Xilinx Memory Interface Generator	
Pin Compatible FPGAs 🖌	Micron Technology, Inc. Simulation Model License Agreement PLEASE READ THIS SIMULATION MODEL LICENSE AGREEMENT ("AGREEMENT") FROM MICRON TECHNOLOGY, INC. ("MTI")
Memory Selection	CAREFULLY BEFORE INSTALLING OR USING THIS SIMULATION MODEL (THE "MODEL"). BY INSTALLING OR USING THE MODEL, YOU ARE ACCEPTING AND AGREEING TO THE TERMS AND CONDITIONS OF THIS AGREEMENT. IF YOU DO NOT AGREE WITH THE TERMS AND CONDITIONS OF THIS AGREEMENT, THEN DO NOT INSTALL OR USE THE MODEL.
FPGA Options Extended FPGA Options Bank Selection Summary	SOFTWARE LICENSE: You acknowledge and agree that it is your sole responsibility to obtain the appropriate license or permission from the owner(s) of the software platform(s) that are necessary for you to operate the Model. MTI is under no obligation whatsoever to offer, provide or secure such license or permission for you.
Memory Model PCB Information Design Notes	<u>MODEL LICENSE</u> : MTI hereby grants to you the right to install, use and modify the Model solely for testing the Model and designing your product(s) in connection with the Model. You shall not use the Model or any modifications for any other purpose, and shall not copy, rent, or lease the Model or the
	modifications to any third party. MTI may make changes to the Model at any time without notice to you. MTI is under no obligation whatsoever to update, maintain, or provide new
	Print Check Accept or Decline to proceed. By clicking Accept,
E XILINX _®	memory model will be outputted in output simulation directory. By dicking Decline, you will need to acquire and configure a memory model appropriately.
Version Info User Guide View Data	Sheet ABack Nevts Cancel

Accept Simulation license, if desired

 Otherwise, Decline license

- 🗆 × 💐 Xilinx Memory Interface Generator Creating Printed Circuit Boards for MIG Designs REFERENCE DESIGN 🔠 The Virtex-6 Memory Interface User Guide, UG406, has information on printed circuit board (PCB) design guidelines. These important rules must be followed to ensure that the design generated by MIG works correctly in hardware. The User Guide can be accessed by clicking the User Guide button in the lower left corner of this tool. \checkmark **Pin Compatible FPGAs** The following rules apply when changing pin assignments after the \checkmark Memory Selection MIG tool has generated a design: Controller Options • The address and control pin assignments can be swapped with each other as needed except clock pins \checkmark Memory Options DQ and DM pin assignments within the same byte can be \checkmark FPGA Options swapped with each other \checkmark Extended FPGA Options The affected bits require a change to the pin assignment LOC constraints in the UCE. Bank Selection Summary Memory Model Design Notes **XILINX** Print View Data Sheet Version Info User Guide < Back Next> Cancel

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Click Generate

 After the MIG core finishes generating, click Close on the Datasheet window

1	Readme mig_v3_4	<u>? ×</u>]
	The design files are located at C:/ml605_mig_design:		
	- mig_v3_4.veo: veo template file containing code that can be used as a model for instantiating a CORE Generator module in a HDL design.		
	- mig_v3_4.xco: CORE Generator input file containing the parameters used to regenerate a core.		
	- mig_v3_4_flist.txt: Text file listing all of the output files produced when a customized core was generated in the CORE Generator.		
	- mig_v3_4_readme.txt: Text file indicating the files generated and how they are used.		
	- mig_v3_4_xmdf.tcl: ISE Project Navigator interface file. ISE uses this file to determine how the files output by CORE Generator for the core can be integrated into your ISE project.		
	- mig_v3_4 directory.		
	In the mig_v3_4 directory, three folders are created: - docs:		
	This folder contains Virtex-6 FPGA Memory Interface Solutions user guide	-	
	<u>C</u> lose <u>H</u> el	P	

• MIG design appears in Project IP

💐 Xilinx CORE Generator - C:\ml605_mig_design\ml605_mig_design.cgp			
File Project View Help			
Project IP 🗗 🕹 🕹			
Instance Name \bigtriangledown Core Name Version Last Modified Status		MIG	3
Image mig_v3_4 MIG 3.4 2010-04-29 at 09:21 Pre-Production	DESIGN	Show	Project
	Core Selected: M	IG	
	This core was ger	nerated for a virtex6 (xc6vlx240t-1ff1156) on 2010-04-29 at 09:21	
	This core is suppo	rted at status Pre-Production by your chosen part.	
	Informati	on	
	Core type:	MIG	
	Version:	3.4	
	Core Summary:	This Memory Interface Generator is a simple menu driven tool to generate advanced memory interfaces. This tool generates HDL and in placement constraints that will help you design your application.	
Search Project IP: Clear_		Spartan-3 family supports DDR & DDR2 SDRAM. Spartan-6 supports	
V Project IP V IP Catalog		LPDDR, DDR, DDR2 & DDR3 SDRAM. Virtex-4 supports DDR & DDR2 SDRAM and QDRII & DDRII SRAM and RLDRAM II. Virtex-5 supports	•
		Part: xc6vlx240t-1ff1156 Design Entry: Ver	ilog 🚺 //

Modifications to Example Design

RDF0011.zip includes

- ChipScope Project File, UCF, and Verilog Files

Modifications to RTL Files for ML605 Example Design

- Changed design to support a single 200 MHz LVDS clock input
- Added Debug display code to drive LEDs
- Added ChipScope ILA and VIO port assignments for ML605 board debug

- Removed IIC Signals sda, scl
- Changed various parameter to match the ML605 board
 - DIVCLK_DIVIDE = 1 (was 2 in MIG 3.4 output)
 - OUTPUT_DRV to "HIGH"
 - nDQS_COLx
 - DQS_LOC_COLx
 - RST_ACT_LOW = 0 (was 1)

Modifications to Example Design

Updates to UCF file specifically required for ML605 board:

- Updated IO Locations to match ML605
- Remove IIC Signals sda, scl
- Merged Default two clocks into one clock for ML605
- Moved sys_reset to CPU_RESET
- Edited DCI_CASCADE to match ML605
- Removed CONFIG_PROHIBIT lines
- Added LOC for GPIO LED signals (2.5V bank voltage)

Added LOCs for RSYNC OSERDES and IODELAY

Modifications to Example Design

• Unzip the rdf0011.zip file to your C:\ml605_mig_design directory

- Available through http://www.xilinx.com/ml605
- This adds modifications to the example design (1)
- A fully pre-built ML605 example design is included in the zip file (2)
 - Use the included bitstream to run MIG with ChipScope
 - Run ise_flow.bat in <design directory>\ml605_prebuilt_example_design\ mig_v3_4\example_design\par to recompile the pre-built example design

🗐 WinZip Pro - rdf0011.zip		
File Actions View Jobs Options He	elp	
🏷 🐼 🐼 🐼 🖉 🥬		
Name	Path	Modified 🔺
example_top.ucf	mig_v3_4\example_design\par\	4/28/2010 10:12 AM
example_top.v	mig_v3_4\example_design\rtl\jp_top\	4/28/2010 9:50 AM
infrastructure.v	mig_v3_4\example_design\rtl\jp_top\	4/26/2010 1:57 PM
🔊 iodelay_ctrl.v	mig_v3_4\example_design\rtl\jp_top\	4/27/2010 3:48 PM
memc_ui_top.v	mig_v3_4\example_design\rtl\jp_top\	4/23/2010 5:20 PM
example_top.prj	mig_v3_4\example_design\synth\	4/29/2010 9:24 AM
synplify_pro.tcl	mig_v3_4\example_design\synth\	4/29/2010 9:24 AM
mig_v3_4.gise	ml605_prebuilt_example_design\	4/29/2010 9:32 AM
🔊 mig_v3_4.veo	ml605_prebuilt_example_design\	4/29/2010 9:32 AM
mig_v3_4.xco	ml605_prebuilt_example_design\	4/29/2010 9:32 AM
Mig_v3_4.xise	ml605_prebuilt_example_design\	4/29/2010 9:32 AM
Selected 0 files, 0 bytes	Total 123 files, 58,071KB	🖯 🔿 //

Note: Overwrites Core Generator output files with ML605 specific files (1)

Compile Example Design

 Start a windows command shell and enter these commands: cd ml605_mig_design\mig_v3_4\example_design\par

ise_flow.bat





- Power on the ML605 board
- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC



- After the design compiles, open ChipScope Pro Analyzer
 - Click on the Open Cable Button (1)
 - Click OK (2)

👰 ChipScope Pro Analyzer [new projec	t]	
<u>File View JTAG Chain Device Win</u>	idow <u>H</u> elp	
₩← 1		
New Project		
JTAG Chain		
		Г
C	hipScope Pro Analyzer	
	ITAG Chain Device Order	
	Index Name Device Name IR Length Device IDCODE USERCODE	
	0 MyDevice0 System_ACE_CF 8 0a001093	
A T.	1 MyDevice1 XC6VLX240T 10 44250093	
		0%
	2 → OK Cancel Read USERCODEs	

EXILINX.

- Select Device → DEV:0 MyDevice0 (XC6VLX240T) → Configure...
- Select <Design
 Path>\mig_v3_4\example_design\par\example_top.bit

	- Foreman in the		ChipScope Pro Analyzer [new project]	
ChipScope Pro Analyze	r [new project]		JTAG Configuration	
File View JIAG Chain	Device Window Help		File: example ton hit	
	DEV:0 MyDevice0 (System_ACE_CF))	•	File. example_top.bit	
New Project	DEV: <u>1</u> MyDevice1 (XC6VLX240T)	<u>R</u> ename	Directory: C:\ml605_mig_design\ready_for_download	
JTAG Chain	105.05	Configure	Partial Reconfiguration Bitstream	
DEV:0 MyDevice0 (Syst DEV:1 MyDevice1 (XC6 System Monitor Con	em_ACE_CF) VLX240T) nsole	Show IDCODE Show USERCODE	Clean previous project setting	
		Show Configuration	Select New File	
	Ch	ND.	Import Design-level CDC File NOTE: This operation cannot be undone.	10
			Design-level CDC File	
			Auto-create Buses	
			File:	
₩. 	1		Directory: C:\ml605_mig_design\ready_for_download	
			Select New File	,
Note: Presenta	tion applies to the ML60	5	OK Cancel	E XILINX _®

- Select File → Open Project...
- Select <Design Path>\ready_for_download\ ML605_SODIMM_example_design.cpj

🗟 ChipScope Pro An	alyzer [new project]		
<u>File</u> <u>View</u> <u>J</u> TAG C	hain <u>D</u> evice <u>W</u> indow	<u>H</u> elp	
<u>N</u> ew Project			
<u>O</u> pen Project	4		
Save Project			
Save Project As	(System_ACE_CF)		
Page Setup	(XC6VLX240T)		
Print •	0 (ILA)		-
Import	1 (VIO)		
<u>E</u> xport	2 (VIO) 3 (VIO)		
E <u>x</u> it	4 (VIO)		
			,
A			
Reading file: C:	\ml605_mig_design\read	dy_for_download\example_top.bit	

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Click on Trigger Setup to view trigger settings

The error bit value should be set to 1

ChipScope Pro Analyzer [ML605_SODII	4M_e	xample_design]				_	
<u>File View JTAG Chain Device Trigge</u>	er Seti	up W <u>a</u> veform <u>W</u> indow <u>H</u>	lelp				
😫 🕑 Trigger Run Mode: Single 💌		• T! 🗐 🛇 🛇 •	<u> </u>	辺			
Project: ML605_SODIMM_example_desi		Trigger Setup - DEV:1 MyD	evice1 (XC6VLX	240T) UNIT:0 MyILAO (ILA)		° C	\mathbf{X}
JTAG Chain	×	Match Unit	Function	Value	Radix	Counter	
 DEV.0 MyDevice0 (System_ACE_CF) DEV:1 MyDevice1 (XC6VLX240T) 	latc	P− M0:TRIG0	==	XX1X_XXXX	Bin	disabled	
- System Monitor Console	3	-/TRIG0[7]		Х			
♀– UNIT:0 MyILA0 (ILA)		-/TRIG0[6]		Х	í		
- Trigger Setup		- error		1			
- Listing		/dfi_init_complete		Х	í		
- Bus Plot		/dbg_rdlvl_err[1]		Х			
 UNIT:1 MyVIO1 (VIO) 		/dbg_rdlvl_err[0]		Х			
 UNIT:2 MyVIO2 (VIO) UNIT:2 MyVIO2 (VIO) 		/dbg_rdlvl_done[1]		Х			
 UNIT:4 MyVIO3 (VIO) UNIT:4 MyVIO4 (VIO) 		/dbg rdlvl done[0]		Х			-
• 0111.4 MyVI04 (VIO)	► Capt	Type: Window	Windows:	1 Depth: 1024 💌 Positi	ion:	512	
	ure	Storage Qualification:		All Data			
	▶ 1	Trigger Conditions					
						IDLE	
A 7.	:						
Reading project file: C:\ml605_mig_c	lesiar	vready for download/MI 605	5 SODIMM exam	nple design.cpi			

- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger

👷 ChipScope Pro Analyzer [ML605_50DIMM_example_design]	그×
<u>File View JTAG Chain Device Trigger Setup Waveform Window H</u> elp	
韓 🕑 Trigger Run Mode: Single 🔽 🕨 ◆ T! 1 😵 🗞 🌾 🖗 👂 🖉	
Project: ML605_SODIMM_example_desi JTAG Chain → DEV:0 MyDevice0 (System_ACE_CF) → DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA) → System Monitor Console → UNIT:0 MyILA0 (ILA) → Trigger Setup → Waveform → Listing → Bus Plot ↔ UNIT:1 MyVI01 (VIO) ↔ UNIT:3 MyVI03 (VIO) ↔ UNIT:4 MyVI04 (VIO)	

The Example Design should run error free (no trigger on error)

To force a trigger, click the T! button (1)

(and	chi-c	Des Annie Tre		CODT		destand					11.5
堕	ChipSco	ope Pro Analyzer [M	11605	SODIP	IM_example_	_design]					11 5
<u>F</u> il	le <u>V</u> iev	v <u>J</u> TAG Chain <u>D</u> e	evice	<u>T</u> rigge	r Setup W <u>a</u> v	eform <u>W</u> indow <u>H</u> elp					
	• P	Trigger Run Mode: S	ingle	•] 	י ¢ <mark>1 אר א</mark> ו	9 9 9 19				
	🕲 Wa	veform - DEV:1 MyD)evice1	(XC6	VLX240T) UNI	T:0 MyILA0 (ILA)				ਾ ਹੱ	X
		Bus/Signal	х	0	84 	385 	386 	387 	388 	389 	
	/df	i_init_complete	1	1							^
	∽ /db	g_rdlvl_done	3	3				3			
	∽ /db	g_rdlvl_err	0	0				0			
	err	or	0	0							
	- app	_rd_data_valid	0	0							
	∽ /db	g_rddata_rise0	00921	00921	00092B9C0)	0092B9E00092B9E0	0092BA000092BA00)	0092BA2	00092BA20	X 0092B82000	
	∽ /db	g_rddata_fall0	00921	00921	<u>0009289C0</u>)	0092B9E00092B9E0	0092BA000092BA00 X	0092BA2	00092BA20	X 0012082000	
	∽ /db	g_rddata_rise1	00921	00921	<u>0009289C0</u> X	0092B9E00092B9E0	0092BA000092BA00 X	0092BA2	00092BA20	X 0000002100	
	∽ /db	g_rddata_fall1	00921	00921	<u>0009289C0</u>)	0092B9E00092B9E0	0092BA000092BA00 X	0092BA2	00092BA20	X 0000002100	-
	•	Þ	• •	• •	•		III			•	
	Wave	form captured Apr 29	9, 2010	11:46	:46 AM		X:	0 4 🕨 0:	0 ◀ ► Δ (X-O): 0	
<u>, , ,</u>										DONE	

Select VIO Console 4

Set tg_mod_en_sel to 1

🙀 ChipScope Pro Analyzer [ML605_SODI	MM_example_design]	
<u>File View JTAG Chain Device VIO</u>	<u>W</u> indow <u>H</u> elp	
😫 🕑 JTAG Scan Rate: 250 ms 🔻] S! U! ຽ 🗶	
Project: ML605_SODIMM_example_desi	VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)
DEV:0 MyDevice0 (System_ACE_CF)	Bus/Signal	Value
- System Monitor Console	- dbg_pd_maintain_0_only	0
 P─ UNIT:0 MylLA0 (ILA) ─ Trigger Setup ─ Waveform ─ Listing ─ Bus Plot 	- dbg_ocb_mon_off	0
	← dbg_inc_dec_sel	0
	- dbg_inc_cpt	л.
 UNIT:1 MyVIO1 (VIO) VIO Console 	- dbg_dec_cpt	<u> </u>
- UNIT:2 MyVIO2 (VIO)	- dbg_inc_rd_dqs	<u> </u>
 VIO Console UNIT:3 MyVIO3 (VIO) 	-dbg_dec_rd_dqs	<u> </u>
VIO Console - UNIT:4 MyVIO4 (VIO) - VIO Console	tg_clr_error	<u> </u>
	tg_mod_en_sel	1
	• tg_addr_mode	3
▲ ▼	tg_data_mode	2
<u> </u>		

DONI

Set tg_data_mode to "3" for HAMMER_DATA_MODE

🕵 ChipScope Pro Analyzer [ML605_SODIM	1M_example_design]	
<u>File View JTAG Chain Device VIO V</u>	<u>V</u> indow <u>H</u> elp	
JTAG Scan Rate: 250 ms 👻	S! U! 🖸 🕸	
Project: ML605_SODIMM_example_desi	VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)
DEV:0 MyDevice0 (System_ACE_CF)	Bus/Signal	Value
System Monitor Console	-dbg_pd_maintain_0_only	0
 UNIT:0 MylLA0 (ILA) Trigger Setup Waveform Listing Bus Plot UNIT:1 MyVIO1 (VIO) 	dbg_ocb_mon_off	0
	← dbg_inc_dec_sel	0
	- dbg_inc_cpt	<u></u>
	dbg_dec_cpt	
- UNIT:2 MyVIO2 (VIO)	dbg_inc_rd_dqs	<u> </u>
- VIO Console - UNIT:3 MyVIO3 (VIO)	dbg_dec_rd_dqs	<u> </u>
	- tg_clr_error	<u> </u>
	tg_mod_en_sel	1
	• tg_addr_mode	3
	← tg_data_mode	3 🗸
▲ ▼		DONE

Select VIO Console 1

Note error is active

ChipScope Pro Analyzer [ML605_SODIN	IM_example_design]	
<u>File View JTAG Chain Device VIO V</u>	<u>V</u> indow <u>H</u> elp	
😫 🕑 JTAG Scan Rate: 250 ms 💌	S! U! 🔊 🗶	
Project: ML605_SODIMM_example_desi	VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO) 🗗 🗹 🗵
DEV:0 MyDevice0 (System_ACE_CF)	Bus/Signal	Value
System Monitor Console	dbg_rdlvl_done[0]	A 10 10 10 10 10 10 10 10 10 10 10 10 10
UNIT:0 MyILA0 (ILA) Triager Setup	dbg_rdlvl_done[1]	•
- Waveform	-dfi_init_complete	
- Listing Bus Plot	-rst_pll_ck_fb	e
← UNIT:1 MyVIO1 (VIO)	error	•
— <u>VIO Console</u> • UNIT:2 MvVIO2 (VIO)	∽ compare_count	0
- VIO Console	⊶ dbg_wl_dqs_inverted	FF
UNIT:3 MyVIO3 (VIO) UO Console	← dbg_wl_odelay_dqs_tap_cnt_0	0D
P− UNIT:4 MyVIO4 (VIO) VIO Connocio	∽ dbg_wl_odelay_dq_tap_cnt_0	05
- vio console	← dbg_wl_odelay_dqs_tap_cnt_1	0E
	← dbg_wl_odelay_dq_tap_cnt_1	06
▲ ▼		· · · · · · · · · · · · · · · · · · ·

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DONE



 Press and release the CPU RESET switch, SW10, after each change to tg_mod_en_sel or tg_data_mode



Error is now cleared

🕵 ChipScope Pro Analyzer [ML605_SODIM	M_example_design]	
<u>File View JTAG Chain Device VIO W</u>	/indow <u>H</u> elp	
P JTAG Scan Rate: 250 ms	S! U! 🔊 🛣	
Project: ML605_SODIMM_example_desi	VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (vio)
JTAG Chain - DEV:0 MyDevice0 (System_ACE_CF)	Bus/Signal	Value
System Monitor Console	dbg_rdlvl_done[0]	•
UNIT:0 MyILA0 (ILA) Trigger Setup	- dbg_rdlvl_done[1]	•
- Trigger Setup - Waveform - Listing	-dfi_init_complete	
	-rst_pll_ck_fb	a
← UNIT:1 MyVIO1 (VIO)	- error	•
− <u>VIO Console</u> • UNIT:2 MyVIO2 (VIO)	• compare_count	0
- VIO Console	• dbg_wl_dqs_inverted	FF
UNIT:3 MyVIO3 (VIO) VIO Console	• dbg_wl_odelay_dqs_tap_cnt_0	0D
P- UNIT:4 MyVIO4 (VIO)	• dbg_wl_odelay_dq_tap_cnt_0	05
- VIO Console	• dbg_wl_odelay_dqs_tap_cnt_1	0E
	<pre>% dbg_wl_odelay_dq_tap_cnt_1</pre>	06

- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)

ChipScope Pro Analyzer [ML605_SODIMM_example_design]	
<u>File View JTAG Chain Device Trigger Setup Waveform Window H</u> elp	
🛱 🕑 Trigger Run Mode: Single 🔽 🕨 🔳 T! 🔄 😪 😚 🍄 🍄 🎾 🖉	
Waveform - DEV:1 MyDevice1 (XC6VLX 40T) UN T:0 MyILA0 (ILA)	бØ

Hammer PRBS Data Mode

- 64 bit DQ data bus hammer pattern

9	ChipScope Pro Analyzer [M	L605_	SODIM	IM_example_des	sign]					×
<u>F</u> i	le <u>V</u> iew <u>J</u> TAG Chain <u>D</u> e	vice	<u>T</u> rigge	r Setup W <u>a</u> vefor	rm <u>W</u> indow <u>H</u> elp					
	🛛 🕑 Trigger Run Mode: S	ingle	-	> = T!	3 8 8 9	♀ ♪ <i>▶</i> ₽ ₽				
	🞯 Waveform - DEV:1 MyD	evice1	1 (XC6	VLX240T) UNIT:0	MyILAO (ILA)				. 여다 🗵	3
	Bus/Signal	х	0	380 	381 	382 	383 	384 	3	
	/dfi_init_complete	1	1						-	-
	∽ /dbg_rdlvl_done	3	3				3			
	► /dbg_rdlvl_err	0	0				0			
	- error	0	0							
	-app_rd_data_valid	0	0					1		
	∽/dbg_rddata_rise0	0000	0000)	FFFFF	FFFFFFFFFF	X 001800011F080800	<u> , 00000000000000000)</u>	0000000	
	🗠 /dbg_rddata_fall0	0000	0000)	χ				0000000	
	∽/dbg_rddata_rise1	0000	0000	003F19000000)	FFFFF	FFFFFFFFF	X 000000000000000000000000000000000000	X 00000001	00000000	
	🗠 /dbg_rddata_fall1	0000	0000	003859000000)		000000000000000000000000000000000000000		<u> 000000010000000</u>	\square_{-}	_
				•						2
	Waveform captured Apr 29	9, 2010) 11:50	:54 AM		X:	0 4 🕨 0:	0 ◀ ► Δ(X-O):	0	
<u>, ,</u>	₩								DONE	

- Set tg_data_mode to "7" for PRBS data pattern
- Push CPU Reset, click Arm Trigger button, click T! button



PRBS Data Mode

Ð	ChipScope Pro Analyzer [M	1L605_	SODI	MM_example_design	1				2	×
<u>F</u> i	le <u>V</u> iew <u>J</u> TAG Chain <u>D</u> e	evice	<u>T</u> rigge	er Setup Waveform	Window Help					
2	Trigger Run Mode: S	ingle	-	🕨 🔳 T! 📃	<u>2</u> <u>8</u> <u>9</u> <u>9</u> <u>9</u>	*				
∢ ĕ	🞯 Waveform - DEV:1 MyD	Device1	I (XC6	VLX240T) UNIT:0 My	ILAO (ILA)				• 다 🗵	1
	Bus/Signal	х	0	376	377	378	379 	380 		
	/dfi_init_complete	1	1						^	
	∽ /dbg_rdlvl_done	3	3				3			
	← /dbg_rdlvl_err	0	0				0			
	- error	0	0							
	-app_rd_data_valid	0	0							
	⊶ /dbg_rddata_rise0	0000	0000	00000300000000)	000000080000000	X 58F25ACA58F25ACAX	B1E4B59	4B1E4B594	<u> </u>	
	🗠 /dbg_rddata_fall0	0000	0000		0000000800000000	X 58F25ACA58F25ACAX	B1E4B59	4B1E4B594	<u> </u>	
	⊶ /dbg_rddata_rise1	0000	0000	00000300000000)	0000000800000000	X 58F25ACA58F25ACAX	B1E4B59	4B1E4B594	0000	
	⊶ /dbg_rddata_fall1	0000	0000	00000300000000)	0000000808000000	X 58F25ACA58F25ACAX	B1E4B59	4B1E4B594		
	•	• •	• •	•					•	
	Waveform captured Apr 29	9, 2010	11:51	1:57 AM		X: 0	• • 0: 0 •	► Δ(X-0):	0	
~	.								DONE	

- Useful for PHY layer logic debug and status
- Available if "debug" option is checked in MIG GUI
 - Monitor PHY outputs
 - Status of write calibration
 - Status of read calibration
 - Phase detector control
 - Read data capture clock adjustment
 - Disable selected PHY features

Reference documentation in UG406

- "PHY Layer Debug Port" section
- Table 1-25 for signal definitions and descriptions
- VIO port assignments (4 cores) defined in "example_top.v"

DONE

ChipScope Pro Analyzer [ML605_SODIMM_exam	ple_design]					
ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice V <u>I</u> O <u>W</u> indow <u>H</u> elp						
🖹 🕐 JTAG Scan Rate: 250 ms 🛛 🔽 S! U! 🛇 🛣						
WIO Console - DEV:1 MyDevice1 (XC6VLX240	T) UNIT:1 MyVIO1 (VIO) 🛛 🗗	\boxtimes				
Bus/Signal	Value					
dbg_rdlvl_done[0]	٩					
- dbg_rdlvl_done[1]	•					
-dfi_init_complete	•					
-rst_pll_ck_fb	9					
- error		=				
• compare_count	0					
• dbg_wl_dqs_inverted	FF					
⊶ dbg_wl_odelay_dqs_tap_cnt_0	0D					
⊶ dbg_wl_odelay_dq_tap_cnt_0	05	H				
⊶ dbg_wl_odelay_dqs_tap_cnt_1	0E					
<pre>o- dbg_wl_odelay_dq_tap_cnt_1</pre>	06					
⊶ dbg_wl_odelay_dqs_tap_cnt_2	0D					
✿ dbg_wl_odelay_dq_tap_cnt_2	05					
chop_wl_odelay_dqs_tap_cnt_3	0E					
o- dbg_wl_odelay_dq_tap_cnt_3	06					
⊶ dbg_wl_odelay_dqs_tap_cnt_4	0F	-				

VIO Console 1

- Write Path Calibration Status
- Read Leveling Done, Read Leveling Error
- Initialization complete, PLL reset
- Note: Press CPU RESET to clear error status in this VIO console



DONE

ChipScope Pro Analyzer [ML605_SODIMM_example_design]					
VIO Console - DEV:1 MyDevice1 (XC6VLX240	T) UNIT:2 MyVIO2 (VIO)	\boxtimes			
Bus/Signal	Value	\square			
⊶ dbg_cpt_tap_cnt_0	12				
← dbg_cpt_tap_cnt_1	11				
⊶ dbg_cpt_tap_cnt_2	14				
⊶ dbg_cpt_tap_cnt_3	07				
• dbg_cpt_tap_cnt_4	07				
⊶ dbg_cpt_tap_cnt_5	15				
⊶ dbg_cpt_tap_cnt_6	08				
⊶ dbg_cpt_tap_cnt_7	07	=			
• dbg_rd_active_dly	0C				
⊶ dbg_rd_bitslip_cnt_0	3				
• dbg_rd_bitslip_cnt_1	3				
⊶ dbg_rd_bitslip_cnt_2	3				
• dbg_rd_bitslip_cnt_3	2				
⊶ dbg_rd_bitslip_cnt_4	2				
• dbg_rd_bitslip_cnt_5	3				
- dbg_rd_bitslip_cnt_6	2	-			

- VIO Console 2 & VIO Console 3
 - Read Path Calibration Status



DONE

Ņ	ChipScope Pro Analyzer [ML605_SODIMM_exam	ple_design]					
	ile View JTAG Chain Device VIO Window Help						
1	🛱 🕑 JTAG Scan Rate: 250 ms 🔽 S! U! 🖸 🛣						
	VIO Console - DEV:1 MyDevice1 (XC6VLX240	T) UNIT:3 MyVIO3 (VIO) 🛛 🗖	X				
	Bus/Signal	Value					
	<pre> dbg_cpt_first_edge_cnt_0</pre>	0C					
	<pre>o- dbg_cpt_second_edge_cnt_0</pre>	17					
	<pre> dbg_cpt_first_edge_cnt_1 </pre>	0B					
	• dbg_cpt_second_edge_cnt_1	17					
	dbg_cpt_first_edge_cnt_2	0E					
	← dbg_cpt_second_edge_cnt_2	19					
	dbg_cpt_first_edge_cnt_3	01					
	<pre>o- dbg_cpt_second_edge_cnt_3</pre>	0C					
	← dbg_cpt_first_edge_cnt_4	01					
	<pre>o- dbg_cpt_second_edge_cnt_4</pre>	0D					
	dbg_cpt_first_edge_cnt_5	0F	H				
	dbg_cpt_second_edge_cnt_5	1A					
	dbg_cpt_first_edge_cnt_6	02					
	<pre>chdpg_cpt_second_edge_cnt_6</pre>	0D					
	dbg_cpt_first_edge_cnt_7	01					
	• dbg_cpt_second_edge_cnt_7	0C	•				

- VIO Console 2 & VIO Console 3
 - Read Path Calibration Status

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ChipScope Pro Analyzer [ML605_SODIMM_example_design] Image: ChipScope Pro Analyzer [ML605_SODIMM_example_design] Ie View JTAG Chain Device VIO Window Help						
🗄 🕑 JTAG Scan Rate: 250 ms 💌 S! U! 🖸 🛣						
VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO) 🛛 🗗 🖾					
Bus/Signal	Value					
dbg_pd_off	0					
-dbg_pd_maintain_off	0					
- dbg_pd_maintain_0_only	0					
-dbg_ocb_mon_off	0					
• dbg_inc_dec_sel	0					
-dbg_inc_cpt	л					
-dbg_dec_cpt	л					
-dbg_inc_rd_dgs	л					
-dbg_dec_rd_dgs	л					
-tg_clr_error	л					
-tg_mod_en_sel	1					
• tg_addr_mode	3					
• tg_data_mode	7					

VIO Console 4

- Phase Detector Controls
- Read Data Capture Clock Adjustment



Generate MIG ACE File (Optional)

Type these commands in a windows command shell:

cd C:\ml605_mig_design\ready_for_download make_ace.bat









References

- Virtex-6 Memory
 - Virtex-6 FPGA Memory Interface Solutions User Guide UG406

http://www.xilinx.com/support/documentation/ip_documentation/ug406.pdf

– Virtex-6 FPGA Memory Interface Solutions – DS186

http://www.xilinx.com/support/documentation/ip_documentation/ds186.pdf







Documentation

Virtex-6

- Virtex-6 FPGA Family

http://www.xilinx.com/products/virtex6/index.htm

ML605 Documentation

- Virtex-6 FPGA ML605 Evaluation Kit

http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards and kits/ug535.pdf

