

XTP046

ML605 GTX IBERT Design Creation

May 2010



ML605 IBERT Overview

- Xilinx ML605 Board
- Software Requirements
- Setup for the ML605 IBERT Designs
 - Running the ML605 IBERT Design Bank 113
 - Running the ML605 IBERT Design Bank 114
 - Running the ML605 IBERT Design Bank 115
 - Running the ML605 IBERT Design Bank 116

ML605 IBERT Design Creation

- Create IBERT CORE Generator Project
- Create IBERT Design Bank 113 (FMC_HPC)
- Create IBERT Design Bank 114 (PCIe)
- Create IBERT Design Bank 115 (PCIe)
- Create IBERT Design Bank 116 (FMC_LPC, SFP, SMA, SGMII)

References

ML605 IBERT Overview

Description

 The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Virtex-6 GTX transceivers. A graphical user interface is provided through the IBERT console window of the ChipScope Pro Analyzer

Reference Design IP

- LogiCORE IBERT Example Designs
 - SFP (1), SGMII (1), SMA (1), PCIe (8), FMC_HPC (4), FMC_LPC (1)
- ChipScope Pro Analyzer
 - ChipScope Pro Software and Cores User Guide (UG029)

Xilinx ML605 Board





ISE Software Requirements

Xilinx ISE 12.1 software





ChipScope Pro Software Requirement

Xilinx ChipScope Pro 12.1 software



Release Version: 12.1 Application Version: M.53d (Build 12100.10.99.1220) Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.



EXILINX



- Unzip the rdf0010.zip file to your C:\ drive
 - Available through http://www.xilinx.com/ml605

🗐 WinZip - rdf0010.zip		_ 🗆 ×
File Actions Options Help		
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Name	Path	Modified 🔺
bert_bank113.asy	ml605_ibert\	11/30/2009 3:54 PM
🖬 ibert_bank113.bit	ml605_ibert\	11/30/2009 3:53 PM
🖬 ibert_bank113.gise	ml605_ibert\	11/30/2009 3:54 PM
ibert_bank113.ise	ml605_ibert\	11/30/2009 3:54 PM
ibert_bank113.ngc	ml605_ibert\	11/30/2009 3:34 PM
ibert_bank113.ucf	ml605_ibert\	11/30/2009 3:26 PM
ibert_bank113.v	ml605_ibert\	11/30/2009 3:27 PM
ibert_bank113.veo	ml605_ibert\	11/30/2009 3:27 PM
ibert_bank113.xco	ml605_ibert\	11/30/2009 3:54 PM
ibert_bank113.xise	ml605_ibert\	11/30/2009 3:54 PM
📄 ibert_bank113_flist.txt	ml605_ibert\	11/30/2009 3:54 PM
Selected 0 files, 0 bytes	Total 67 files, 101,915KB	🖯 🛈 /i.

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- Set S2 to 0101XX (X = Don't care, 1 = on, Position 6 \rightarrow Position 1)
 - This selects JTAG
- Set S1 to 0XXX (Position $4 \rightarrow$ Position 1)
 - This disables JTAG configuration from the Compact Flash



- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC





SMA Cables

- www.flrst.com
- P/N: ASPI-024-ASPI-S402





- Using the SMA cables:
 - Connect J28 to J26
 - Connect J29 to J27



EXILINX.

- Connect Optical Loopback Adapter
 - www.molex.com
 - SFP Loopback Adapter,3.5 db Attenuation
 - Part # 74720-0501
 - Alternatively, use an SFP transceiver with a fiber optic cable

Insert into the SFP Connector on the ML605 board





PCIe Testing Hardware:

Catalyst <u>PXP-100 DVT</u>
 Platform



Catalyst <u>PELOOP-BACK</u>





 On the Catalyst, set the reference clock jumper to open

Insert the PELOOP-BACK into one of the PCIe slots









- Insert the ML605 into the other slot
- Connect the ML605 and Catalyst power
- Power up the ML605 and Catalyst





- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ready_for_download\ibert_bank113_top.bit

🗟 ChipScope Pro Analyze	r [new project]				
<u>File View</u> <u>J</u> TAG Chain	Device Window Help			ChipScope Pro Analyzer [new project]	1
# P	DEV:0 MyDevice0 (System_/	ACE_CF) 🕨		JTAG Configuration	
New Project	DEV: <u>1</u> MyDevice1 (XC6VLX2	40T) 🕨	<u>R</u> ename	File: ibert_bank113_top.bit	
JTAG Chain			Configure	Directory: C:\ml605_ibert\ready_for_download	
DEV:0 MyDevice0 (System_ACE_CF) DEV:1 MyDevice1 (XC6VLX240T) System Meniter Canada			Show IDCODE Show USERCODE	Partial Reconfiguration Bitstream	
			<u>Show Configuration State</u>	Clean previous project setting	
		· · · · · · · · · · · · · · · · · · ·	Show JTAG Instruction R	Select New File	
		C	hip	Import Design-level CDC File NOTE: This operation cannot be undone. Design-level CDC File	Pro
				Auto-create Buses	
▲ ▼				File:	
**				Directory: C:\m1605_ibert\ready_for_download	
				Select New File	
Note: Presenta	tion applies to the	e ML605	5	OK Cancel	E XILINX.

- Select File → Open Project...
- Select <Design Path>\ready_for_download\ml605_bank113.cpj

ChipScope Pro An	alyzer [new project]		_ 🗆 🗵
<u>File View J</u> TAG C	hain <u>D</u> evice <u>W</u> indow <u>H</u> elp		
New Project			
Open Project		٩	
Save Project			
Save Project As	(System_ACE_CF)		
Page Setup	(XC6VLX240T)		
<u>P</u> rint ►	BERT V6 GTX1_0 (IBERT V6 GTX)		
Import	nsole		
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A			
Reading file: C:	:\ml605_ibert\ready_for_download\it	vert_bank113_top.bit	

Click Yes on this Dialog

🗐 Cl	iipScop	e Pro Analyze	er [ml605_bank113]	_ 🗆 🗵
<u>F</u> ile	<u>V</u> iew	JTAG Chain	Device Window Help	
	P			
I I) IBERT	Console - DE	EV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX) pe Pro Analyzer - IBert V6GTX Project Settings Project settings do not match current core! Do you want to set up the IBERT V6GTX core with settings from the current project? Yes No	j d ĝ ⊠
<u> </u>	Readin	ig project file:	C:\ml605_ibert\ready_for_download\ml605_bank113.cpj	



- The line rate is 5.0 Gbps for all four GTXs (1)
- Near-End PCS is selected for all four GTXs (2)

(ChipScope Pro Analyzer [ml6	05_bank113]				<u>_ ×</u>		
<u>F</u> il	ile <u>V</u> iew JTAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp							
	🗄 🕑 📑 💋 👏 JTAG Sca	n Rate: 1 s 💌 S!						
	IBERT Console - DEV:1 My	/Device1 (XC6VLX240T) UNIT:1_0	MyIBERT V6 GTX1_0 (IBERT V6 G	6TX)	e ^k	o' 🛛		
	MGT/BERT Settings DF	RP Settings Port Settings	Sweep Test Settings					
		GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7			
			· · · · · · · · · · · · · · · · · · ·			4		
	- MGT Alias	GTX0_113	GTX1_113	GTX2_113	GTX3_113			
	- Tile Location	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7			
	- MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps			
	- MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps			
	- TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
	- RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
	- Loopback Mode	Near-End PCS 🔹	Near-End PCS 🔍 💌	Near-End PCS 🔍 💌	Near-End PCS	-,		
	Reading project file: C:\ml6	05_ibert\ready_for_download\ml6	05_bank113.cpj					
					1			

Note: Bank 113: FMC HPC

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

(ChipScope Pro Analyzer [ml6	05_bank113]				×			
<u>F</u> il	<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp								
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	BERT Console - DEV:1 My	yDevice1 (XC6VLX240T) UNIT:1_0) MyIBERT V6 GTX1_0 (IBERT V6 (STX)	r ⊡ [Ā			
	MGT/BERT Settings DF	RP Settings Port Settings	Sweep Test Settings						
		GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7				
	- Channel Reset	Reset	Reset	Reset	Reset				
	- TX Polarity Invert								
	- TX Error Inject	Inject	Inject	Inject	Inject				
	- TX Diff Output Swing	445 mV (0100) 🗸 🗸	445 mV (0100) 💌	445 mV (0100) 🗸 🗸	445 mV (0100)				
	- TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)				
	- TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)				
	- RX Polarity Invert								
	- RX AC Coupling En	V	×	×					
	[
	Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank113.cpj								

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

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<u>F</u> il	e <u>V</u> i	ew JTAG Chain Devi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e an Rate: 1 ₅ ▼ S!	lp		
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	MG	GT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings		
			GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
	<u>م</u>	MGT Settings				A
	φ E	BERT Settings			1	
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
		- RX Bit Error Ratio	2.915E-001	2.916E-001	2.932E-001	2.932E-001
		RX Received Bit Co	9.889E011	9.890E011	9.841E011	9.843E011
		- RX Bit Error Count	2.883E011	2.884E011	2.885E011	2.886E011
		BERT Reset	Reset	Reset	Reset	Reset
	Re	ading project file: C:\ml6	605_ibert\ready_for_download\ml6	05_bank113.cpj		

EXILINX.

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

()	Chips	Scope Pro Analyzer [ml6	05_bank113]						
<u>F</u> il	ile <u>V</u> iew JTAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp								
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	1	BERT Console - DEV:1 M	yDevice1 (XC6VLX240T) UNIT:1_() MyIBERT V6 GTX1_0 (IBERT V6 (STX)	r 0 🛛			
	M	GT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings					
			GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7			
	~	MGT Settings				4			
	9	BERT Settings							
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Bit Error Ratio	4.657E-012	4.661E-012	4.665E-012	4.667E-012			
		- RX Received Bit Co	2.147E011	2.145E011	2.144E011	2.143E011			
		- RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000			
		BERT Reset	Reset	Reset	Reset	Reset			
~	Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank113.cpj								



- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ready_for_download\ibert_bank114_top.bit

ChipScope Pro Analyze	r [new project]				
<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain	Device Window Help			ChipScope Pro Analyzer [new project]	1
# P	DEV:0 MyDevice0 (System_/	ACE_CF) 🕨		JTAG Configuration	
New Project	DEV: <u>1</u> MyDevice1 (XC6VLX2	40T) 🕨	<u>R</u> ename	File: ibert_bank114_top.bit	
JTAG Chain			Configure	Directory: C:\ml605_ibert\ready_for_download	
DEV:0 MyDevice0 (System_ACE_CF) DEV:1 MyDevice1 (XC6VLX240T) System Monitor Console		-	Show IDCODE Show USERCODE	Partial Reconfiguration Bitstream	
			Show Configuration State	Clean previous project setting	
			Show JTAG Instruction R	Select New File	
		C	hip	Import Design-level CDC File NOTE: This operation cannot be undone. Design-level CDC File	Pro
				Auto-create Buses	
* *				File:	
A. 7				Directory: C:\m1605_ibert\ready_for_download	
				Select New File	
Note: Presenta	tion applies to the	e ML60	5	OK Cancel	

- Select File → Open Project...
- Select <Design Path>\ready_for_download\ml605_bank114.cpj



Click Yes on this Dialog

ChipScope Pro Analyzer [ml605_bank114]	
<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice <u>W</u> indow <u>H</u> elp	
IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX) ChipScope Pro Analyzer - IBert V6GTX Project Settings ? Project settings do not match current core! Do you want to set up the IBERT V6GTX core with settings from Initia Image: Im	■ I I I I I I I I I I I I I I I I I I I
Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank114.cpj	

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The line rate is 5.0 Gbps for all four GTXs (1)

9	Chip	Scope Pro Analyzer [ml6	605_bank114]				<u> </u>		
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	1	BERT Console - DEV:1 M	yDevice1 (XC6VLX240T) UNIT:1_0	MyIBERT V6 GTX1_0 (IBERT V6 C	6TX)	r 0	\boxtimes		
	M	GT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings					
			GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11			
	9	MGT Settings		-					
		- MGT Alias	GTX0_114	GTX1_114	GTX2_114	GTX3_114			
		 Tile Location 	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11			
		- MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps			
		 MGT Edit Line Rate 	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps			
		- TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
		- RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
		- Loopback Mode	None	None 🗸	None 💌	None			
			· · · · · · · · · · · · · · · · · · ·			· ·			
Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank114.cpj									

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- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

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	IBERT Console - DEV:1 M	lyDevice1 (XC6VLX240T) UNIT:1_() MyIBERT V6 GTX1_0 (IBERT V6 (STX)	r ⊠ 2	3			
	MGT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings						
		GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11				
	- Channel Reset	Reset	Reset	Reset	Reset				
	- TX Polarity Invert								
	- TX Error Inject	Inject	Inject	Inject	Inject				
	- TX Diff Output Swing	445 mV (0100) 💌	445 mV (0100) 🗸 🗸	445 mV (0100) 🗸 🗸	445 mV (0100)				
	- TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)				
	- TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000) 🗸	0.000 dB (00000) 🗸	0.000 dB (00000)				
	- RX Polarity Invert								
	- RX AC Coupling En	2	~	×					
					·				
Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank114.cpj									

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

🖗 ChipScope Pro Analyzer [ml605_bank114]												
File View JTAG Chain Device IBERT_V6GTX Window Help Image: Image												
	📓 IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)											
	MGT/BERT Settings DRP Settings Port Settings Sweep Test Settings											
		GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11							
	← MGT Settings				4							
	P BERT Settings			,								
	- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit							
	- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit							
	- RX Bit Error Ratio	7.046E-003	4.095E-002	1.941E-002	3.979E-002							
	- RX Received Bit Co	5.164E011	5.162E011	5.160E011	5.159E011							
	- RX Bit Error Count	3.639E009	2.114E010	1.001E010	2.053E010							
	BERT Reset	Reset	Reset	Reset	Reset							
		-										
Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank114.cpj												

EXILINX.

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

🗟 ChipScope Pro Analyzer [ml605_bank114]											
<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp											
🟥 😰 📑 🕺 🚫 JTAG Scan Rate: 15 💌 S!											
IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)											
	MGT/BERT Settings DRP Settings Port Settings Sweep Test Settings										
			GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11					
	~	MGT Settings				4					
	9	BERT Settings									
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit					
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit					
		- RX Bit Error Ratio	7.949E-012	8.246E-012	8.566E-012	8.920E-012					
		- RX Received Bit Co	1.258E011	1.213E011	1.167E011	1.121E011					
		- RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000					
		BERT Reset	Reset	Reset	Reset	Reset					
	R	eading project file: C:\ml6									



- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)


- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ready_for_download\ibert_bank115_top.bit

ChipScope Pro Analyze	r [new project]				
<u>File</u> <u>View</u> <u>JTAG</u> Chain	Device Window Help			ChipScope Pro Analyzer [new project]	
# P	DEV:0 MyDevice0 (System_A	CE_CF) ▶		JTAG Configuration	
New Project	DEV: <u>1</u> MyDevice1 (XC6VLX24	0T) 🕨	<u>R</u> ename	File: ibert_bank115_top.bit	
JTAG Chain			<u>C</u> onfigure	Directory: C:\ml605_ibert\ready_for_download	
DEV:0 MyDevice0 (System_ACE_CF) DEV:1 MyDevice1 (XC6VLX240T) System Monitor Console			Show <u>I</u> DCODE Show <u>U</u> SERCODE	Partial Reconfiguration Bitstream	
			Show Configuration State	Clean previous project setting	
			Show JTAG Instruction R	Select New File	
		C	hip	Import Design-level CDC File NOTE: This operation cannot be undone. Design-level CDC File	Pro
				Auto-create Buses	
▲ ▼				File:	
A		<u>.</u>		Directory: C:\ml605_ibert\ready_for_download	
				Select New File	
Note: Presenta	tion applies to the	ML605	5	OK Cancel	

- Select File → Open Project...
- Select <Design Path>\ready_for_download\ml605_bank115.cpj



Click Yes on this Dialog

()	ChipS	cope	Pro Analyz	er [ml6	505_bank115]	_ 🗆 🗙
<u>F</u> il	e <u>V</u> ie	ew 🛓	JTAG Chair	n <u>D</u> evi	ice <u>W</u> indow <u>H</u> elp	
	P					
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	Re	ading	project file	: C:\ml6	605_ibert\ready_for_download\ml605_bank115.cpj	

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The line rate is 5 Gbps for all four GTXs (1)

9	ChipScope Pro Analyzer [ml605_bank115]								
<u>F</u> il	e <u>V</u>	iew <u>J</u> TAG Chain <u>D</u> evi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e	lp					
	🟥 🕑 🛙 🏭 🕺 JTAG Scan Rate: 1s 🔹 🐨 S!								
	📓 IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)								
	M	GT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings					
			GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15			
	9	MGT Settings		-					
		- MGT Alias	GTX0_115	GTX1_115	GTX2_115	GTX3_115			
		 Tile Location 	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15			
		- MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps			
		 MGT Edit Line Rate 	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps			
		- TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
		- RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED			
		- Loopback Mode	None	None	None 💌	None	2.		
	R	eading project file: C:\ml6	05_ibert\ready_for_download\ml6	05_bank115.cpj					

EXILINX.

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

1	ChipScope Pro Analyzer [ml605_bank115]							
<u>F</u> ile	<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp							
	🟥 🕑 🛙 🧱 🕺 🟷 JTAG Scan Rate: 15 🔍 🗸 S!							
🛿 🔯 IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)								
	MGT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings					
		GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15			
	- Channel Reset	Reset	Reset	Reset	Reset			
	- TX Polarity Invert							
	- TX Error Inject	Inject	Inject	Inject	Inject			
	- TX Diff Output Swing	445 mV (0100) 🗸 🗸	445 mV (0100) 💌	445 mV (0100) 🗸 🗸	445 mV (0100) 🗨 🗖			
	- TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)			
	- TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)			
	- RX Polarity Invert							
	- RX AC Coupling En	×	V	V				
	Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank115.cpj							

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

🗐 Chi	ipScope Pro Analyzer [ml6	505_bank115]						
Eile	View JTAG Chain Devi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e an Rate: 1 ₅ ▼ S!	lp					
	IBERT Console - DEV:1 M	yDevice1 (XC6VLX240T) UNIT:1_0) MyIBERT V6 GTX1_0 (IBERT V6 (GTX)	් d 🛛			
	MGT/BERT Settings	RP Settings Port Settings	Sweep Test Settings					
		GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15			
9	MGT Settings				A			
9	BERT Settings			,				
	- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
	- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
	- RX Bit Error Ratio	1.579E-001	1.645E-001	1.077E-001	9.243E-002			
	- RX Received Bit Co	3.777E011	3.775E011	3.773E011	3.772E011			
	- RX Bit Error Count	5.964E010	6.210E010	4.064E010	3.487E010			
	BERT Reset	Reset	Reset	Reset	Reset			
	Reading project file: C:\ml6	605_ibert\ready_for_download\ml6	05_bank115.cpj					

EXILINX.

Note: Presentation applies to the ML605

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

(ChipScope Pro Analyzer [ml605_bank115]								
<u>F</u> ile	e <u>V</u>	iew <u>J</u> TAG Chain <u>D</u> evi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e	lp					
	🖹 🕑 📑 💋 🚫 JTAG Scan Rate: 15 🔍 S!								
	🛿 🞯 IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)								
	MGT/BERT Settings DRP Settings Port Settings Sweep Test Settings								
			GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15			
	o -1	MGT Settings				4			
	9	BERT Settings							
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Bit Error Ratio	3.320E-012	3.384E-012	3.440E-012	3.490E-012			
		- RX Received Bit Co	3.012E011	2.955E011	2.907E011	2.866E011			
		- RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000			
		BERT Reset	Reset	Reset	Reset	Reset			
	Re	eading project file: C:\ml6	05_ibert\ready_for_download\ml6	05_bank115.cpj					



- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ready_for_download\ibert_bank116_top.bit

🗟 ChipScope Pro Analyze	r [new project]				
<u>File View</u> <u>J</u> TAG Chain	Device Window Help			ChipScope Pro Analyzer [new project]	1
# P	DEV:0 MyDevice0 (System_	ACE_CF) 🕨		JTAG Configuration	
New Project	DEV: <u>1</u> MyDevice1 (XC6VLX2	40T) 🕨	<u>R</u> ename	File: ibert_bank116_top.bit	
JTAG Chain			Configure	Directory: C:\ml605_ibert\ready_for_download	
DEV:0 MyDevice0 (Syst DEV:1 MyDevice1 (XC6 System Monitor Cor	em_ACE_CF) VLX240T) Isole		Show IDCODE Show USERCODE	Partial Reconfiguration Bitstream	
			Show Configuration State	Clean previous project setting	
		· · · · · · · · · · · · · · · · · · ·	Show JTAG Instruction R	Select New File	
		C	hip	Import Design-level CDC File NOTE: This operation cannot be undone. Design-level CDC File	Pro
				Auto-create Buses	
				File:	
A T				Directory: C:\m1605 ibert\ready for download	
				Select New File	
Note: Presenta	tion applies to the	e ML605	5	OK Cancel	E XILINX.

- Select File → Open Project...
- Select <Design Path>\ready_for_download\ml605_bank116.cpj



Click Yes on this Dialog

🗐 C	ipScop	e Pro Analyze	er [ml605_bank116]	
<u>F</u> ile	<u>V</u> iew	JTAG Chain	Device Window Help	
#-85 (#-8	P			
	҈∎ IBERT	Console - DE	EV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX) pe Pro Analyzer - IBert V6GTX Project Settings Project settings do not match current core! Do you want to set up the IBERT V6GTX core with settings from the current project? Yes No	or or ⊠
<u> </u>	Readin	ig project file:	C:\ml605_ibert\ready_for_download\ml605_bank116.cpj	



- The line rates are 5.0 and 1.25 Gbps for the four GTXs (1)
- Near-End PCS and PMA is selected for FMC and SGMII (2)

<u>کار اور</u>	ChipScope Pro Analyzer [ml6 e View ITAG Chain Devi	505_bank116] ce_IBERT_V6GTX_Window_He	lo.				
	🕑 🛛 📑 😥 🔊 JTAG Sc	an Rate: 1s VOINT Mindow Me	ар -				
	IBERT Console - DEV:1 M	yDevice1 (XC6VLX240T) UNIT:1_() MyIBERT V6 GTX1_0 (IBERT V6 () (X1	r 0' X		
	MGT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings				
		GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19		
	MGT Settings		· · · · · · · · · · · · · · · · · · ·		f /		
	- MGT Alias	GTX0_116	GTX1_116	GTX2_116	GTX3_116		
	- Tile Location	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19		
	- MGT Link Status	5 Gbps	5 Gbps	5 Gbps	1.25 Gbps		
	- MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	1.25 Gbps		
	- TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED		
	- RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED		
	- Loopback Mode	Near-End PCS 🔍	None	None	Near-End PMA		
		^			ł		
	Reading project file: C:\ml605 ibert\ready for download\ml605 bank116.cpj						
_		2			2		

Note: Bank 116: FMC LPC, SFP, SMA, SGMII

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

1	ChipScope Pro Analyzer [ml605_bank116]								
<u>F</u> il	<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> elp								
	🟥 🕑 🛙 📑 😥 🔊 JTAG Scan Rate: 15 🔹 S!								
	IBERT Console - DEV:1 My	yDevice1 (XC6VLX240T) UNIT:1_0) MyIBERT V6 GTX1_0 (IBERT V6 (STX)	r ⊿	\boxtimes			
	MGT/BERT Settings DI	RP Settings Port Settings	Sweep Test Settings						
		GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19				
	- Channel Reset	Reset	Reset	Reset	Reset	ā			
	- TX Polarity Invert								
	- TX Error Inject	Inject	Inject	Inject	Inject				
	- TX Diff Output Swing	445 mV (0100) 🗸 🗸	445 mV (0100) 🗸 🗸	445 mV (0100) 🗸 🗸	445 mV (0100)				
	- TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)				
	- TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)				
	- RX Polarity Invert								
	- RX AC Coupling En	×	×	×	V				
	Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank116.cpj								

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

1	ChipS	cope Pro Analyzer [ml6	05_bank116]					
<u>F</u> il	e <u>V</u> i	ew JTAG Chain Devi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e an Rate: 1 ₅ ▼ S!	lp				
	<u>ا ال</u>	BERT Console - DEV:1 M	yDevice1 (XC6VLX240T) UNIT:1_0) MyIBERT V6 GTX1_0 (IBERT V6 (STX)	r Q 🛛		
	м	GT/BERT Settings D	RP Settings Port Settings	Sweep Test Settings				
			GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19		
	~ ∎	MGT Settings						
	φ E	BERT Settings			1			
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit		
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit		
		- RX Bit Error Ratio	3.064E-001	5.260E-002	4.611E-002	3.124E-001		
		RX Received Bit Co	9.301E011	9.302E011	9.303E011	2.326E011		
		- RX Bit Error Count	2.850E011	4.893E010	4.289E010	7.268E010		
		BERT Reset	Reset	Reset	Reset	Reset		
	Re	ading project file: C:\ml6	05_ibert\ready_for_download\ml6	05_bank116.cpj				

EXILINX.

Note: Presentation applies to the ML605

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

١	ChipScope Pro Analyzer [ml605_bank116]								
<u>F</u> i	le <u>\</u>	iew JTAG Chain Devi	ce IBERT <u>V</u> 6GTX <u>W</u> indow <u>H</u> e	lp					
8	🚔 🕐 📑 🗭 JTAG Scan Rate: 1s 🔍 S!								
	😰 IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)								
MGT/BERT Settings DRP Settings Port Settings Sweep Test Settings									
			GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19			
	•	MGT Settings				4			
	9	BERT Settings							
		- TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit			
		- RX Bit Error Ratio	1.671E-012	1.678E-012	1.688E-012	6.793E-012			
		- RX Received Bit Co	5.984E011	5.959E011	5.925E011	1.472E011			
		- RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000			
		BERT Reset	Reset	Reset	Reset	Reset			
	Reading project file: C:\ml605_ibert\ready_for_download\ml605_bank116.cpj								

ML605 IBERT Design Creation



Create IBERT CORE Generator Project

Open the CORE Generator

Start \rightarrow All Programs \rightarrow Xilinx ISE Design Suite 12.1 \rightarrow

 $\mathsf{ISE} \to \mathsf{Accessories} \to \mathsf{CORE}$ Generator

■ Create a new project; select File → New Project

(🕴	Cilinx CORE Gen	erator - No	Proje	ect						<u> </u>	
<u>F</u> ile	View Help										
	New Project	Ctrl+N	1					₽×			
9	Open Project	Ctrl+O	ame						IndiCORE	Xilinx CORE Generator	r
	<u>C</u> lose Project	Ctrl+W		Version	Status	License			Legi CA		
	<u>R</u> ecent Projects	•									
	Save	Ctrl+S							There is no	project open.	
_	Save <u>A</u> s,		king						You may browse	the IP Catalog but you will not be able to	
	Preferences		n							res until you open or create a project.	_
	E <u>x</u> it	Ctrl+Q							Copyright (c) 1995-2	2010 Xilinx, Inc. All rights reserved.	
÷.	 Memories at Standard Bus Video & Imag 	s Interfaces ge Processing	g								
Sear	ch IP Catalo <u>g</u> :							Clear			
	I IP versions						Only IP compatible v	ith chosen part			
Nev	v Project									Part: Unset Design Entry: Unset) //

EXILINX.

Create IBERT CORE Generator Project

🖣 Project Options 🔹 🤶					
Part	-Part				
Generation	Select the part for				
	Fa <u>m</u> ily	Virtex6	•]	
	De <u>v</u> ice	xc6vlx240t	•]	
	P <u>a</u> ckage	ff1156	•]	
	Speed Grade	-1	-]	
	<u>O</u> K	<u>C</u> ancel	<u>A</u> pply	Help	

Note: Presentation applies to the ML605

- Create a project directory: ml605_ibert
- Name the project: ml605_ibert.cgp
- The Project options will appear
- Set the Part (as seen here):
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1

Create IBERT CORE Generator Project

🂐 Project Options		<u>? ×</u>
Part	Flow	
- Generation - Advanced	Design Entry	Verilog
	Custom Output Products	
	Please refer to the online help for int models using compxlib and using .VE	formation about compiling behavioral O (Verilog) templates.
	Flow Settings	
	<u>V</u> endor	Other 💌
	Netlist <u>B</u> us Format	B <n:m> ▼</n:m>
	Simulation Files	
	Preferred Simulation Model	Preferred Language
	Behavioral	C VHDL
	C Structural	Verilog
	C None	
	Other Output Products	
	ASY Symbol File	
	<u>O</u> K <u>C</u> ancel	<u>A</u> pply <u>H</u> elp

Note: Presentation applies to the ML605

Select Generation

EXILINX.

- Set the Design Entry to Verilog
- Click OK

IBERT Design Creation Bank 113



- Right click on the IBERT Virtex6 GTX (ChipScope Pro IBERT, Version 2.02a
 - Select Customize and Generate

File Project View Help IP Catalog IP Catalog View by Function View by Name Name Version Status License IBERT Virtex6 Show Project Openation	Xilinx CORE Generator - C:\ml605_ibert\ml605_ibert.cgp								
IP Catalog Image: Name Image: Name								t View Help	File Project Viev
View by Function View by Name Illerst			₽×						IP Catalog
Name A Version Status License GTX (ChipScope Show Project		IBERT Virtex6 🤇						nction View by Name	View by Function
ChipScope Pro ChipScope Pro ChipScope Pro - Agilent Trace Core 2) I.03.a Production IBERT Spartan6 GTP (ChipScope Pro - IBERT) IBERT Virtex5 GTX (ChipScope Pro - IBERT) IBERT Virtex6 GTH (ChipScope Pro - IBERT)		CTV (ChinScone)		License	Status	Version	Δ		Name
IBERT Spartan6 GTP (ChipScope Pro - IBERT) 2.01.a Production IBERT Virtex5 GTX (ChipScope Pro - IBERT) 2.00.a Production IBERT Virtex6 GTH (ChipScope Pro - IBERT) 2.00.a Production IBERT Virtex6 GTH (ChipScope Pro - IBERT) 2.00.a Production IBERT Virtex6 GTH (ChipScope Pro - IBERT) IBERT Virtex6 GTH (ChipScope Pro - IBERT) Image: Customize and Generate		Pro - IBERT)			Production	1.03.a	Agilent Trace Core 2)	ug & Verification ChipScope Pro 嶺 ATC2 (ChipScope Pro	È 🥟 Debug & V È 🃂 ChipSo
		This core is supported at status Production by your chosen part.		Generate	Production Production	2.01.a 2.00.a	hipScope Pro - IBERT) Scope Pro - IBERT) Scope Pro - IBERT)	 IBERT Spartan6 GTP IBERT Virtex5 GTX (C IBERT Virtex6 GTH (C IBERT Virtex6 GTK (C 	🖞 IB 🌾 IB 🌾 IB
ICON (ChipScope Pro - Integrated Controller) ILA (ChipScope Pro - Integrated Logic Analyzer) Image: Wiew Answer Records Image: Core type: IBERT Virtex6 GTX (ChipScope Pro - IBERT) Image: View Data Sheet Image: Digital Signal Processing View Version Information Image: View Version Information Image: View Version Information Image: View Version Information		Core type: IBERT Virtex6 GTX (ChipScope Pro - IBERT) Version: 2.02.a Core Summary: The ChipScope Pro Series Integrated Bit Error Ratio Tester for Virtex6 GTX.		rds mation	Answer Reco Data Sheet Version Inforr	ViewViewViewView	Integrated Controller) tegrated Logic Analyzer) rtual Input/Output)	ICON (ChipScope Pro ILA (ChipScope Pro - VIO (ChipScope Pro - tal Signal Processing	EPGA Feat
Search IP Catalog: Clear Clear Clear Clear Clear	•	Supported Families Current Project Options Part: xc6vlx240t-1ff1156 Design Entry: Verilog	Clear hosen part	atible with ch	Only IP compa			talog:	Search IP Catalog:

- Make the following settings:
 - Component name:
 ibert_bank113
 - Set the number of Line
 Rates: 1
 - Set the line rate to Max
 Rate: **5 Gbps**
- On the ML605, Bank 113 is connected to the 250 MHz OSC
 - Set the RefClk frequency to: 250 MHz
- Click Next

TOLICI VII LEXO	dix (chipscope Fio - ibeki	·)				
<u>V</u> iew						
LogiC ^{&RE}	IBERT (ChipSco	Virtex6 pe Pro -	GTX IBERT) 2.02		
Component Name ibert_bank113						
Line Rate Setti Number of Line	ings Rates (protocols) 1 💌					
Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)		
1	Start from scratch	5	20 💌	250.00 💌		

Help

- The line rate is 5 Gbps
- Select a GTX from Bank 114
 - This enables the clock used for Bank 113
- Select the four GTXs for Bank 113:
 - X0Y7
 - X0Y6
 - X0Y5
 - X0Y4
- Connect the Refclks for all GTXs to:
 - REFCLK0 Q2
 - This connects Bank 113 to the Bank 114 250 MHz Clock
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

<u>V</u>iew

LogiCRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

Select GTXs and Reference Clocks for Line Rate 1

GTX (Location)	TXREFCLK	RXREFCLK
GTX3_116 (X0Y19)	REFCLK1_Q4	REFCLK1 Q4
GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3
GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
GTX3_114 (X0Y11)	REFCLK0_Q2	REFCLK0 Q2
GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
GTX3_113 (X0Y7)	REFCLK0_Q2	REFCLK0 Q2
GTX2_113 (X0Y6)	REFCLK0_Q2	REFCLK0 Q2
GTX1_113 (X0Y5)	REFCLK0_Q2	REFCLK0 Q2
GTX0_113 (X0Y4)	REFCLK0_Q2	REFCLK0 Q2
GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0 🔽
GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0 💌
GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0
	Active GTXs : 5	

Datasheet

< Back | Page 2

Page 2 of 5 Next >

<u>G</u>enerate

Cancel

<u>H</u>elp

- Leave this screen as is
 - Click Next

View

LogiCZRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

Enable RXRECCLK Probes

RXRECCLK PIN OUT							
Enable	GTX	Location*	IO Standard				
	X0Y4 RXRECCLK	\$	LVDS 25				
	X0Y5 RXRECCLK	\$	LVDS 25				
	X0Y6 RXRECCLK	\$	LVDS 25				
	X0Y7 RXRECCLK	\$	LVDS 25				
	X0Y11 RXRECCLK	\$	LVDS 25				

* In case the selected Input standard in Differential, Please enter only P Pin Location.

- Select the following settings:
 - Use External Clock source
 - Location: **J9**
- Click Next

×.	TOPOTA	C-1	CTV IC	L:		TOPOTA
Π.	TREKT A	irtex6	GIX (C	nipScot	e Pro -	IBERT)

<u>V</u>iew

LogiCZRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

- 🗆 🗵

System Clock				
Set the system clock for FPGA's internal debug bus				
Use External Clock source *				
Frequency (MHz) Location * Input Standard	200 J9 LVDS 25			
C Use MGT TXOUTCLK**				

* In case the selected input standard is differential, please enter only "p" pin location. **Select at least one GTX from the clock selection panels to use TXOUTCLK

- Deselect
 - Implement Design
- Click Generate

🂐 IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCZPL

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

IBERT Core Summary

System						
System Clock	uency	IBERT_SY	IBERT_SYSCLOCK / 200 MHz			
BUFGs used /		12 / 1				
Line Rates						
Index Prot	tocol	Line Rate	Data Width	REFCLK	GTXs selected	
1 Star	t from scratch	5	20	250.00	V0v4 V0v5 V0v6	v0v7_v0v11
1 500	scratch	5	20	200.00	x0y4 x0y5 x0y0	x0y7 x0y11

🔲 Implement Design



 After the IBERT core finishes generating, click Close on the Readme File window

Readme ibert_bank113	[
The following files were generated for 'ibert_bank113' in directory C:\ml605_ibert\	
ibert_bank113_flist.txt: Text file listing all of the output files produced when a customized core was g in the CORE Generator.	generated
ibert_bank113.asy: Graphical symbol information file. Used by the ISE tools and some third party tool create a symbol representing the core.	s to
ibert_bank113.bit: Please see the core data sheet.	
ibert_bank113.gise: ISE Project Navigator support file. This is a generated file and should not be edit directly.	ed
ibert_bank113.ise: ISE Project Navigator support file. This is a generated file and should not be edited	d directly.
ibert_bank113.ngc: Binary Xilinx implementation netlist file containing the information required to imple module in a Xilinx (R) FPGA.	ement the
ibert_bank113.ucf: Please see the core data sheet.	
ibert_bank113.v: Verilog wrapper file provided to support functional simulation. This file contains simul model customization data that is passed to a parameterized simulation model for the core.	ation
ibert_bank113.veo: VEO template file containing code that can be used as a model for instantiating a Generator module in a Verilog design.	CORE
ibert_bank113.xco: CORE Generator input file containing the parameters used to regenerate a core.	
ibert_bank113.xise: ISE Project Navigator support file. This is a generated file and should not be edit directly.	ed

Help

Close

Compile IBERT Design

Type these commands in a windows command shell:

cd C:\ml605_ibert\ibert_bank113\implement implement.bat > implement.log 2>&1



IBERT Design Creation Bank 114



- Right click on the IBERT Virtex6 GTX (ChipScope Pro IBERT, Version 2.02a
 - Select Customize and Generate

Xilinx CORE Generator - C:\ml605_ibert\ml605_ibert.cgp								
File Project View Help								
IP Catalog	Ð	×						
View by Function View by Name		IBERT Virtex6 🥥						
Name /	Version Status License	CTV (ChinScope						
🕂 💆 Debug & Verification		GTX (ChipScope						
🖻 📂 📂 ChipScope Pro		Pro - IBERT)						
	1.03.a Production							
🤯 IBERT Spartan6 GTP (ChipScope Pro - IBERT)	2.01.a Production	This area is a second of a table to Bee doo then have an effect of the						
🙀 IBERT Virtex5 GTX (ChipScope Pro - IBERT)	2.00.a Production	This core is supported at status Production by your chosen part.						
	Customize and Generate	T. C						
- 📲 IBERT Virtex6 GTX (ChipScope Pro - IBERT)	A Manu Annuna Danada	Information						
	30 View Answer Records	Core type: IBERT Virtex6 GTX (ChipScope Pro - IBERT)						
) 📑 View Data Sheet	Version: 2.02.a						
VIO (ChipScope Pro - Virtual Input/Output)	E View Version Information	Core Summary: The ChipScope Pro Series Integrated Bit Error Ratio Tester for Virtex6 GTX.						
Search IP Catalog:	Clear							
All IP versions	Only IP compatible with chosen pa	t Supported Families						
🍕 Project IP 🔄 IP Catalog		Current Project Options						
		Part: xc6vlx240t-1ff1156 Design Entry: Verilog 🌍 🎢						

EXILINX.

- Make the following settings:
 - Component name:
 ibert_bank114
 - Set the number of Line
 Rates: 1
 - Set the line rate to Max
 Rate: **5 Gbps**
- On the ML605, Bank 114 is connected to the 250 MHz OSC
 - Set the RefClk frequency to: 250 MHz
- Click Next

<u>V</u> iew				
LogiC ^{&RE}	IBERT (ChipSco	' Virtex6 pe Pro -	GTX IBERT) 2.02
Component Nam	ne ibert_bank114			
Line Rate Sett Number of Line	ings Rates (protocols) 1 💌			
Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch 💌	5	20 💌	250.00 💌

IBERT Virtex6 GTX (ChinScone Pro - IBERT

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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- The line rate is 5 Gbps
- Select the four GTXs for Bank 114:
 - X0Y11
 - X0Y10
 - X0Y9
 - X0Y8
- Connect the Refciks to:
 - REFCLK0 Q2
- Click Next

GTX (Location) TXREFCLK RXREFCLKI GTX3_116 (X0Y19) REFCLK1_Q4 REFCLK1 Q4 ✓ GTX2_116 (X0Y18) REFCLK1_Q4 REFCLK1 Q4 ✓ GTX1_116 (X0Y17) REFCLK1_Q4 REFCLK1 Q4 ✓ GTX0_116 (X0Y16) REFCLK1_Q4 REFCLK1 Q4 ✓ GTX3_115 (X0Y15) REFCLK1_Q3 REFCLK1 Q3 ✓ GTX2_115 (X0Y14) REFCLK1_Q3 REFCLK1 Q3 ✓ GTX1_115 (X0Y12) REFCLK1_Q3 REFCLK1 Q3 ✓ GTX1_115 (X0Y12) REFCLK1_Q3 REFCLK1 Q3 ✓ GTX1_115 (X0Y12) REFCLK0_Q2 REFCLK0 Q2 ✓ GTX1_114 (X0Y10) REFCLK0_Q2 REFCLK0 Q2 ✓ GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ✓ GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ✓ GTX1_113 (X0Y6) REFCLK1_Q1 REFCLK1 Q1 ✓ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q1 ✓ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 ✓ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ✓ GTX	Select GTXs and Reference Clocks for Line Rate 1					
GTX3_116 (X0Y19) REFCLK1_Q4 REFCLK1_Q4 REFCLK1_Q4 Y GTX2_116 (X0Y18) REFCLK1_Q4 REFCLK1_Q4 Y GTX1_116 (X0Y17) REFCLK1_Q4 REFCLK1_Q4 Y GTX1_116 (X0Y16) REFCLK1_Q4 REFCLK1_Q4 Y GTX3_115 (X0Y15) REFCLK1_Q3 REFCLK1_Q3 Y GTX2_115 (X0Y14) REFCLK1_Q3 REFCLK1 Q3 Y GTX1_115 (X0Y12) REFCLK1_Q3 REFCLK1 Q3 Y GTX3_114 (X0Y11) REFCLK0_Q2 REFCLK0 Q2 Y GTX1_114 (X0Y10) REFCLK0_Q2 REFCLK0 Q2 Y GTX1_114 (X0Y9) REFCLK0_Q2 REFCLK0 Q2 Y GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 Y GTX1_113 (X0Y3) REFCLK1_Q1 REFCLK1 Q1 Y GTX1_113 (X0Y4) REFCLK1_Q1 REFCLK1 Q1 Y GTX2_112 (X0Y2) REFCLK1_Q0 REFCLK1 Q0 Y GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 Y GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 Y GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0	[GTX (Location)	TXREFCLK	RXREFCLK	
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		Γ	GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4	
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□ GTX1_115 (X0Y13) REFCLK1_Q3 REFCLK1 Q3 ✓ □ GTX0_115 (X0Y12) REFCLK1_Q3 REFCLK1 Q3 ✓ □ GTX3_114 (X0Y11) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX2_114 (X0Y10) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX1_114 (X0Y9) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX0_114 (X0Y8) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX1_114 (X0Y8) REFCLK1_Q1 REFCLK0 Q2 ✓ □ GTX1_114 (X0Y8) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX1_113 (X0Y6) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX1_113 (X0Y4) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓		Γ	GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3	
□ GTX0_115 (X0Y12) REFCLK1_Q3 REFCLK1 Q3 ✓ □ GTX3_114 (X0Y11) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX2_114 (X0Y10) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX1_114 (X0Y9) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX0_114 (X0Y9) REFCLK0_Q2 REFCLK0 Q2 ✓ □ GTX1_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX2_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX2_113 (X0Y6) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX1_113 (X0Y5) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX3_112 (X0Y3) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX3_112 (X0Y2) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓			GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3	
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▼ GTX2_114 (X0Y10) REFCLK0_Q2 REFCLK0 Q2 ▼ ▼ GTX1_114 (X0Y9) REFCLK0_Q2 REFCLK0 Q2 ▼ ▼ GTX0_114 (X0Y8) REFCLK0_Q2 REFCLK0 Q2 ▼ □ GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 Q1 ▼ □ GTX2_113 (X0Y6) REFCLK1_Q1 REFCLK1 Q1 ▼ □ GTX1_113 (X0Y5) REFCLK1_Q1 REFCLK1 Q1 ▼ □ GTX0_113 (X0Y4) REFCLK1_Q1 REFCLK1 Q1 ▼ □ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX2_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ▼		☑	GTX3_114 (X0Y11)	REFCLK0_Q2	REFCLK0 Q2	
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GTX1_113 (X0Y5) REFCLK1_Q1 REFCLK1 Q1 Image: Constraint of the second sec		Γ	GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1 🗾	
□ GTX0_113 (X0Y4) REFCLK1_Q1 REFCLK1 Q1 ✓ □ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX2_112 (X0Y2) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ✓ □ GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓ ■ GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ✓		Γ	GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1 🗾	
□ GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX2_112 (X0Y2) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 ▼ □ GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 ▼ Active GTXs : 4 4			GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1 🛛	
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GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0 Active GTXs : 4		Γ	GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0 💌	
GTX0_112 (X0Y0) REFCLK1_Q0 REFCLK1 Q0		Γ	GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0 🔽	
Active GTXs : 4		Γ	GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0	
				Active GTXs : 4		

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<u>Cancel</u>

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- Leave this screen as is
 - Click Next

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

Enable RXRECCLK Probes

- RXRECCLK PIN OUT					
Enable	GTX	Location*	IO Standard		
	X0Y8 RXRECCLK	\$	LVDS 25		
	X0Y9 RXRECCLK	\$	LVDS 25		
	X0Y10 RXRECCLK	\$	LVDS 25		
Г	X0Y11 RXRECCLK	\$	LVDS 25		

* In case the selected Input standard in Differential, Please enter only P Pin Location.

- Select the following settings:
 - Use External Clock source
 - Location: **J9**
- Click Next

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<u>V</u>iew

LogiCZRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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System Clock					
Set the system clock for FPGA's internal debug bus					
Use External Clock source *					
Frequency (MHz)200Location *J9Input StandardLVDS 25					
C Use MGT TXOUTCLK**					

* In case the selected input standard is differential, please enter only "p" pin location. **Select at least one GTX from the clock selection panels to use TXOUTCLK

- Deselect
 - Implement Design
- Click Generate

🖣 IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

IBERT Core Summary

System				
System Clock Source / Frequencies	IBERT_SY	IBERT_SYSCLOCK / 200 MHz		
BUFGs used / MMCMs used	10 / 1	10 / 1		
Line Rates				
Index Protocol	Line Rate	Data Width	REFCLK	GTXs selected
1 Start_from_scratch	5	20	250.00	x0y8 x0y9 x0y10 x0y11

🔲 Implement Design

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 Generate
 Cancel
 Help
After the IBERT core finishes generating, click Close on the Readme File window

Readme ibert_bank114	?
The following files were generated for 'ibert_bank114' in directory C: \ml605_ibert\	Ŀ
ibert_bank114_flist.txt: Text file listing all of the output files produced when a customized core was generate in the CORE Generator.	d
ibert_bank114.asy: Graphical symbol information file. Used by the ISE tools and some third party tools to create a symbol representing the core.	
ibert_bank114.bit: Please see the core data sheet.	
ibert_bank114.gise: ISE Project Navigator support file. This is a generated file and should not be edited directly.	
ibert_bank114.ise: ISE Project Navigator support file. This is a generated file and should not be edited directly	<i>ı</i> .
ibert_bank114.ngc: Binary Xilinx implementation netlist file containing the information required to implement th module in a Xilinx (R) FPGA.	e
ibert_bank114.ucf: Please see the core data sheet.	
ibert_bank114.v: Verilog wrapper file provided to support functional simulation. This file contains simulation model customization data that is passed to a parameterized simulation model for the core.	
ibert_bank114.veo: VEO template file containing code that can be used as a model for instantiating a CORE Generator module in a Verilog design.	
ibert_bank114.xco: CORE Generator input file containing the parameters used to regenerate a core.	
ibert_bank114.xise: ISE Project Navigator support file. This is a generated file and should not be edited directly.	

Help

<u>Close</u>

Compile IBERT Design

Type these commands in a windows command shell:

cd C:\ml605_ibert\ibert_bank114\implement implement.bat > implement.log 2>&1



IBERT Design Creation Bank 115



- Right click on the IBERT Virtex6 GTX (ChipScope Pro IBERT, Version 2.02a
 - Select Customize and Generate

🂐 Xilinx CORE Generator - C:\ml605_ibert\ml605_ibert.	cgp						
File Project View Help							
P Catalog				₽×			
View by Function View by Name					PE	IBERT Virtex6 🛛 🤍	
Name /	Version	Status	License	_	logic	CTV (ChinScope	ect
🕂 📂 Debug & Verification						GIX (ChipScope	
🖻 📂 📂 ChipScope Pro						Pro - IBERT)	
🏹 ATC2 (ChipScope Pro - Agilent Trace Core 2)	1.03.a	Production		1			
🖑 IBERT Spartan6 GTP (ChipScope Pro - IBERT)	2.01.a	Production					
🖑 IBERT Virtex5 GTX (ChipScope Pro - IBERT)	2.00.a	Production			This core is support	ted at status Production by your chosen part.	
🖑 IBERT Virtex6 GTH (ChipScope Pro - IBERT)	Cust	omize and G	ienerate		_ .		
IBERT Virtex6 GTX (ChipScope Pro - IBERT)	4				Informatio	n	
ICON (ChipScope Pro - Integrated Controller)	🗊 View /	Answer Recor	ds		Core type:	IBERT Virtex6 GTX (ChipScope Pro - IBERT)	
ILA (ChipScope Pro - Integrated Logic Analyzer	, 🔚 View I	Data Sheet		1	Version:	2.02.a	
VIO (ChipScope Pro - Virtual Input/Output)		Version Inform	ation		Core Summary:	The ChipScope Pro Series Integrated Bit Error	
		Version Inform				Ratio Tester for Virtex6 GTX.	
Search IP Catalog:				Clear			
All IP versions		Only IP compa	tible with ch	osen part	Supported Fam	ilies	
😲 Broject IB. 🔅 TD Catalan				<u> </u>	Current Project	t Options	
						Part: xc6vlx240t-1ff1156 Design Entry: Verilog	D //.

EXILINX.

- Make the following settings:
 - Component name: ibert_bank115
 - Set the number of Line Rates: 1
 - Set the line rate to:
 - Max Rate: **5 Gbps**
- On the ML605, Bank 115 is connected to the 100 **MHz OSC**
 - Set the RefClk frequency to: 100 MHz
- Click Next

🏺 IBERT Virtex6	GTX (ChipScope Pro - IBERT	r)		
<u>V</u> iew				
Logi <mark>C^XRE</mark>	IBERT (ChipSco	' Virtex6 pe Pro -	GTX IBERT) 2.02.a
Component Nam	ne ibert_bank115			
Line Rate Setti	ings			
Number of Line	Rates (protocols) 1 💌			
Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch 💌	5	20 💌	100.00

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

Help

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Select GTXs and Reference Clocks for Line Rate 1

LogiCRE

		GTX (Location)	TXREFCLK	RXREFCLK
	Γ	GTX3_116 (X0Y19)	REFCLK1_Q4	REFCLK1 Q4
	Γ	GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4 🗾
	Γ	GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
	Γ	GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
	◄	GTX3_115 (X0Y15)	REFCLK0_Q3	REFCLK0 Q3
	◄	GTX2_115 (X0Y14)	REFCLK0_Q3	REFCLK0 Q3
	◄	GTX1_115 (X0Y13)	REFCLK0_Q3	REFCLK0 Q3
	◄	GTX0_115 (X0Y12)	REFCLK0_Q3	REFCLK0 Q3
	Γ	GTX3_114 (X0Y11)	REFCLK1_Q2	REFCLK1 Q2
	Γ	GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
	Γ	GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
	Γ	GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
	Γ	GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1
	Γ	GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1
	Γ	GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1 🗾
	Γ	GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1 🗾 👻
	Γ	GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0 🔽
	Γ	GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
	Γ	GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0 🗸
	Γ	GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0
			Active GTXs : 4	
tasheet		< Back Page 2 of	5 Next > G	enerate Cancel

- The rate is 5 Gbps
- Select the four GTXs for **Bank 115:**
 - X0Y15
 - X0Y14
 - X0Y13
 - X0Y12
- Connect the Refclks to:
 - REFCLK0 Q3
- Click Next

- Leave this screen as is
 - Click Next

View

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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Enable RXRECCLK Probes

-RXRECCLK PIN OUT								
Enable	GTX	Location*	IO Standard					
	X0Y12 RXRECCLK	\$	LVDS 25					
	X0Y13 RXRECCLK	\$	LVDS 25					
	X0Y14 RXRECCLK	\$	LVDS 25					
Γ	X0Y15 RXRECCLK	\$	LVDS 25					

* In case the selected Input standard in Differential, Please enter only P Pin Location.



- Select the following settings:
 - Use External Clock source
 - Location: J9
- Click Next

×.	TOPOTA	C-1	CTV IC	L:		TOPOTA
Υ.	TREKT A	irtex6	GIX (C	nipScot	e Pro -	IBERI)

<u>V</u>iew

LogiCZRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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System Clock						
Set the system clock for FPGA's internal debug bus						
Use External Clock source *						
Frequency (MHz)200Location *J9Input StandardLVDS 25						
C Use MGT TXOUTCLK**						

* In case the selected input standard is differential, please enter only "p" pin location. **Select at least one GTX from the clock selection panels to use TXOUTCLK

- Deselect
 - Implement Design
- Click Generate

🖣 IBERT Virtex6 GTX (ChipScope Pro - IBERT)

<u>V</u>iew

LogiCRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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IBERT Core Summary

-9	System					
5	System	Clock Source / Frequ	uency	IBERT_SY	SCLOCK /	200 MHz
E	BUFGs u	sed / MMCMs used		10 / 1		
-L	ine Rat	es				
Γ						
	Index	Protocol	Line Rate	Data Width	REFCLK	GTXs selected
	1	Start_from_scratch	5	20	100.00	x0y12 x0y13 x0y14 x0y15

🔲 Implement Design

 Datasheet
 < Back</th>
 Page 5 of 5
 Next >
 Generate
 Cancel
 Help

 After the IBERT core finishes generating, click Close on the Readme File window

Readme ibert_bank115	?
The following files were generated for 'ibert_bank115' in directory C:\ml605_ibert\	-
ibert_bank115_flist.txt: Text file listing all of the output files produced when a customized core was in the CORE Generator.	generated
ibert_bank115.asy: Graphical symbol information file. Used by the ISE tools and some third party too create a symbol representing the core.	ls to
ibert_bank115.bit: Please see the core data sheet.	
ibert_bank115.gise: ISE Project Navigator support file. This is a generated file and should not be edi directly.	ted
ibert_bank115.ise: ISE Project Navigator support file. This is a generated file and should not be edite	ed directly.
ibert_bank115.ngc: Binary Xilinx implementation netlist file containing the information required to imp module in a Xilinx (R) FPGA.	lement the
ibert_bank115.ucf: Please see the core data sheet.	
ibert_bank115.v: Verilog wrapper file provided to support functional simulation. This file contains simu model customization data that is passed to a parameterized simulation model for the core.	Ilation
ibert_bank115.veo: VEO template file containing code that can be used as a model for instantiating a Generator module in a Verilog design.	3 CORE
ibert_bank115.xco: CORE Generator input file containing the parameters used to regenerate a core	
ibert_bank115.xise: ISE Project Navigator support file. This is a generated file and should not be edi directly.	ted

<u>H</u>elp

<u>Close</u>

Compile IBERT Design

Type these commands in a windows command shell:

cd C:\ml605_ibert\ibert_bank115\implement implement.bat > implement.log 2>&1





IBERT Design Creation Bank 116



- Right click on the IBERT Virtex6 GTX (ChipScope Pro IBERT, Version 2.02a
 - Select Customize and Generate

🂐 Xilinx CORE Gen	erator - C:\ml605_ibert\ml605_ibert.c	gp				
File Project View	Help					
IP Catalog					Β×	
View by Function	View by Name					IBERT Virtex6
Name	Δ	Version	Status	License		CTV (ChinScone
🖻 📂 Debug & Ver	ification pe Pro					Pro - IBERT)
IBEF	2 (ChipScope Pro - Agilent Trace Core 2) RT Spartan6 GTP (ChipScope Pro - IBERT) RT Virtex5 GTX (ChipScope Pro - IBERT)	1.03.a 2.01.a 2.00.a	Production Production Production	1		This core is supported at status Production by your chosen part.
	RT Virtex6 GTH (ChipScope Pro - IBERT) RT Virtex6 GTX (ChipScope Pro - IBERT)	Custo	o <mark>mize and G</mark> Answer Record	enerate Is		Information
	N (ChipScope Pro - Integrated Controller) (ChipScope Pro - Integrated Logic Analyzer) (ChipScope Pro - Virtual Input/Output)	View [Data Sheet			Version: 2.02.a Core Summary: The ChinScope Pro Series Integrated Bit Error
Search IP Catalog:		View \	ersion Inform	ation Cle	ear	Ratio Tester for Virtex6 GTX.
All IP versions			Only IP compa	tible with chose	en part	Supported Families
🍕 Project IP 🔇	IP Catalog					Current Project Options
						Part: xc6vlx240t-1ff1156 Design Entry: Verilog 🌔 🏸

E XILINX.

- Make the following settings:
 - Component name:
 ibert_bank116
 - Set the number of Line Rates: 2
 - Set the first line rate to: Max Rate: 1.25 Gbps
 - Set the second line rate to:

Max Rate: 5 Gbps

Set both RefClk
 frequencies to: **125 MHz**

Click Next

<u>V</u> iew				
logi <mark>C^õRE</mark>	IBER [®] (ChipSco	T Virtex6 ope Pro -	GTX IBERT) 2.02.8
Component Nam	ne ibert_bank116			
Line Rate Setti Number of Line	ings Rates (protocols) 2 💌			
Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch	1.25	20 💌	125.00 💌
2	Start from scratch	- 5	20 💌	125.00 💌

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

Datasheet < Back</th> Page 1 of 5 Next > Generate Cancel

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💐 IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

Help

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- Select GTXs and Reference Clocks for Line Rate 1

	GTX (Location)	TXREFCLK	RXREFCLK
F	GTX3_116 (X0Y19)	REFCLK0_Q4	REFCLK0 Q4
Г	GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
Г	GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
Г	GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
Г	GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
Г	GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3 🗾
Γ	GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
Γ	GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
Г	GTX3_114 (X0Y11)	REFCLK1_Q2	REFCLK1 Q2 🔻
Г	GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2 🔻
Г	GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
Г	GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2 🔻
Г	GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1 🗾
Г	GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1 🗾
Г.	GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1 🗾
Г.	GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1 🗾
Г	GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0 🔻
Г	GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0 🔽
Г	GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0 🔽
Г.	GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0 🔽
		Active GTXs : 1	
Datasheet	< Back Page 2 of	7 <u>N</u> ext > Ge	enerate <u>C</u> ancel

- The first line rate is 1.25
 Gbps
- Select the first GTX for Bank 116:
 - X0Y19
- Connect the RefClk to:
 - REFCLK0 Q4
 - This connects Bank 116 to the 125 MHz SGMII OSC
- Click Next

🖥 IBERT Virtex6 GTX (ChipScope Pro - IBERT)

<u>V</u>iew

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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Select GTXs and Reference Clocks for Line Rate 2

GTX (Location) RXREFCLK TXREFCLK GTX3_116 (X0Y19) REFCLK0_Q4 REFCLK0 Q4 GTX2_116 (X0Y18) REFCLK0_Q4 REFCLK0 Q4 GTX1_116 (X0Y17) REFCLK0_Q4 REFCLK0 Q4 GTX0_116 (X0Y16) REFCLK0_Q4 REFCLK0 Q4 GTX3_115 (X0Y15) REFCLK1_Q3 REFCLK1 Q3 GTX2_115 (X0Y14) REFCLK1_Q3 REFCLK1 03 GTX1_115 (X0Y13) REFCLK1_Q3 REFCLK1 Q3 REFCLK1_Q3 GTX0_115 (X0Y12) REFCLK1 Q3 GTX3_114 (X0Y11) REFCLK1_Q2 REFCLK1 Q2 GTX2_114 (X0Y10) REFCLK1_Q2 REFCLK1 02 GTX1_114 (X0Y9) REFCLK1_Q2 REFCLK1 Q2 GTX0_114 (X0Y8) REFCLK1_Q2 REFCLK1 Q2 GTX3_113 (X0Y7) REFCLK1_Q1 REFCLK1 01 GTX2_113 (X0Y6) REFCLK1_Q1 REFCLK1 Q1 GTX1_113 (X0Y5) REFCLK1_Q1 REFCLK1 Q1 GTX0_113 (X0Y4) REFCLK1 01 REFCLK1_Q1 GTX3_112 (X0Y3) REFCLK1_Q0 REFCLK1 Q0 GTX2_112 (X0Y2) REFCLK1_Q0 REFCLK1 Q0 GTX1_112 (X0Y1) REFCLK1_Q0 REFCLK1 Q0 GTX0_112 (X0Y0) REFCLK1 Q0 REFCLK1_Q0 Active GTXs : 3

Next >

<u>D</u>atasheet

< Back | Page

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Generate

Cancel

<u>H</u>elp

- The second line rate is 5 Gbps
- Select the second and third GTXs for Bank 116:
 - X0Y18
 - X0Y17
 - X0Y16
- Connect the Refclks to:
 - REFCLK0 Q4
- Click Next

- Leave this screen as is
 - Click Next

View

LogiCZRE

Datasheet

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Next >

Cancel

Help

Generate

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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Enable RXRECCLK Probes

RXRECCLK PIN OUT

Enable	GTX	Location*	IO Standard	
	X0Y0 RXRECCLK	\$	LVDS 25	-

* In case the selected Input standard in Differential, Please enter only P Pin Location.

- Leave this screen as is
 - Click Next

View

LogiCZPL

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

- 🗆 🗵

Enable RXRECCLK Probes

Enable		Location*	IO Standard
LIIdble	GIX	Location	10 Standard
	X0Y16 RXRECCLK	\$	LVDS 25
	X0Y17 RXRECCLK	\$	LVDS 25 💌
	X0Y18 RXRECCLK	\$	LVDS 25
	X0Y19 RXRECCLK	\$	LVDS 25

* In case the selected Input standard in Differential, Please enter only P Pin Location.

- Select the following settings:
 - Use External Clock source
 - Location: **J9**
- Click Next

1	DEDTW		CTV I			TOCOT)
и 🦻	BERT V	irtex6	GIX (1	CubSco	pe Pro -	IBERT)

<u>V</u>iew

LogiCZRE

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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System Clock			
Set the system clock for FPGA's internal debug bus			
Use External Clock source	ce *		
Frequency (MHz) Location * Input Standard	200 J9 LVDS 25		
C Use MGT TXOUTCLK**			

* In case the selected input standard is differential, please enter only "p" pin location. **Select at least one GTX from the clock selection panels to use TXOUTCLK

- Deselect
 - Implement Design
- Click Generate

View

LogiCZPL

Datasheet

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IBERT Virtex6 GTX (ChipScope Pro - IBERT)

2.02.a

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IBERT Core Summary

IBERT_SYSCLOCK / 200 MHz	
12 / 1	
ate Data Width REFCLK GTXs selected	
20 125.00 x0y19	
20 125.00 x0y16 x0y17 x0y18	
	IBERT_SYSCLOCK / 200 MHz 12 / 1 te Data Width REFCLK GTXs selected 20 125.00 x0y19 20 125.00 x0y16 x0y17 x0y18

🔲 Implement Design

<u>N</u>ext > <u>Generate</u>

erate <u>C</u>ancel

<u>H</u>elp

 After the IBERT core finishes generating, click Close on the Readme File window

Readme ibert_bank116	?
The following files were generated for 'ibert_bank116' in directory C: \ml605_ibert\	
ibert_bank116_flist.txt: Text file listing all of the output files produced when a customized core was generate in the CORE Generator.	d
ibert_bank116.asy: Graphical symbol information file. Used by the ISE tools and some third party tools to create a symbol representing the core.	
ibert_bank116.bit: Please see the core data sheet.	
ibert_bank116.gise: ISE Project Navigator support file. This is a generated file and should not be edited directly.	
ibert_bank116.ise: ISE Project Navigator support file. This is a generated file and should not be edited directly	
ibert_bank116.ngc: Binary Xilinx implementation netlist file containing the information required to implement th module in a Xilinx (R) FPGA.	e
ibert_bank116.ucf: Please see the core data sheet.	
ibert_bank116.v: Verilog wrapper file provided to support functional simulation. This file contains simulation model customization data that is passed to a parameterized simulation model for the core.	
ibert_bank116.veo: VEO template file containing code that can be used as a model for instantiating a CORE Generator module in a Verilog design.	
ibert_bank116.xco: CORE Generator input file containing the parameters used to regenerate a core.	
ibert_bank116.xise: ISE Project Navigator support file. This is a generated file and should not be edited directly.	
Close Helr	

EXILINX.

Compile IBERT Design

Type these commands in a windows command shell:

cd C:\ml605_ibert\ibert_bank116\implement implement.bat > implement.log 2>&1



Generate IBERT ACE Files (Optional)

Type these commands in a windows command shell:

cd C:\ml605_ibert\ready_for_download

make_ace.bat









References

ChipScope Pro

- ChipScope Pro Software and Cores User Guide

http://www.xilinx.com/support/documentation/sw_manuals/ xilinx12_1/chipscope_pro_sw_cores_ug029.pdf







Documentation

Virtex-6

- Virtex-6 FPGA Family

http://www.xilinx.com/products/virtex6/index.htm

ML605 Documentation

- Virtex-6 FPGA ML605 Evaluation Kit

http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards and kits/ug535.pdf

