ML605 PCIe x4 Gen2 Design Creation

May 2010

Overview

- **Virtex-6 PCIe x4 Gen2 Capability**
- **Xilinx ML605 Board**
- **Software Requirements**
- **Generate PCIe Core**
- **Compile PCIe Core**
- **Program Platform Flash with PCIe Design**
- **ML605 Setup**
- **Running the PCIe x4 Gen2 Design**
- **References**
  - IP Release Notes Guide XTP025

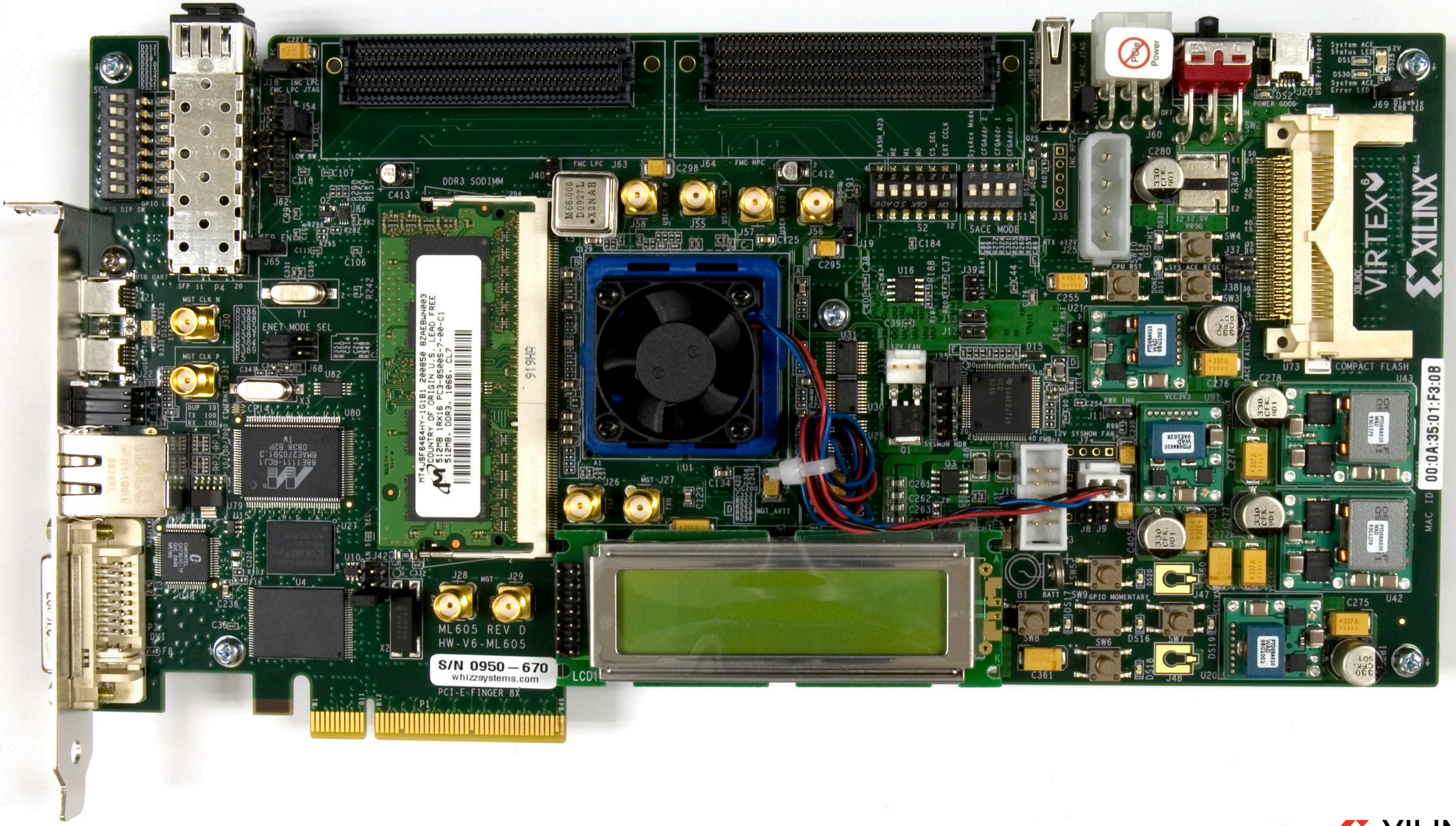
Note: This presentation applies to the ML605

Virtex-6 PCIe x4 Gen2 Capability

- **Integrated Block for PCI Express**
  - PCI Express Base 2.0 Specification
- **Generation 2 (5 GT/s) data rates**
  - x4, x2, or x1 Gen2 lane width
  - x8 Gen2 not supported in -1 parts
- **Configurable for Endpoint or Root Port Applications**
  - ML605 configured for Endpoint Applications
- **GTX Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering
- **Management and Statistics Interface**

Note: Presentation applies to the ML605

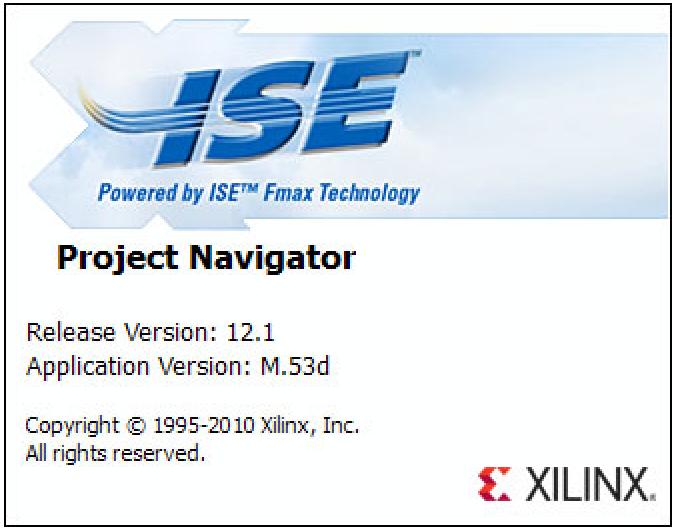
Xilinx ML605 Board



Note: Presentation applies to the ML605

ISE Software Requirements

- **Xilinx ISE 12.1 software**



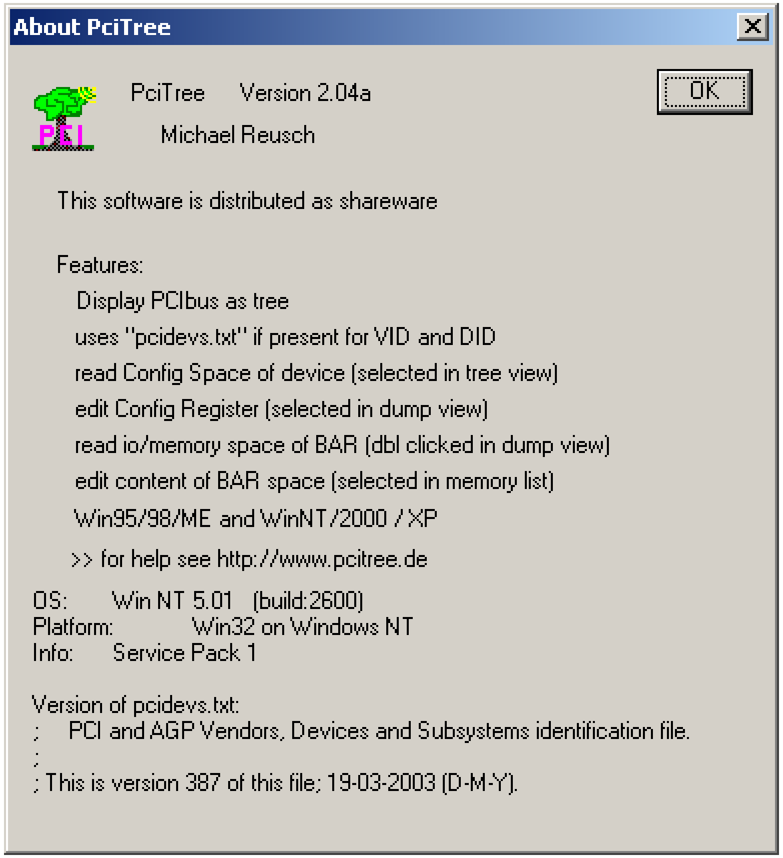
Project Navigator

Release Version: 12.1
Application Version: M.53d

Note: Presentation applies to the ML605

PciTree Software Requirement

- **PciTree Bus Viewer**
  - Free download
  - HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory



About PciTree

PciTree Version 2.04a

Michael Reusch

This software is distributed as shareware

Features:

Display PCIbus as tree
uses "pcidevs.txt" if present for VID and DID
read Config Space of device (selected in tree view)
edit Config Register (selected in dump view)
read io/memory space of BAR (dbl clicked in dump view)
edit content of BAR space (selected in memory list)
Win95/98/ME and WinNT/2000 / XP
>> for help see http://www.pcitree.de

```
OS:       Win NT 5.01   (build:2600)
Platform:           Win32 on Windows NT
Info:     Service Pack 1

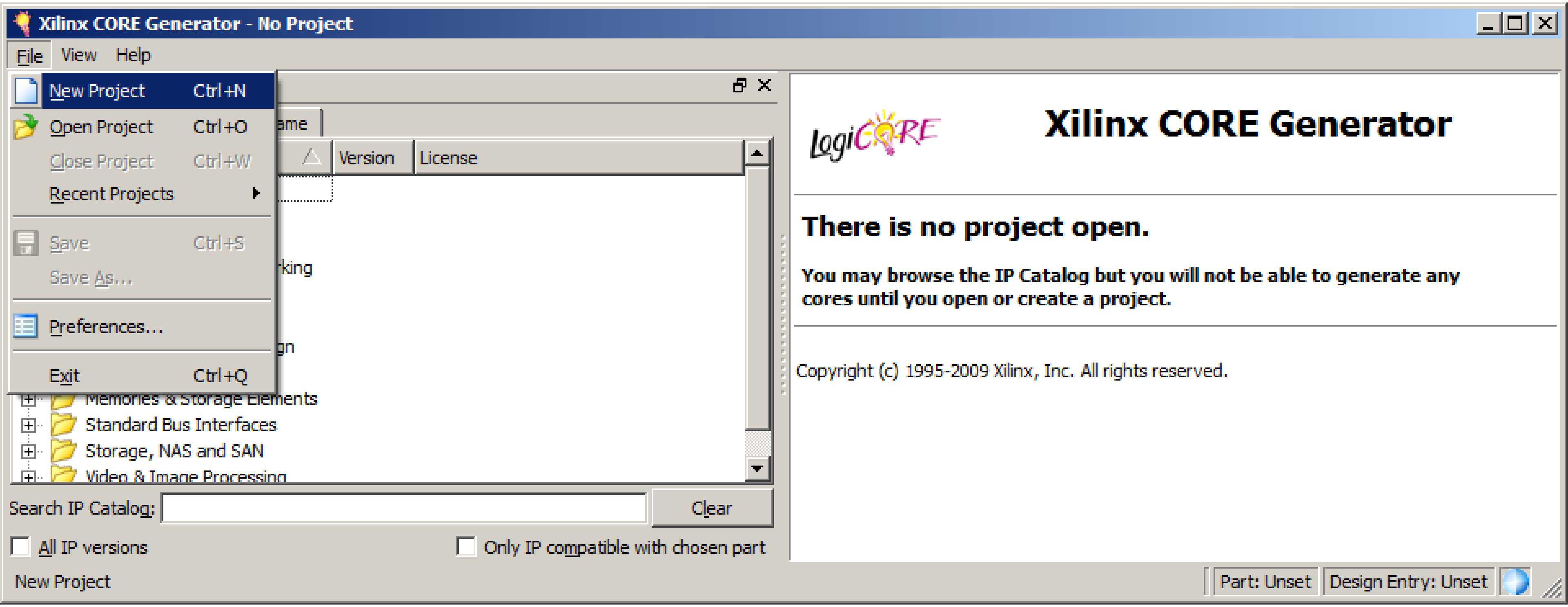
Version of pcidevs.txt:
;    PCI and AGP Vendors, Devices and Subsystems identification file.
;
; This is version 387 of this file; 19-03-2003 (D-M-Y).
```

Generate PCIe Core

- **Open the CORE Generator**

  Start → All Programs → Xilinx ISE Design Suite 12.1 → ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



Xilinx CORE Generator

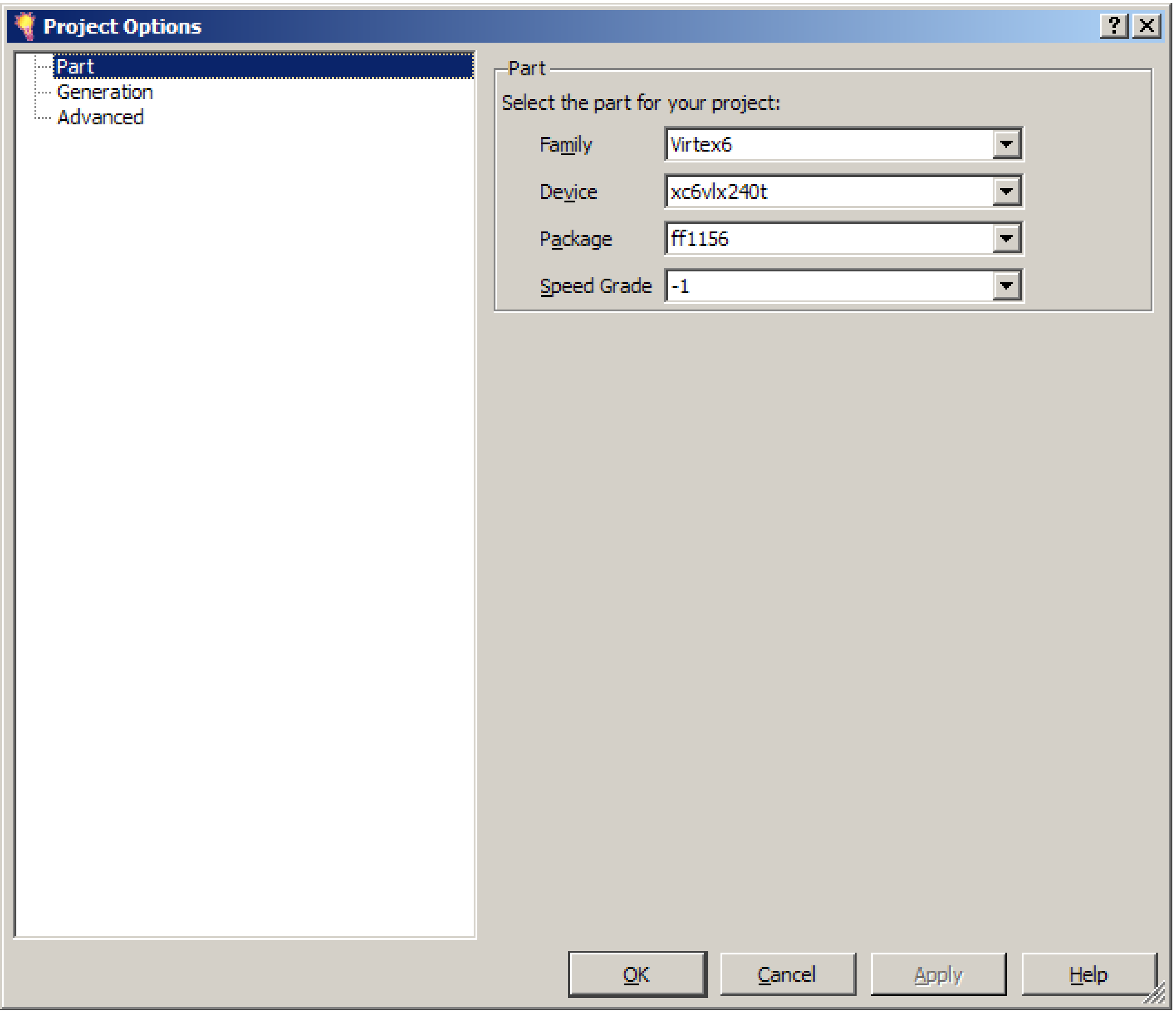
There is no project open.

You may browse the IP Catalog but you will not be able to generate any cores until you open or create a project.

Copyright (c) 1995-2009 Xilinx, Inc. All rights reserved.

Note: Pre-built design, RDF0009, available through http://www.xilinx.com/ml605

Generate PCIe Core



Part

Select the part for your project:

Family: Virtex6

Device: xc6vlx240t

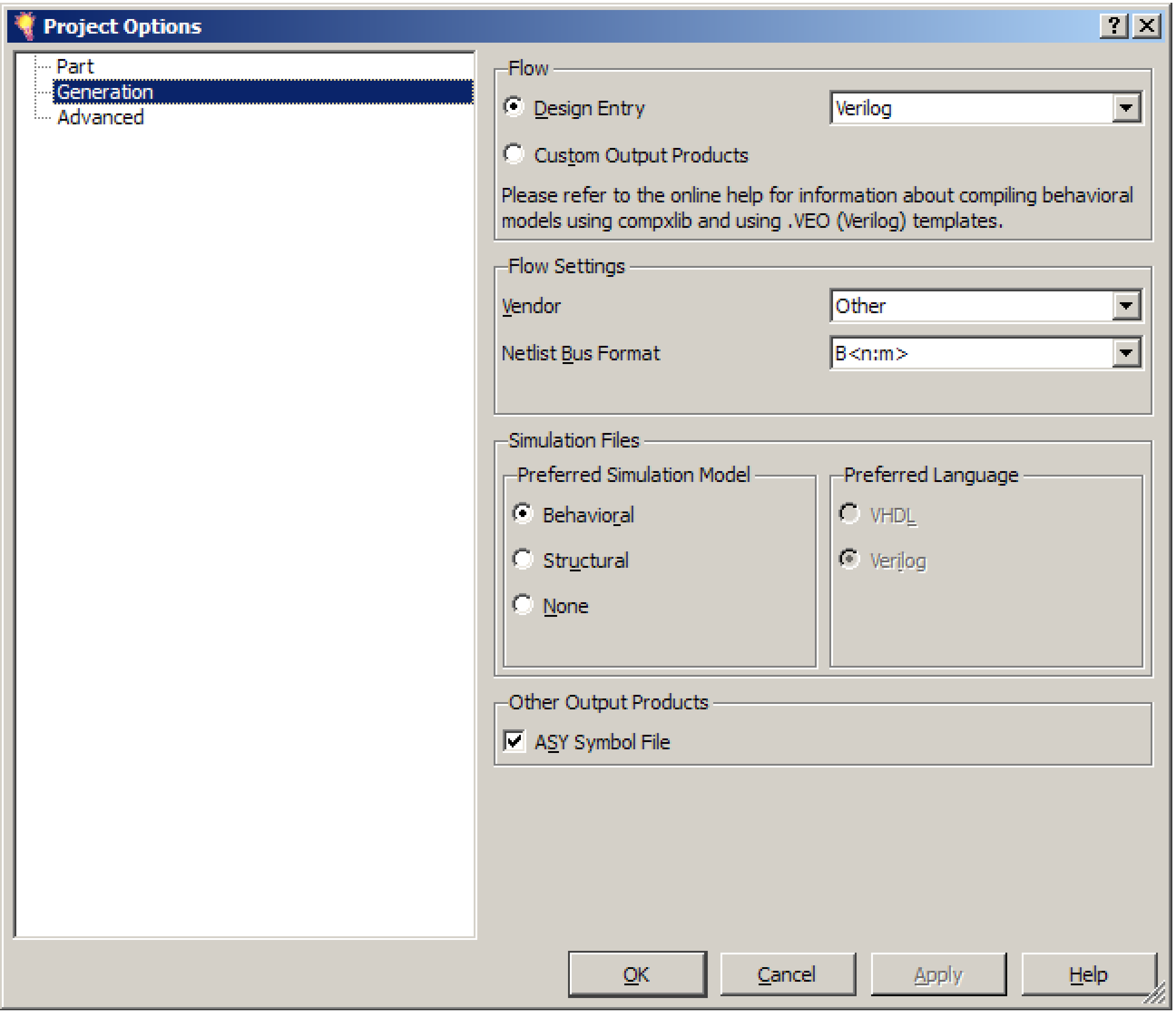
Package: ff1156

Speed Grade: -1

- Create a project directory: ml605_pcie_x4_gen2
- Name the project: ml605_pcie_x4_gen2 .cgp
- The Project options will appear
- Set the Part (as seen here):
  - Family: Virtex6
  - Device: xc6vlx240t
  - Package: ff1156
  - Speed Grade: -1

Note: Presentation applies to the ML605

Generate PCIe Core



Project Options

- Part
- Generation
- Advanced

Flow

● Design Entry: Verilog

○ Custom Output Products

Please refer to the online help for information about compiling behavioral models using compxlib and using .VEO (Verilog) templates.

Flow Settings

Vendor: Other

Netlist Bus Format: B<n:m>

Simulation Files

Preferred Simulation Model

● Behavioral

○ Structural

○ None

Preferred Language

○ VHDL

● Verilog

Other Output Products

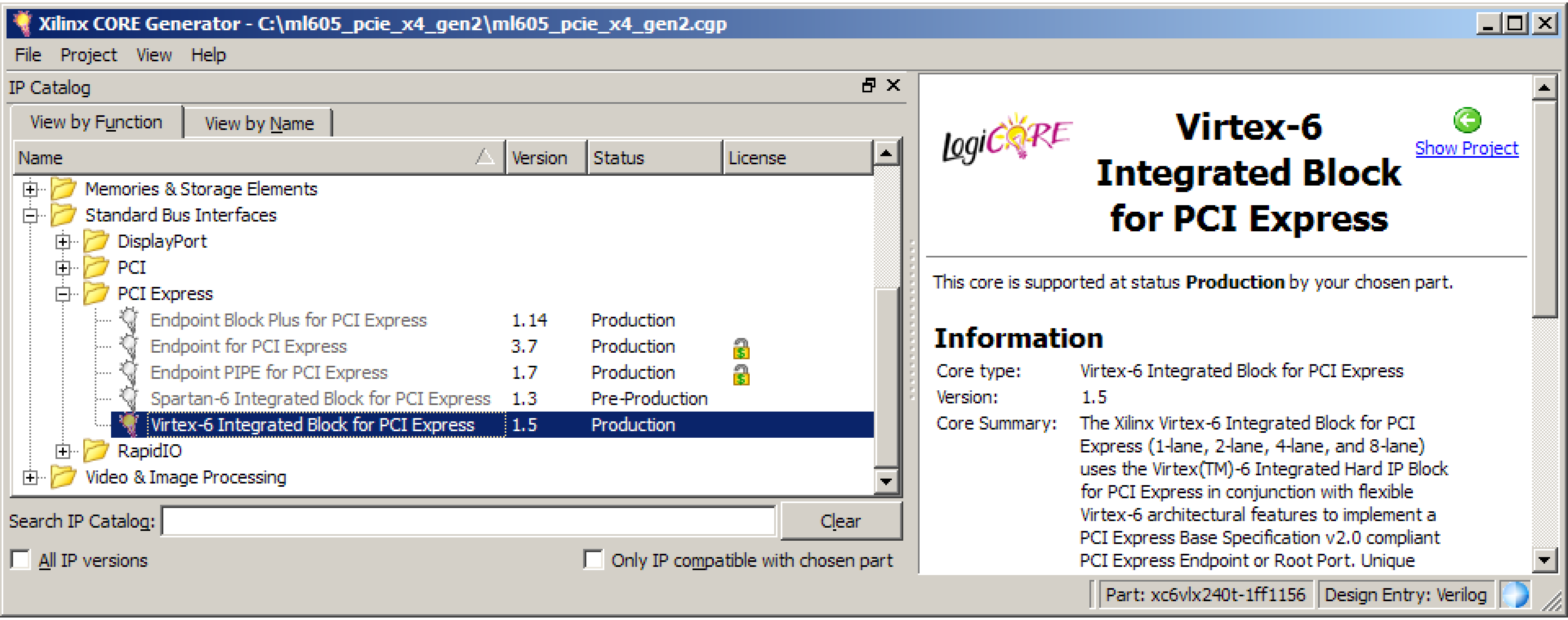
☑ ASY Symbol File

- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML605

Generate PCIe Core

- **Select**
  - Virtex-6 Integrated Block for PCI Express, **Version 1.5**



Name	Version	Status	License
Memories & Storage Elements			
Standard Bus Interfaces			
DisplayPort			
PCI			
PCI Express			
Endpoint Block Plus for PCI Express	1.14	Production	
Endpoint for PCI Express	3.7	Production	🔒
Endpoint PIPE for PCI Express	1.7	Production	🔒
Spartan-6 Integrated Block for PCI Express	1.3	Pre-Production	
Virtex-6 Integrated Block for PCI Express	1.5	Production	
RapidIO			
Video & Image Processing			

□ All IP versions

□ Only IP compatible with chosen part

Virtex-6 Integrated Block for PCI Express

This core is supported at status **Production** by your chosen part.

Information

Core type: Virtex-6 Integrated Block for PCI Express

Version: 1.5

Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane) uses the Virtex(TM)-6 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-6 architectural features to implement a PCI Express Base Specification v2.0 compliant PCI Express Endpoint or Root Port. Unique

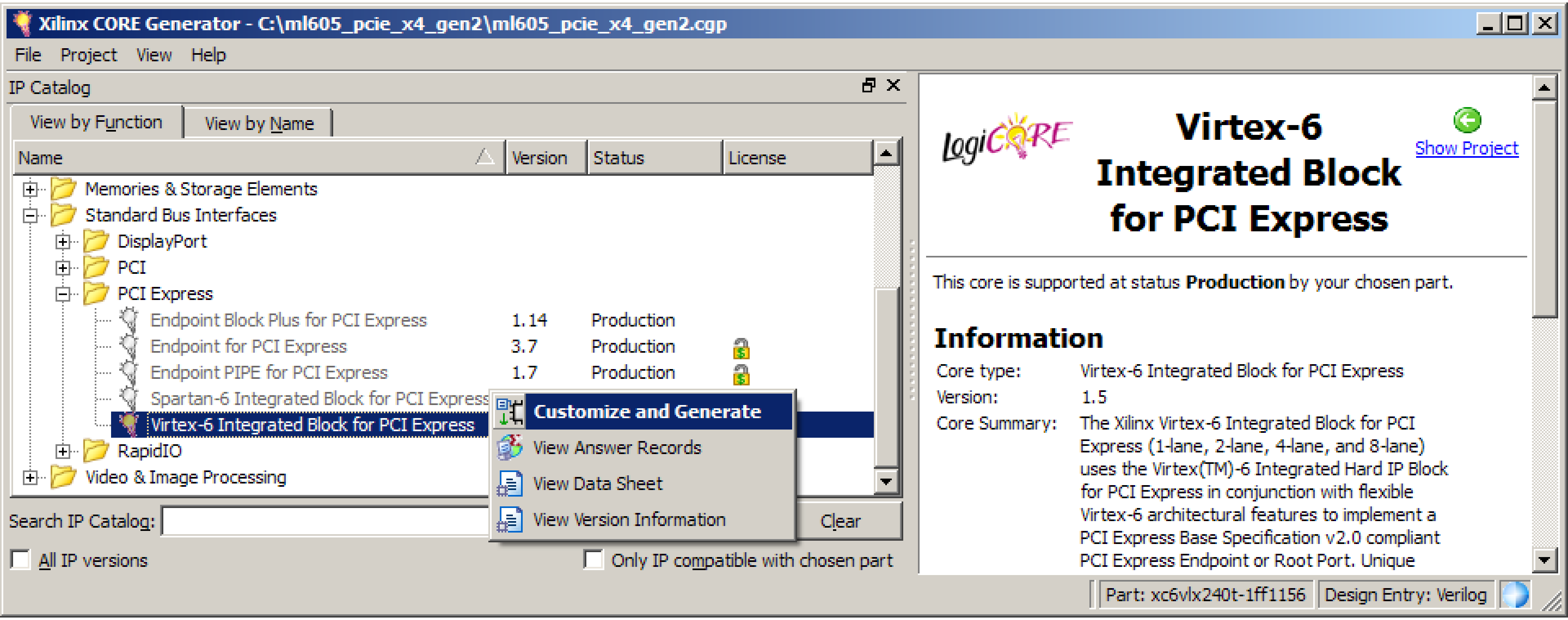
Part: xc6vlx240t-1ff1156

Design Entry: Verilog

Note: Presentation applies to the ML605

Generate PCIe Core

- **Right click on the Virtex-6 Integrated Block for PCI Express, Version 1.5**
  - Select **Customize and Generate**



Xilinx CORE Generator - C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp

File Project View Help

IP Catalog

View by Function | View by Name

Name	Version	Status	License
Memories & Storage Elements			
Standard Bus Interfaces			
DisplayPort			
PCI			
PCI Express			
Endpoint Block Plus for PCI Express	1.14	Production	
Endpoint for PCI Express	3.7	Production	🔒
Endpoint PIPE for PCI Express	1.7	Production	🔒
Spartan-6 Integrated Block for PCI Express			
Virtex-6 Integrated Block for PCI Express			
RapidIO			
Video & Image Processing			

Search IP Catalog: Clear

□ All IP versions □ Only IP compatible with chosen part

LogiCORE

Virtex-6 Integrated Block for PCI Express

Show Project

This core is supported at status **Production** by your chosen part.

Information

Core type: Virtex-6 Integrated Block for PCI Express

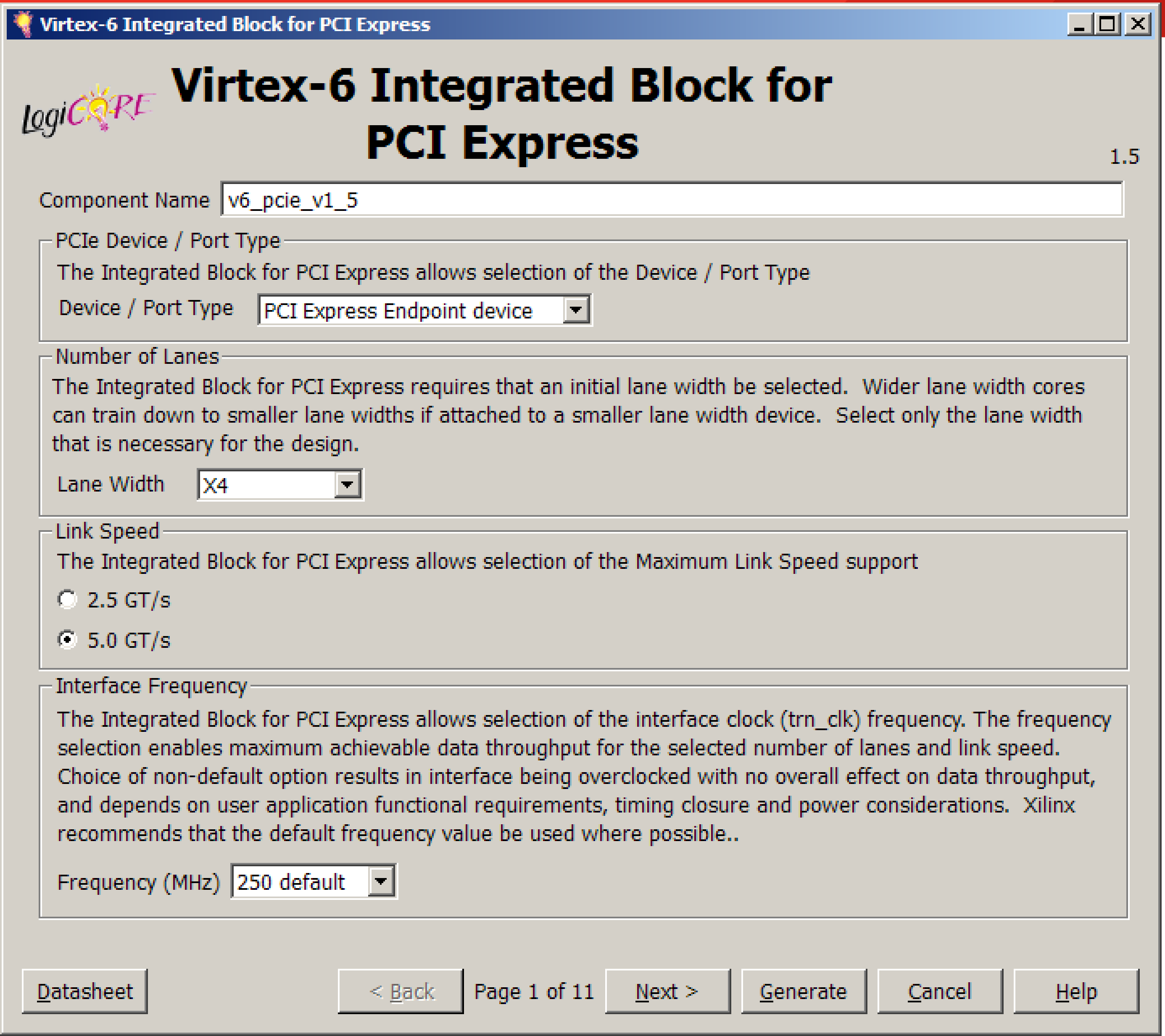
Version: 1.5

Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane) uses the Virtex(TM)-6 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-6 architectural features to implement a PCI Express Base Specification v2.0 compliant PCI Express Endpoint or Root Port. Unique

Part: xc6vlx240t-1ff1156 Design Entry: Verilog

Note: Presentation applies to the ML605

Generate PCIe Core



Virtex-6 Integrated Block for PCI Express

Virtex-6 Integrated Block for PCI Express

1.5

Component Name: v6_pcie_v1_5

PCIe Device / Port Type

The Integrated Block for PCI Express allows selection of the Device / Port Type

Device / Port Type: PCI Express Endpoint device

Number of Lanes

The Integrated Block for PCI Express requires that an initial lane width be selected. Wider lane width cores can train down to smaller lane widths if attached to a smaller lane width device. Select only the lane width that is necessary for the design.

Lane Width: X4

Link Speed

The Integrated Block for PCI Express allows selection of the Maximum Link Speed support

○ 2.5 GT/s

● 5.0 GT/s

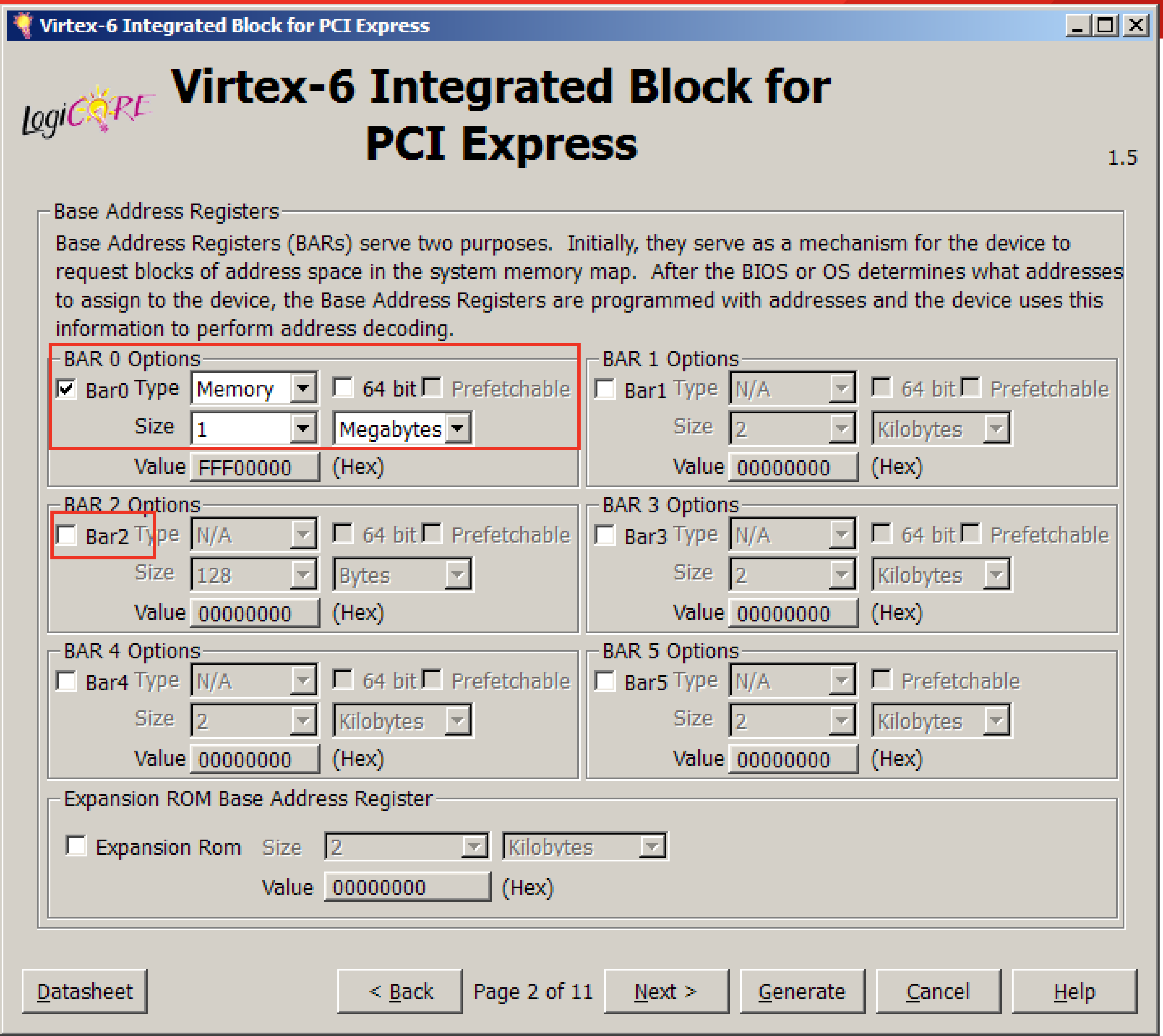
Interface Frequency

The Integrated Block for PCI Express allows selection of the interface clock (trn_clk) frequency. The frequency selection enables maximum achievable data throughput for the selected number of lanes and link speed. Choice of non-default option results in interface being overclocked with no overall effect on data throughput, and depends on user application functional requirements, timing closure and power considerations. Xilinx recommends that the default frequency value be used where possible..

Frequency (MHz): 250 default

- Set the lane Width to X4
- Set the Link Speed to 5.0 GT/s
- Click Next

Generate PCIe Core



Virtex-6 Integrated Block for PCI Express

LogiCORE

Virtex-6 Integrated Block for PCI Express

1.5

Base Address Registers

Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.

BAR 0 Options
☑ Bar0 Type Memory □ 64 bit □ Prefetchable
Size 1 Megabytes
Value FFF00000 (Hex)

BAR 1 Options
□ Bar1 Type N/A □ 64 bit □ Prefetchable
Size 2 Kilobytes
Value 00000000 (Hex)

BAR 2 Options
□ Bar2 Type N/A □ 64 bit □ Prefetchable
Size 128 Bytes
Value 00000000 (Hex)

BAR 3 Options
□ Bar3 Type N/A □ 64 bit □ Prefetchable
Size 2 Kilobytes
Value 00000000 (Hex)

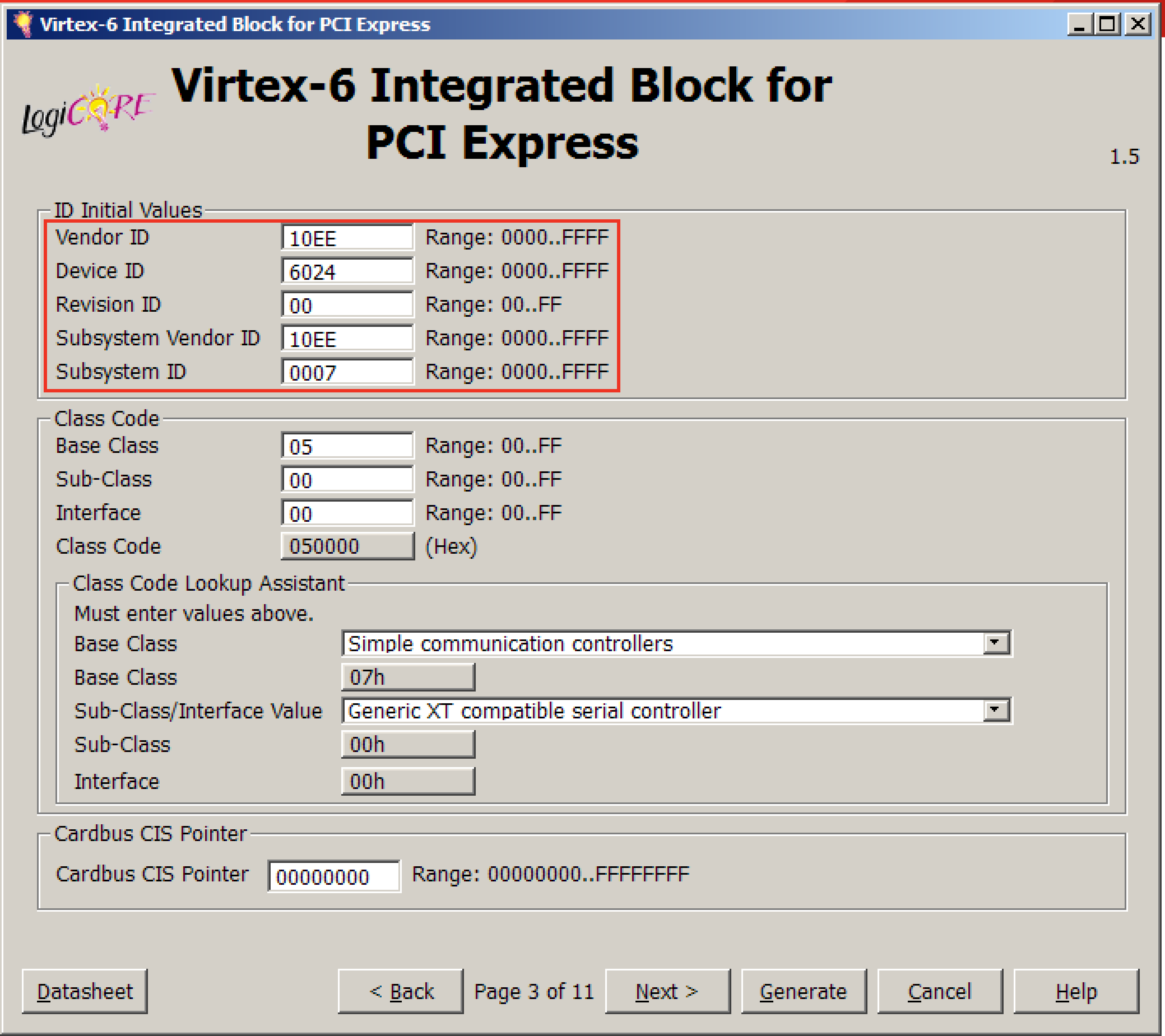
BAR 4 Options
□ Bar4 Type N/A □ 64 bit □ Prefetchable
Size 2 Kilobytes
Value 00000000 (Hex)

BAR 5 Options
□ Bar5 Type N/A □ Prefetchable
Size 2 Kilobytes
Value 00000000 (Hex)

Expansion ROM Base Address Register
□ Expansion Rom Size 2 Kilobytes
Value 00000000 (Hex)

- **BAR 0**
  - Set to 1 Megabytes
- **BAR 2**
  - Deselect BAR 2
- **Click Next**

Generate PCIe Core



Virtex-6 Integrated Block for PCI Express
LogiCORE
Virtex-6 Integrated Block for PCI Express
1.5

ID Initial Values

Vendor ID	10EE	Range: 0000..FFFF
Device ID	6024	Range: 0000..FFFF
Revision ID	00	Range: 00..FF
Subsystem Vendor ID	10EE	Range: 0000..FFFF
Subsystem ID	0007	Range: 0000..FFFF

Class Code

Base Class	05	Range: 00..FF
Sub-Class	00	Range: 00..FF
Interface	00	Range: 00..FF
Class Code	050000	(Hex)

Class Code Lookup Assistant

Must enter values above.

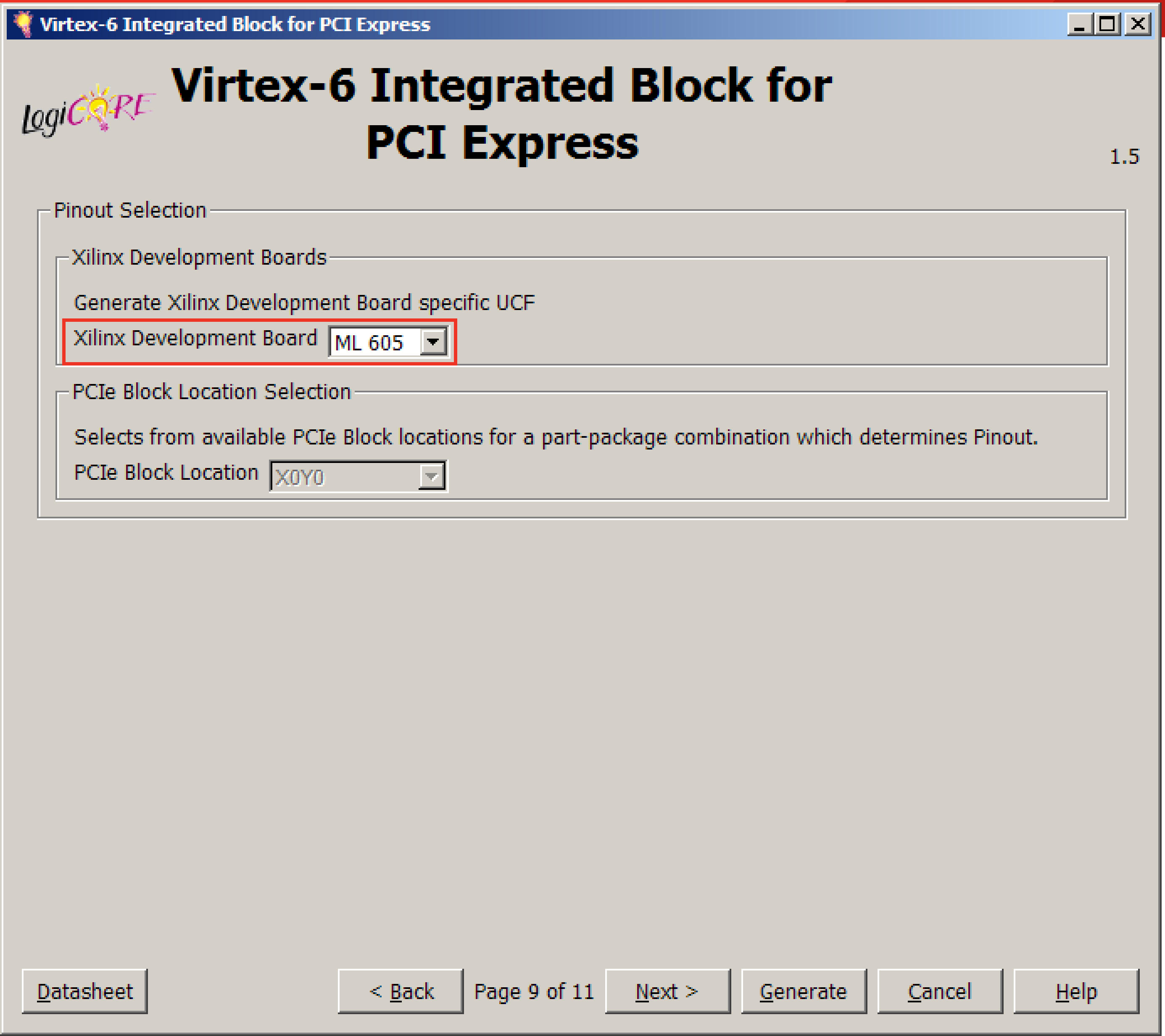
Base Class	Simple communication controllers
Base Class	07h
Sub-Class/Interface Value	Generic XT compatible serial controller
Sub-Class	00h
Interface	00h

Cardbus CIS Pointer

Cardbus CIS Pointer 00000000 Range: 00000000..FFFFFFFF

- **Note ID Initial Values**
  - Vendor ID = **10EE**
  - Device ID = **6024**
  - Revision ID = **00**
  - Subsystem Vendor ID = **10EE**
  - Subsystem ID = **0007**
- **Click Next 6 times**

Generate PCIe Core



Virtex-6 Integrated Block for PCI Express
LogiCORE
Virtex-6 Integrated Block for PCI Express
1.5

Pinout Selection

Xilinx Development Boards

Generate Xilinx Development Board specific UCF

Xilinx Development Board: ML 605

PCIe Block Location Selection

Selects from available PCIe Block locations for a part-package combination which determines Pinout.

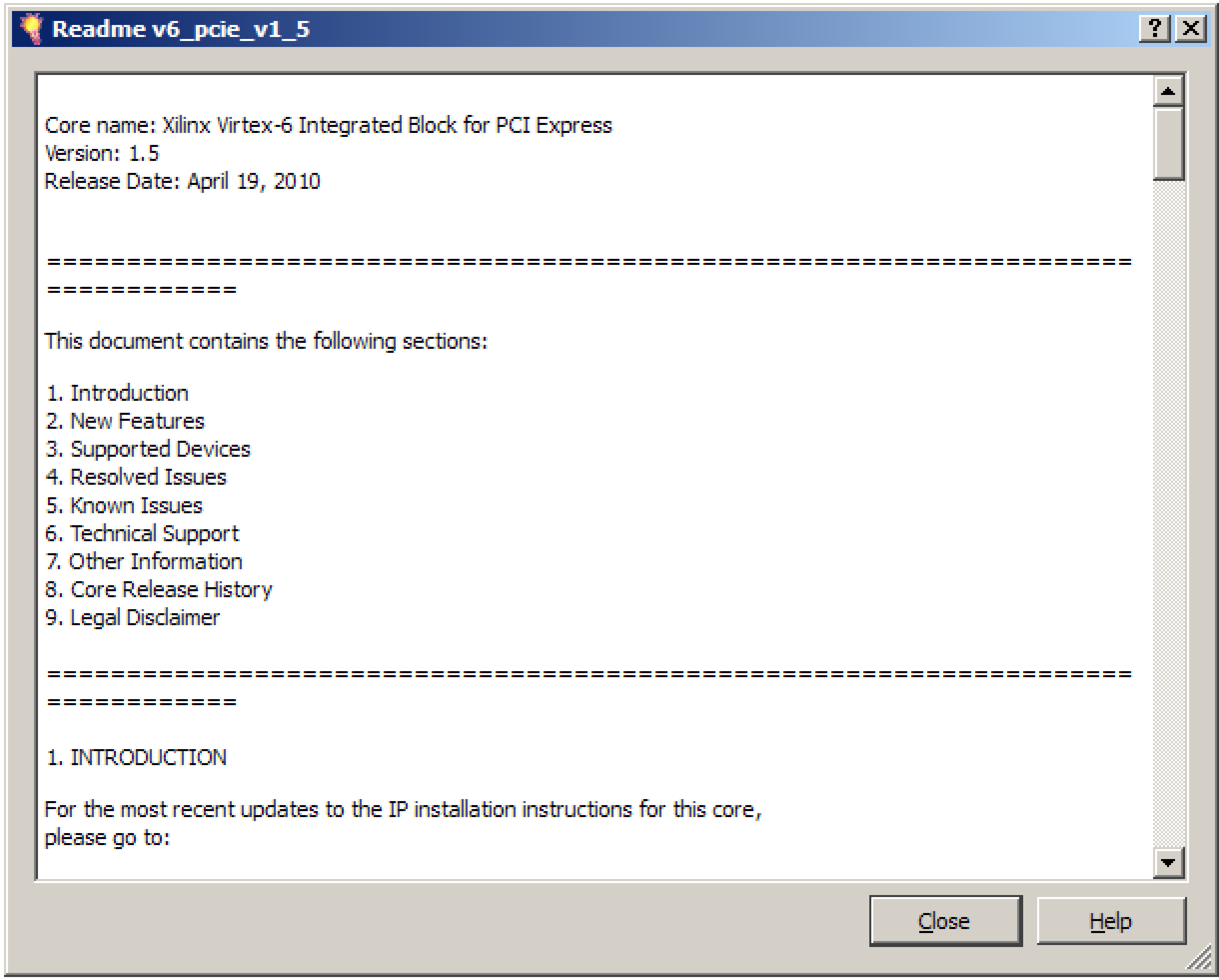
PCIe Block Location: X0Y0

Datasheet
< Back
Page 9 of 11
Next >
Generate
Cancel
Help

- **On Page 9**
  - Select ML605
- **Click Generate**

Generate PCIe Core

- **After the PCIe core finishes generating, click Close on the Readme File window**



Core name: Xilinx Virtex-6 Integrated Block for PCI Express
Version: 1.5
Release Date: April 19, 2010

```
========================================================================
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```

This document contains the following sections:

1. Introduction
2. New Features
3. Supported Devices
4. Resolved Issues
5. Known Issues
6. Technical Support
7. Other Information
8. Core Release History
9. Legal Disclaimer

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```

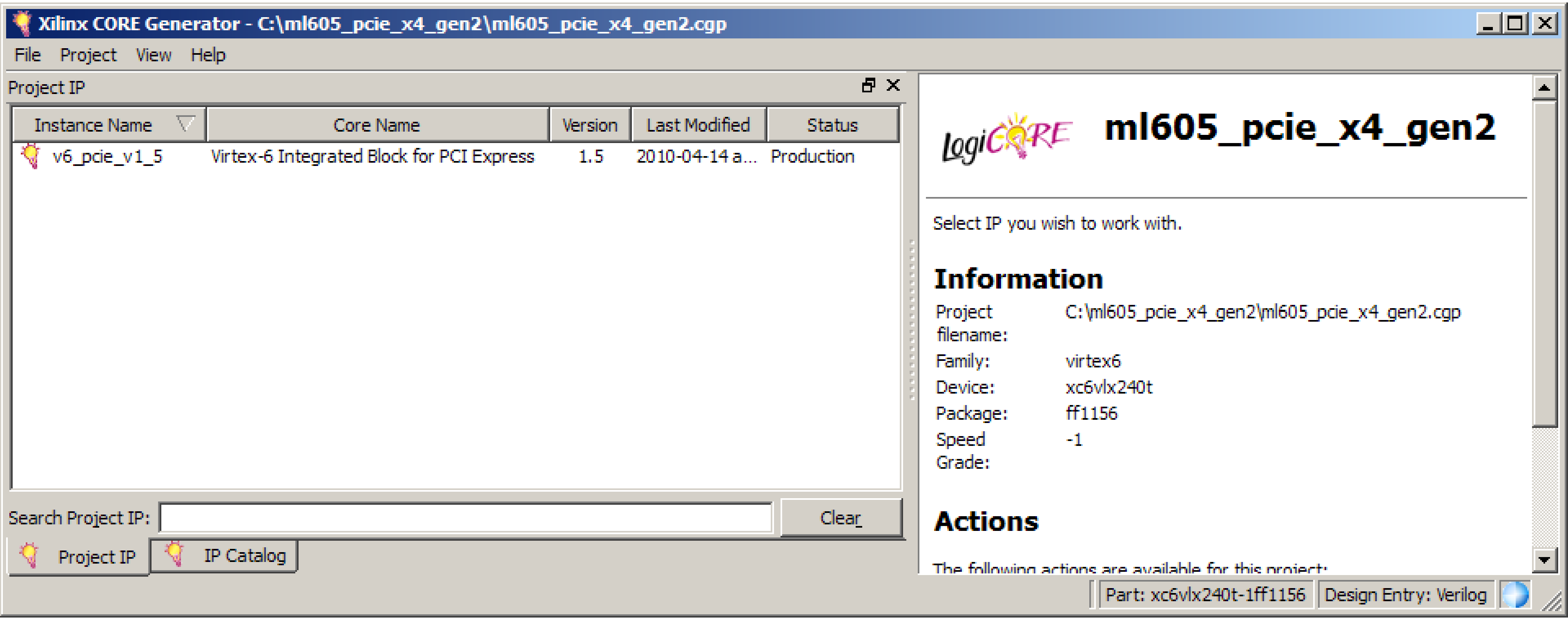
1. INTRODUCTION

For the most recent updates to the IP installation instructions for this core,
please go to:

Note: Presentation applies to the ML605

Generate PCIe Core

- The v6_pcie_v1_5 IP appears under the Project IP tab



Xilinx CORE Generator - C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp

Instance Name	Core Name	Version	Last Modified	Status
v6_pcie_v1_5	Virtex-6 Integrated Block for PCI Express	1.5	2010-04-14 a...	Production

ml605_pcie_x4_gen2

Select IP you wish to work with.

Information

Project filename:	C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp
Family:	virtex6
Device:	xc6vlx240t
Package:	ff1156
Speed Grade:	-1

Actions

The following actions are available for this project:

Part: xc6vlx240t-1ff1156

Design Entry: Verilog

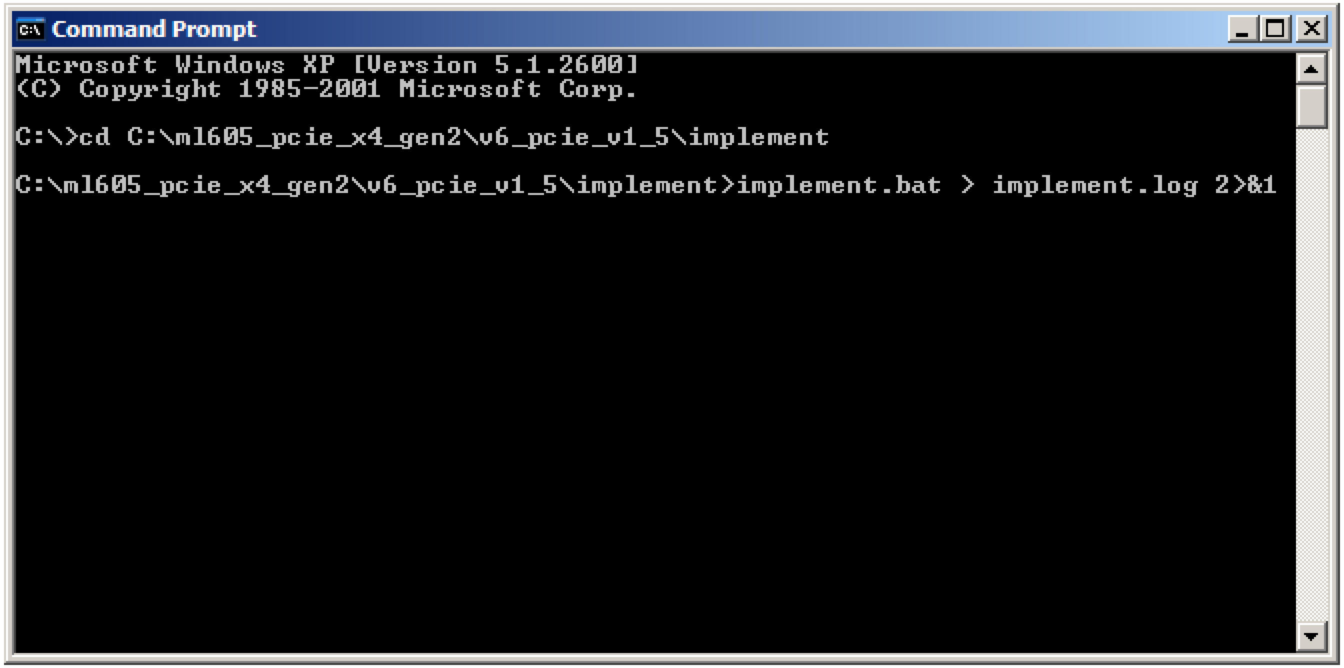
Note: Presentation applies to the ML605

Compile PCIe Core

- Type these commands in a windows command shell:

  cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement

  implement.bat > implement.log 2>&1



```
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement

C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement>implement.bat > implement.log 2>&1
```

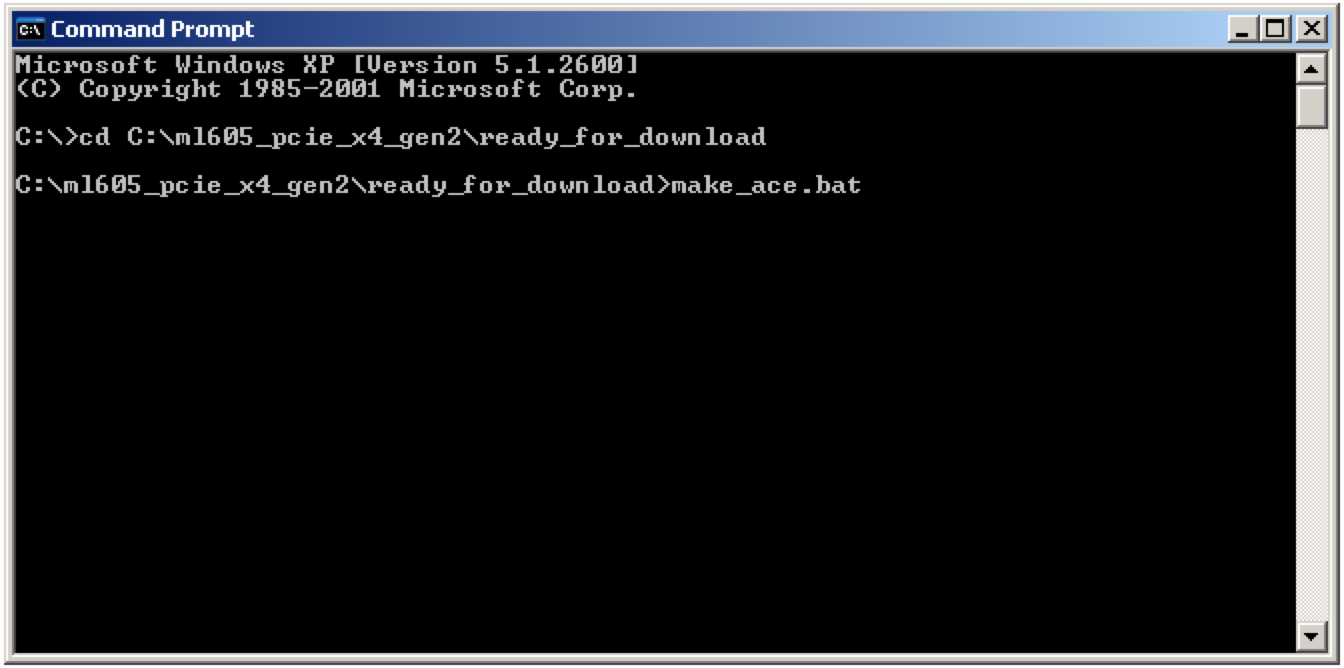
Note: Presentation applies to the ML605

Create PCIe ACE File (Optional)

- Type these commands in a windows command shell:

cd C:\ml605_pcie_x4_gen2\ready_for_download

make_ace.bat



```
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

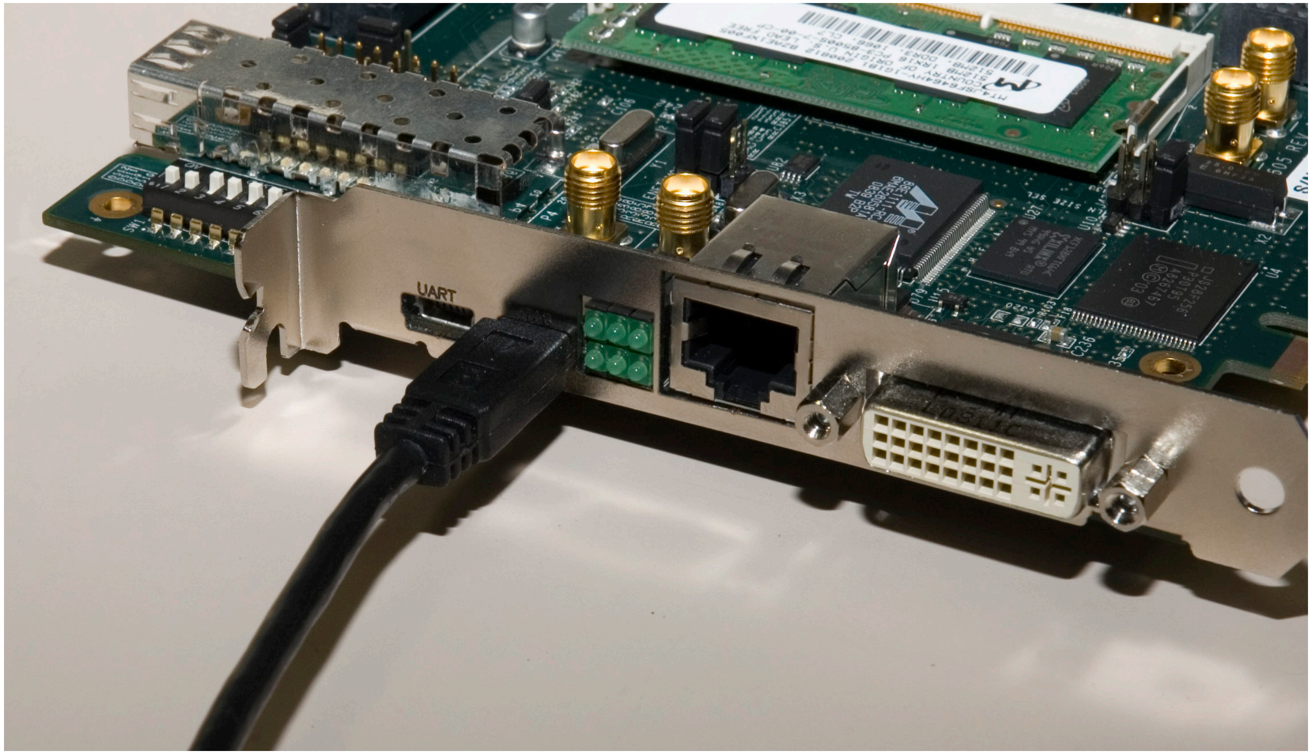
C:\>cd C:\ml605_pcie_x4_gen2\ready_for_download

C:\ml605_pcie_x4_gen2\ready_for_download>make_ace.bat
```

Note: The make_ace.bat file is included with RDF0009

Program Platform Flash with PCIe Design

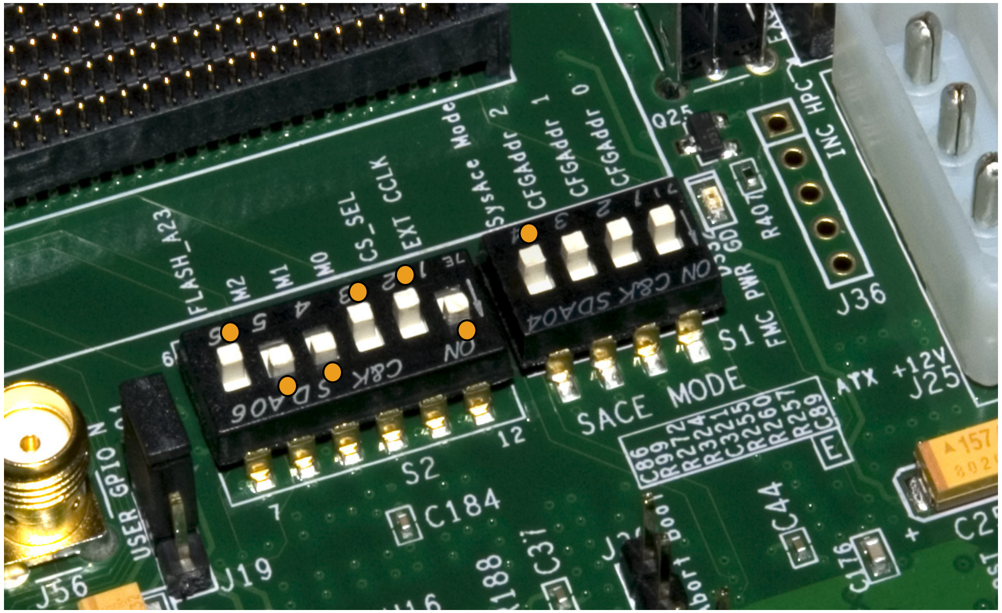
- **Power on the ML605**
- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
  - – Connect this cable to your PC



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Set S2 to 011001 (1 = on, Position 6 → Position 1)**
  - This selects Slave SelectMAP (Positions 5, 4, and 3), Platform Flash (2) and EXT CCLK (1, for PCIe compliance)
- **Set S1 to 0XXX (X = Don’t care, Position 4 → Position 1)**
  - This disables the Compact Flash

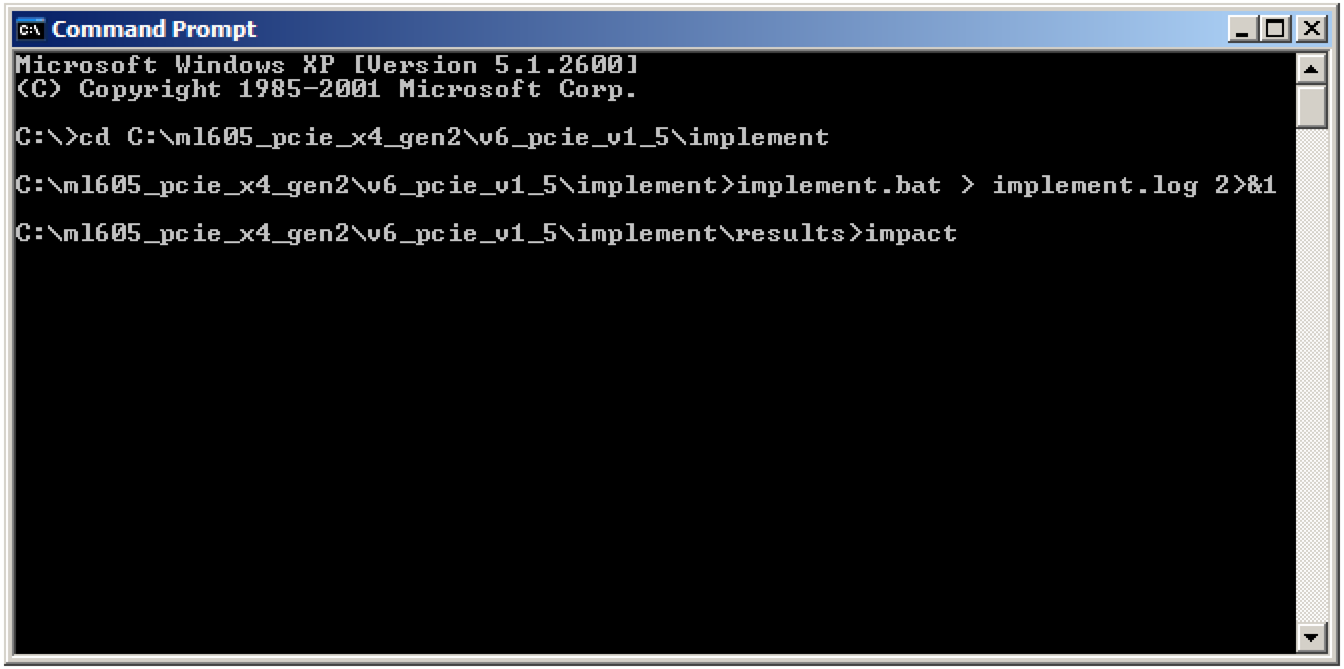


Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Run iMPACT:**

  impact



```
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement

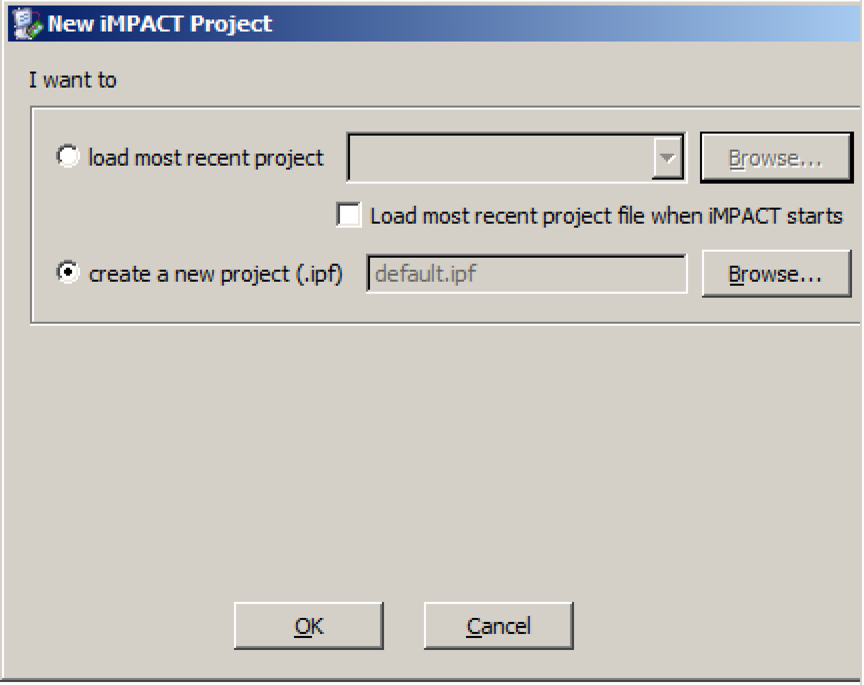
C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement>implement.bat > implement.log 2>&1

C:\ml605_pcie_x4_gen2\v6_pcie_v1_5\implement\results>impact
```

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Select**
  - Create a new project
  - Prepare a PROM File



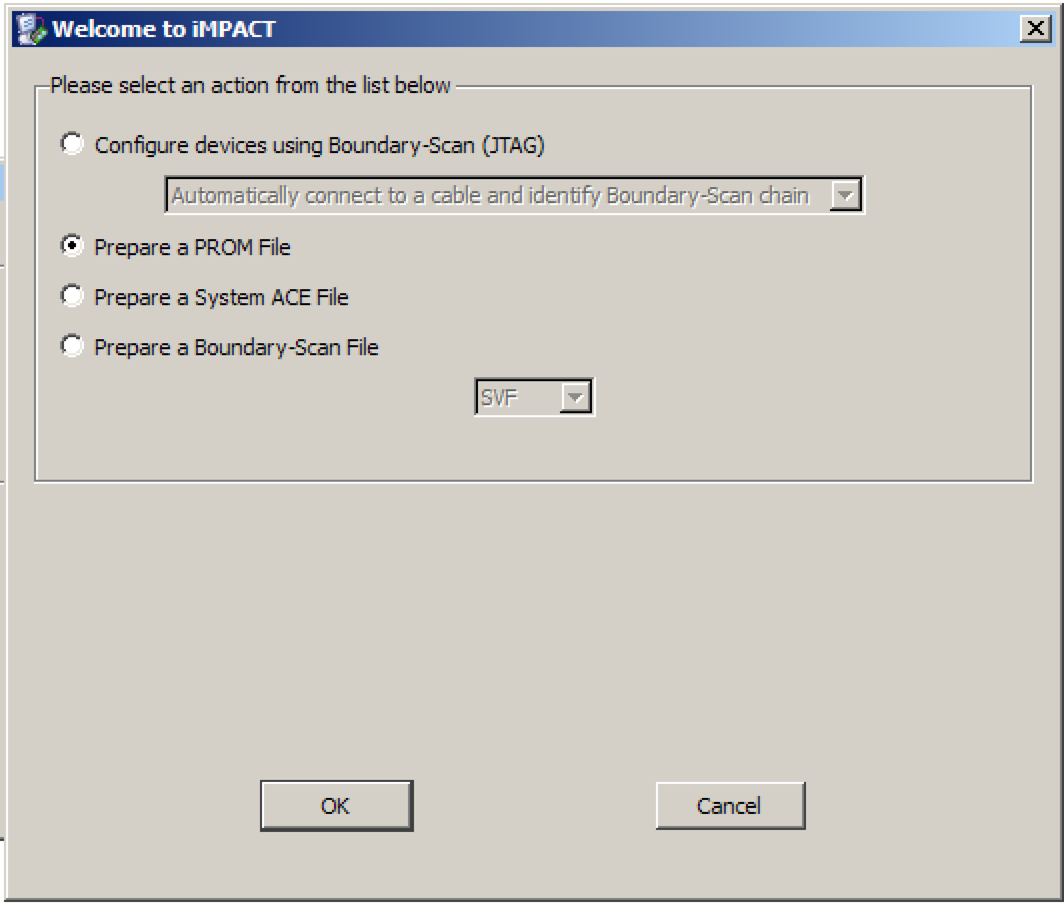
New iMPACT Project

I want to

○ load most recent project

□ Load most recent project file when iMPACT starts

● create a new project (.ipf) default.ipf



Welcome to iMPACT

Please select an action from the list below

○ Configure devices using Boundary-Scan (JTAG)

Automatically connect to a cable and identify Boundary-Scan chain

● Prepare a PROM File

○ Prepare a System ACE File

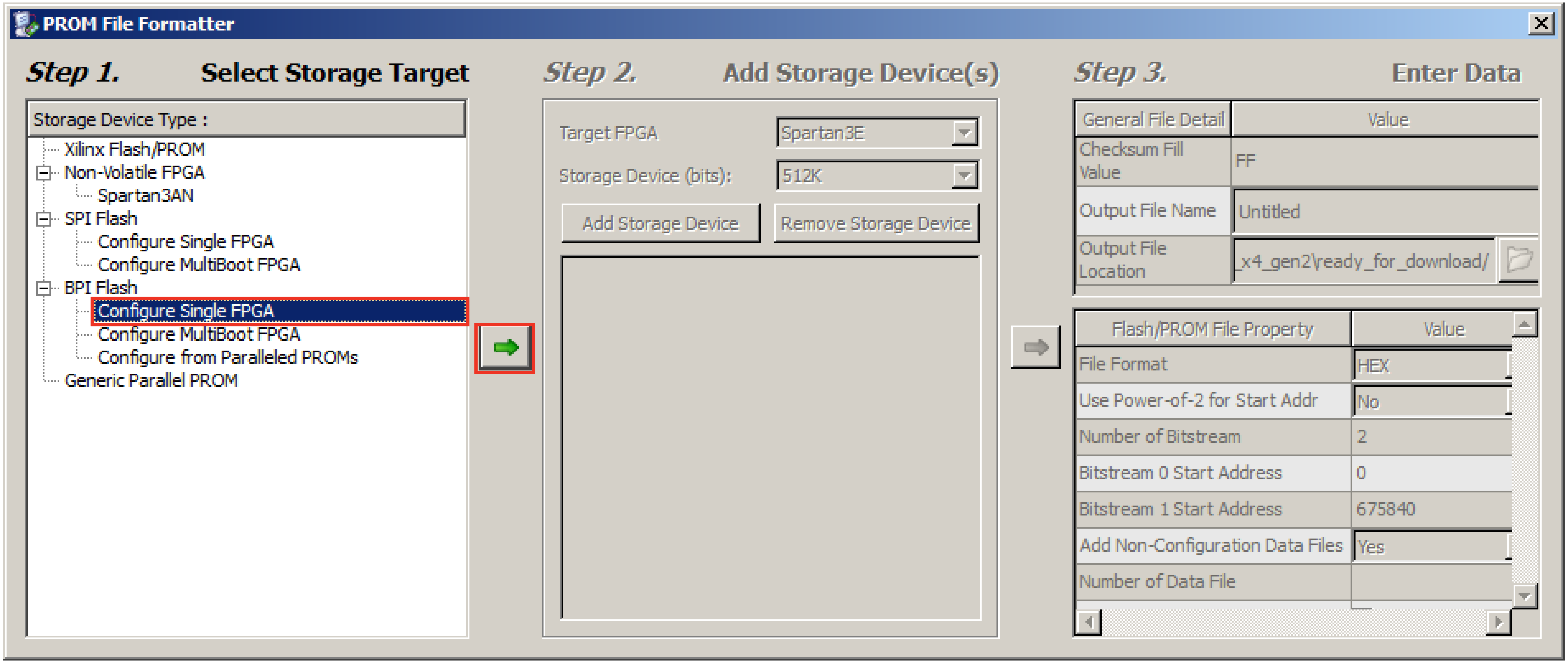
○ Prepare a Boundary-Scan File

SVF

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **To generate a PROM file for the XCF128X Platform Flash, select:**
  - BPI – Configure Single FPGA



PROM File Formatter

Step 1. Select Storage Target

Storage Device Type :

- Xilinx Flash/PROM
- Non-Volatile FPGA
  - Spartan3AN
- SPI Flash
  - Configure Single FPGA
  - Configure MultiBoot FPGA
- BPI Flash
  - Configure Single FPGA
  - Configure MultiBoot FPGA
  - Configure from Paralleled PROMs
- Generic Parallel PROM

Step 2. Add Storage Device(s)

Target FPGA: Spartan3E

Storage Device (bits): 512K

Step 3. Enter Data

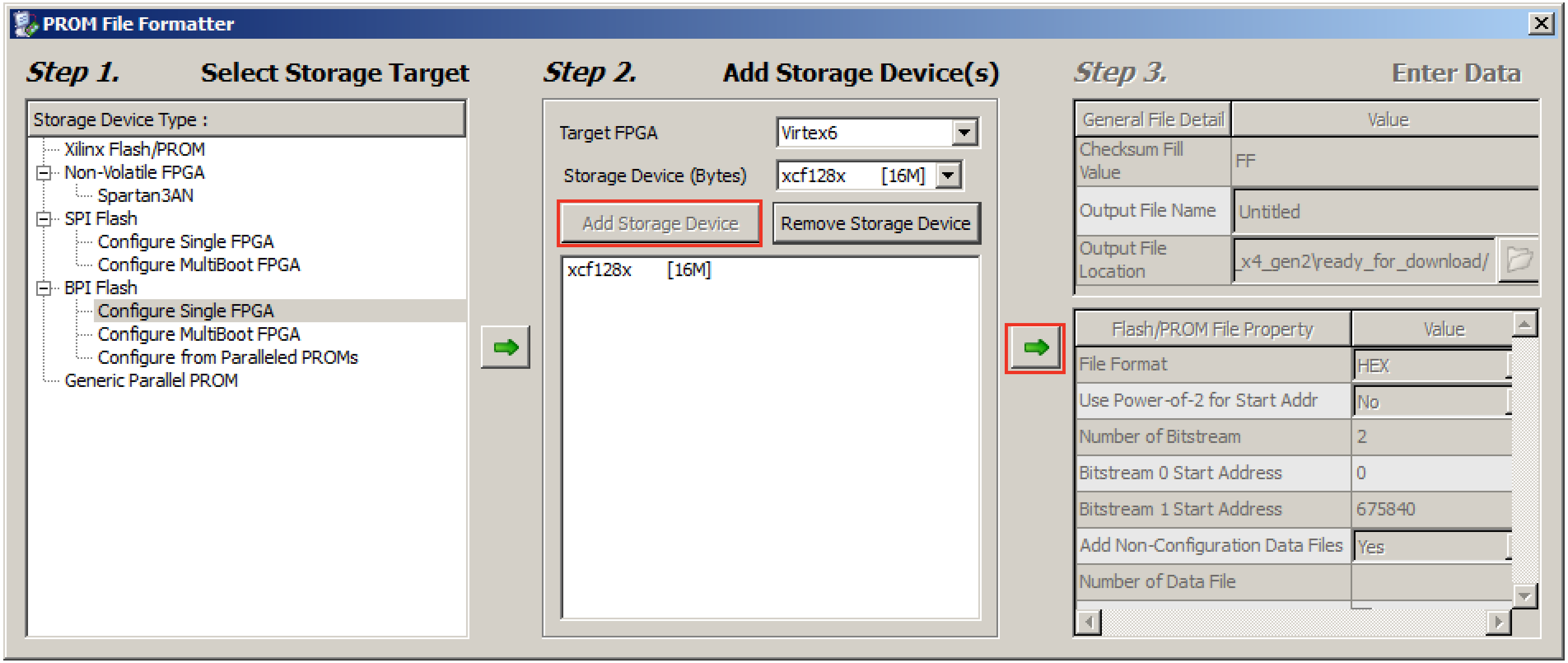
General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	x4_gen2\ready_for_download/

Flash/PROM File Property	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Add xcf128x



PROM File Formatter

Step 1. Select Storage Target

Storage Device Type :

- Xilinx Flash/PROM
- Non-Volatile FPGA
  - Spartan3AN
- SPI Flash
  - Configure Single FPGA
  - Configure MultiBoot FPGA
- BPI Flash
  - Configure Single FPGA
  - Configure MultiBoot FPGA
  - Configure from Paralleled PROMs
- Generic Parallel PROM

Step 2. Add Storage Device(s)

Target FPGA: Virtex6

Storage Device (Bytes): xcf128x [16M]

xcf128x [16M]

Step 3. Enter Data

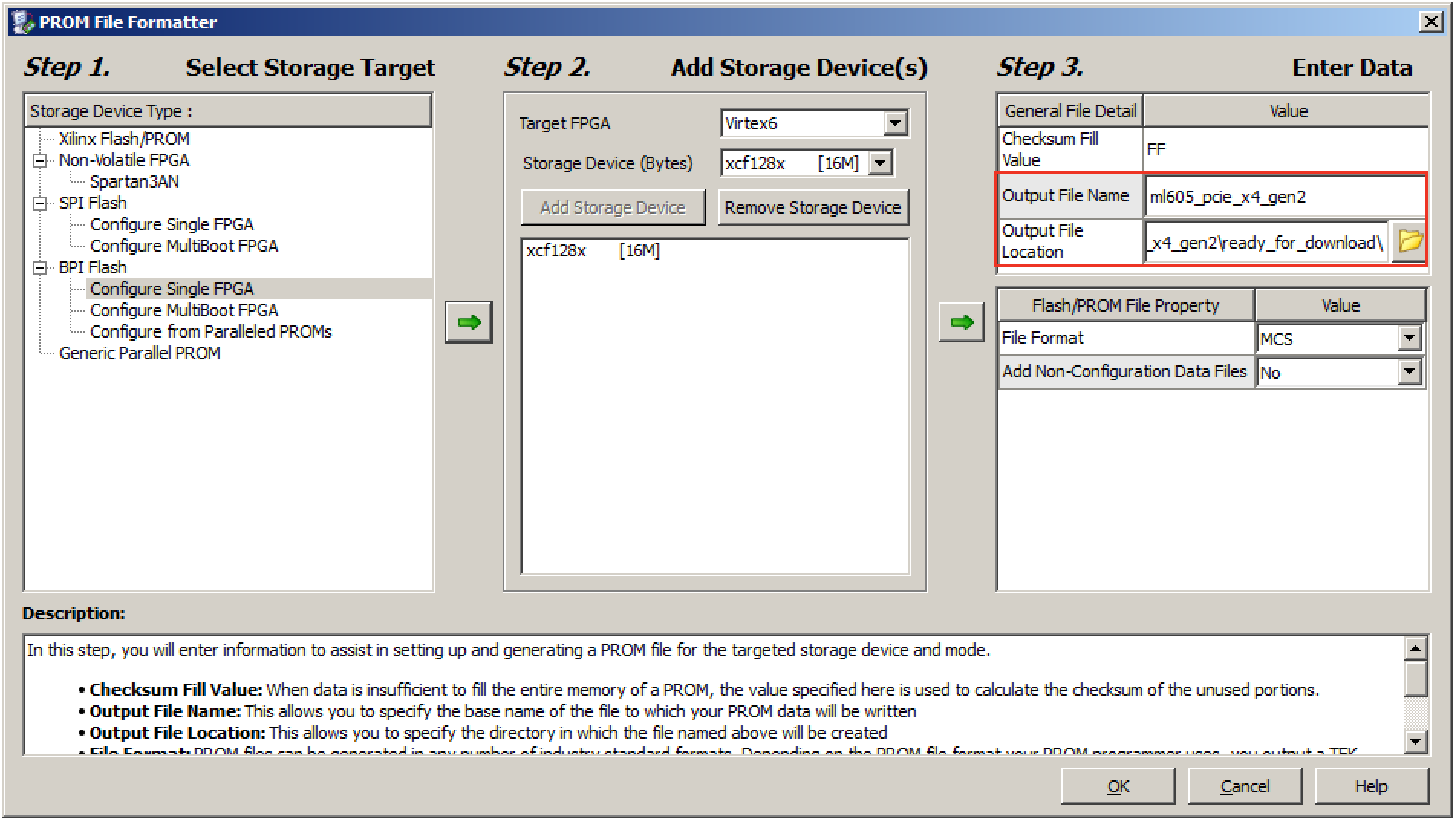
General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	x4_gen2\ready_for_download/

Flash/PROM File Property	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Set file name and location as desired and click OK



Step 1. Select Storage Target

Step 2. Add Storage Device(s)

Target FPGA: Virtex6

Storage Device (Bytes): xcf128x [16M]

xcf128x [16M]

Step 3. Enter Data

General File Detail	Value
Checksum Fill Value	FF
Output File Name	ml605_pcie_x4_gen2
Output File Location	_x4_gen2\ready_for_download\

Flash/PROM File Property	Value
File Format	MCS
Add Non-Configuration Data Files	No

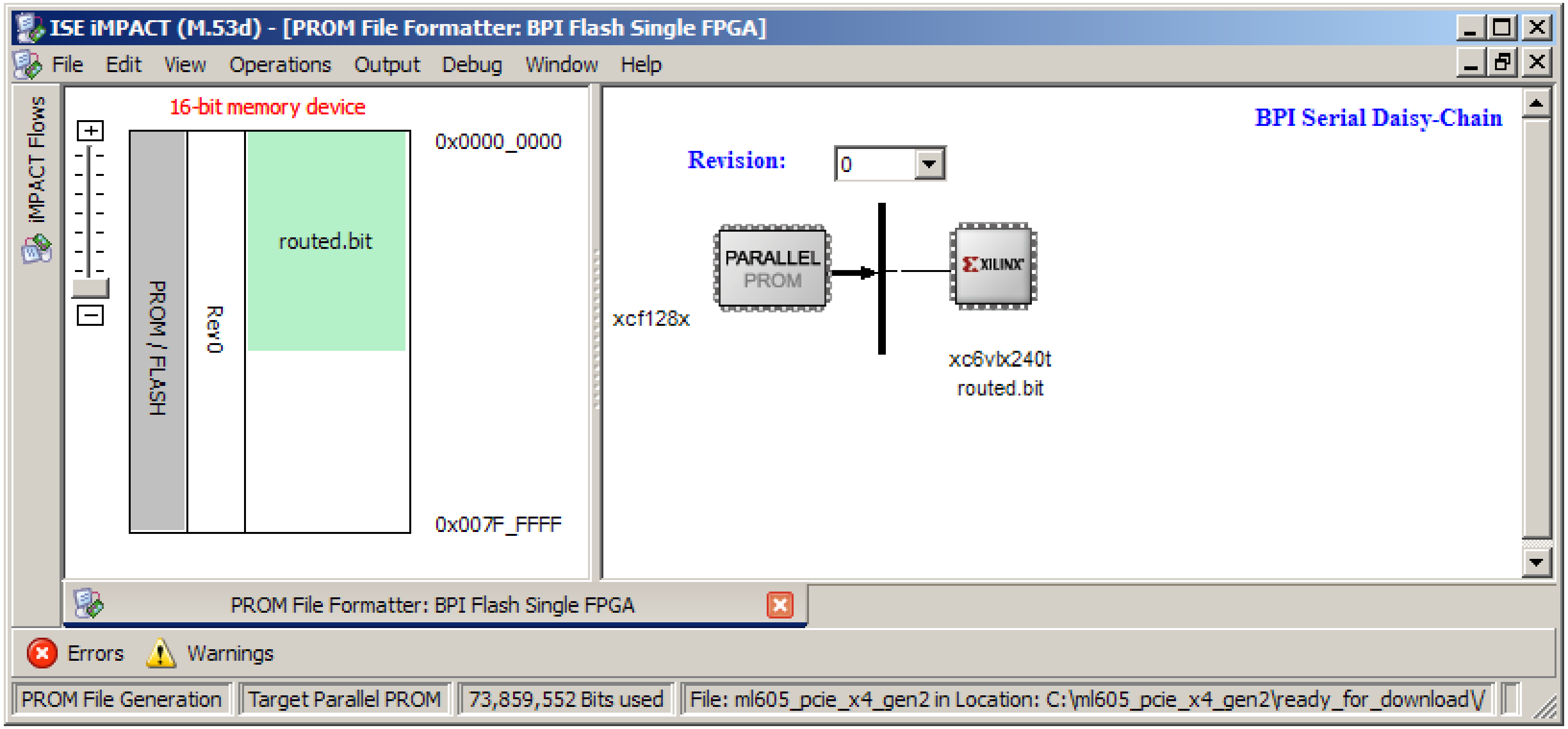
Description:

In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.

- **Checksum Fill Value:** When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
- **Output File Name:** This allows you to specify the base name of the file to which your PROM data will be written
- **Output File Location:** This allows you to specify the directory in which the file named above will be created
- **File Format:** PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a TEK

Program Platform Flash with PCIe Design

- Add routed.bit from the <design path>\v6_pcie_v1_5\implement\results



ISE iMPACT (M.53d) - [PROM File Formatter: BPI Flash Single FPGA]

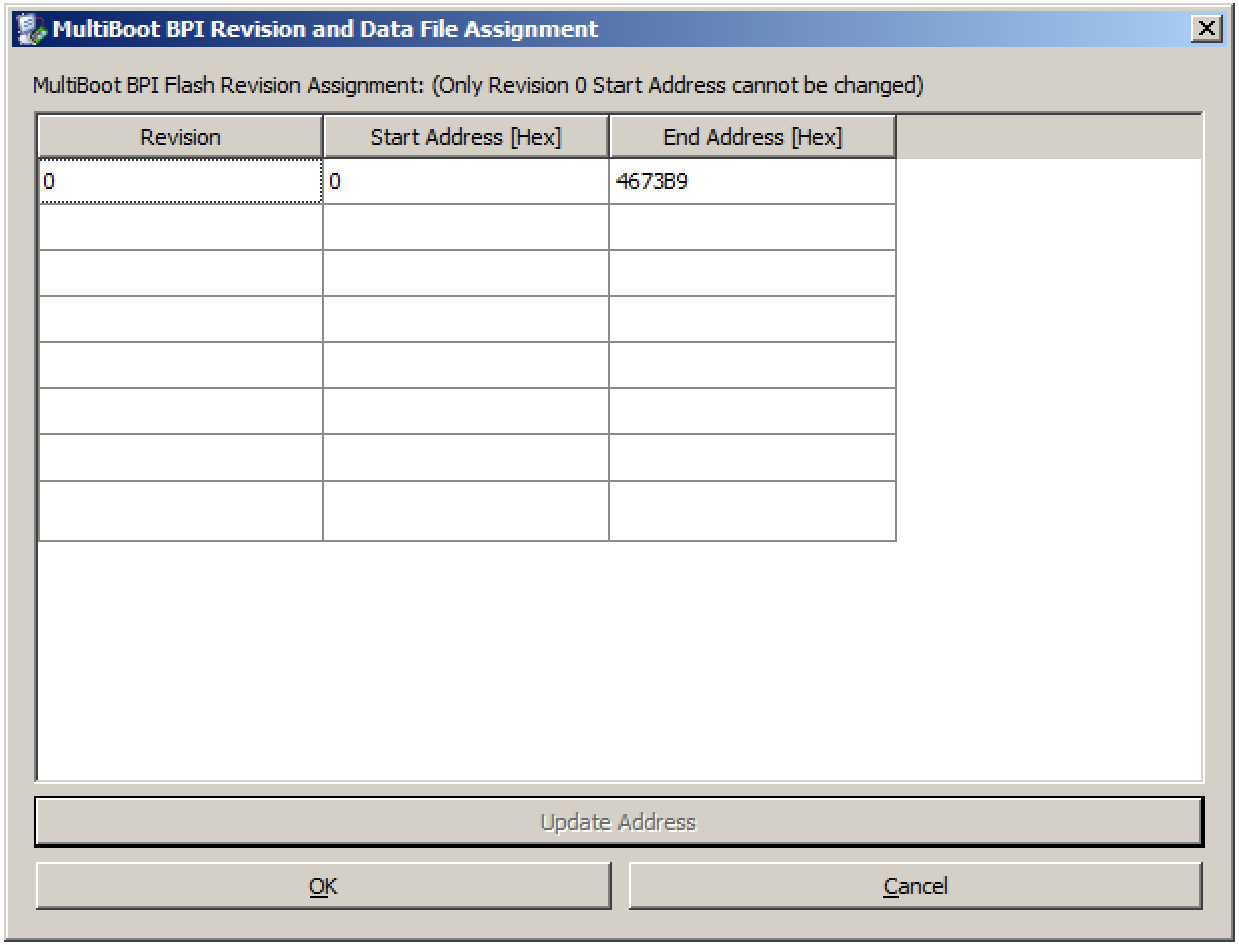
Revision: 0

PROM File Generation | Target Parallel PROM | 73,859,552 Bits used | File: ml605_pcie_x4_gen2 in Location: C:\ml605_pcie_x4_gen2\ready_for_download\

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Click OK on this dialog**



MultiBoot BPI Revision and Data File Assignment

MultiBoot BPI Flash Revision Assignment: (Only Revision 0 Start Address cannot be changed)

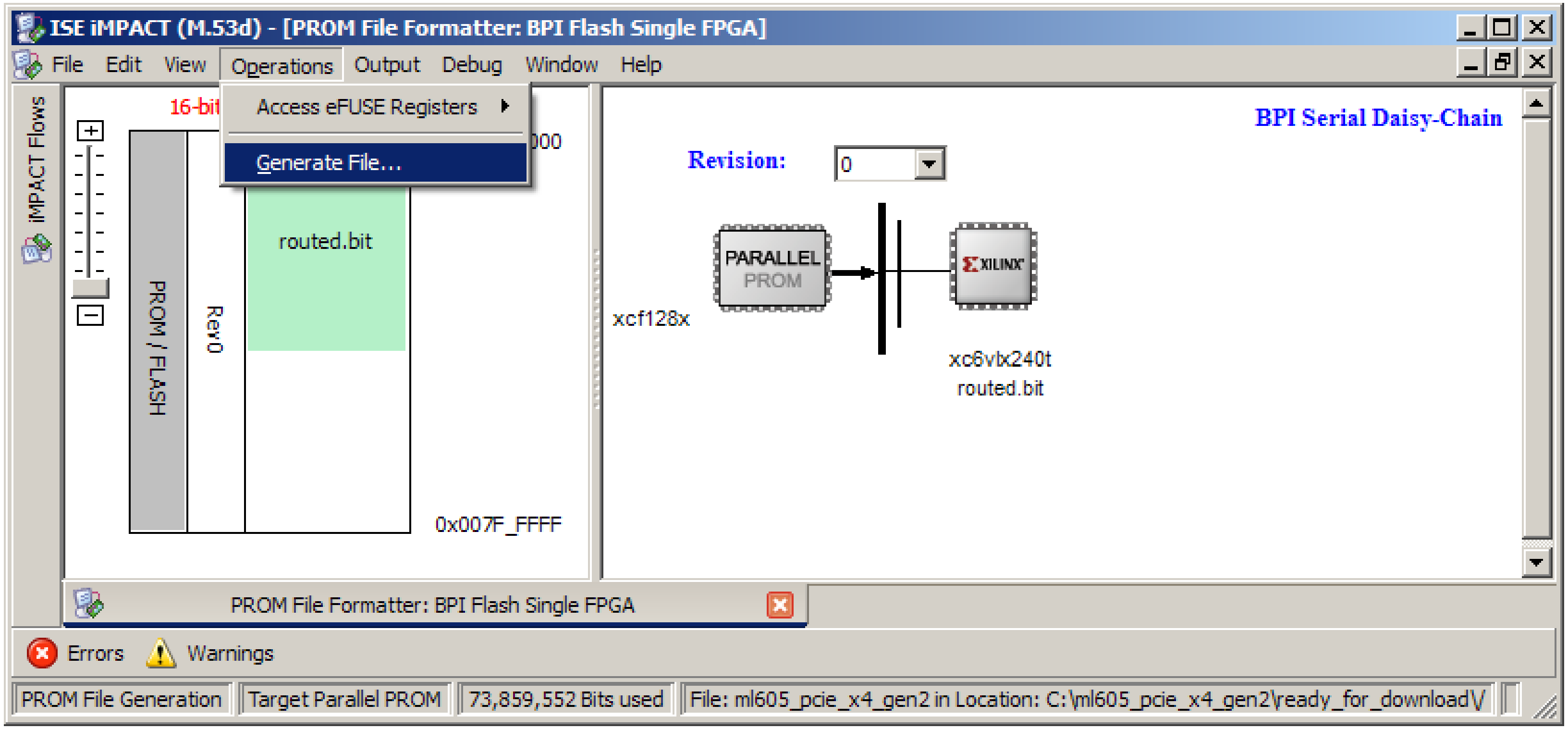
Revision	Start Address [Hex]	End Address [Hex]
0	0	4673B9

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **From the iMPACT menu, select**

  Operations → Generate File…

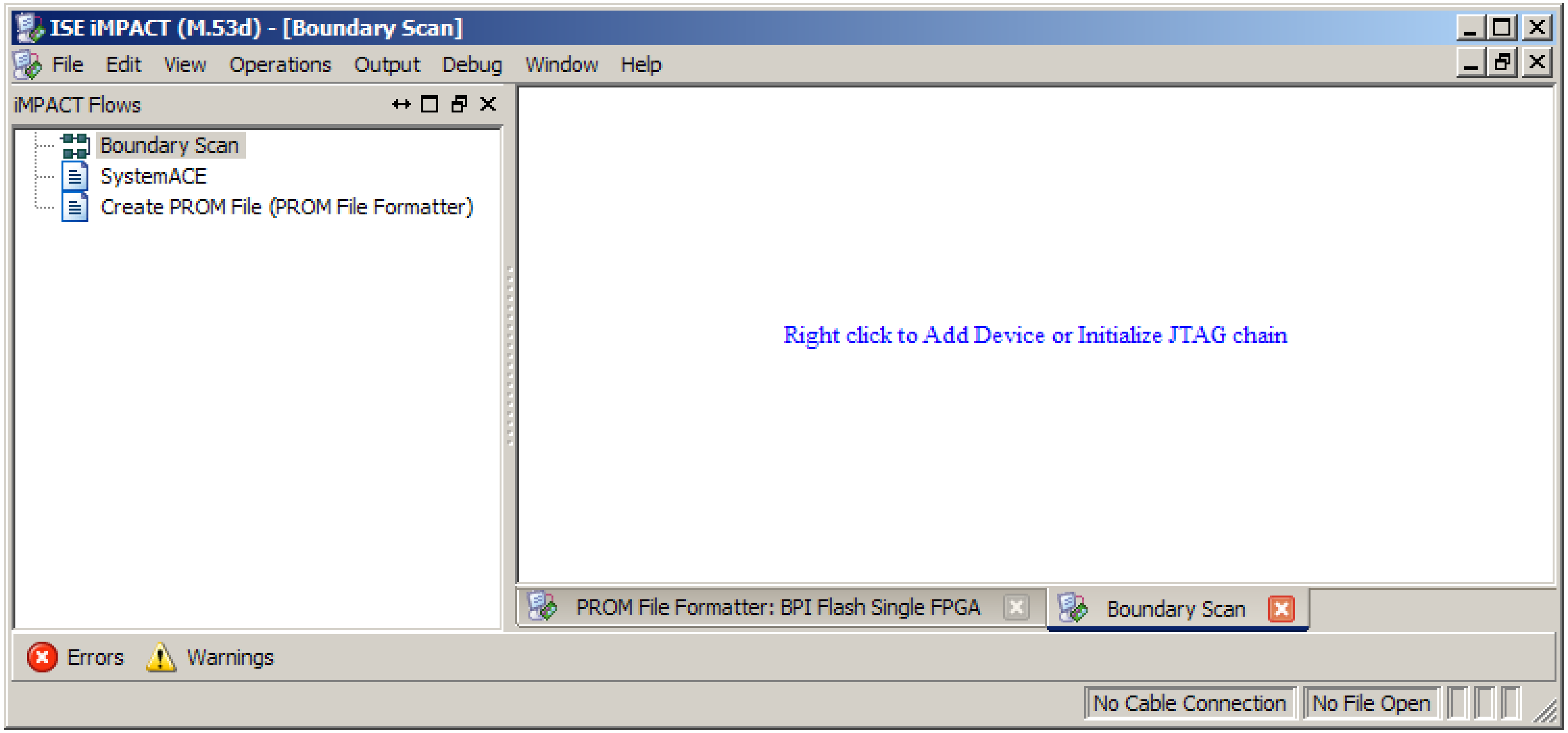


PROM File Generation | Target Parallel PROM | 73,859,552 Bits used | File: ml605_pcie_x4_gen2 in Location: C:\ml605_pcie_x4_gen2\ready_for_download\

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **After generation completes, under the iMPACT Flows, double click on Boundary Scan**



ISE iMPACT (M.53d) - [Boundary Scan]

Right click to Add Device or Initialize JTAG chain

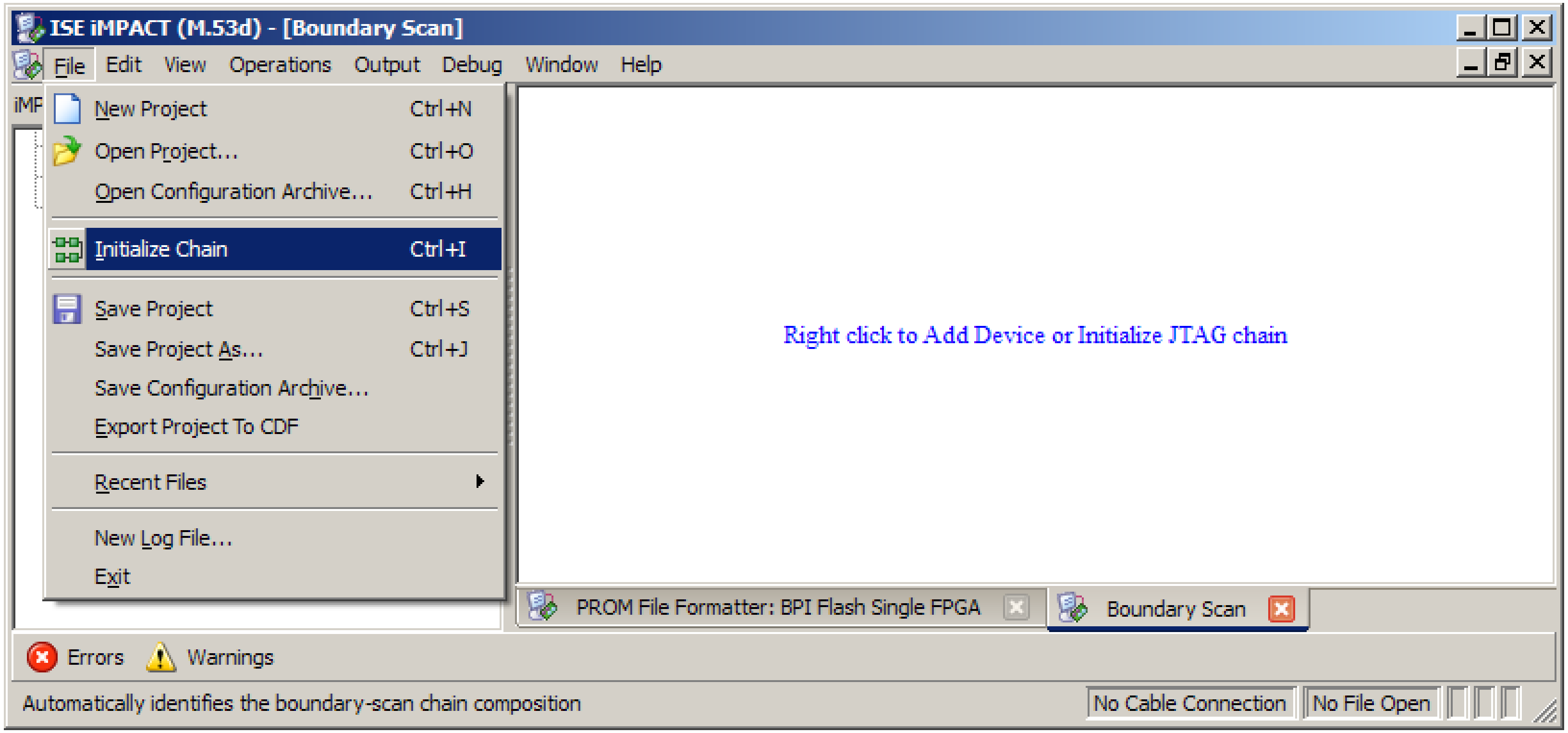
No Cable Connection | No File Open

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **From the iMPACT menu, select**

  File → Initialize Chain



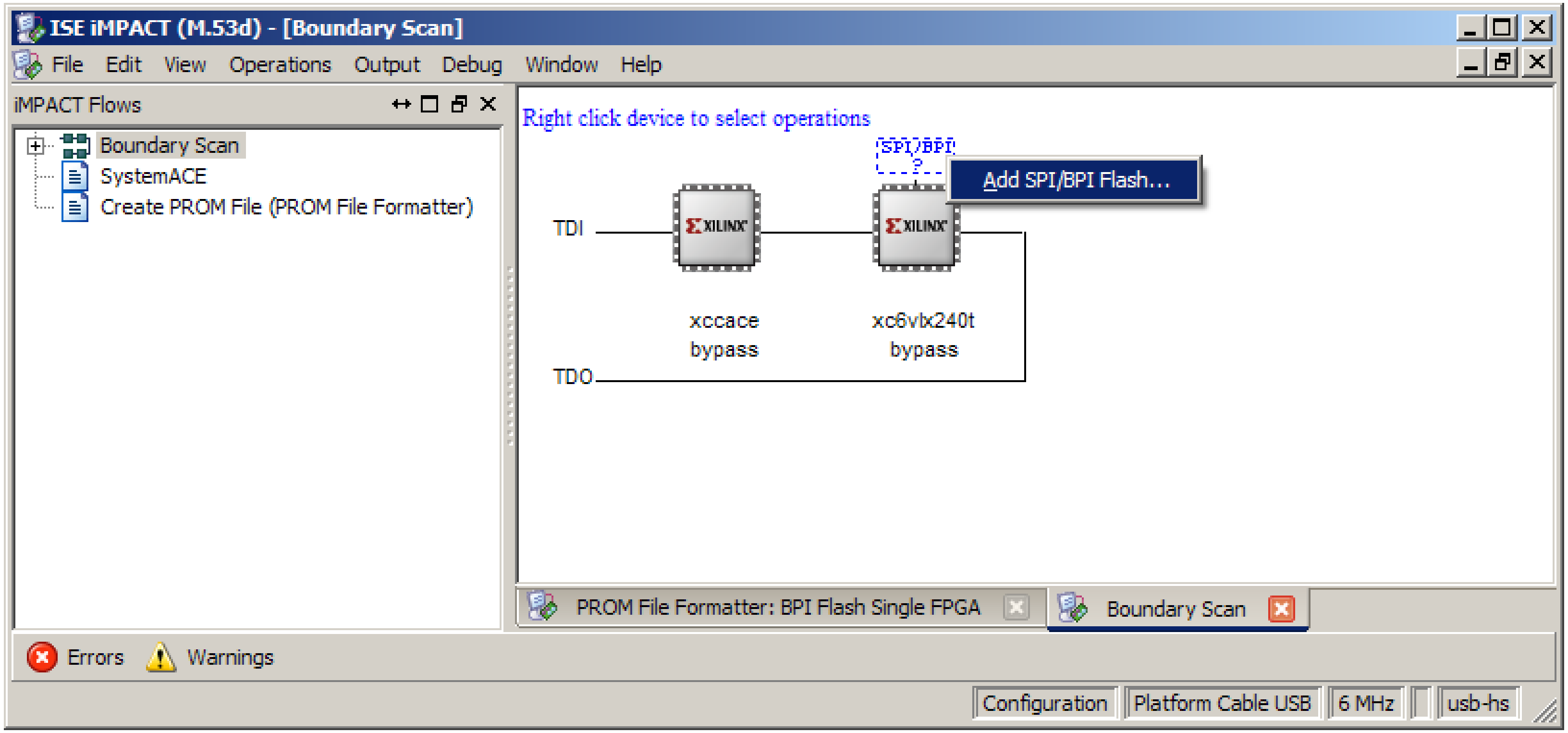
Right click to Add Device or Initialize JTAG chain

Automatically identifies the boundary-scan chain composition

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Right click on the SPI/BPI ? and select Add SPI/BPI Flash…
  – Add <design path>\ready_for_download\ml605_pcie_x4_gen2.mcs

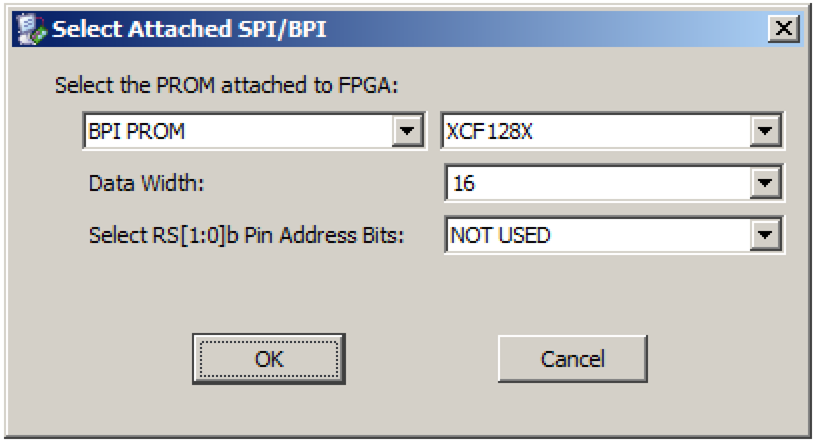


Right click device to select operations

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Click OK for this dialog



Select Attached SPI/BPI

Select the PROM attached to FPGA:

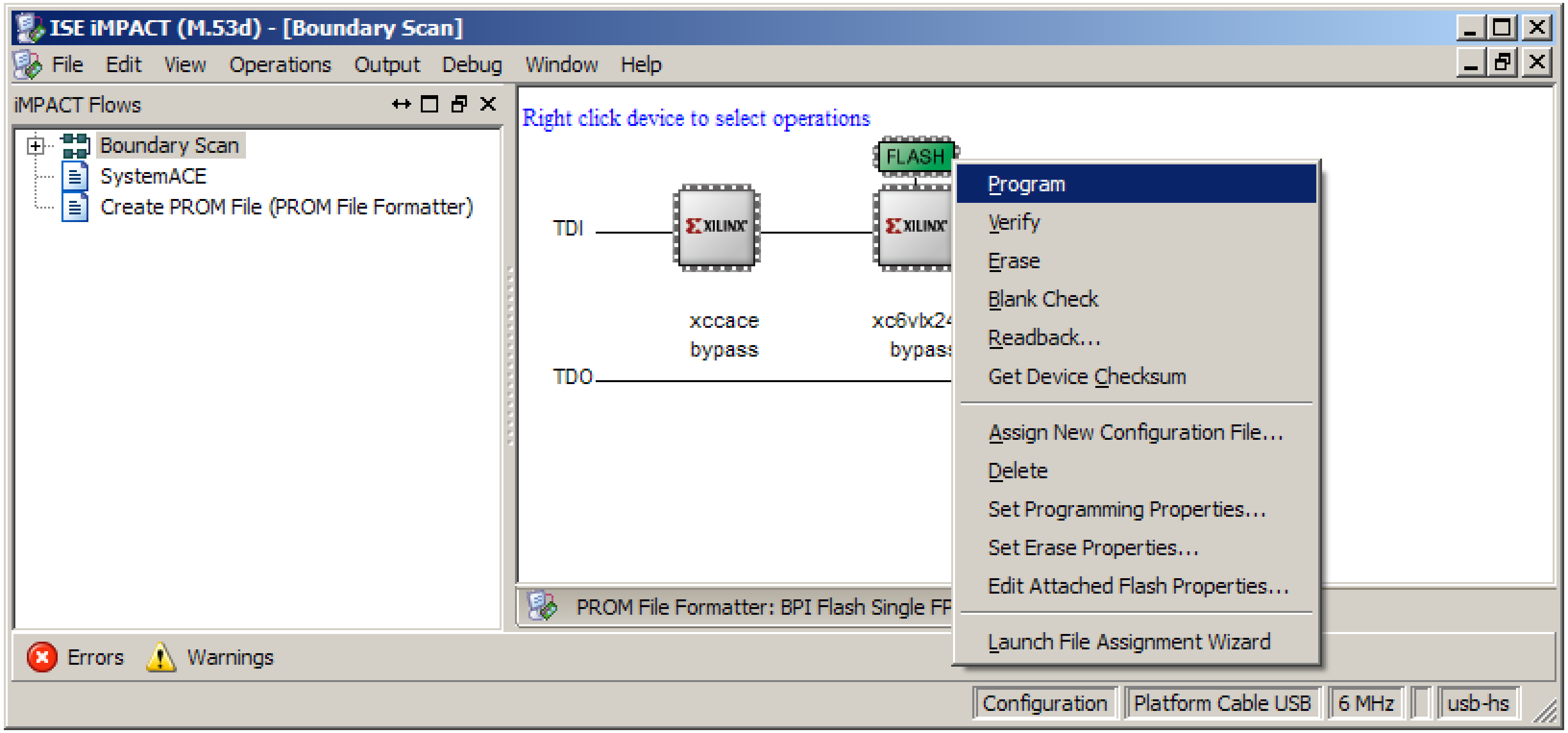
BPI PROM — XCF128X

Data Width: 16

Select RS[1:0]b Pin Address Bits: NOT USED

Program Platform Flash with PCIe Design

- **Right click on the Flash and select Program**
  – Use default settings to Erase and Verify device

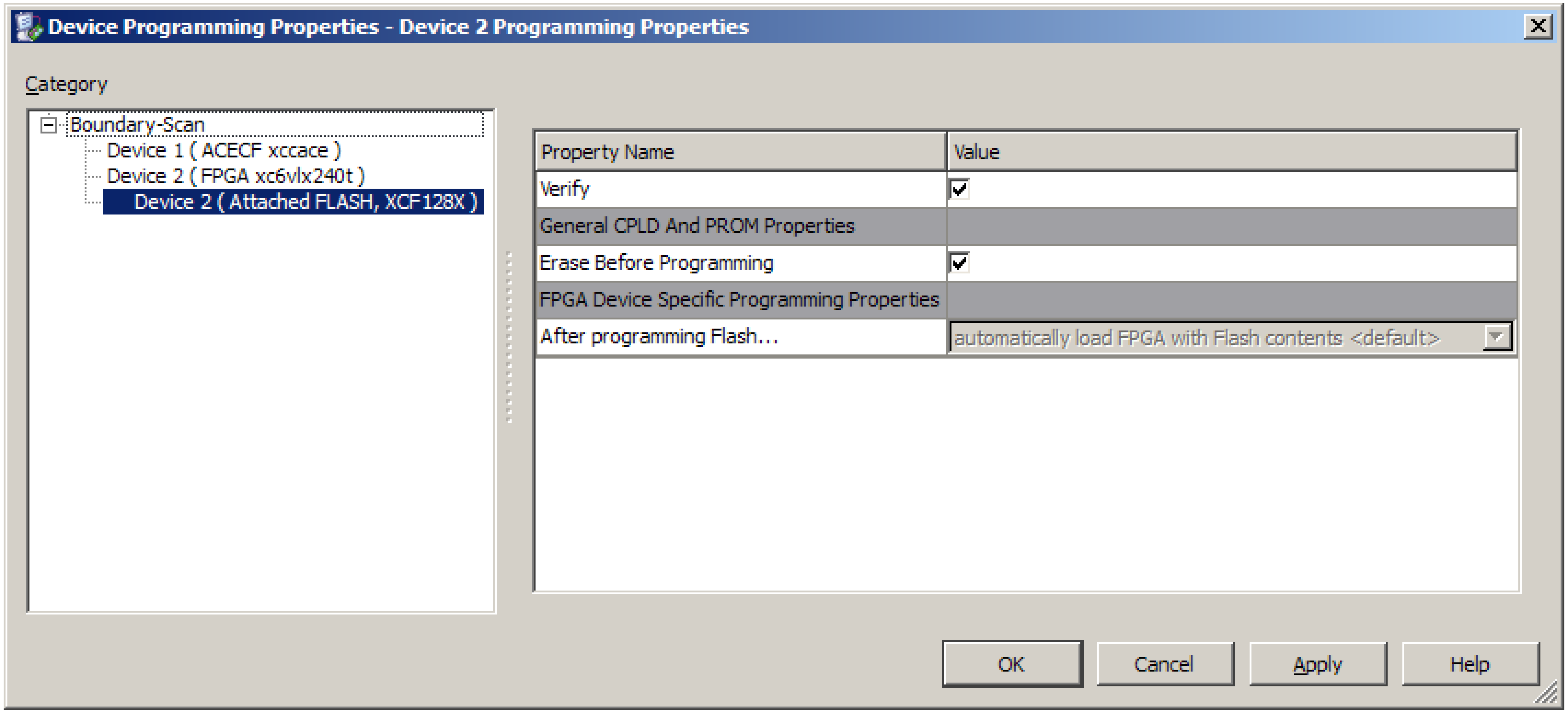


ISE iMPACT (M.53d) - [Boundary Scan]
File
Edit
View
Operations
Output
Debug
Window
Help
iMPACT Flows
Boundary Scan
SystemACE
Create PROM File (PROM File Formatter)
Right click device to select operations
FLASH
TDI
TDO
xccace
bypass
xc6vlx24
bypass
Program
Verify
Erase
Blank Check
Readback...
Get Device Checksum
Assign New Configuration File...
Delete
Set Programming Properties...
Set Erase Properties...
Edit Attached Flash Properties...
Launch File Assignment Wizard
PROM File Formatter: BPI Flash Single FP
Errors
Warnings
Configuration
Platform Cable USB
6 MHz
usb-hs

Note: Programming takes about 12 minutes

Program Platform Flash with PCIe Design

- **Erase Before Programming must be selected**



Device Programming Properties - Device 2 Programming Properties

Category

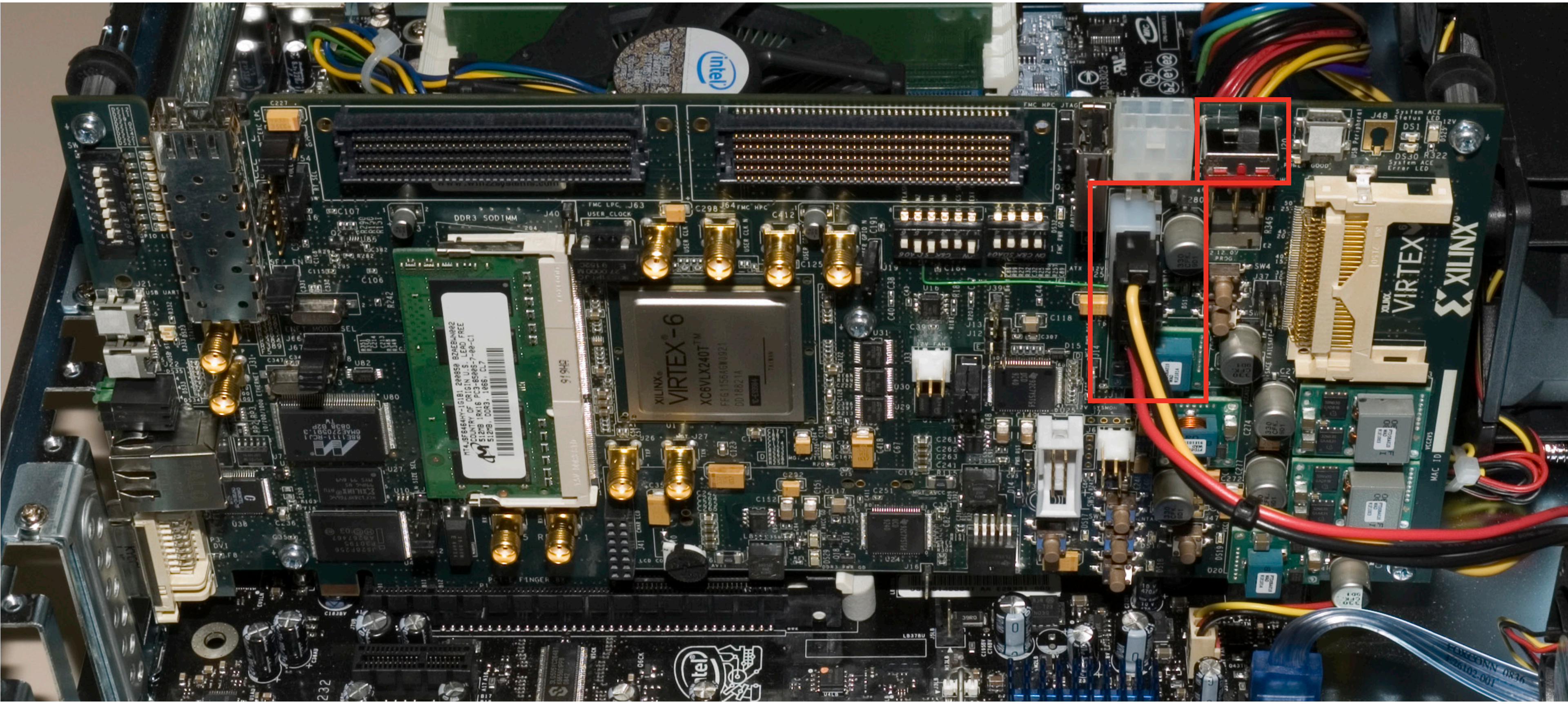
- Boundary-Scan
  - Device 1 (ACECF xccace)
  - Device 2 (FPGA xc6vlx240t)
  - Device 2 (Attached FLASH, XCF128X)

Property Name	Value
Verify	☑
General CPLD And PROM Properties	
Erase Before Programming	☑
FPGA Device Specific Programming Properties	
After programming Flash...	automatically load FPGA with Flash contents <default>

Note: Presentation applies to the ML605

Hardware Setup

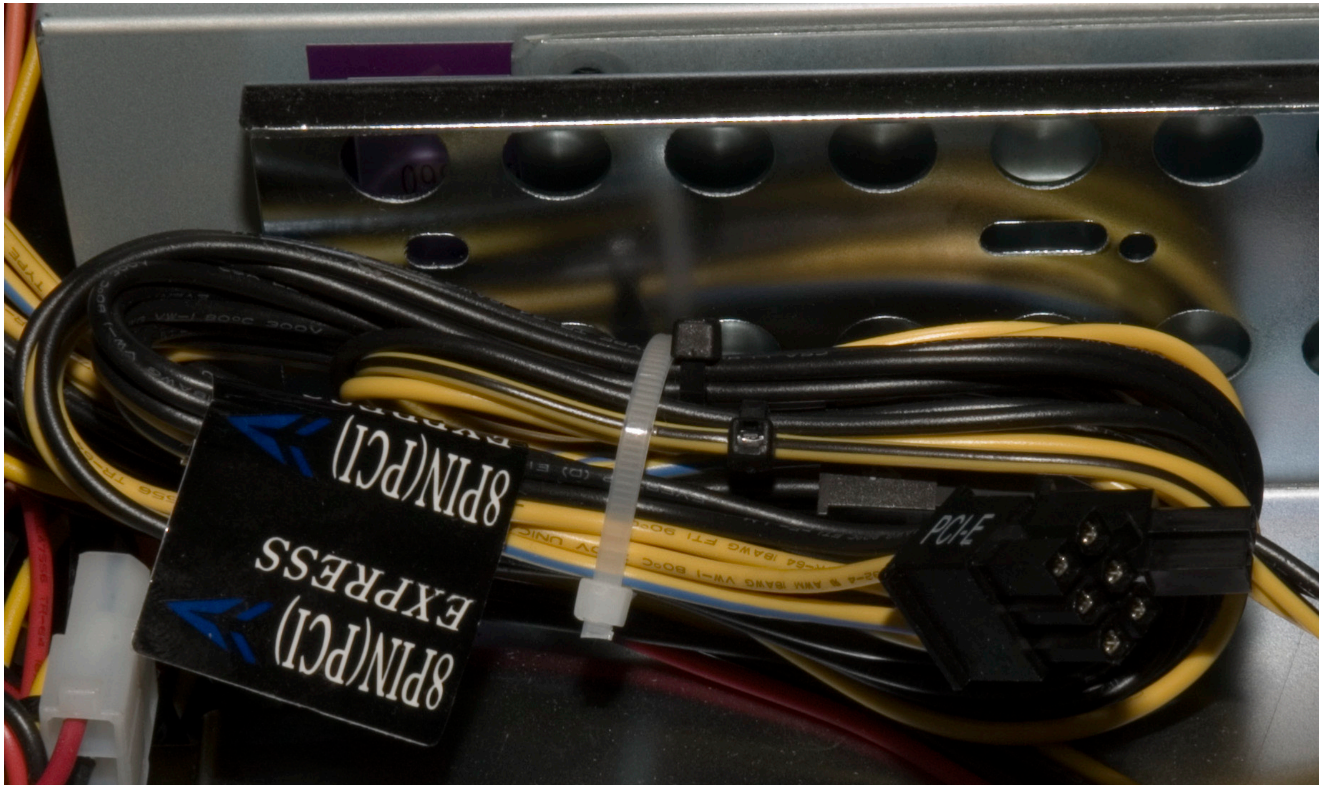
- **Insert the ML605 Board into a PCIe x4 slot (x16 shown)**
  - Connect PC power to J25, turn on Power Switch



Note: Presentation applies to the ML605

Hardware Setup

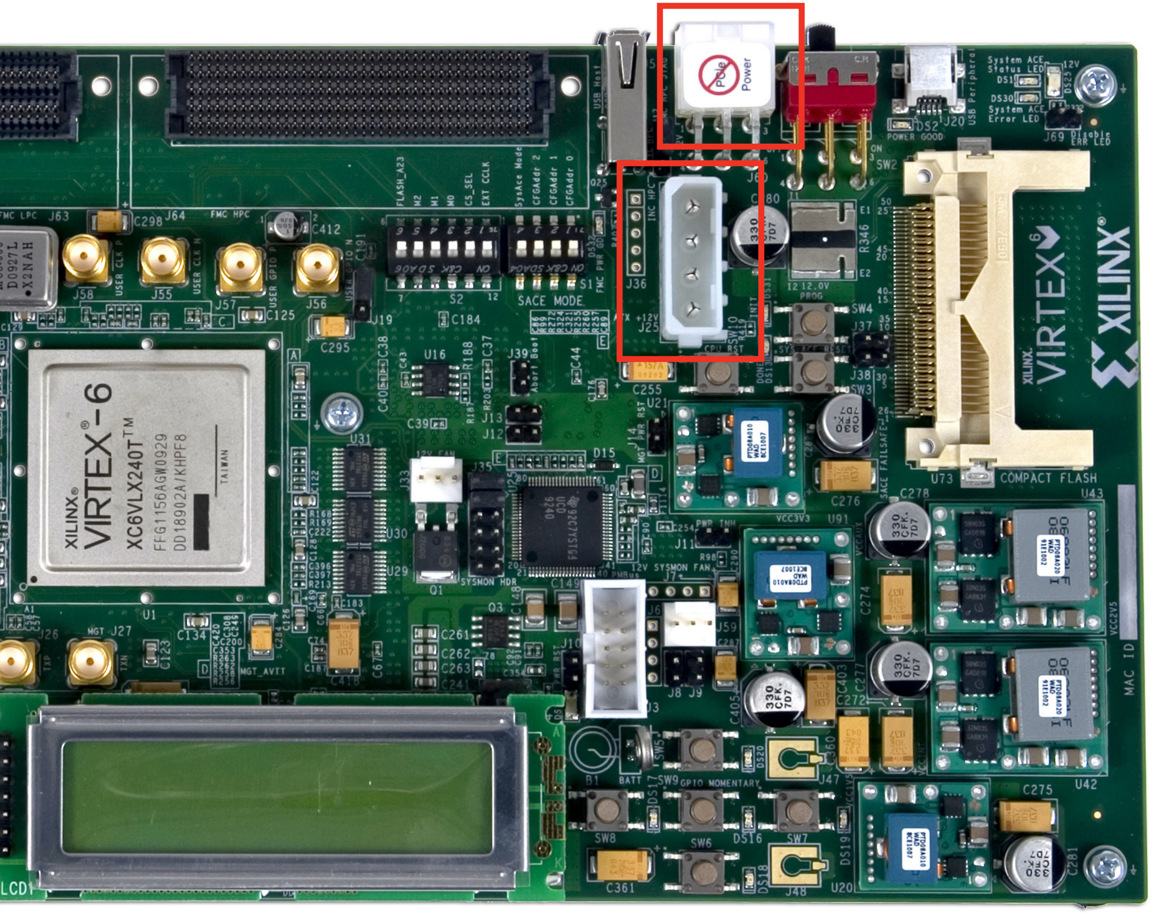
- Do not use the PCIe connector from the PC power supply



Note: Presentation applies to the ML605

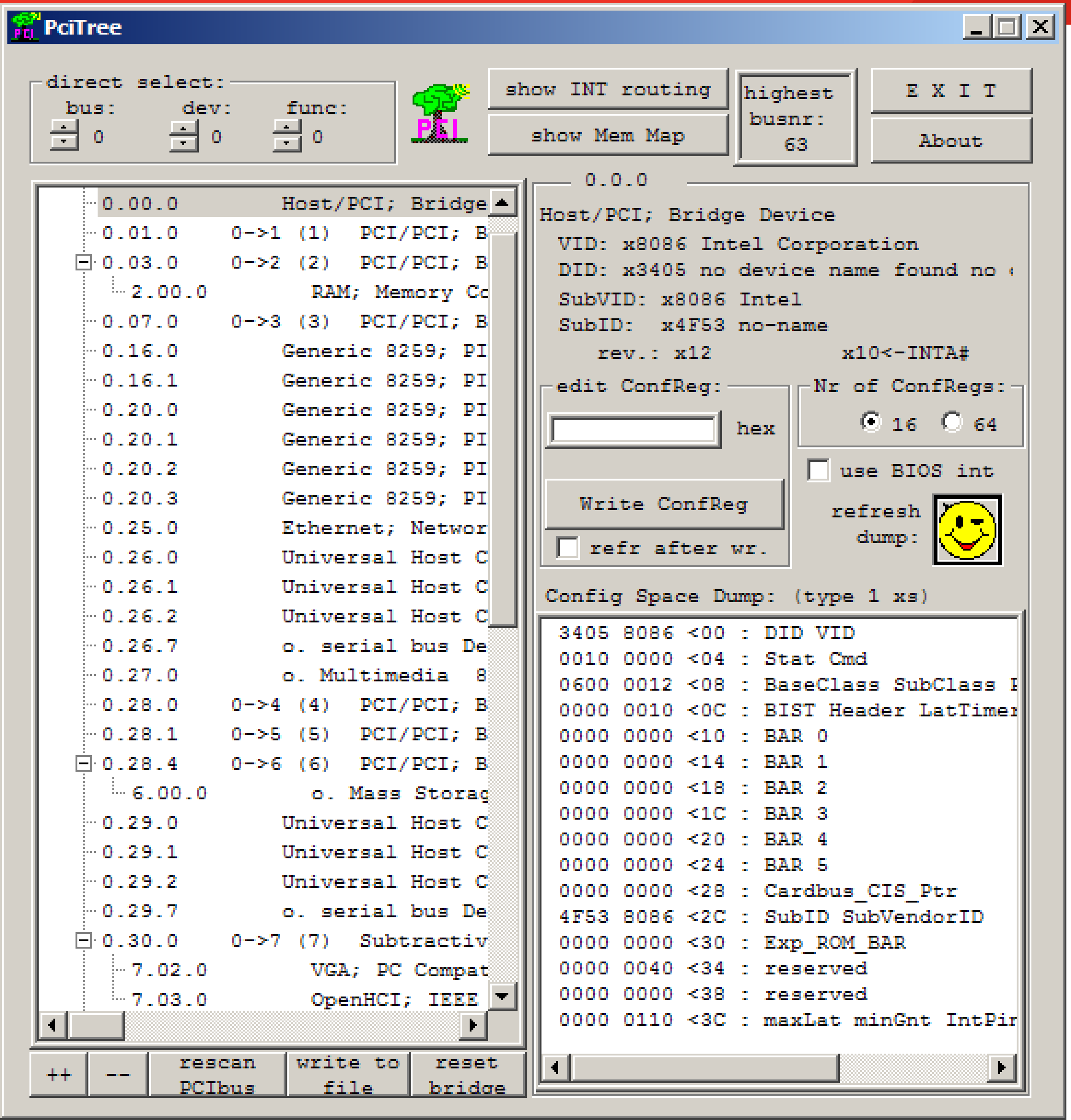
Hardware Setup

- Do not connect both the ML605 power brick connector (J60) and the four pin ATX power connector at the same time



Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



bus: 0 dev: 0 func: 0

highest busnr: 63

```
0.00.0        Host/PCI; Bridge
0.01.0   0->1 (1)   PCI/PCI; B
0.03.0   0->2 (2)   PCI/PCI; B
  2.00.0          RAM; Memory Cc
0.07.0   0->3 (3)   PCI/PCI; B
0.16.0        Generic 8259; PI
0.16.1        Generic 8259; PI
0.20.0        Generic 8259; PI
0.20.1        Generic 8259; PI
0.20.2        Generic 8259; PI
0.20.3        Generic 8259; PI
0.25.0        Ethernet; Networ
0.26.0        Universal Host C
0.26.1        Universal Host C
0.26.2        Universal Host C
0.26.7        o. serial bus De
0.27.0        o. Multimedia  8
0.28.0   0->4 (4)   PCI/PCI; B
0.28.1   0->5 (5)   PCI/PCI; B
0.28.4   0->6 (6)   PCI/PCI; B
  6.00.0          o. Mass Storag
0.29.0        Universal Host C
0.29.1        Universal Host C
0.29.2        Universal Host C
0.29.7        o. serial bus De
0.30.0   0->7 (7)   Subtractiv
  7.02.0          VGA; PC Compat
  7.03.0          OpenHCI; IEEE
```

0.0.0

Host/PCI; Bridge Device
VID: x8086 Intel Corporation
DID: x3405 no device name found no
SubVID: x8086 Intel
SubID: x4F53 no-name
rev.: x12 x10<-INTA#

edit ConfReg:

Nr of ConfRegs: ● 16 ○ 64

□ use BIOS int

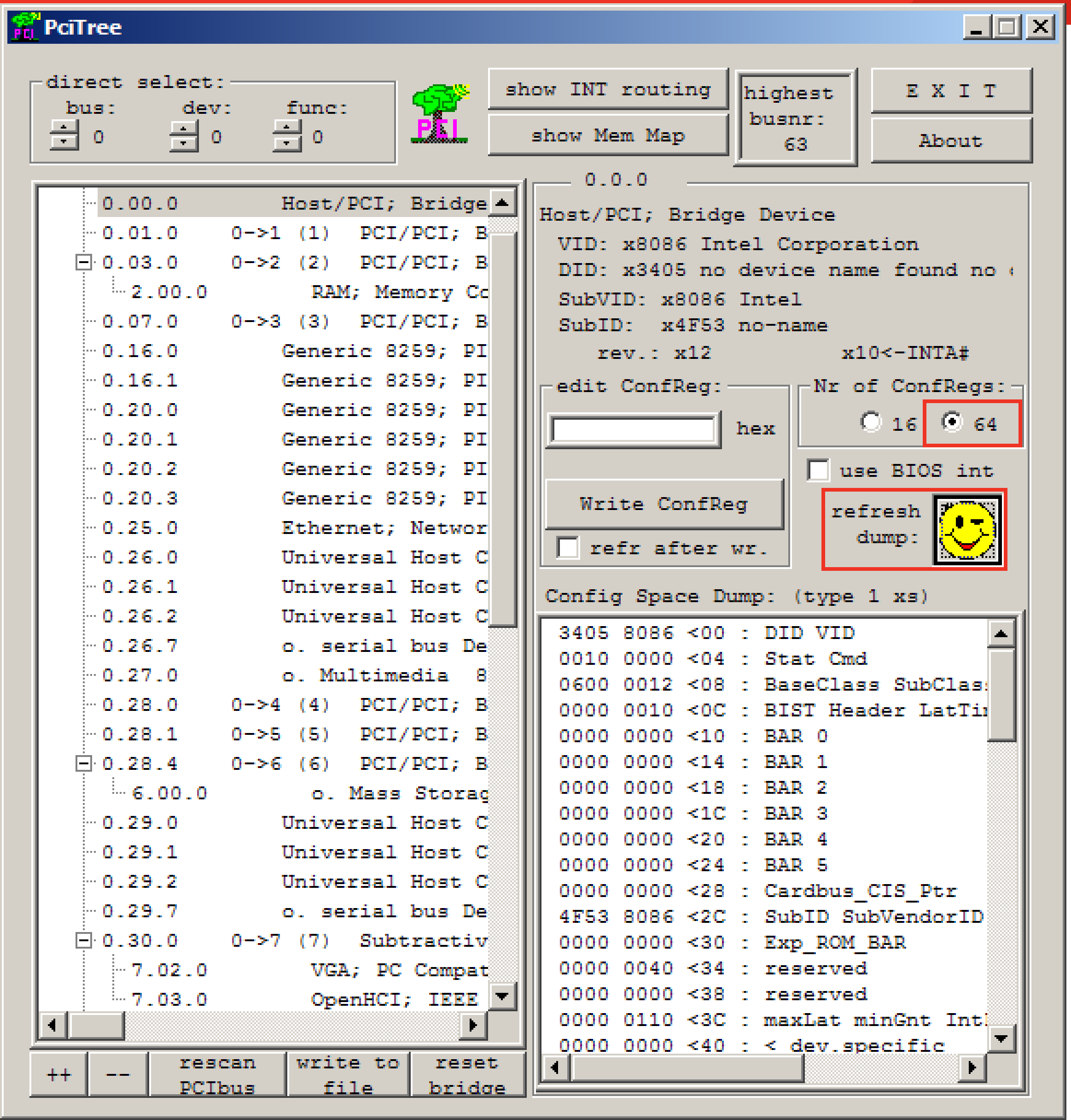
□ refr after wr.

Config Space Dump: (type 1 xs)

```
3405 8086 <00 : DID VID
0010 0000 <04 : Stat Cmd
0600 0012 <08 : BaseClass SubClass I
0000 0010 <0C : BIST Header LatTimer
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
4F53 8086 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 0110 <3C : maxLat minGnt IntPin
```

- Power on the PC
- Start PciTree

Running the PCIe x4 Gen2 Design



direct select: bus: 0 dev: 0 func: 0

highest busnr: 63

```
0.00.0          Host/PCI; Bridge
0.01.0    0->1 (1)   PCI/PCI; B
0.03.0    0->2 (2)   PCI/PCI; B
   2.00.0        RAM; Memory Cc
0.07.0    0->3 (3)   PCI/PCI; B
0.16.0          Generic 8259; PI
0.16.1          Generic 8259; PI
0.20.0          Generic 8259; PI
0.20.1          Generic 8259; PI
0.20.2          Generic 8259; PI
0.20.3          Generic 8259; PI
0.25.0          Ethernet; Networ
0.26.0          Universal Host C
0.26.1          Universal Host C
0.26.2          Universal Host C
0.26.7          o. serial bus De
0.27.0          o. Multimedia  8
0.28.0    0->4 (4)   PCI/PCI; B
0.28.1    0->5 (5)   PCI/PCI; B
0.28.4    0->6 (6)   PCI/PCI; B
   6.00.0        o. Mass Storag
0.29.0          Universal Host C
0.29.1          Universal Host C
0.29.2          Universal Host C
0.29.7          o. serial bus De
0.30.0    0->7 (7)   Subtractiv
   7.02.0        VGA; PC Compat
   7.03.0        OpenHCI; IEEE
```

```
0.0.0
Host/PCI; Bridge Device
  VID: x8086 Intel Corporation
  DID: x3405 no device name found no
  SubVID: x8086 Intel
  SubID:  x4F53 no-name
      rev.: x12              x10<-INTA#
```

Nr of ConfRegs: ○ 16 ● 64

□ use BIOS int

refresh dump:

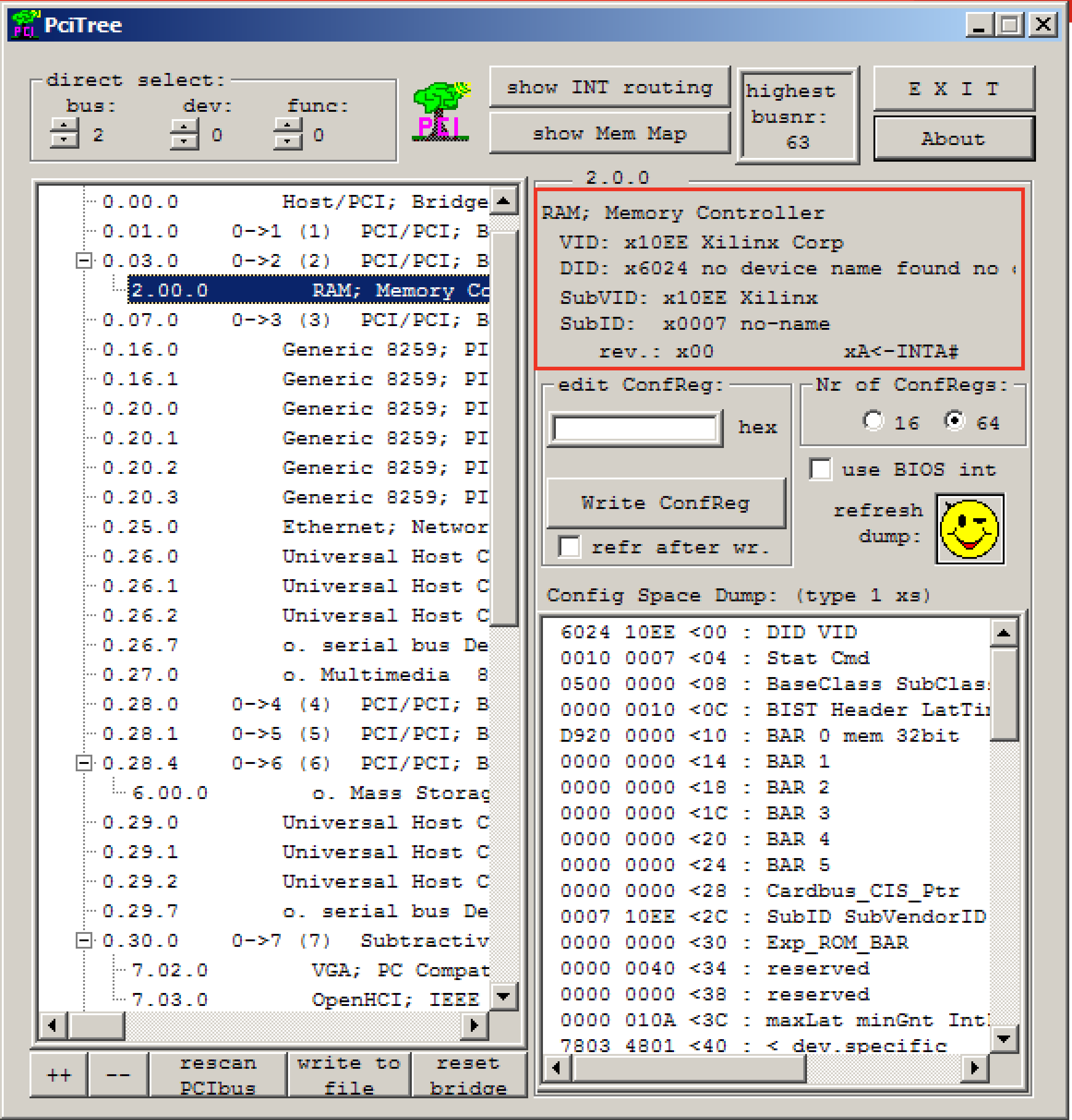
□ refr after wr.

Config Space Dump: (type 1 xs)

```
3405 8086 <00 : DID VID
0010 0000 <04 : Stat Cmd
0600 0012 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTi
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
4F53 8086 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 0110 <3C : maxLat minGnt Int
0000 0000 <40 : < dev.specific
```

- Set Number of Configuration Registers to 64
- Click on Refresh dump

Running the PCIe x4 Gen2 Design



direct select: bus: 2 dev: 0 func: 0

highest busnr: 63

```
0.00.0          Host/PCI; Bridge
0.01.0    0->1 (1)  PCI/PCI; B
0.03.0    0->2 (2)  PCI/PCI; B
  2.00.0          RAM; Memory Cc
0.07.0    0->3 (3)  PCI/PCI; B
0.16.0          Generic 8259; PI
0.16.1          Generic 8259; PI
0.20.0          Generic 8259; PI
0.20.1          Generic 8259; PI
0.20.2          Generic 8259; PI
0.20.3          Generic 8259; PI
0.25.0          Ethernet; Networ
0.26.0          Universal Host C
0.26.1          Universal Host C
0.26.2          Universal Host C
0.26.7          o. serial bus De
0.27.0          o. Multimedia  8
0.28.0    0->4 (4)  PCI/PCI; B
0.28.1    0->5 (5)  PCI/PCI; B
0.28.4    0->6 (6)  PCI/PCI; B
  6.00.0          o. Mass Storag
0.29.0          Universal Host C
0.29.1          Universal Host C
0.29.2          Universal Host C
0.29.7          o. serial bus De
0.30.0    0->7 (7)  Subtractiv
  7.02.0          VGA; PC Compat
  7.03.0          OpenHCI; IEEE
```

2.0.0

```
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
    rev.: x00             xA<-INTA#
```

edit ConfReg: hex

Nr of ConfRegs: ○ 16 ● 64

□ use BIOS int

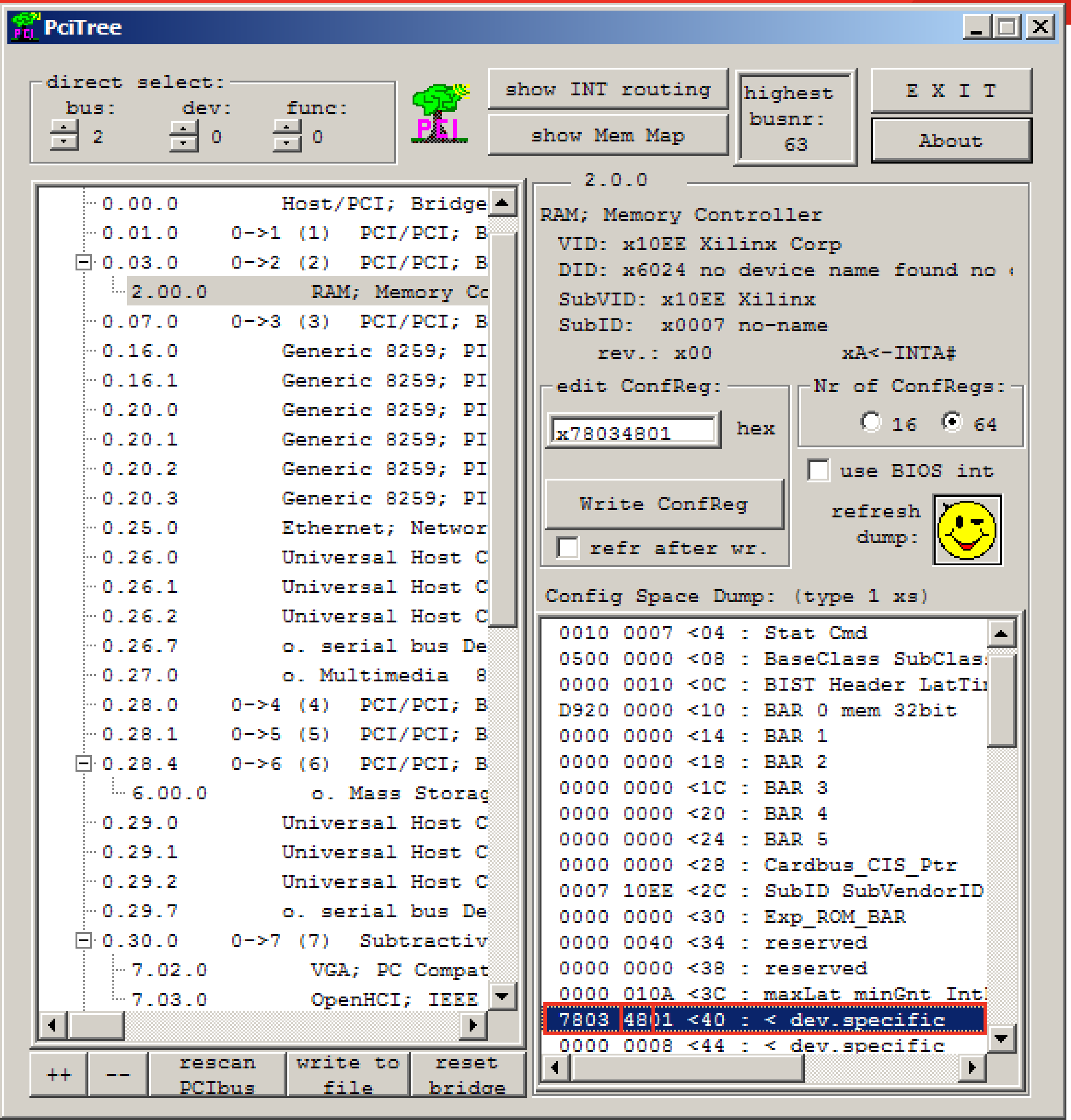
□ refr after wr.

Config Space Dump: (type 1 xs)

```
6024 10EE <00 : DID VID
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTi
D920 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minGnt Int
7803 4801 <40 : < dev.specific
```

- **Locate the Xilinx Device**
  - Vendor ID is **0x10EE**
  - The x4 Gen2 configuration will have a Device ID of **0x6024**

Running the PCIe x4 Gen2 Design



```
  0.00.0          Host/PCI; Bridge
  0.01.0    0->1  (1)   PCI/PCI; B
⊟ 0.03.0    0->2  (2)   PCI/PCI; B
     2.00.0          RAM; Memory Cc
  0.07.0    0->3  (3)   PCI/PCI; B
  0.16.0          Generic 8259; PI
  0.16.1          Generic 8259; PI
  0.20.0          Generic 8259; PI
  0.20.1          Generic 8259; PI
  0.20.2          Generic 8259; PI
  0.20.3          Generic 8259; PI
  0.25.0          Ethernet; Networ
  0.26.0          Universal Host C
  0.26.1          Universal Host C
  0.26.2          Universal Host C
  0.26.7          o. serial bus De
  0.27.0          o. Multimedia  8
  0.28.0    0->4  (4)   PCI/PCI; B
  0.28.1    0->5  (5)   PCI/PCI; B
⊟ 0.28.4    0->6  (6)   PCI/PCI; B
     6.00.0          o. Mass Storag
  0.29.0          Universal Host C
  0.29.1          Universal Host C
  0.29.2          Universal Host C
  0.29.7          o. serial bus De
⊟ 0.30.0    0->7  (7)   Subtractiv
     7.02.0          VGA; PC Compat
     7.03.0          OpenHCI; IEEE
```

```
2.0.0
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
     rev.: x00            xA<-INTA#
```

edit ConfReg: x78034801 hex

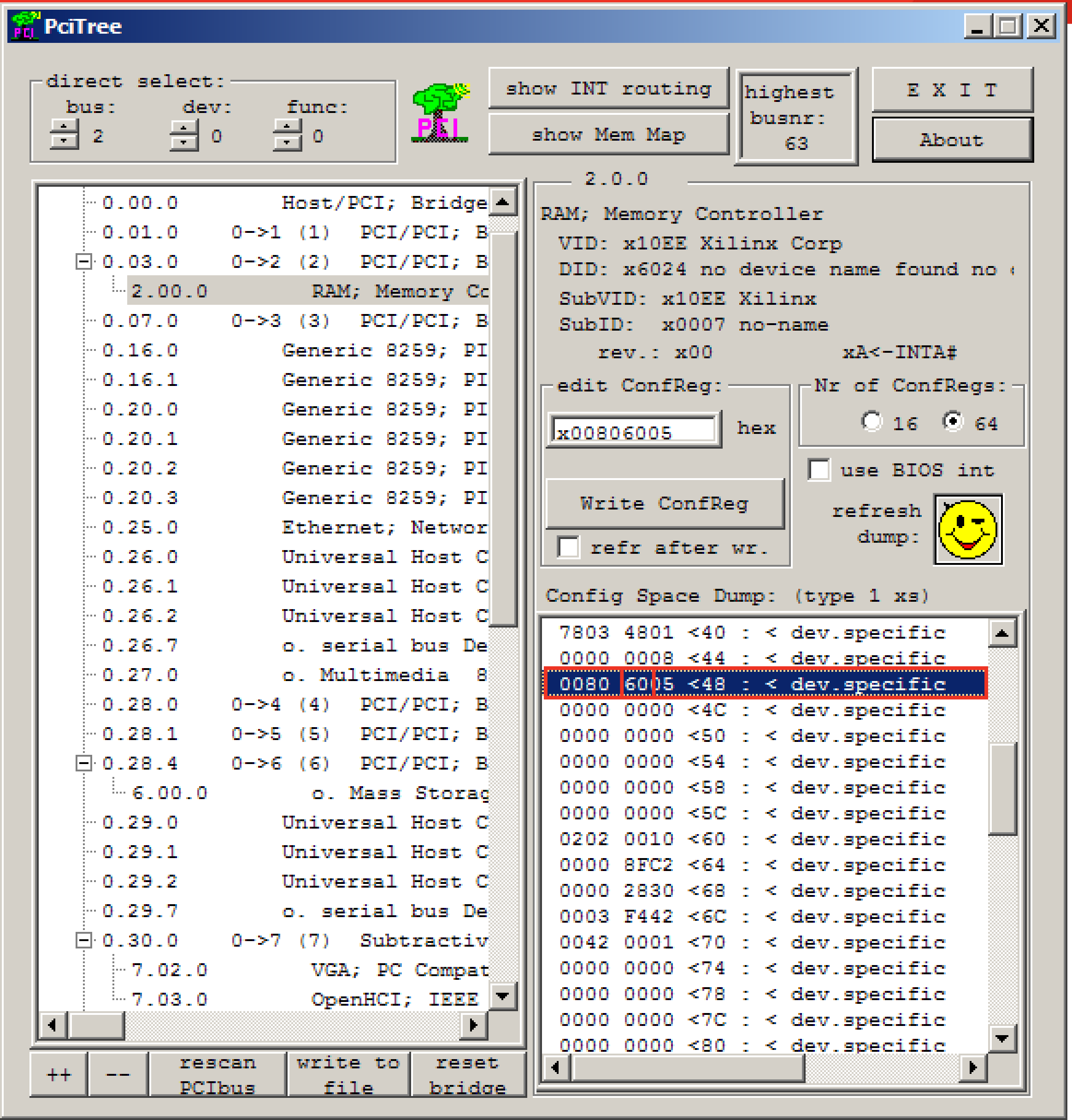
Nr of ConfRegs: ○ 16 ● 64

Config Space Dump: (type 1 xs)

```
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTi
D920 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minGnt Int
7803 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
```

- **Navigate the linked list in configuration space to locate the PCIe Capabilities Structure**
  - See UG517 for details
- **With the Xilinx device selected, select Register 0x40**
  - Register 0x40 points to the next structure
  - 0x48 is the address of the next structure

Running the PCIe x4 Gen2 Design



direct select: bus: 2 dev: 0 func: 0

highest busnr: 63

```
  0.00.0          Host/PCI; Bridge
  0.01.0   0->1 (1)  PCI/PCI; B
⊟ 0.03.0   0->2 (2)  PCI/PCI; B
    2.00.0          RAM; Memory Co
  0.07.0   0->3 (3)  PCI/PCI; B
  0.16.0          Generic 8259; PI
  0.16.1          Generic 8259; PI
  0.20.0          Generic 8259; PI
  0.20.1          Generic 8259; PI
  0.20.2          Generic 8259; PI
  0.20.3          Generic 8259; PI
  0.25.0          Ethernet; Networ
  0.26.0          Universal Host C
  0.26.1          Universal Host C
  0.26.2          Universal Host C
  0.26.7          o. serial bus De
  0.27.0          o. Multimedia  8
  0.28.0   0->4 (4)  PCI/PCI; B
  0.28.1   0->5 (5)  PCI/PCI; B
⊟ 0.28.4   0->6 (6)  PCI/PCI; B
    6.00.0          o. Mass Storag
  0.29.0          Universal Host C
  0.29.1          Universal Host C
  0.29.2          Universal Host C
  0.29.7          o. serial bus De
⊟ 0.30.0   0->7 (7)  Subtractiv
    7.02.0          VGA; PC Compat
    7.03.0          OpenHCI; IEEE
```

2.0.0

```
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
     rev.: x00              xA<-INTA#
```

edit ConfReg: x00806005 hex

Nr of ConfRegs: ○ 16 ● 64

□ use BIOS int

□ refr after wr.

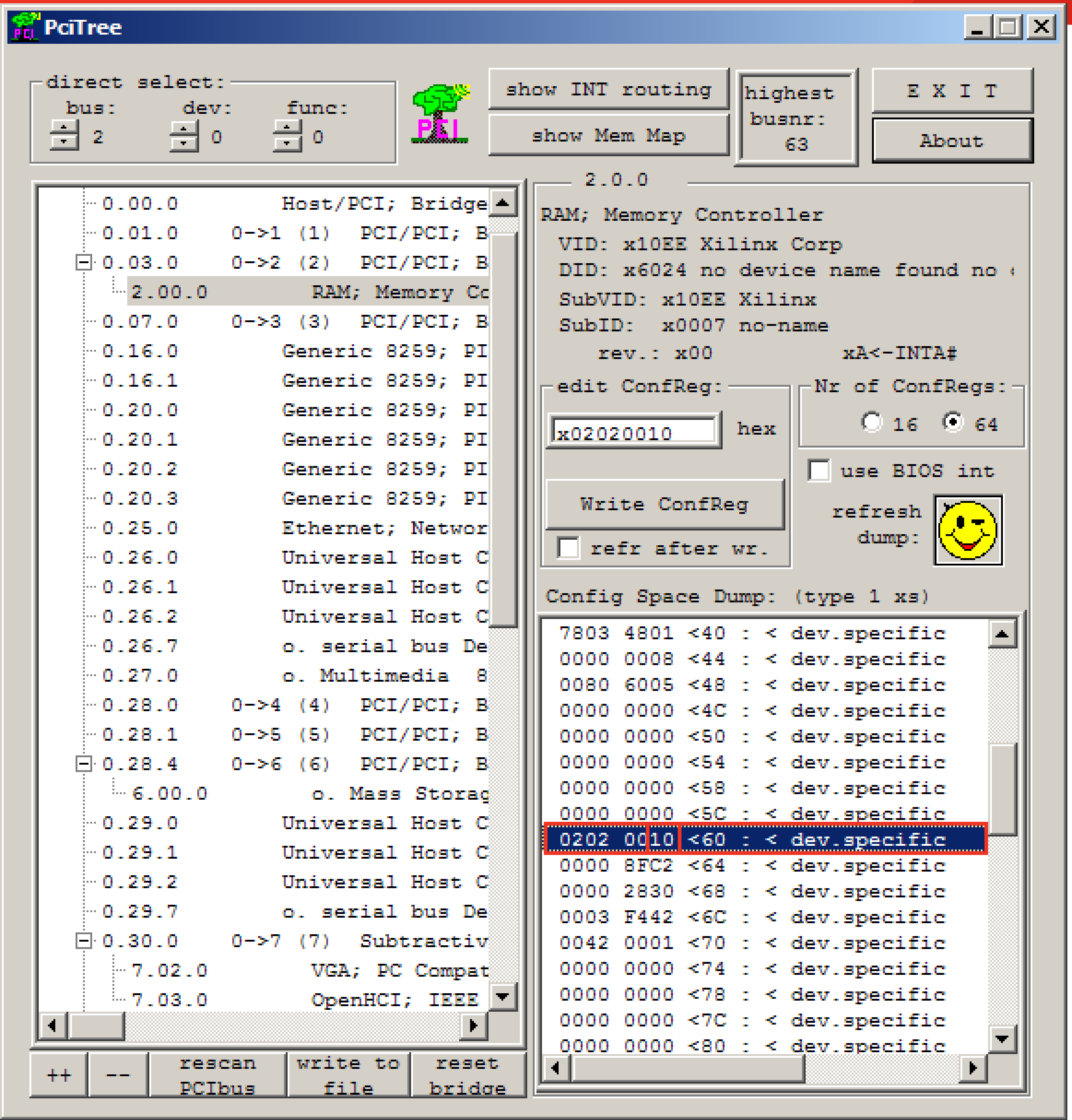
refresh dump:

Config Space Dump: (type 1 xs)

```
7803 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
0080 6005 <48 : < dev.specific
0000 0000 <4C : < dev.specific
0000 0000 <50 : < dev.specific
0000 0000 <54 : < dev.specific
0000 0000 <58 : < dev.specific
0000 0000 <5C : < dev.specific
0202 0010 <60 : < dev.specific
0000 8FC2 <64 : < dev.specific
0000 2830 <68 : < dev.specific
0003 F442 <6C : < dev.specific
0042 0001 <70 : < dev.specific
0000 0000 <74 : < dev.specific
0000 0000 <78 : < dev.specific
0000 0000 <7C : < dev.specific
0000 0000 <80 : < dev.specific
```

- **Select Register 0x48**
  - Register 0x48 points to the next structure
  - 0x60 is the address of the next structure

Running the PCIe x4 Gen2 Design



```
0.00.0          Host/PCI; Bridge
0.01.0    0->1 (1)   PCI/PCI; B
0.03.0    0->2 (2)   PCI/PCI; B
  2.00.0          RAM; Memory Co
0.07.0    0->3 (3)   PCI/PCI; B
0.16.0          Generic 8259; PI
0.16.1          Generic 8259; PI
0.20.0          Generic 8259; PI
0.20.1          Generic 8259; PI
0.20.2          Generic 8259; PI
0.20.3          Generic 8259; PI
0.25.0          Ethernet; Networ
0.26.0          Universal Host C
0.26.1          Universal Host C
0.26.2          Universal Host C
0.26.7          o. serial bus De
0.27.0          o. Multimedia  8
0.28.0    0->4 (4)   PCI/PCI; B
0.28.1    0->5 (5)   PCI/PCI; B
0.28.4    0->6 (6)   PCI/PCI; B
  6.00.0          o. Mass Storag
0.29.0          Universal Host C
0.29.1          Universal Host C
0.29.2          Universal Host C
0.29.7          o. serial bus De
0.30.0    0->7 (7)   Subtractiv
  7.02.0          VGA; PC Compat
  7.03.0          OpenHCI; IEEE
```

```
2.0.0
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
     rev.: x00            xA<-INTA#
```

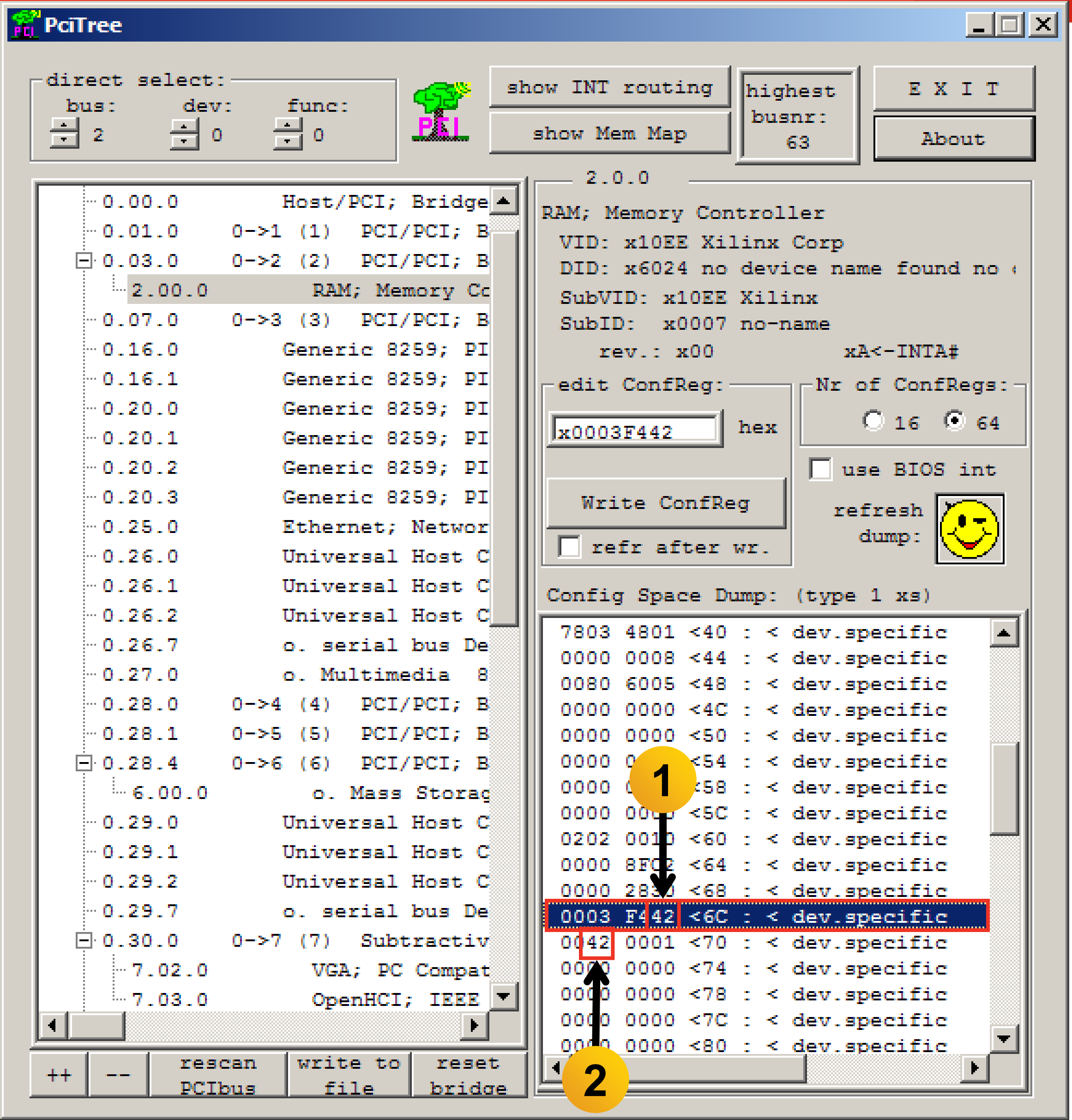
edit ConfReg: x02020010 hex

Config Space Dump: (type 1 xs)

```
7803 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
0080 6005 <48 : < dev.specific
0000 0000 <4C : < dev.specific
0000 0000 <50 : < dev.specific
0000 0000 <54 : < dev.specific
0000 0000 <58 : < dev.specific
0000 0000 <5C : < dev.specific
0202 0010 <60 : < dev.specific
0000 8FC2 <64 : < dev.specific
0000 2830 <68 : < dev.specific
0003 F442 <6C : < dev.specific
0042 0001 <70 : < dev.specific
0000 0000 <74 : < dev.specific
0000 0000 <78 : < dev.specific
0000 0000 <7C : < dev.specific
0000 0000 <80 : < dev.specific
```

- **Register 0x60**
  - 0x60 is a type 0x10, indicating PCIe Capabilities Structure
  - Last Structure

Running the PCIe x4 Gen2 Design



```
0.00.0         Host/PCI; Bridge
0.01.0   0->1 (1)   PCI/PCI; B
0.03.0   0->2 (2)   PCI/PCI; B
  2.00.0         RAM; Memory Co
0.07.0   0->3 (3)   PCI/PCI; B
0.16.0         Generic 8259; PI
0.16.1         Generic 8259; PI
0.20.0         Generic 8259; PI
0.20.1         Generic 8259; PI
0.20.2         Generic 8259; PI
0.20.3         Generic 8259; PI
0.25.0         Ethernet; Networ
0.26.0         Universal Host C
0.26.1         Universal Host C
0.26.2         Universal Host C
0.26.7         o. serial bus De
0.27.0         o. Multimedia   8
0.28.0   0->4 (4)   PCI/PCI; B
0.28.1   0->5 (5)   PCI/PCI; B
0.28.4   0->6 (6)   PCI/PCI; B
  6.00.0         o. Mass Storag
0.29.0         Universal Host C
0.29.1         Universal Host C
0.29.2         Universal Host C
0.29.7         o. serial bus De
0.30.0   0->7 (7)   Subtractiv
  7.02.0         VGA; PC Compat
  7.03.0         OpenHCI; IEEE
```

```
2.0.0
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
     rev.: x00              xA<-INTA#
```

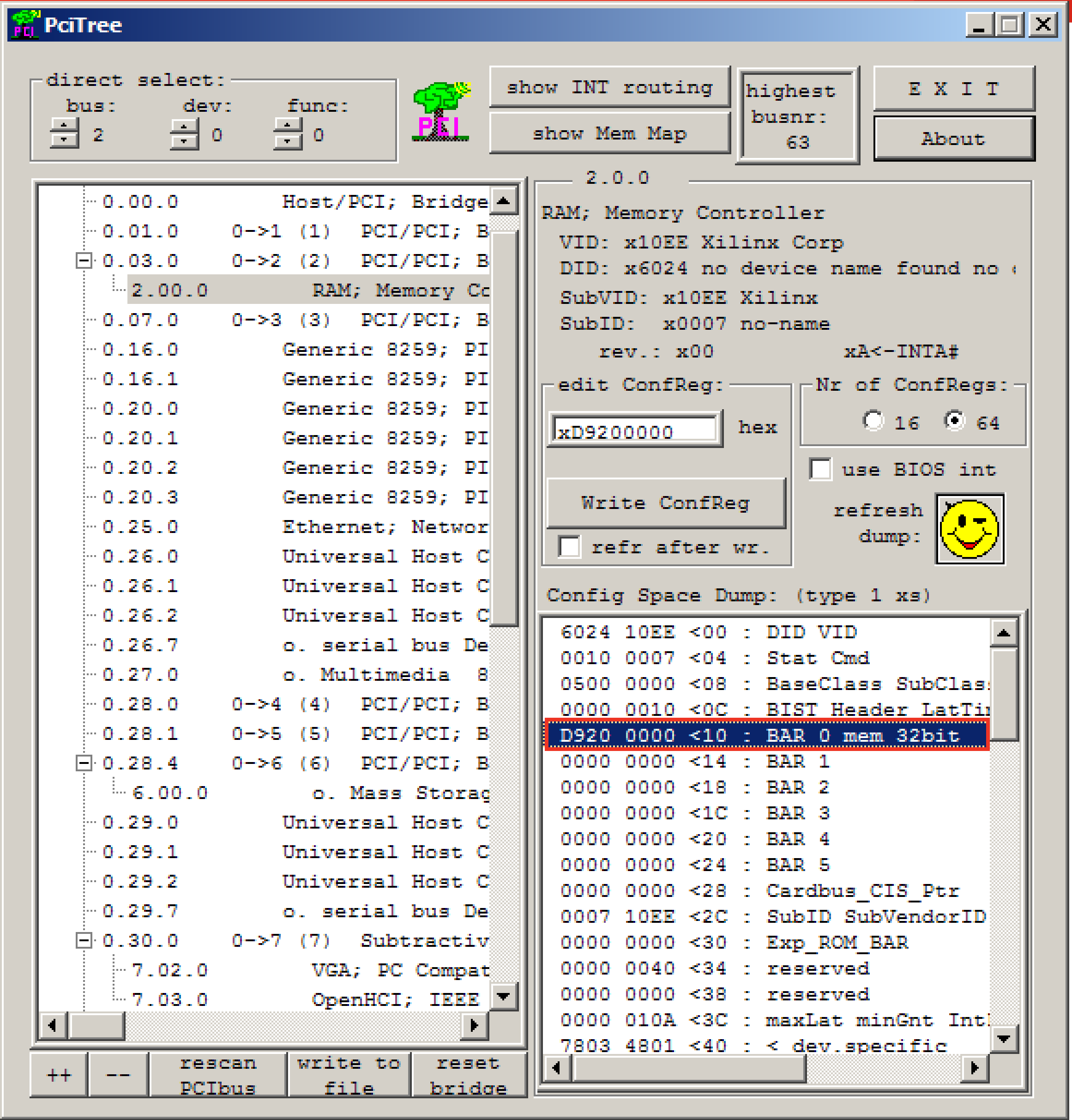
x0003F442

Config Space Dump: (type 1 xs)

```
7803 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
0080 6005 <48 : < dev.specific
0000 0000 <4C : < dev.specific
0000 0000 <50 : < dev.specific
0000 0    <54 : < dev.specific
0000 0    58 : < dev.specific
0000 00   <5C : < dev.specific
0202 001  <60 : < dev.specific
0000 8FC  <64 : < dev.specific
0000 28   <68 : < dev.specific
0003 F 42 <6C : < dev.specific
0042 0001 <70 : < dev.specific
00 0 0000 <74 : < dev.specific
00 0 0000 <78 : < dev.specific
00 0 0000 <7C : < dev.specific
00 0 0000 <80 : < dev.specific
```

- **Register 0x6C**
  - Link Capabilities Register
  - Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
  - The value 0x42 shows this is an x4 Gen2 device (1)
- **Link Status Register**
  - 0x70
  - Shows the current link status
  - This design, in a Gen2 chassis, trained to x4 Gen2 (2)

Running the PCIe x4 Gen2 Design



```
0.00.0          Host/PCI; Bridge
0.01.0    0->1 (1)   PCI/PCI; B
0.03.0    0->2 (2)   PCI/PCI; B
  2.00.0          RAM; Memory Co
0.07.0    0->3 (3)   PCI/PCI; B
0.16.0          Generic 8259; PI
0.16.1          Generic 8259; PI
0.20.0          Generic 8259; PI
0.20.1          Generic 8259; PI
0.20.2          Generic 8259; PI
0.20.3          Generic 8259; PI
0.25.0          Ethernet; Networ
0.26.0          Universal Host C
0.26.1          Universal Host C
0.26.2          Universal Host C
0.26.7          o. serial bus De
0.27.0          o. Multimedia  8
0.28.0    0->4 (4)   PCI/PCI; B
0.28.1    0->5 (5)   PCI/PCI; B
0.28.4    0->6 (6)   PCI/PCI; B
  6.00.0          o. Mass Storag
0.29.0          Universal Host C
0.29.1          Universal Host C
0.29.2          Universal Host C
0.29.7          o. serial bus De
0.30.0    0->7 (7)   Subtractiv
  7.02.0          VGA; PC Compat
  7.03.0          OpenHCI; IEEE
```

```
2.0.0
RAM; Memory Controller
 VID: x10EE Xilinx Corp
 DID: x6024 no device name found no
 SubVID: x10EE Xilinx
 SubID:  x0007 no-name
      rev.: x00          xA<-INTA#
```

edit ConfReg: xD9200000 hex

Nr of ConfRegs: ○ 16 ● 64

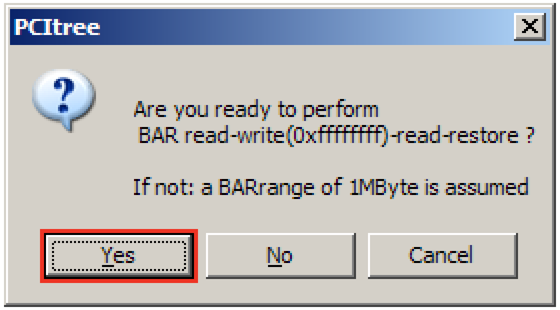
□ use BIOS int

□ refr after wr.

Config Space Dump: (type 1 xs)

```
6024 10EE <00 : DID VID
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTi
D920 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minGnt Int
7803 4801 <40 : < dev.specific
```

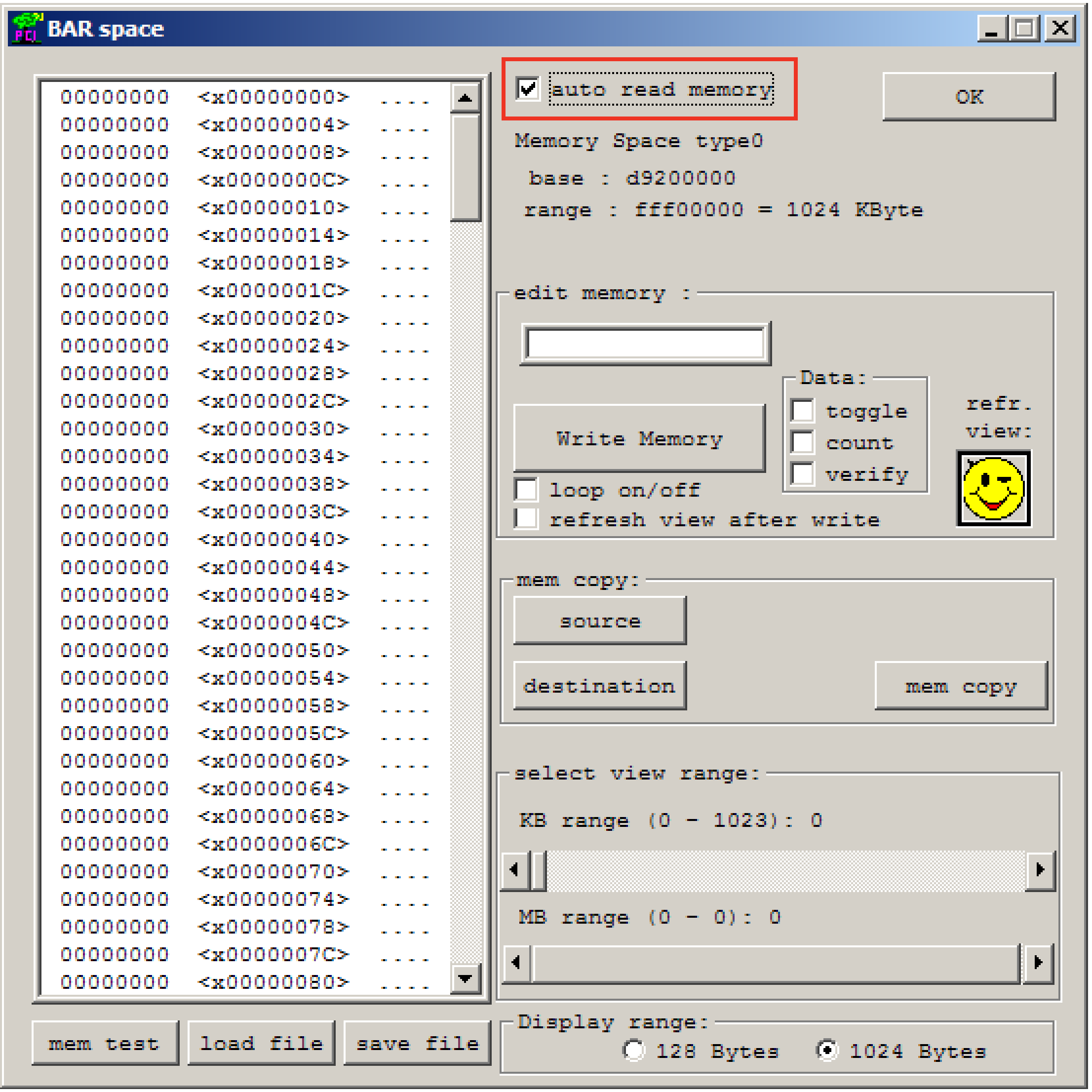
- **Double-click on BAR 0**
  - BAR 0 Address is machine dependent
- **Click Yes on the Dialog box seen below**



Are you ready to perform
BAR read-write(0xffffffff)-read-restore ?

If not: a BARrange of 1MByte is assumed

Running the PCIe x4 Gen2 Design



☑ auto read memory

Memory Space type0

base : d9200000

range : fff00000 = 1024 KByte

Data:
□ toggle
□ count
□ verify

□ loop on/off

□ refresh view after write

KB range (0 - 1023): 0

MB range (0 - 0): 0

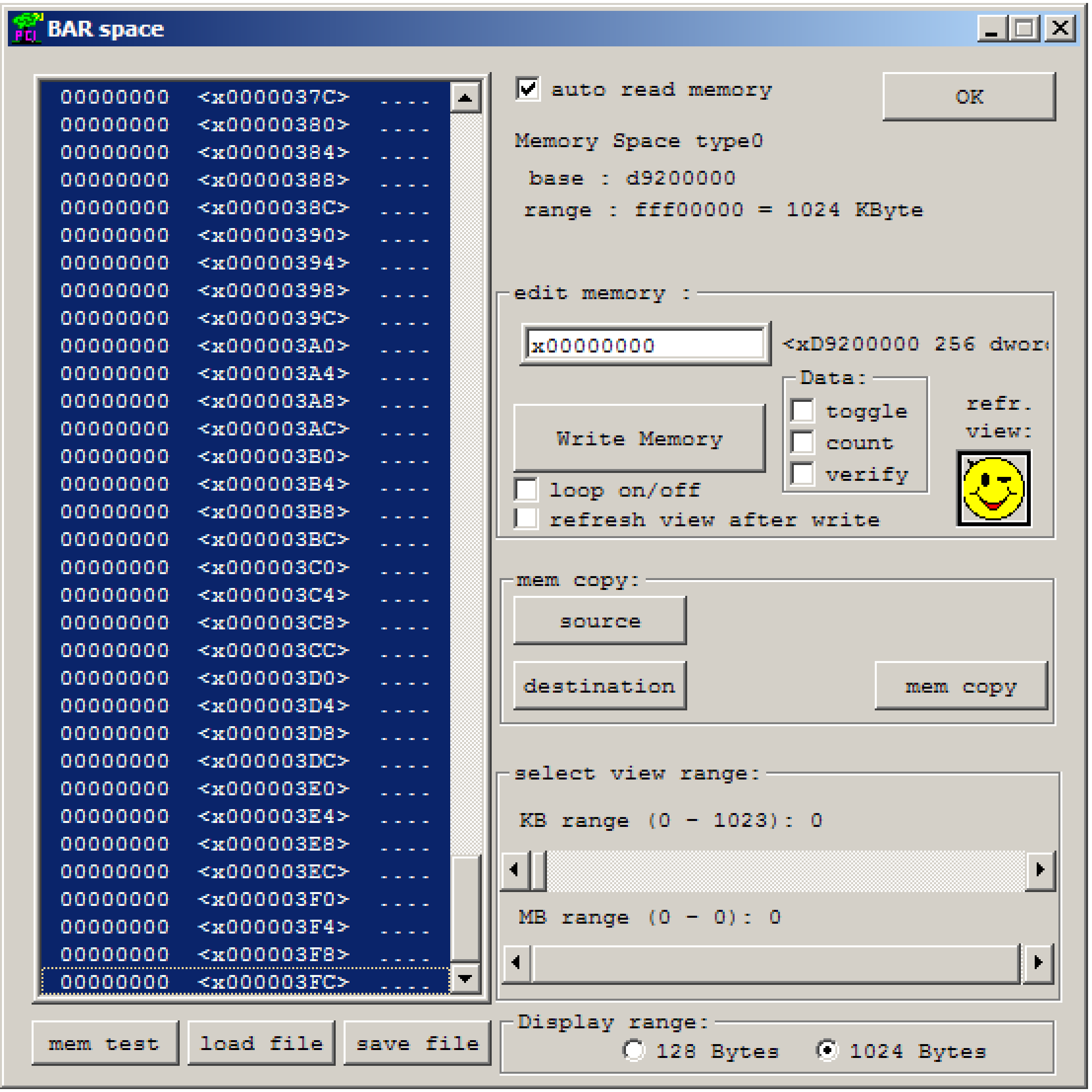
○ 128 Bytes ● 1024 Bytes

```
00000000  <x00000000>  ....
00000000  <x00000004>  ....
00000000  <x00000008>  ....
00000000  <x0000000C>  ....
00000000  <x00000010>  ....
00000000  <x00000014>  ....
00000000  <x00000018>  ....
00000000  <x0000001C>  ....
00000000  <x00000020>  ....
00000000  <x00000024>  ....
00000000  <x00000028>  ....
00000000  <x0000002C>  ....
00000000  <x00000030>  ....
00000000  <x00000034>  ....
00000000  <x00000038>  ....
00000000  <x0000003C>  ....
00000000  <x00000040>  ....
00000000  <x00000044>  ....
00000000  <x00000048>  ....
00000000  <x0000004C>  ....
00000000  <x00000050>  ....
00000000  <x00000054>  ....
00000000  <x00000058>  ....
00000000  <x0000005C>  ....
00000000  <x00000060>  ....
00000000  <x00000064>  ....
00000000  <x00000068>  ....
00000000  <x0000006C>  ....
00000000  <x00000070>  ....
00000000  <x00000074>  ....
00000000  <x00000078>  ....
00000000  <x0000007C>  ....
00000000  <x00000080>  ....
```

- Select auto read memory

Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



```
00000000  <x0000037C>  ....
00000000  <x00000380>  ....
00000000  <x00000384>  ....
00000000  <x00000388>  ....
00000000  <x0000038C>  ....
00000000  <x00000390>  ....
00000000  <x00000394>  ....
00000000  <x00000398>  ....
00000000  <x0000039C>  ....
00000000  <x000003A0>  ....
00000000  <x000003A4>  ....
00000000  <x000003A8>  ....
00000000  <x000003AC>  ....
00000000  <x000003B0>  ....
00000000  <x000003B4>  ....
00000000  <x000003B8>  ....
00000000  <x000003BC>  ....
00000000  <x000003C0>  ....
00000000  <x000003C4>  ....
00000000  <x000003C8>  ....
00000000  <x000003CC>  ....
00000000  <x000003D0>  ....
00000000  <x000003D4>  ....
00000000  <x000003D8>  ....
00000000  <x000003DC>  ....
00000000  <x000003E0>  ....
00000000  <x000003E4>  ....
00000000  <x000003E8>  ....
00000000  <x000003EC>  ....
00000000  <x000003F0>  ....
00000000  <x000003F4>  ....
00000000  <x000003F8>  ....
00000000  <x000003FC>  ....
```

☑ auto read memory

```
Memory Space type0
 base : d9200000
range : fff00000 = 1024 KByte
```

edit memory :

x00000000 <xD9200000 256 dwor

Data:

☐ toggle

☐ count

☐ verify

☐ loop on/off

☐ refresh view after write

mem copy:

select view range:

KB range (0 - 1023): 0

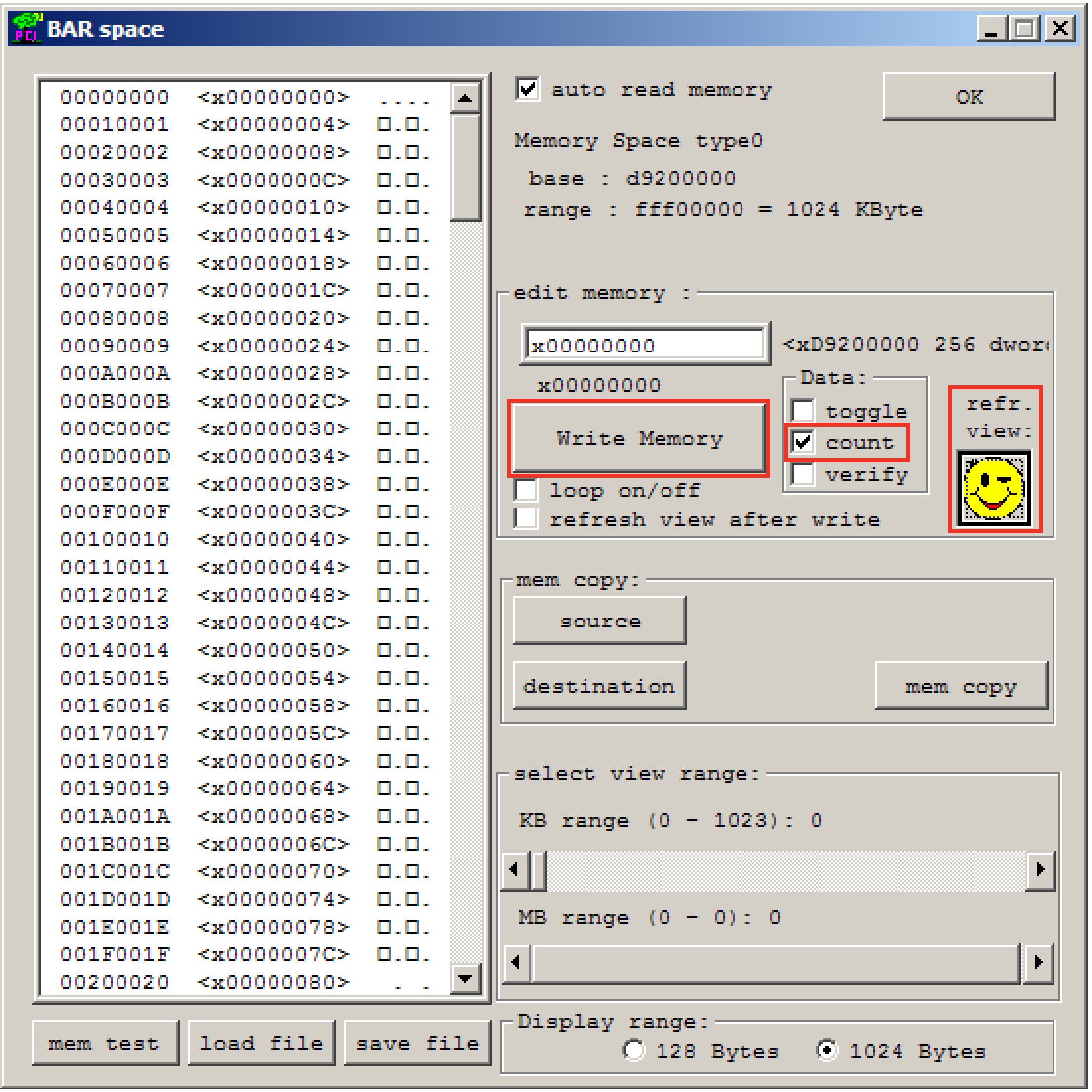
MB range (0 - 0): 0

Display range: ○ 128 Bytes ● 1024 Bytes

- **Click on the first memory location**
  - Type <Shift-End> to select 1024 Bytes

Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



BAR space

```
00000000  <x00000000>  ....
00010001  <x00000004>  □.□.
00020002  <x00000008>  □.□.
00030003  <x0000000C>  □.□.
00040004  <x00000010>  □.□.
00050005  <x00000014>  □.□.
00060006  <x00000018>  □.□.
00070007  <x0000001C>  □.□.
00080008  <x00000020>  □.□.
00090009  <x00000024>  □.□.
000A000A  <x00000028>  □.□.
000B000B  <x0000002C>  □.□.
000C000C  <x00000030>  □.□.
000D000D  <x00000034>  □.□.
000E000E  <x00000038>  □.□.
000F000F  <x0000003C>  □.□.
00100010  <x00000040>  □.□.
00110011  <x00000044>  □.□.
00120012  <x00000048>  □.□.
00130013  <x0000004C>  □.□.
00140014  <x00000050>  □.□.
00150015  <x00000054>  □.□.
00160016  <x00000058>  □.□.
00170017  <x0000005C>  □.□.
00180018  <x00000060>  □.□.
00190019  <x00000064>  □.□.
001A001A  <x00000068>  □.□.
001B001B  <x0000006C>  □.□.
001C001C  <x00000070>  □.□.
001D001D  <x00000074>  □.□.
001E001E  <x00000078>  □.□.
001F001F  <x0000007C>  □.□.
00200020  <x00000080>   . .
```

☑ auto read memory

Memory Space type0
base : d9200000
range : fff00000 = 1024 KByte

edit memory :
x00000000 <xD9200000 256 dwor
x00000000
Data: ☐ toggle ☑ count ☐ verify
☐ loop on/off
☐ refresh view after write

mem copy:

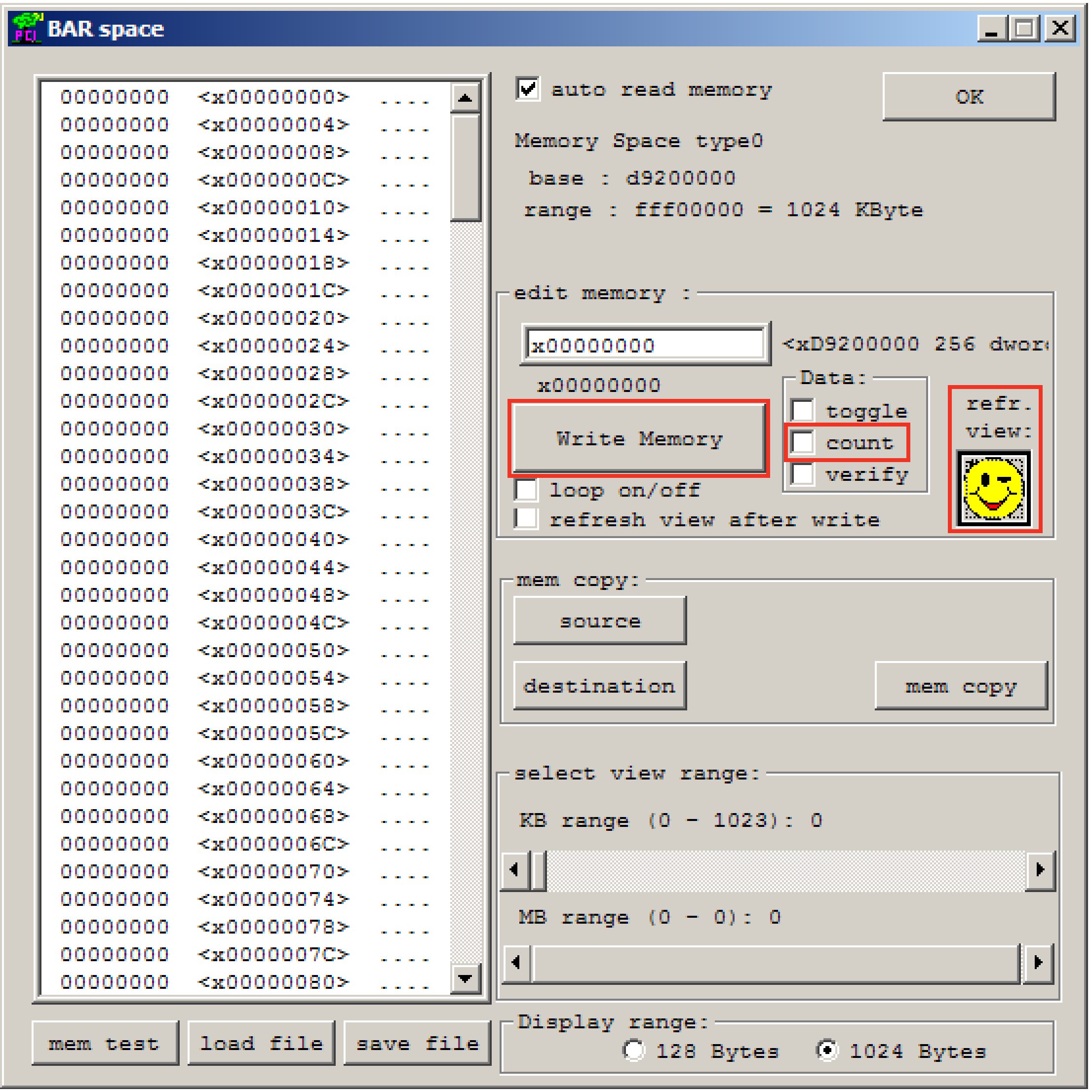
select view range:
KB range (0 - 1023): 0
MB range (0 - 0): 0

Display range: ○ 128 Bytes ● 1024 Bytes

- **Write Memory**
  - Select count
  - Click Write Memory
  - Click refr view
- **View results – counting up to FF**

Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



BAR space

```
00000000  <x00000000>  ....
00000000  <x00000004>  ....
00000000  <x00000008>  ....
00000000  <x0000000C>  ....
00000000  <x00000010>  ....
00000000  <x00000014>  ....
00000000  <x00000018>  ....
00000000  <x0000001C>  ....
00000000  <x00000020>  ....
00000000  <x00000024>  ....
00000000  <x00000028>  ....
00000000  <x0000002C>  ....
00000000  <x00000030>  ....
00000000  <x00000034>  ....
00000000  <x00000038>  ....
00000000  <x0000003C>  ....
00000000  <x00000040>  ....
00000000  <x00000044>  ....
00000000  <x00000048>  ....
00000000  <x0000004C>  ....
00000000  <x00000050>  ....
00000000  <x00000054>  ....
00000000  <x00000058>  ....
00000000  <x0000005C>  ....
00000000  <x00000060>  ....
00000000  <x00000064>  ....
00000000  <x00000068>  ....
00000000  <x0000006C>  ....
00000000  <x00000070>  ....
00000000  <x00000074>  ....
00000000  <x00000078>  ....
00000000  <x0000007C>  ....
00000000  <x00000080>  ....
```

☑ auto read memory

Memory Space type0

base : d9200000

range : fff00000 = 1024 KByte

edit memory :

x00000000 <xD9200000 256 dwor

x00000000

Data:

□ toggle

□ count

□ verify

□ loop on/off

□ refresh view after write

mem copy:

select view range:

KB range (0 - 1023): 0

MB range (0 - 0): 0

Display range:

○ 128 Bytes ● 1024 Bytes

- **Restore Memory**
  - Deselect count
  - Click Write Memory
  - Click refr view
- **Memory is reset to zeros**

Note: Presentation applies to the ML605

Virtex-6 PCIe x4 Gen2 Capability

- **ML605 Supports PCIe Gen1 and Gen2 Capability**
  - x4, x2, or x1 Gen2 lane width
  - x8 Gen2 not supported in -1 parts
- **LogiCORE PIO Example Design**
  - RDF0009.zip
  - Available through http://www.xilinx.com/ml605
- **LogiCORE Integrated Block for PCI Express**
  - See UG517 for details

References

References

- **PCIe Base Specification**
  - PCI SIG Web Site
    http://www.pcisig.com/home
- **Virtex-6 PCIe**
  - PCIe Product Overview
    http://www.xilinx.com/products/ipcenter/V6_PCI_Express_Block.htm
  - Virtex-6 FPGA Integrated Block v1.5 for PCI Express User Guide
    http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ug517.pdf
  - Virtex-6 FPGA Integrated Block v1.5 for PCI Express Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ds715.pdf
  - IP Release Notes Guide
    http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

Documentation

Documentation

- **Virtex-6**
  - Virtex-6 FPGA Family

    http://www.xilinx.com/products/virtex6/index.htm
- **ML605 Documentation**
  - Virtex-6 FPGA ML605 Evaluation Kit

    http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm
  - ML605 Hardware User Guide

    http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf
  - ML605 Reference Design User Guide

    http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf