

# ML605 PCIe x8 Gen1 Design Creation

**May 2010**

# Overview

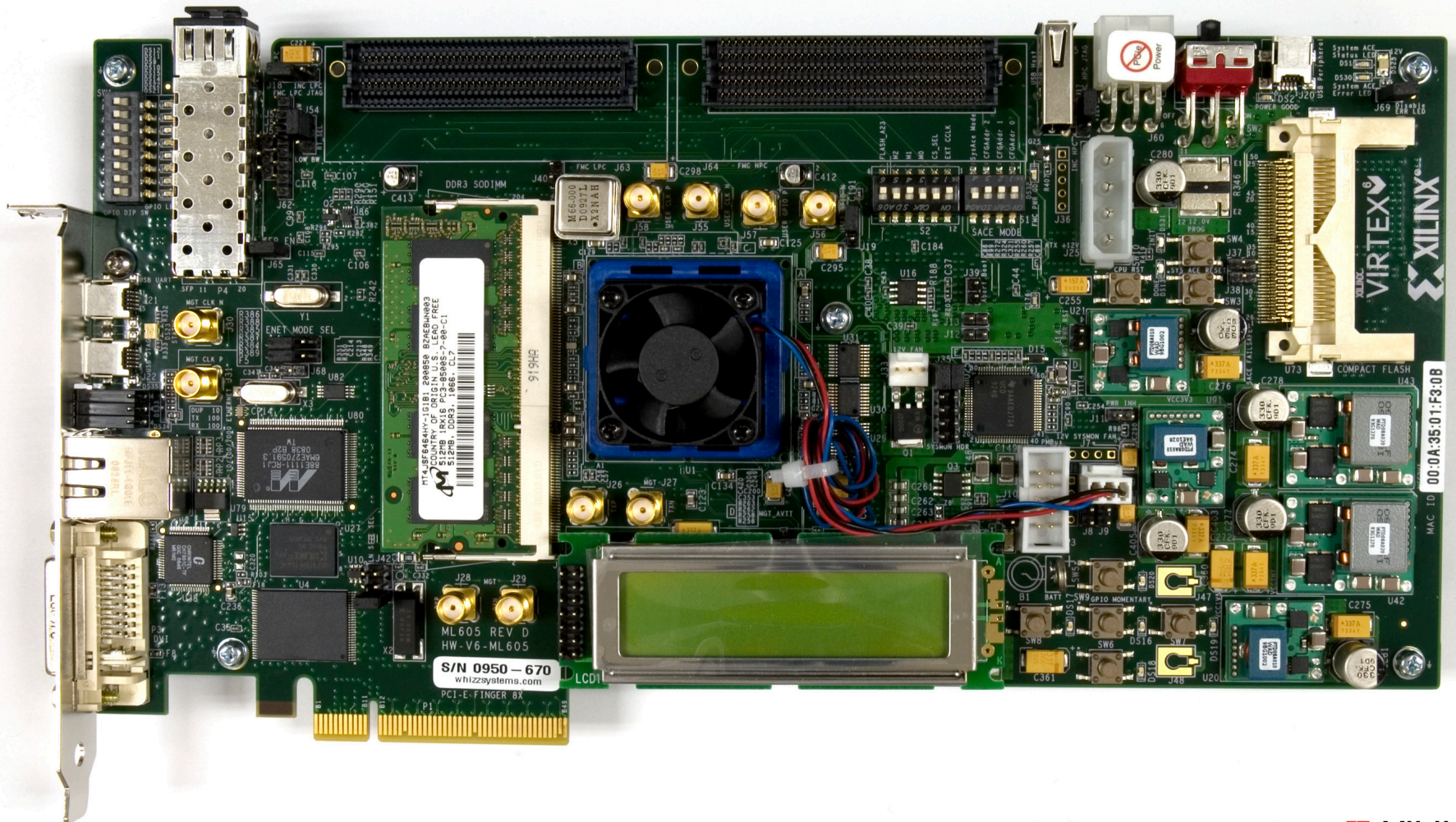
- **Virtex-6 PCIe x8 Gen1 Capability**
- **Xilinx ML605 Board**
- **Software Requirements**
- **Generate PCIe Core**
- **Compile PCIe Core**
- **Program Platform Flash with PCIe Design**
- **ML605 Setup**
- **Running the PCIe x8 Gen1 Design**
- **References**
  - IP Release Notes Guide [XTP025](#)

# Virtex-6 PCIe x8 Gen1 Capability

- **Integrated Block for PCI Express**
  - PCI Express Base 2.0 Specification
- **Generation 1 (2.5 GT/s) data rates**
  - x8, x4, x2, or x1 Gen1 lane width
- **Configurable for Endpoint or Root Port Applications**
  - ML605 configured for Endpoint Applications
- **GTX Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering
- **Management and Statistics Interface**

**Note:** Presentation applies to the ML605

# Xilinx ML605 Board



Note: Presentation applies to the ML605

# ISE Software Requirements

- **Xilinx ISE 12.1 software**



# PciTree Software Requirement

## ■ PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory

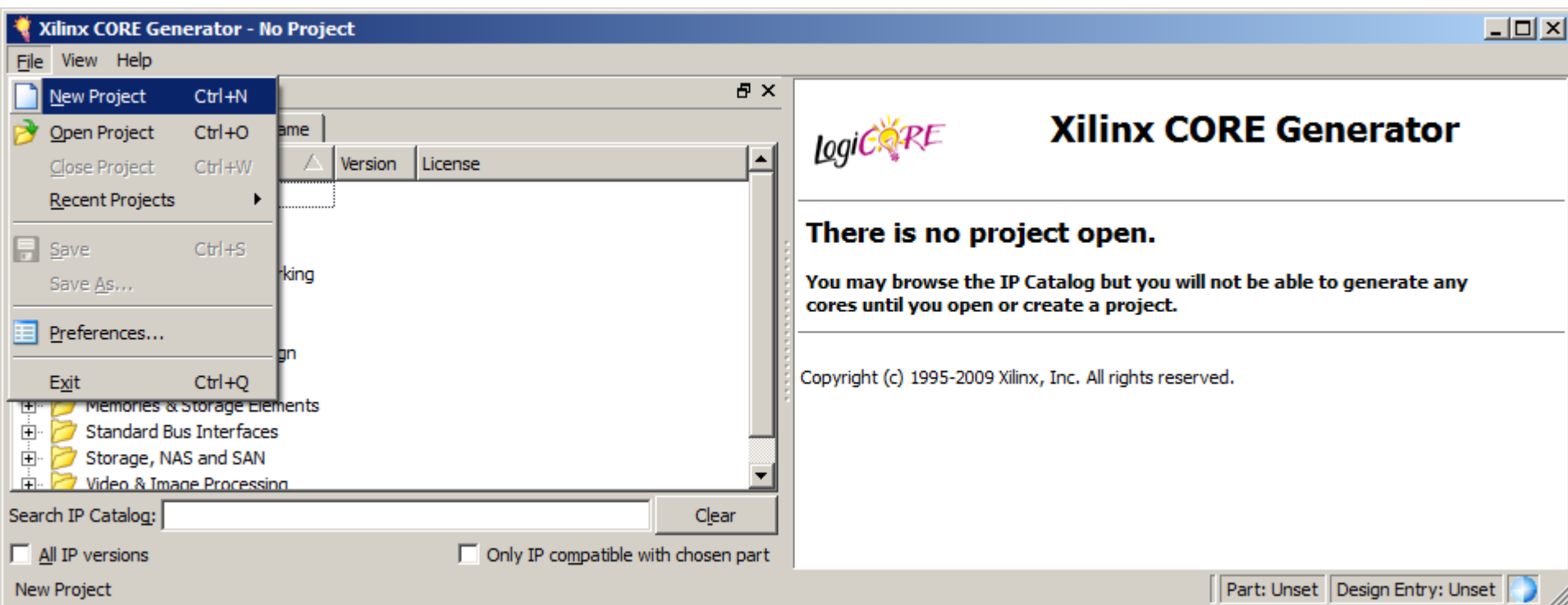


# Generate PCIe Core

- **Open the CORE Generator**

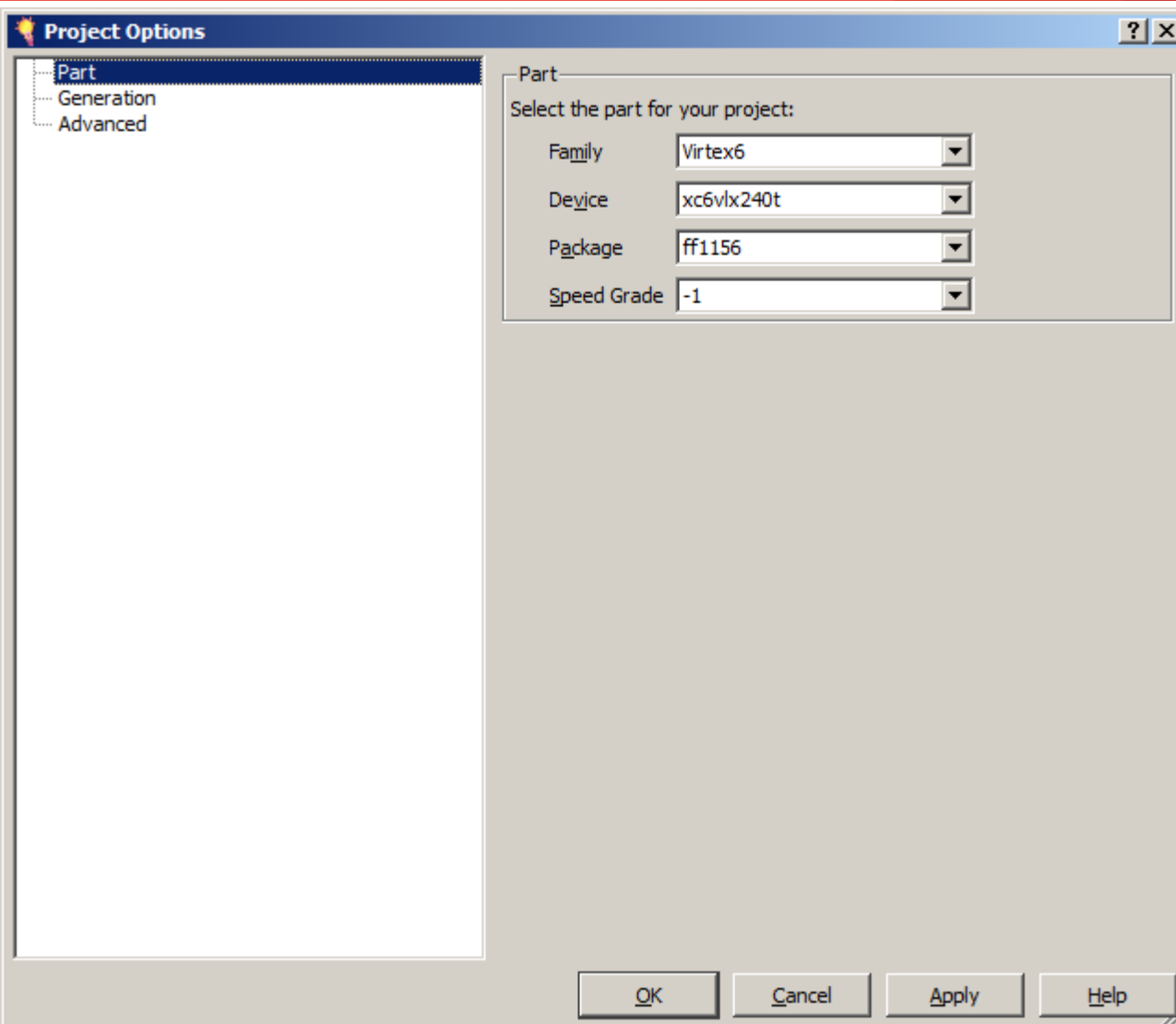
**Start → All Programs → Xilinx ISE Design Suite 12.1 → ISE → Accessories → CORE Generator**

- **Create a new project; select File → New Project**



**Note:** Pre-built design, RDF0008, available through <http://www.xilinx.com/ml605>

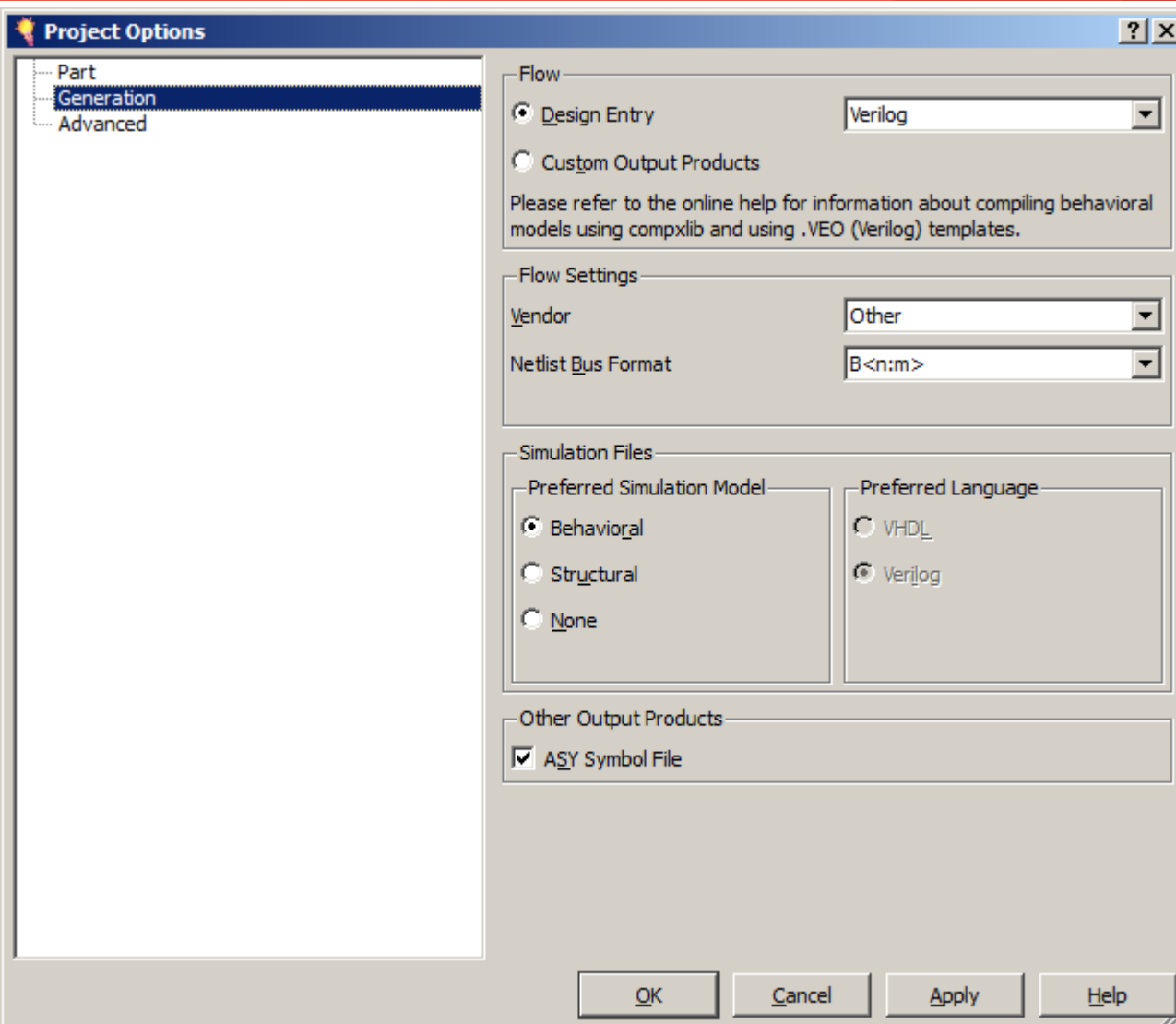
# Generate PCIe Core



- **Create a project directory:**  
ml605\_pcie\_x8\_gen1
- **Name the project:**  
ml605\_pcie\_x8\_gen1.cgp
- **The Project options will appear**
- **Set the Part (as seen here):**
  - Family: Virtex6
  - Device: xc6vlx240t
  - Package: ff1156
  - Speed Grade: -1



# Generate PCIe Core



- Select Generation
- Set the Design Entry to Verilog
- Click OK

**Note:** Presentation applies to the ML605

# Generate PCIe Core

## ▪ Select

- Virtex-6 Integrated Block for PCI Express, **Version 1.5**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog window is open, displaying a tree view of IP blocks. The 'PCI Express' folder is expanded, and the 'Virtex-6 Integrated Block for PCI Express' is selected. The table below shows the details of the selected IP block.

Name	Version	Status	License
Endpoint Block Plus for PCI Express	1.14	Production	
Endpoint for PCI Express	3.7	Production	
Endpoint PIPE for PCI Express	1.7	Production	
Spartan-6 Integrated Block for PCI Express	1.3	Pre-Production	
<b>Virtex-6 Integrated Block for PCI Express</b>	<b>1.5</b>	<b>Production</b>	

The right-hand pane displays the details for the selected IP block:

- LogiCORE** logo
- Virtex-6 Integrated Block for PCI Express**
- [Show Project](#) button
- Text: "This core is supported at status **Production** by your chosen part."
- Information** section:
  - Core type: Virtex-6 Integrated Block for PCI Express
  - Version: 1.5
  - Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane) uses the Virtex(TM)-6 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-6 architectural features to implement a PCI Express Base Specification v2.0 compliant PCI Express Endpoint or Root Port. Unique
- Part: xc6vix240t-1ff1156
- Design Entry: Verilog

**Note:** Presentation applies to the ML605

# Generate PCIe Core

- Right click on the **Virtex-6 Integrated Block for PCI Express, Version 1.5**
  - Select **Customize and Generate**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog is open, displaying a tree view of IP blocks. The 'Virtex-6 Integrated Block for PCI Express' is selected, and a context menu is open with 'Customize and Generate' highlighted. The details pane on the right shows the core's name, version (1.5), and status (Production). It also provides a core summary and design entry information.

Name	Version	Status	License
Endpoint Block Plus for PCI Express	1.14	Production	
Endpoint for PCI Express	3.7	Production	
Endpoint PIPE for PCI Express	1.7	Production	
Spartan-6 Integrated Block for PCI Express			
<b>Virtex-6 Integrated Block for PCI Express</b>			

**Virtex-6 Integrated Block for PCI Express**

This core is supported at status **Production** by your chosen part.

**Information**

Core type: Virtex-6 Integrated Block for PCI Express  
Version: 1.5  
Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane) uses the Virtex(TM)-6 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-6 architectural features to implement a PCI Express Base Specification v2.0 compliant PCI Express Endpoint or Root Port. Unique

Part: xc6vix240t-1ff1156 Design Entry: Verilog

**Note:** Presentation applies to the ML605

# Generate PCIe Core

**Virtex-6 Integrated Block for PCI Express** 1.5

Component Name

**PCIe Device / Port Type**  
The Integrated Block for PCI Express allows selection of the Device / Port Type  
Device / Port Type

**Number of Lanes**  
The Integrated Block for PCI Express requires that an initial lane width be selected. Wider lane width cores can train down to smaller lane widths if attached to a smaller lane width device. Select only the lane width that is necessary for the design.  
Lane Width

**Link Speed**  
The Integrated Block for PCI Express allows selection of the Maximum Link Speed support  
 2.5 GT/s  
 5.0 GT/s

**Interface Frequency**  
The Integrated Block for PCI Express allows selection of the interface clock (trn\_clk) frequency. The frequency selection enables maximum achievable data throughput for the selected number of lanes and link speed. Choice of non-default option results in interface being overclocked with no overall effect on data throughput, and depends on user application functional requirements, timing closure and power considerations. Xilinx recommends that the default frequency value be used where possible..  
Frequency (MHz)

[Datasheet](#) [< Back](#) Page 1 of 11 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

- Set the lane Width to X8
- Click Next

# Generate PCIe Core

**Virtex-6 Integrated Block for PCI Express**

logiCORE Virtex-6 Integrated Block for PCI Express 1.5

Base Address Registers

Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.

**BAR 0 Options**

Bar0 Type **Memory**  64 bit  Prefetchable  
Size **1** **Megabytes**  
Value **FFF00000** (Hex)

**BAR 1 Options**

Bar1 Type **N/A**  64 bit  Prefetchable  
Size **2** **Kilobytes**  
Value **00000000** (Hex)

**BAR 2 Options**

Bar2 Type **N/A**  64 bit  Prefetchable  
Size **128** **Bytes**  
Value **00000000** (Hex)

**BAR 3 Options**

Bar3 Type **N/A**  64 bit  Prefetchable  
Size **2** **Kilobytes**  
Value **00000000** (Hex)

**BAR 4 Options**

Bar4 Type **N/A**  64 bit  Prefetchable  
Size **2** **Kilobytes**  
Value **00000000** (Hex)

**BAR 5 Options**

Bar5 Type **N/A**  Prefetchable  
Size **2** **Kilobytes**  
Value **00000000** (Hex)

Expansion ROM Base Address Register

Expansion Rom Size **2** **Kilobytes**  
Value **00000000** (Hex)

[Datasheet](#) [< Back](#) [Page 2 of 11](#) [Next >](#) [Generate](#) [Cancel](#) [Help](#)

- **BAR 0**
  - Set to 1 Megabytes
- **BAR 2**
  - Deselect BAR 2
- **Click Next**

# Generate PCIe Core

**Virtex-6 Integrated Block for PCI Express** 1.5

**ID Initial Values**

Vendor ID	10EE	Range: 0000..FFFF
Device ID	6018	Range: 0000..FFFF
Revision ID	00	Range: 00..FF
Subsystem Vendor ID	10EE	Range: 0000..FFFF
Subsystem ID	0007	Range: 0000..FFFF

**Class Code**

Base Class	05	Range: 00..FF
Sub-Class	00	Range: 00..FF
Interface	00	Range: 00..FF
Class Code	050000	(Hex)

**Class Code Lookup Assistant**

Must enter values above.

Base Class	Simple communication controllers
Base Class	07h
Sub-Class/Interface Value	Generic XT compatible serial controller
Sub-Class	00h
Interface	00h

**Cardbus CIS Pointer**

Cardbus CIS Pointer	00000000	Range: 00000000..FFFFFFFF
---------------------	----------	---------------------------

[Datasheet](#) < Back Page 3 of 11 Next > Generate Cancel Help

## ■ Note ID Initial Values

- Vendor ID = **10EE**
- Device ID = 6018
- Revision ID = **00**
- Subsystem Vendor ID = **10EE**
- Subsystem ID = **0007**

## ■ Click Next 6 times

# Generate PCIe Core

Virtex-6 Integrated Block for PCI Express

**Virtex-6 Integrated Block for PCI Express** 1.5

Pinout Selection

Xilinx Development Boards

Generate Xilinx Development Board specific UCF

Xilinx Development Board ML 605

PCIe Block Location Selection

Selects from available PCIe Block locations for a part-package combination which determines Pinout.

PCIe Block Location X0Y0

Datasheet < Back Page 9 of 11 Next > Generate Cancel Help

- On Page 9
  - Select ML605
- Click Next 2 times

# Generate PCIe Core

Virtex-6 Integrated Block for PCI Express

**Virtex-6 Integrated Block for PCI Express** 1.5

Advanced Settings 2

Advanced Physical Layer Settings

Enable Lane Reversal  Force No Scrambling

Upconfigure Capable  Disable TX ASPM L0s

Pipeline for PIPE Interface: None

Link Number: 00 Range: 00..FF

DRP Ports

PCIe DRP Ports

Reference Clock Frequency

The Integrated Block for PCI Express allows selection of the reference clock frequency

Frequency (MHz): 250 MHz

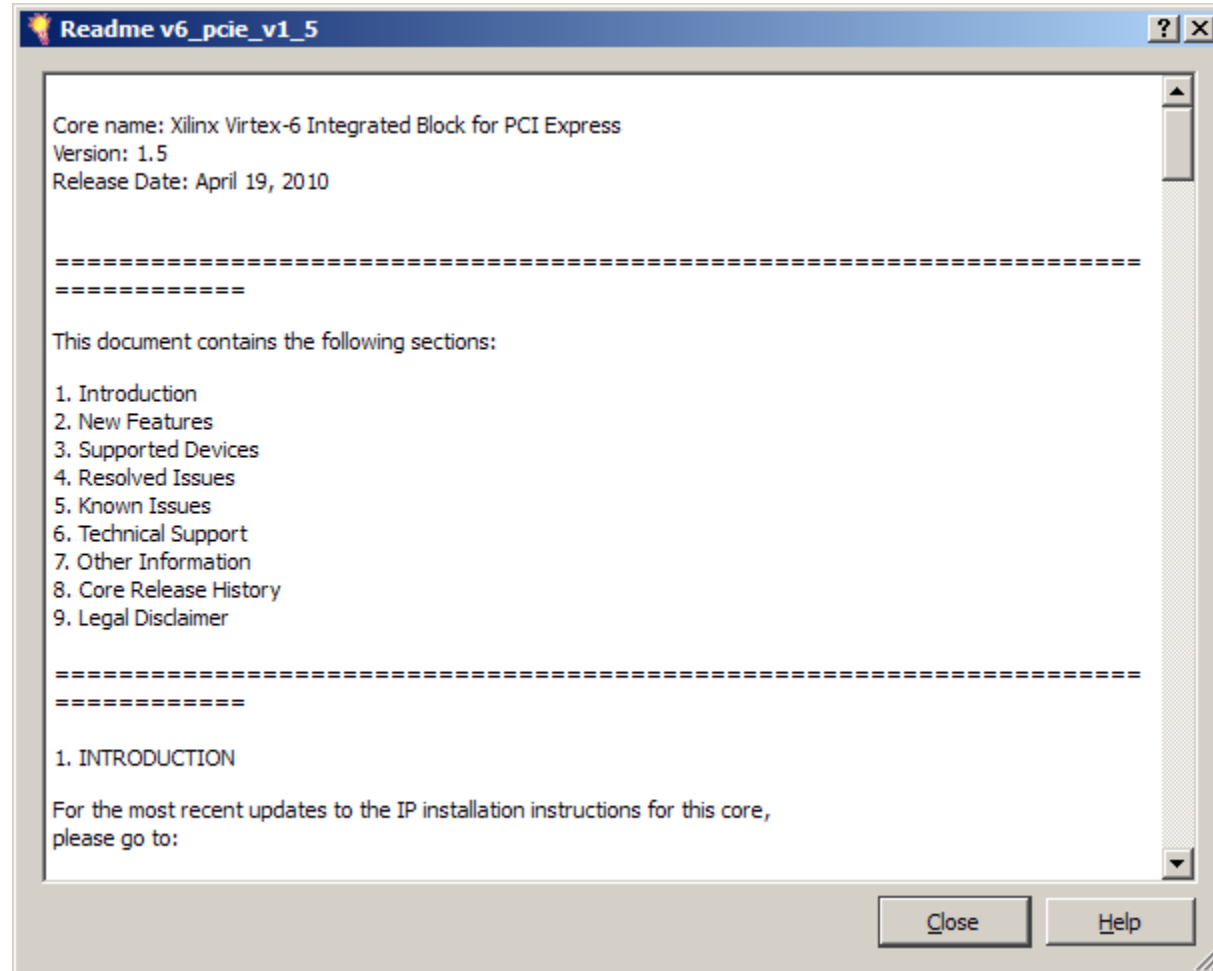
Datasheet < Back Page 11 of 11 Next > Generate Cancel Help

- On Page 11
  - Set the Reference Clock Freq: **250 MHz**
- Click Generate



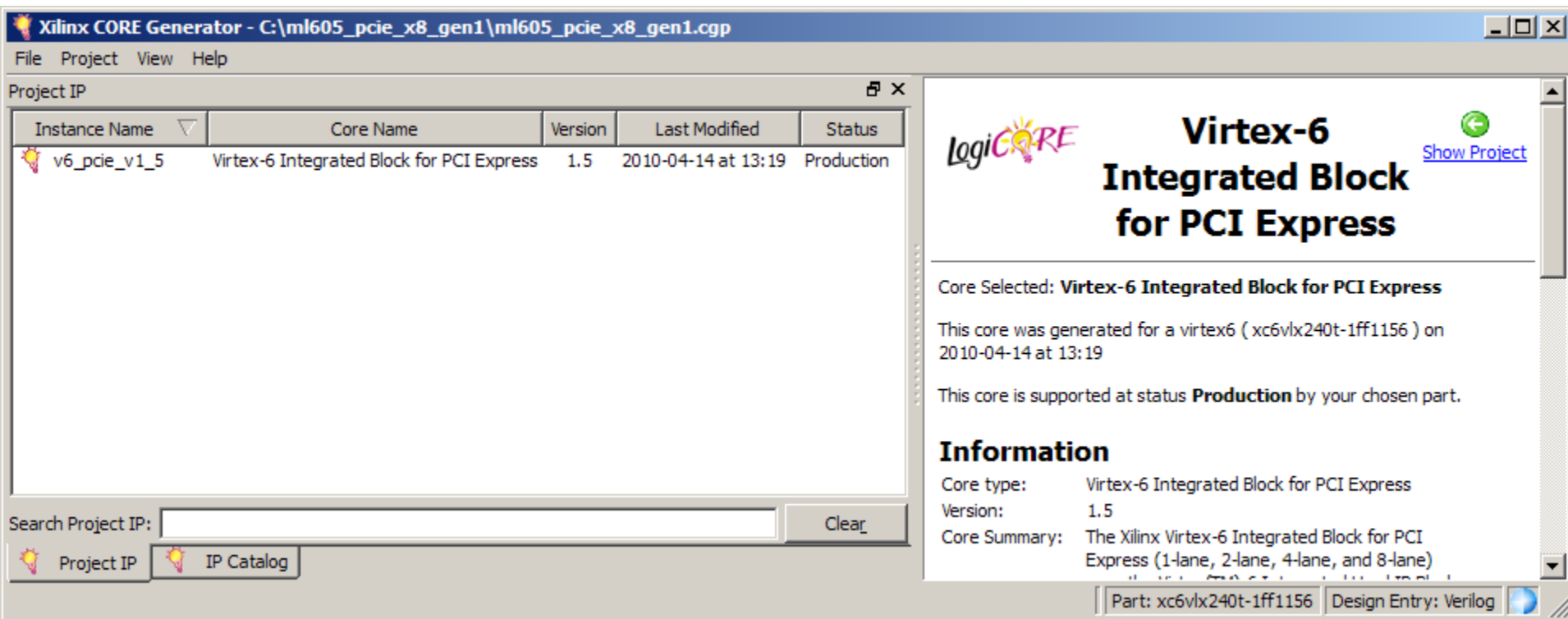
# Generate PCIe Core

- After the PCIe core finishes generating, click **Close** on the **Readme File** window



# Generate PCIe Core

- The v6\_pcie\_v1\_5 IP appears under the Project IP tab



The screenshot shows the Xilinx CORE Generator interface. The title bar reads "Xilinx CORE Generator - C:\ml605\_pcie\_x8\_gen1\ml605\_pcie\_x8\_gen1.cgp". The menu bar includes "File", "Project", "View", and "Help". The "Project IP" tab is active, displaying a table with the following data:

Instance Name	Core Name	Version	Last Modified	Status
v6_pcie_v1_5	Virtex-6 Integrated Block for PCI Express	1.5	2010-04-14 at 13:19	Production

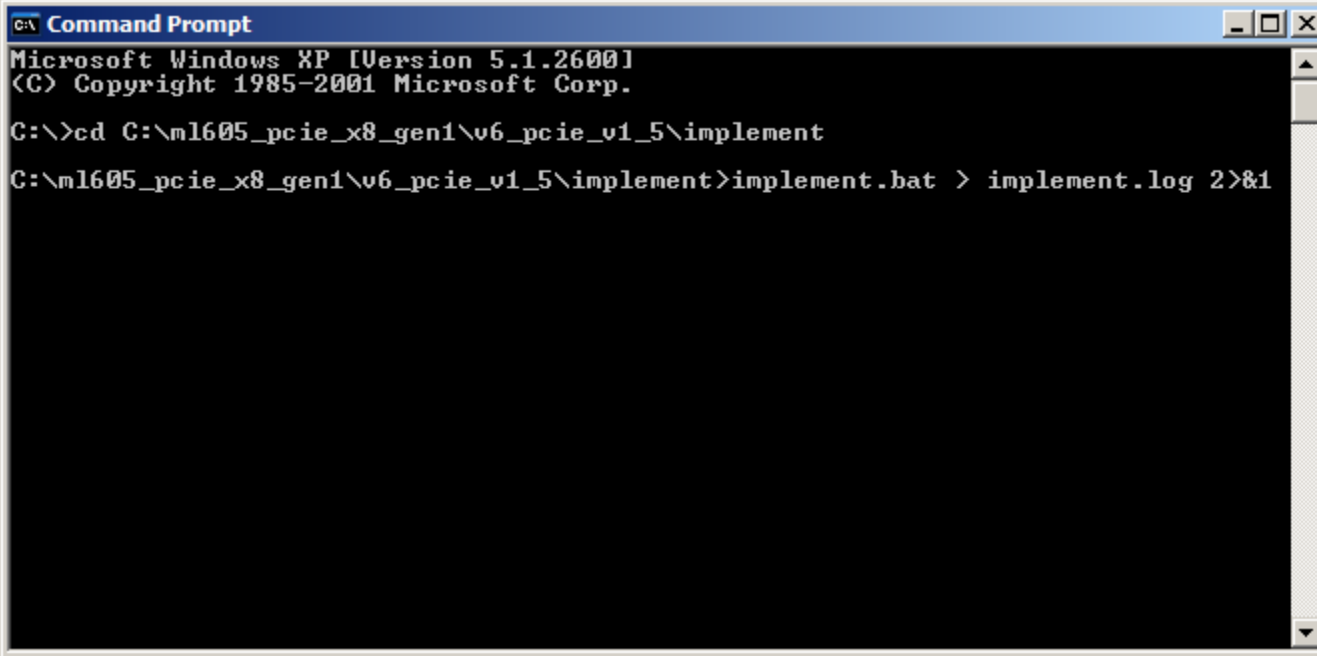
Below the table is a "Search Project IP:" field and a "Clear" button. At the bottom left, there are buttons for "Project IP" and "IP Catalog". The right-hand pane displays the details for the selected core:

- LogiCORE** logo
- Virtex-6 Integrated Block for PCI Express**
- [Show Project](#) button
- Core Selected: **Virtex-6 Integrated Block for PCI Express**
- This core was generated for a virtex6 ( xc6vlx240t-1ff1156 ) on 2010-04-14 at 13:19
- This core is supported at status **Production** by your chosen part.
- Information**
- Core type: Virtex-6 Integrated Block for PCI Express
- Version: 1.5
- Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane)
- Part: xc6vlx240t-1ff1156 | Design Entry: Verilog

# Compile PCIe Core

- **Type these commands in a windows command shell:**

```
cd C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement  
implement.bat > implement.log 2>&1
```

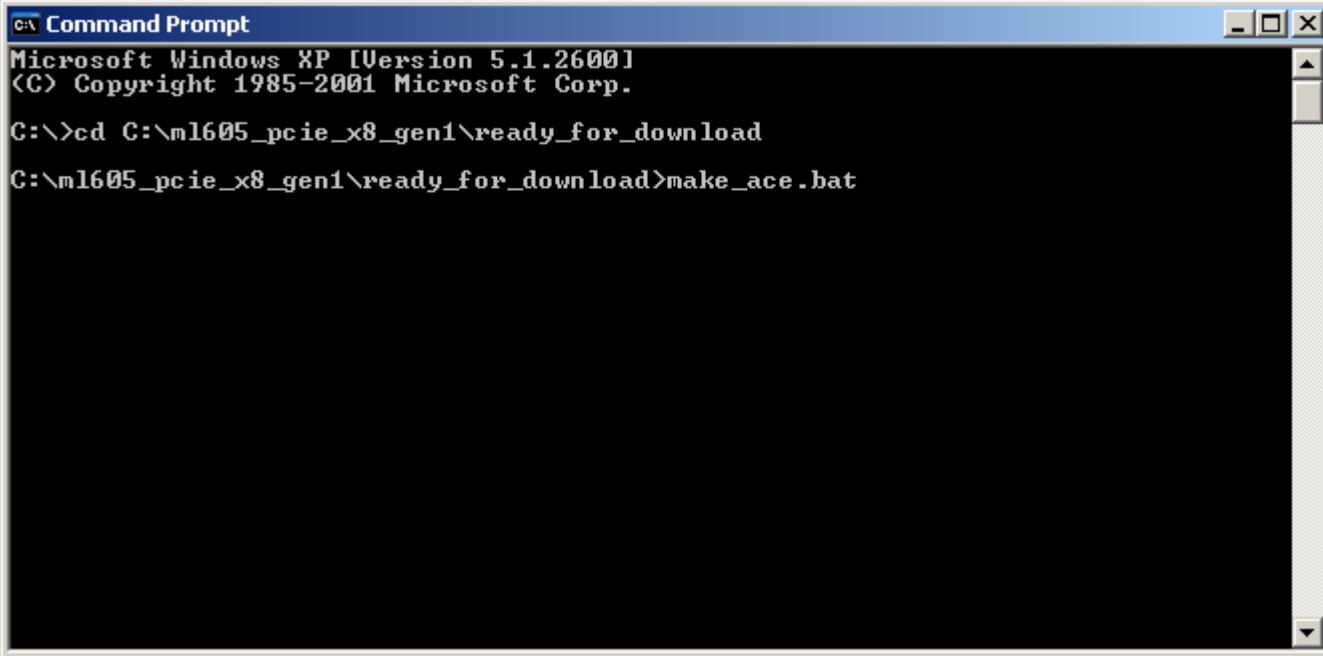


```
C:\> Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
<C> Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement  
C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement>implement.bat > implement.log 2>&1
```

# Create PCIe ACE File (Optional)

- Type these commands in a windows command shell:

```
cd C:\ml605_pcie_x8_gen1\ready_for_download  
make_ace.bat
```



```
C:\> Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd C:\ml605_pcie_x8_gen1\ready_for_download  
C:\ml605_pcie_x8_gen1\ready_for_download>make_ace.bat
```

**Note:** The make\_ace.bat file is included with RDF0008

# Program Platform Flash with PCIe Design

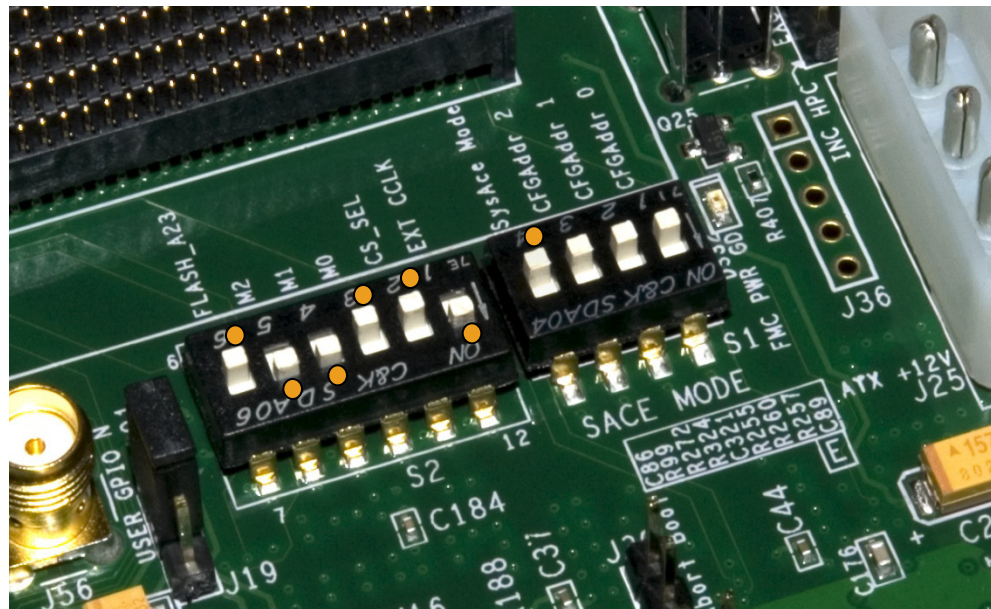
- **Power on the ML605**
- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
  - Connect this cable to your PC



**Note:** Presentation applies to the ML605

# Program Platform Flash with PCIe Design

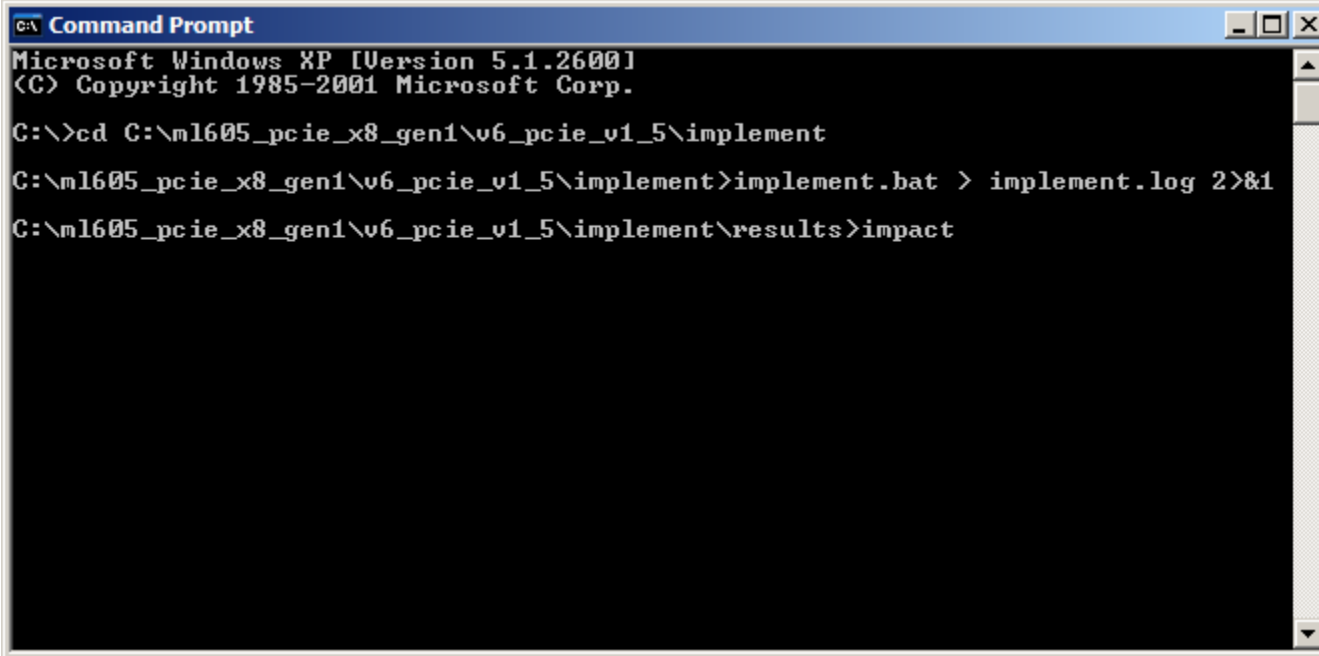
- **Set S2 to 011001 (1 = on, Position 6 → Position 1)**
  - This selects Slave SelectMAP (Positions 5, 4, and 3), Platform Flash (2) and EXT CCLK (1, for PCIe compliance)
- **Set S1 to 0XXX (X = Don't care, Position 4 → Position 1)**
  - This disables the Compact Flash



# Program Platform Flash with PCIe Design

- **Run iMPACT:**

**impact**



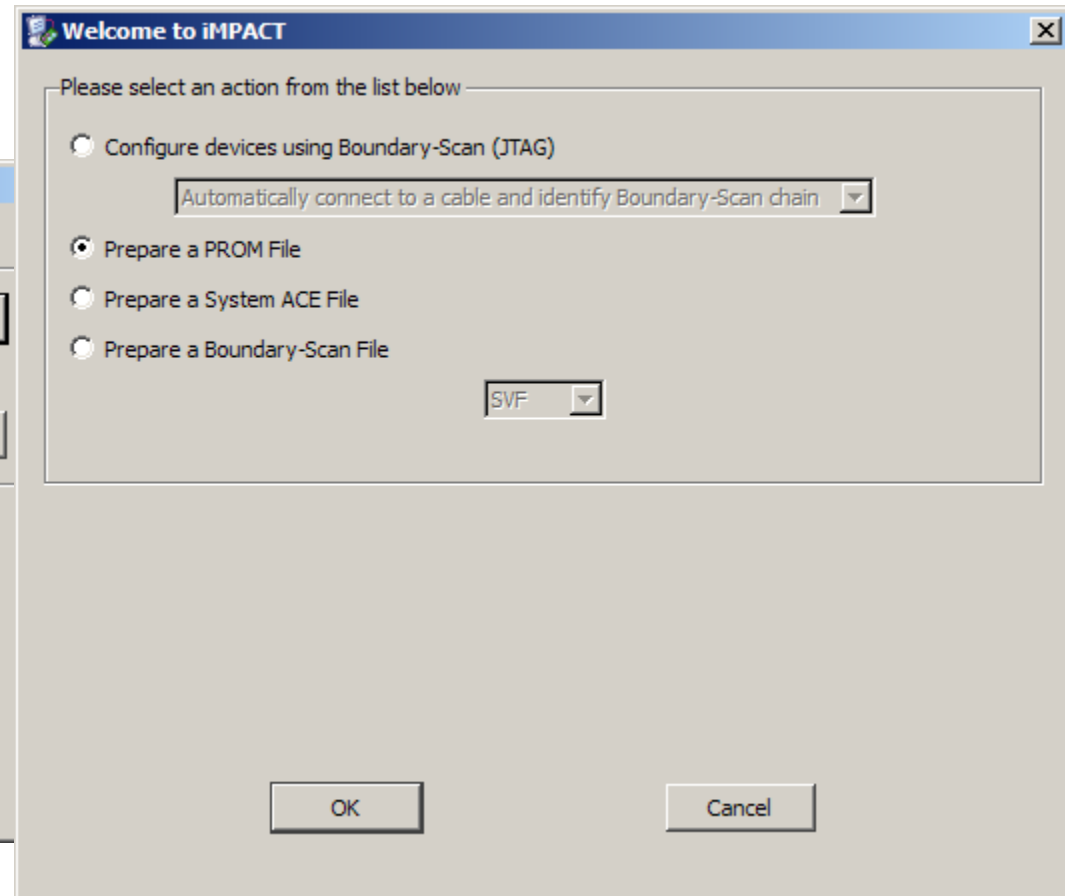
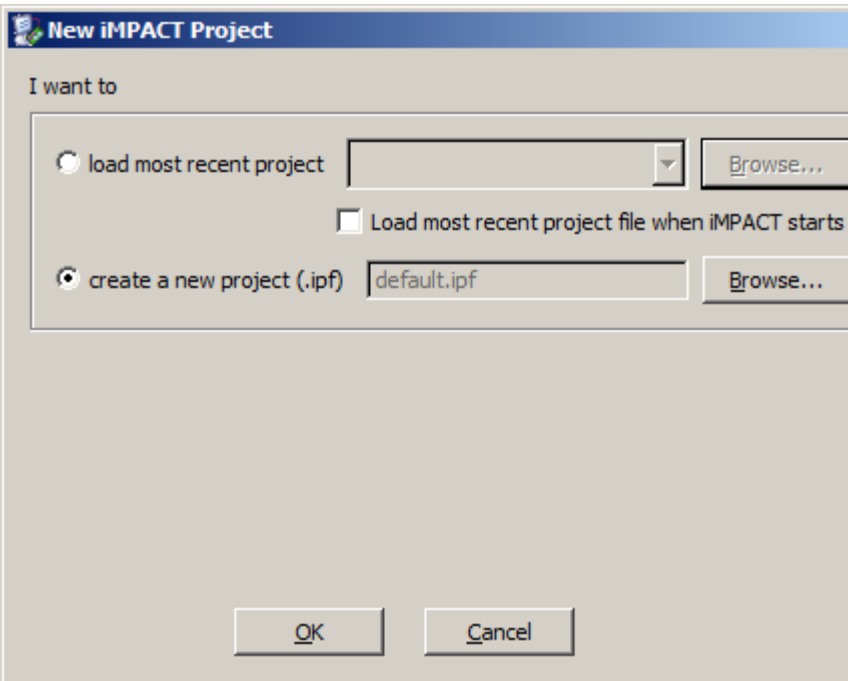
```
C:\ Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement
C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement>implement.bat > implement.log 2>&1
C:\ml605_pcie_x8_gen1\v6_pcie_v1_5\implement\results>impact
```

# Program Platform Flash with PCIe Design

## ▪ Select

- Create a new project
- Prepare a PROM File





# Program Platform Flash with PCIe Design

- To generate a PROM file for the XCF128X Platform Flash, select:
  - BPI – Configure Single FPGA

The screenshot displays the PROM File Formatter application window, which is divided into three main steps:

- Step 1. Select Storage Target:** A tree view on the left shows the hierarchy of storage device types. Under "BPI Flash", the option "Configure Single FPGA" is selected and highlighted with a red dashed border. A green arrow button is located to the right of this selection.
- Step 2. Add Storage Device(s):** This section contains two dropdown menus: "Target FPGA" set to "Spartan3E" and "Storage Device (bits)" set to "512K". Below these are two buttons: "Add Storage Device" and "Remove Storage Device".
- Step 3. Enter Data:** This section contains two tables for configuring file properties.

**General File Detail Table:**

Property	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	_x8_gen1\ready_for_download/

**Flash/PROM File Property Table:**

Property	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

# Program Platform Flash with PCIe Design

- Add xcf128x

The screenshot shows the PROM File Formatter software interface, which is divided into three main steps:

- Step 1. Select Storage Target:** A tree view on the left lists storage device types. Under "BPI Flash", the "Configure Single FPGA" option is selected. A green arrow points from this selection to the right.
- Step 2. Add Storage Device(s):** This panel shows configuration for the target FPGA. The "Target FPGA" is set to "Virtex6". The "Storage Device (Bytes)" is set to "xcf128x [16M]". A red box highlights the "Add Storage Device" button. Below this, a list shows "xcf128x [16M]" has been added.
- Step 3. Enter Data:** This panel contains two tables for file configuration. A red box highlights a green arrow pointing from the "Add Storage Device" button in Step 2 to the "Flash/PROM File Property" table.

General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	_x8_gen1\ready_for_download/

Flash/PROM File Property	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

**Note:** Presentation applies to the ML605

# Program Platform Flash with PCIe Design

- Set file name and location as desired and click OK

The screenshot shows the 'PROM File Formatter' dialog box, specifically Step 3: Enter Data. The dialog is divided into three steps:

- Step 1. Select Storage Target:** A tree view shows 'Storage Device Type' with categories like Xilinx Flash/PROM, Non-Volatile FPGA, SPI Flash, and BPI Flash. 'Configure Single FPGA' is selected under BPI Flash.
- Step 2. Add Storage Device(s):** 'Target FPGA' is set to 'Virtex6' and 'Storage Device (Bytes)' is 'xcf128x [16M]'. A list below shows 'xcf128x [16M]'.
- Step 3. Enter Data:** A table for 'General File Detail' and 'Flash/PROM File Property' is shown.

General File Detail	Value
Checksum Fill Value	FF
Output File Name	ml605_pcie_x8_gen1
Output File Location	_x8_gen1/ready_for_download

Flash/PROM File Property	Value
File Format	MCS
Add Non-Configuration Data Files	No

**Description:**

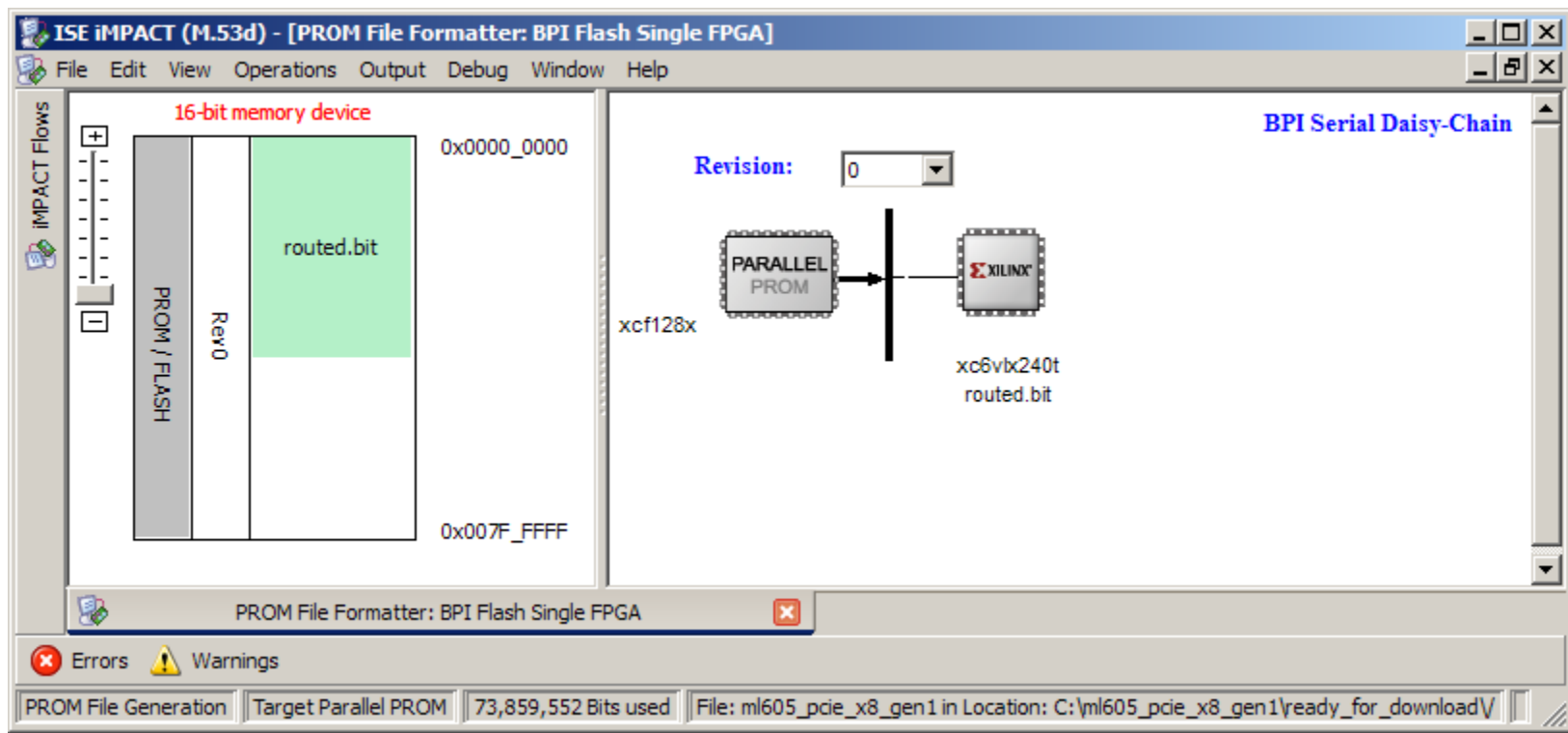
In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.

- **Checksum Fill Value:** When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
- **Output File Name:** This allows you to specify the base name of the file to which your PROM data will be written
- **Output File Location:** This allows you to specify the directory in which the file named above will be created
- **File Format:** PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a .TEK

Buttons: OK, Cancel, Help

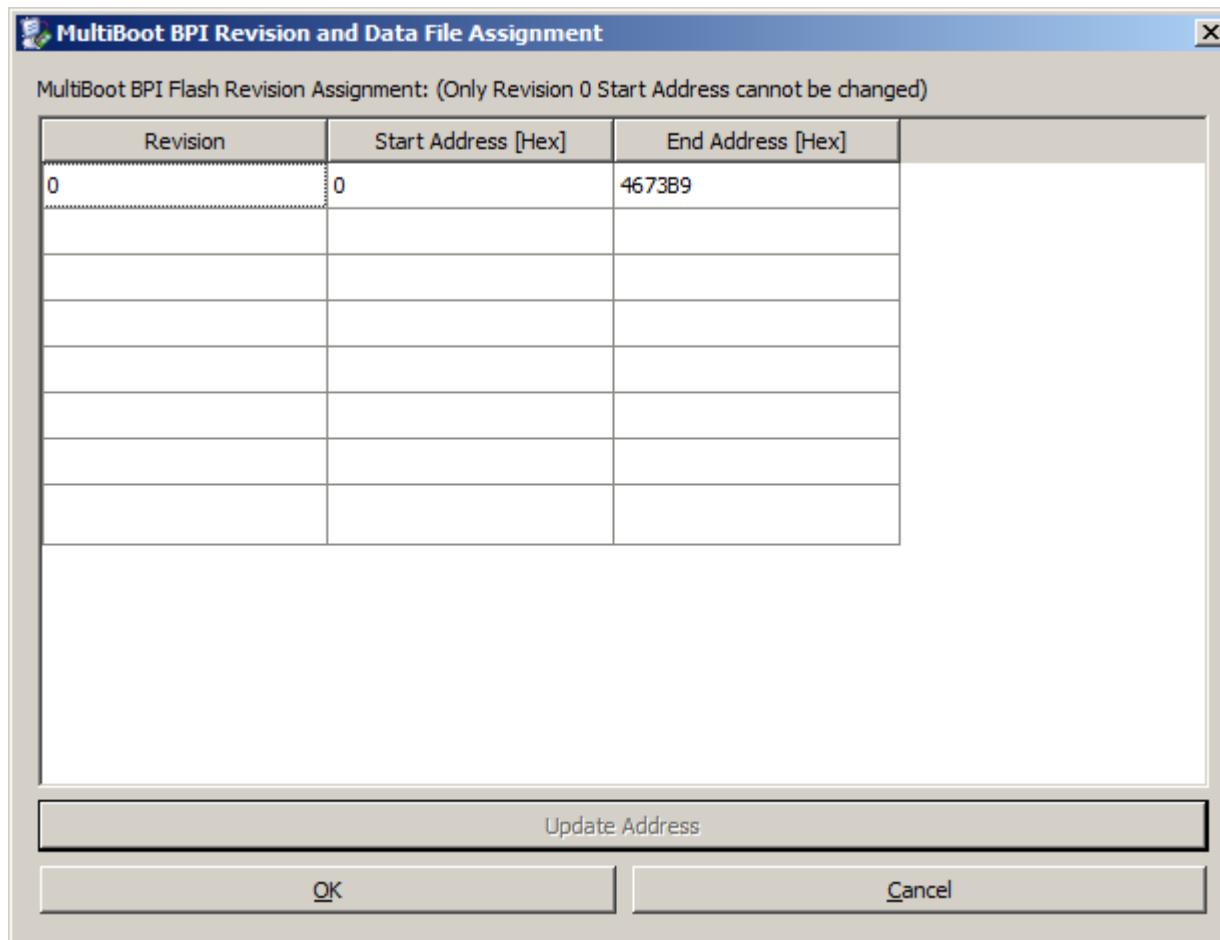
# Program Platform Flash with PCIe Design

- Add routed.bit from the <design path>\v6\_pcie\_v1\_5\implement\results



# Program Platform Flash with PCIe Design

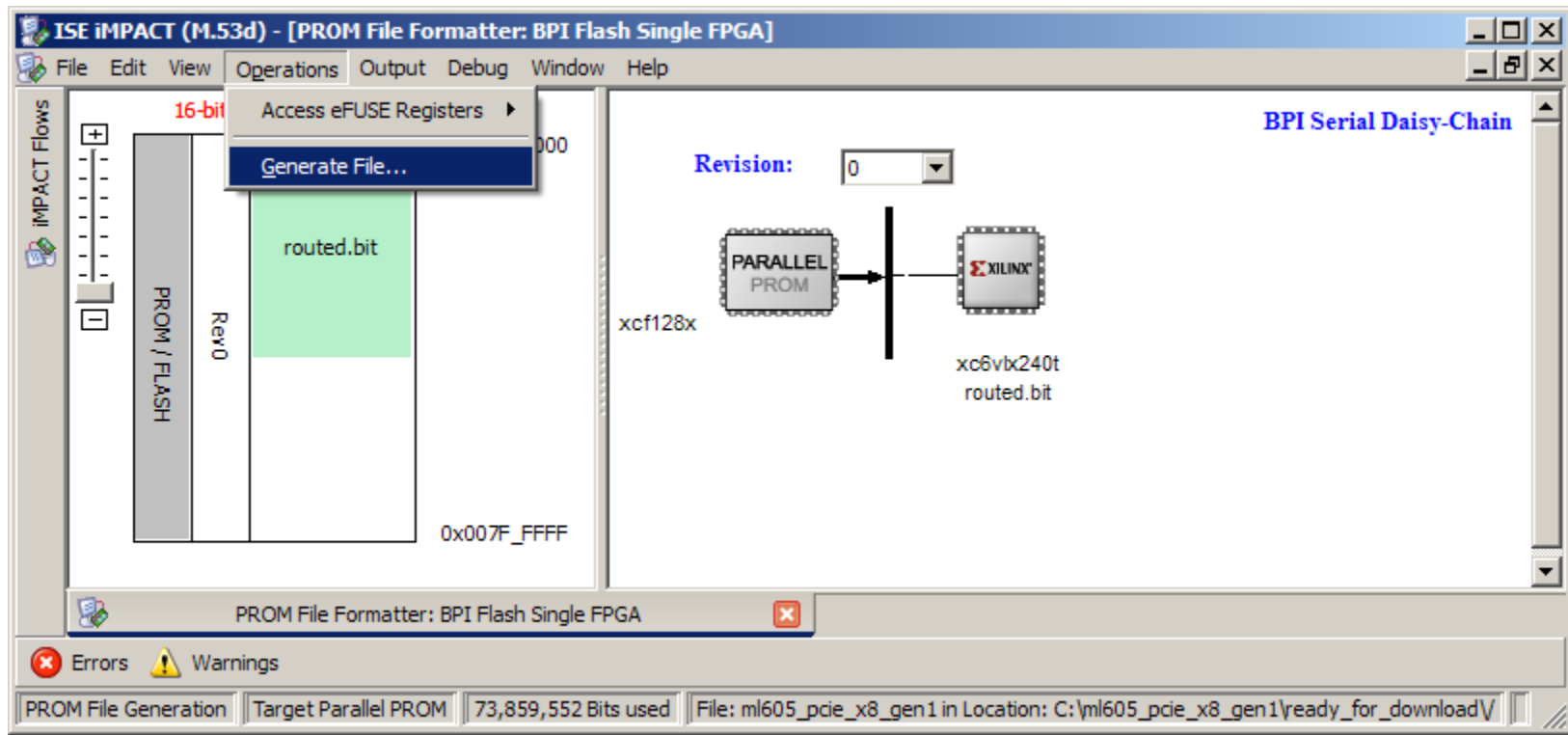
- Click OK on this dialog



**Note:** Presentation applies to the ML605

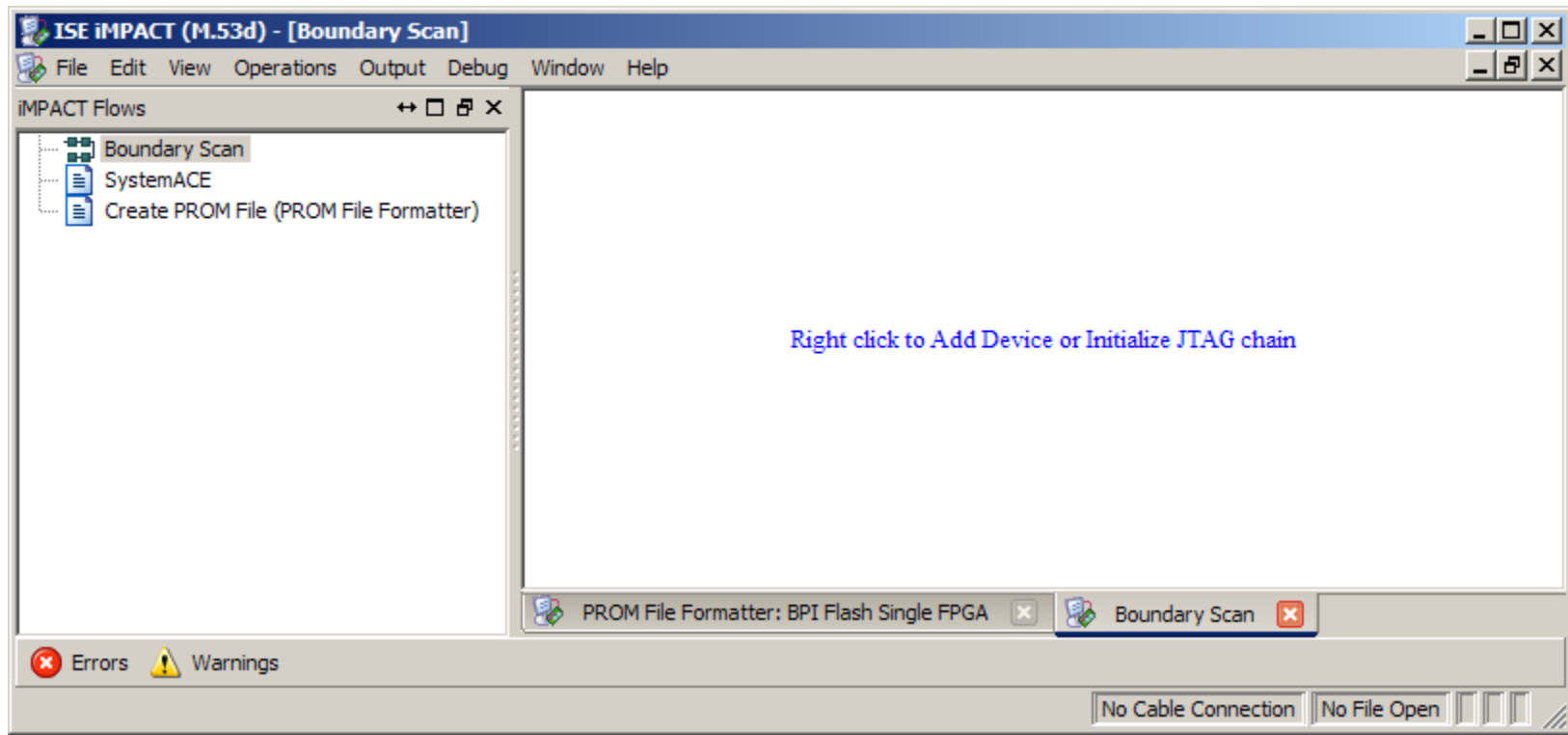
# Program Platform Flash with PCIe Design

- From the iMPACT menu, select  
Operations → Generate File...



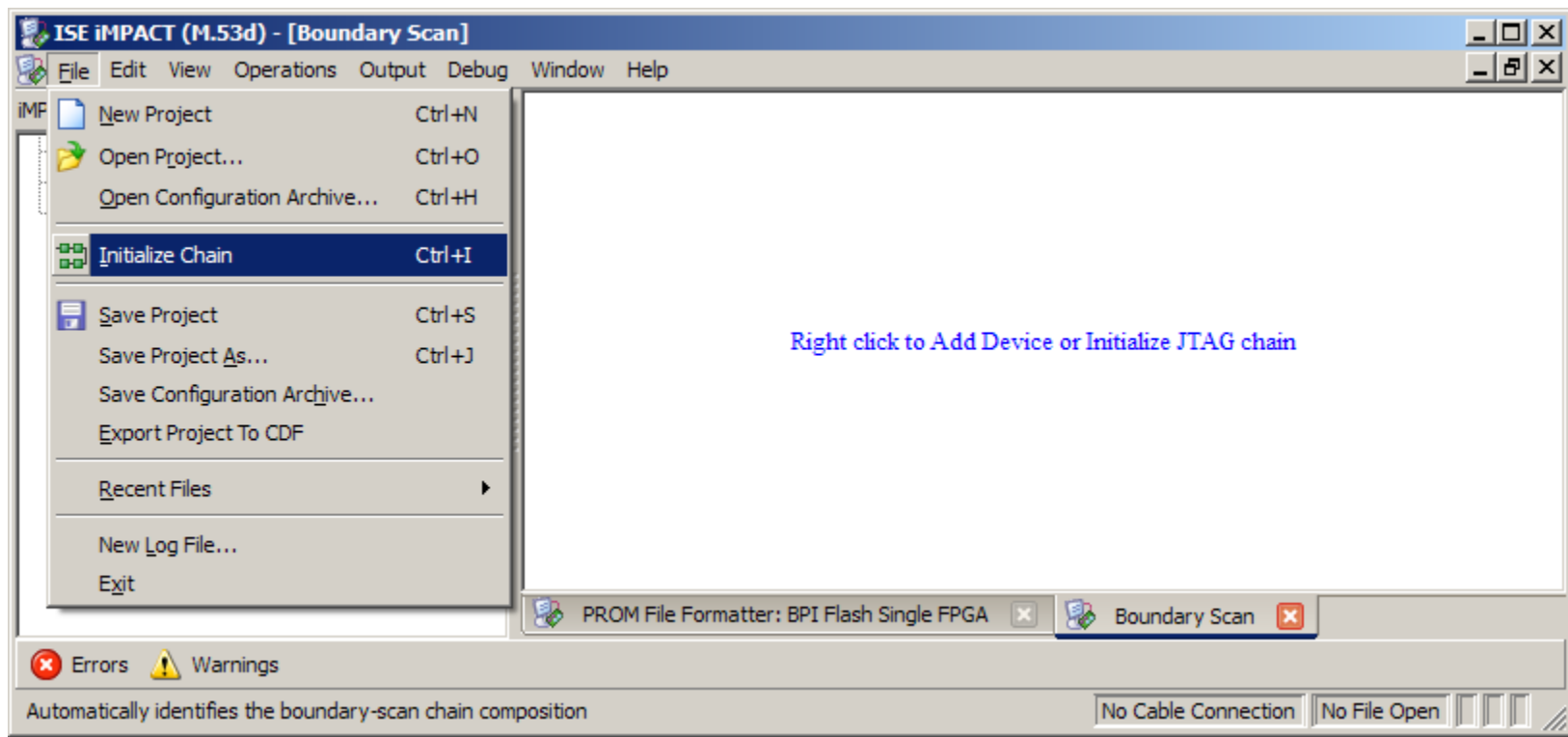
# Program Platform Flash with PCIe Design

- After generation completes, under the iMPACT Flows, double click on Boundary Scan



# Program Platform Flash with PCIe Design

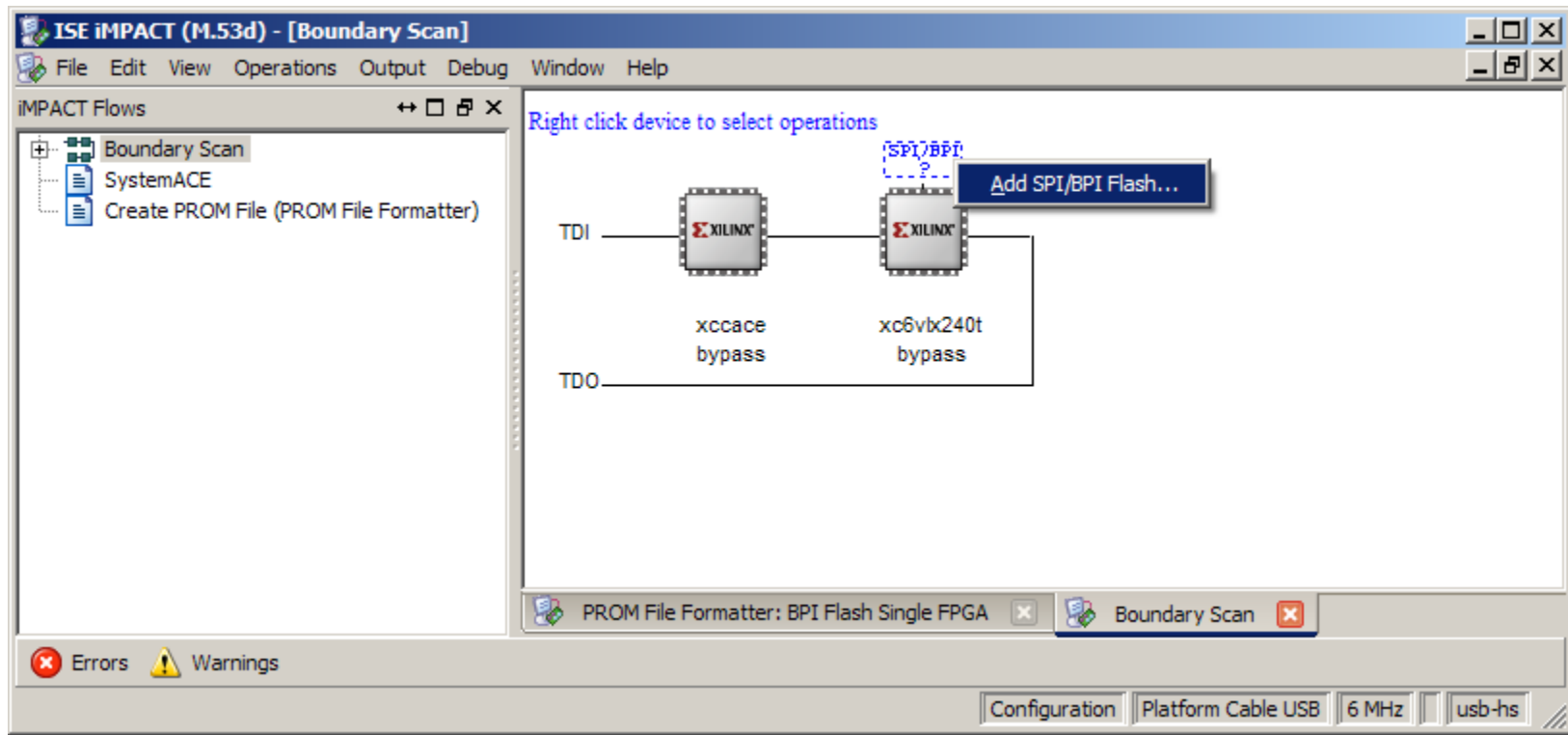
- From the iMPACT menu, select **File → Initialize Chain**





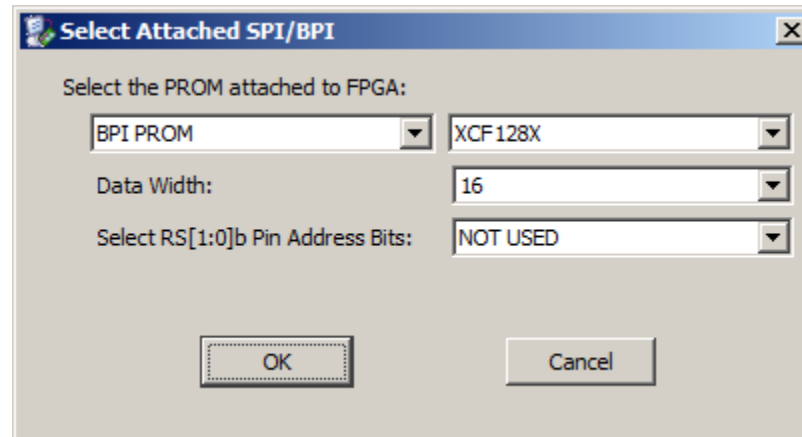
# Program Platform Flash with PCIe Design

- **Right click on the SPI/BPI ? and select Add SPI/BPI Flash...**
  - Add <design path>\ready\_for\_download\ml605\_pcie\_x8\_gen1.mcs



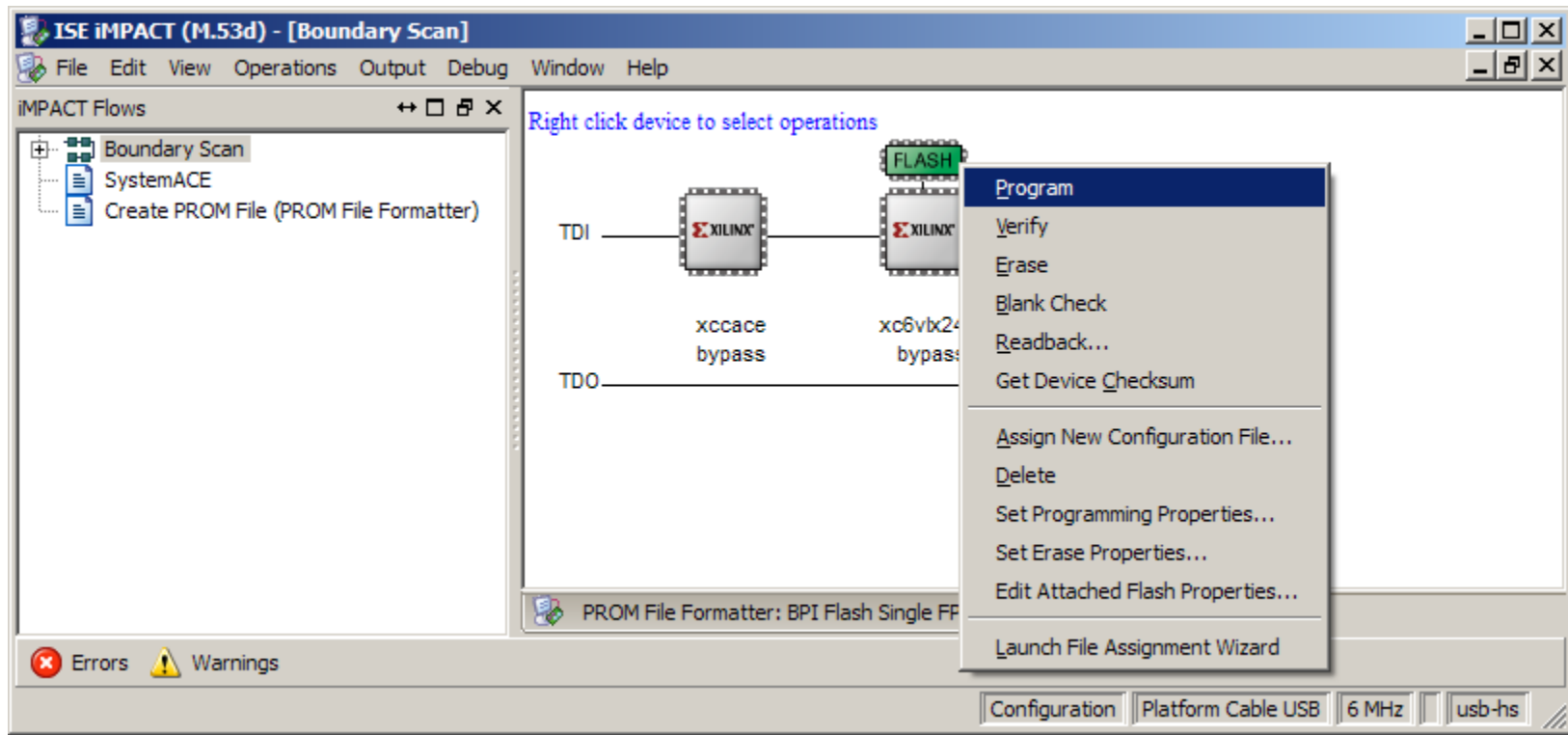
# Program Platform Flash with PCIe Design

- Click OK for this dialog



# Program Platform Flash with PCIe Design

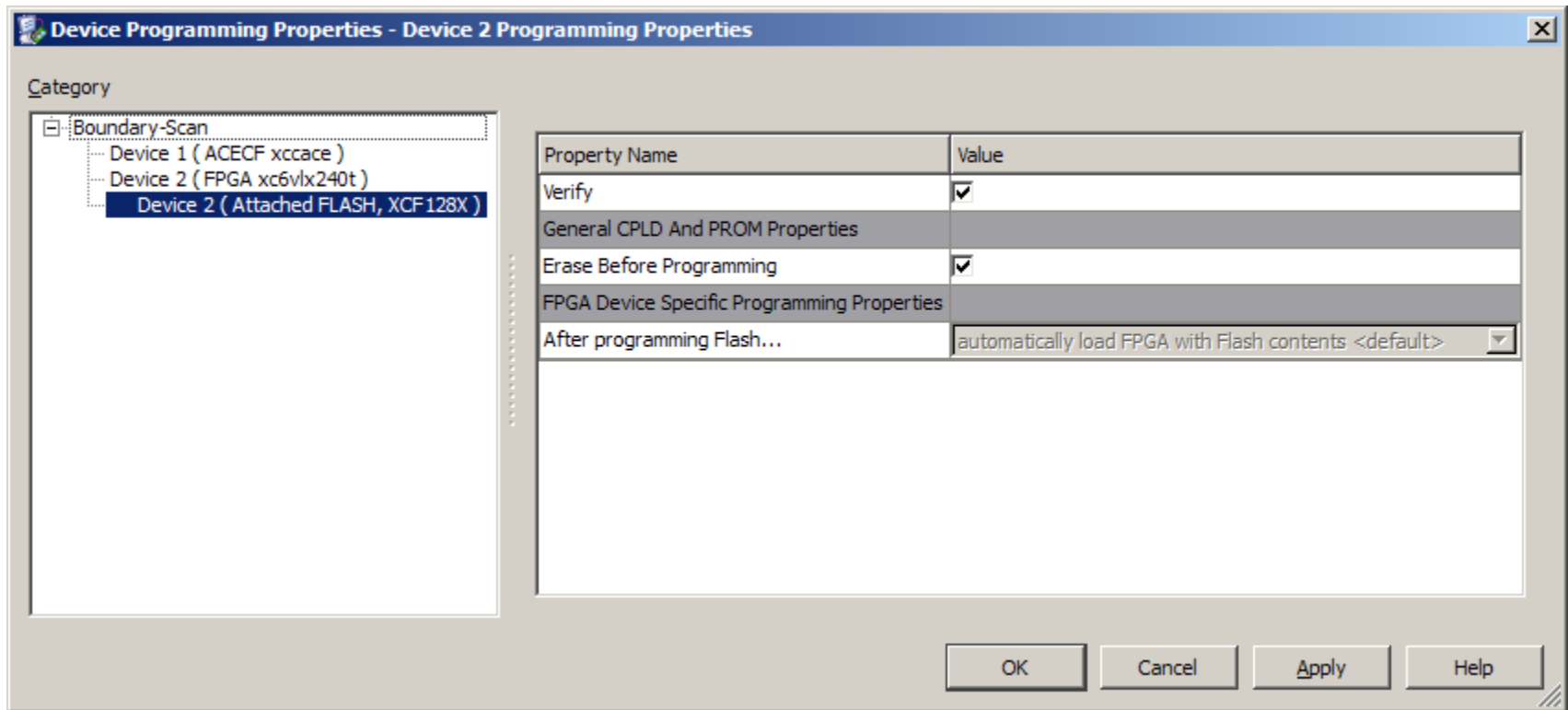
- **Right click on the Flash and select Program**
  - Use default settings to Erase and Verify device



**Note:** Programming takes about 12 minutes

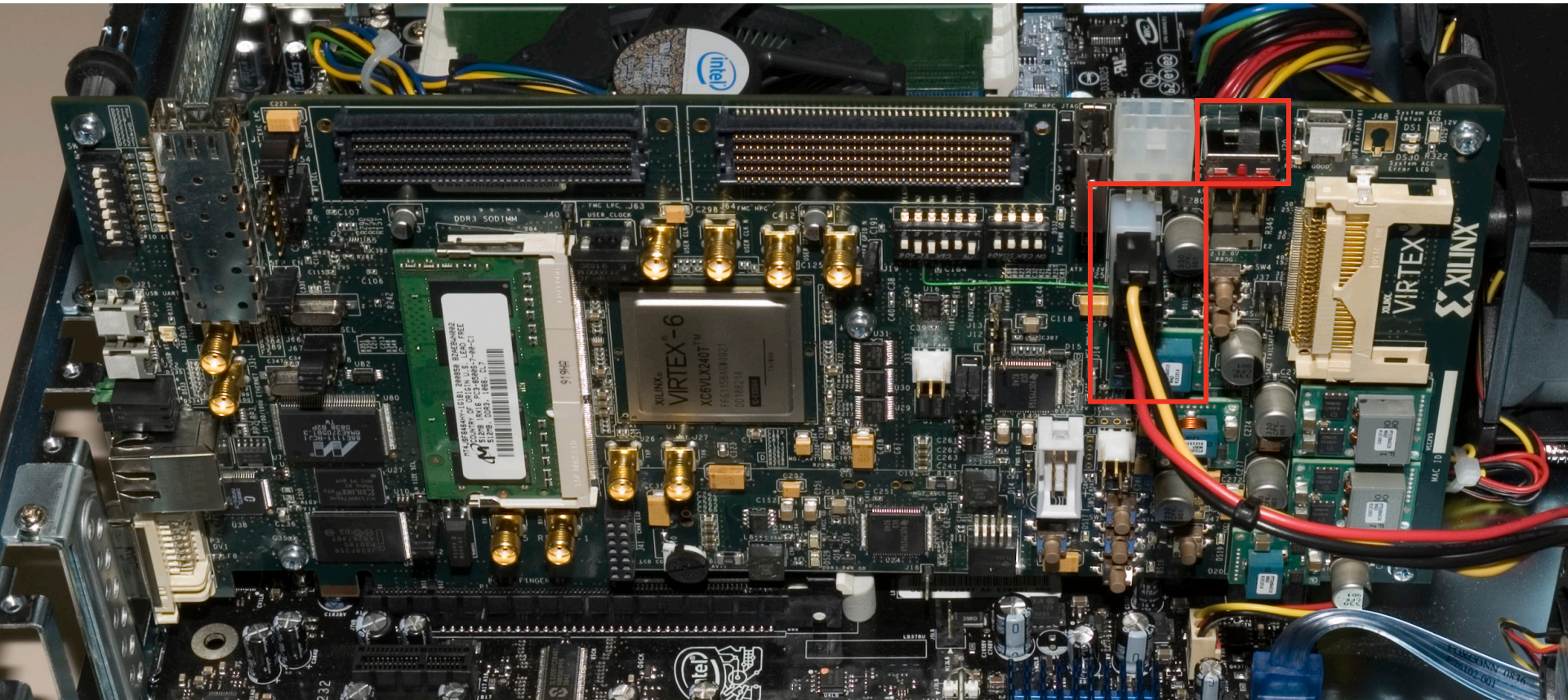
# Program Platform Flash with PCIe Design

- Erase Before Programming must be selected



# Hardware Setup

- Insert the ML605 Board into a PCIe x8 slot (x16 shown)
  - Connect PC power to J25, turn on Power Switch



Note: Presentation applies to the ML605

# Hardware Setup

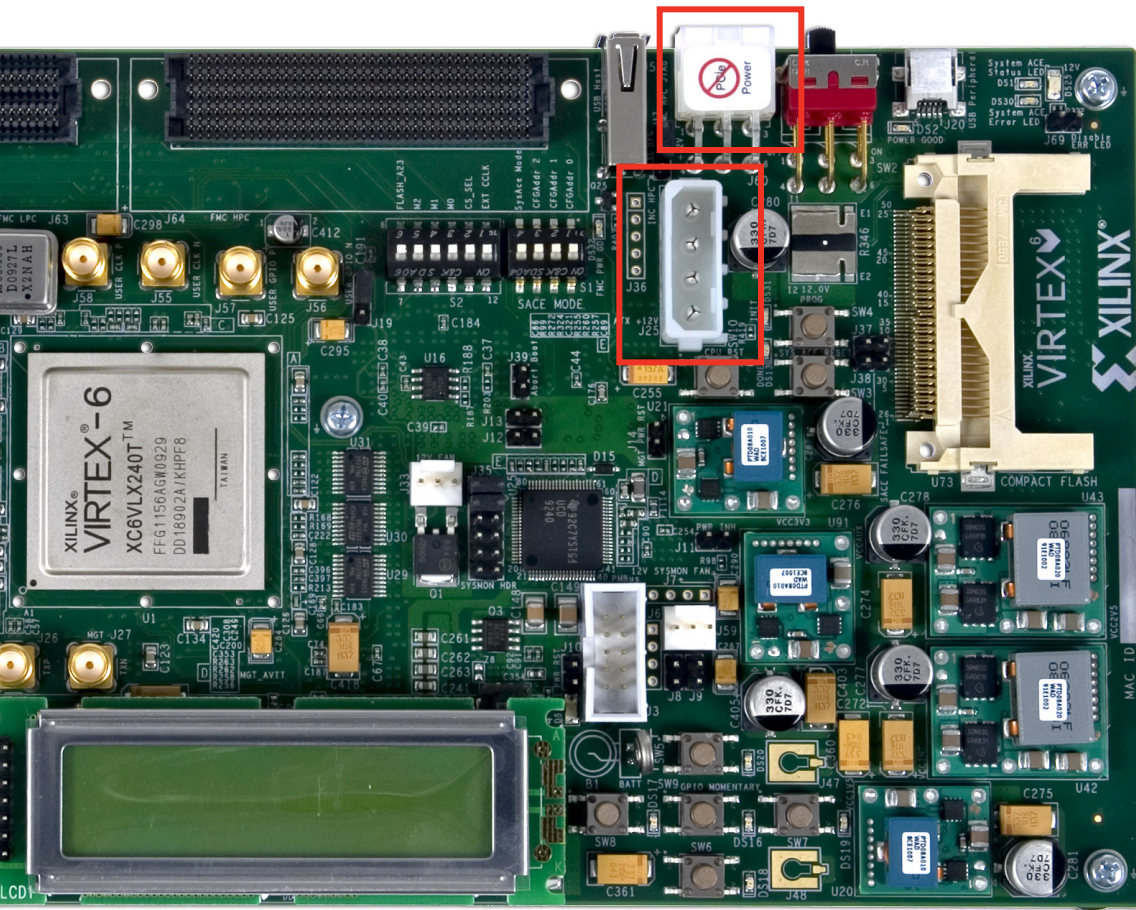
- Do not use the PCIe connector from the PC power supply



**Note:** Presentation applies to the ML605

# Hardware Setup

- Do not connect both the ML605 power brick connector (J60) and the four pin ATX power connector at the same time



Note: Presentation applies to the ML605

# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application window. The top menu bar includes "direct select:", "show INT routing", "highest", and "E X I T". Below the menu bar are input fields for "bus:", "dev:", and "func:" (all set to 0), a "show Mem Map" button, a "busnr:" field (set to 63), and an "About" button. The main window is divided into two panes. The left pane shows a tree view of PCI devices, with the root node "0.00.0 Host/PCI; Bridge" selected. The right pane displays the configuration details for the selected device, including VID, DID, SubVID, and SubID. It also features a "edit ConfReg:" section with a hex input field, a "Write ConfReg" button, and a "refresh" button with a smiley face icon. At the bottom of the right pane is a "Config Space Dump:" section showing a list of configuration registers and their values.

```
0.00.0 Host/PCI; Bridge
├── 0.01.0 0->1 (1) PCI/PCI;
├── 0.03.0 0->2 (2) PCI/PCI;
│   ├── 2.00.0 RAM; Memory
│   ├── 0.07.0 0->3 (3) PCI/PCI;
│   ├── 0.16.0 Generic 8259; P
│   ├── 0.16.1 Generic 8259; P
│   ├── 0.20.0 Generic 8259; P
│   ├── 0.20.1 Generic 8259; P
│   ├── 0.20.2 Generic 8259; P
│   ├── 0.20.3 Generic 8259; P
│   ├── 0.25.0 Ethernet; Netwo
│   ├── 0.26.0 Universal Host
│   ├── 0.26.1 Universal Host
│   ├── 0.26.2 Universal Host
│   ├── 0.26.7 o. serial bus D
│   ├── 0.27.0 o. Multimedia
│   ├── 0.28.0 0->4 (4) PCI/PCI;
│   ├── 0.28.1 0->5 (5) PCI/PCI;
│   ├── 0.28.4 0->6 (6) PCI/PCI;
│       ├── 6.00.0 o. Mass Stora
│       ├── 0.29.0 Universal Host
│       ├── 0.29.1 Universal Host
│       ├── 0.29.2 Universal Host
│       ├── 0.29.7 o. serial bus D
│       └── 0.30.0 0->7 (7) Subtracti
│           ├── 7.02.0 VGA; PC Compa
│           └── 7.03.0 OpenHCI; IEEE
```

Host/PCI; Bridge Device  
VID: x8086 Intel Corporation  
DID: x3405 no device name found no  
SubVID: x8086 Intel  
SubID: x4F53 no-name  
rev.: x12 x10<-INTA#

edit ConfReg: [ ] hex  
Nr of ConfRegs:  16  64  
 use BIOS int  
Write ConfReg  
 refr after wr. refresh dump: 😊

Config Space Dump: (type 1 xs)

```
3405 8086 <00 : DID VID
0010 0000 <04 : Stat Cmd
0600 0012 <08 : BaseClass SubClass I
0000 0010 <0C : BIST Header LatTime
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
4F53 8086 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 0110 <3C : maxLat minGnt IntPir
```

- Power on the PC
- Start PciTree



# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices. The right pane shows the configuration for the selected device (0.03.0). The configuration panel includes fields for bus, device, and function numbers, and buttons for 'show INT routing', 'show Mem Map', 'highest busnr', and 'E X I T'. The 'Nr of ConfRegs' is set to 64, and the 'refresh dump' button is highlighted with a smiley face icon. The 'Config Space Dump' section shows a list of PCI configuration registers and their values.

direct select: bus: 0 dev: 0 func: 0

show INT routing highest busnr: 63 E X I T

show Mem Map About

0.00.0 Host/PCI; Bridge

0.01.0 0->1 (1) PCI/PCI;

0.03.0 0->2 (2) PCI/PCI;

2.00.0 RAM; Memory

0.07.0 0->3 (3) PCI/PCI;

0.16.0 Generic 8259; P

0.16.1 Generic 8259; P

0.20.0 Generic 8259; P

0.20.1 Generic 8259; P

0.20.2 Generic 8259; P

0.20.3 Generic 8259; P

0.25.0 Ethernet; Netwo

0.26.0 Universal Host

0.26.1 Universal Host

0.26.2 Universal Host

0.26.7 o. serial bus D

0.27.0 o. Multimedia

0.28.0 0->4 (4) PCI/PCI;

0.28.1 0->5 (5) PCI/PCI;

0.28.4 0->6 (6) PCI/PCI;

6.00.0 o. Mass Stora

0.29.0 Universal Host

0.29.1 Universal Host

0.29.2 Universal Host

0.29.7 o. serial bus D

0.30.0 0->7 (7) Subtracti

7.02.0 VGA; PC Comp

7.03.0 OpenHCI; IEEE

Host/PCI; Bridge Device

VID: x8086 Intel Corporation

DID: x3405 no device name found no

SubVID: x8086 Intel

SubID: x4F53 no-name

rev.: x12 x10<-INTA#

edit ConfReg: hex

Nr of ConfRegs: 16 64

use BIOS int

Write ConfReg

refresh dump:

refr after wr.

Config Space Dump: (type 1 xs)

```
3405 8086 <00 : DID VID
0010 0000 <04 : Stat Cmd
0600 0012 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTi
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
4F53 8086 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 0110 <3C : maxLat minGnt Int
0000 0000 <40 : < dev.specific
```

++ -- rescan write to reset  
PCIbus file bridge

- Set Number of Configuration Registers to 64
- Click on Refresh dump

# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application interface. The left pane displays a tree view of PCI devices, with the device at bus 2, device 0, function 0 selected. The right pane shows the configuration details for this device, including Vendor ID (x10EE Xilinx Corp), Device ID (x6018), SubVendor ID (x10EE Xilinx), and SubID (x0007). The Config Space Dump shows the following entries:

```
6018 10EE <00 : DID VID
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas
0000 0010 <0C : BIST Header LatTim
D920 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minGnt Int
7803 4801 <40 : < dev.specific
```

## Locate the Xilinx Device

- Vendor ID is **0x10EE**
- The x8 Gen1 configuration will have a Device ID of **0x6018**

# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices. The right pane shows the configuration space dump for a selected device (2.00.0). The dump includes fields like Stat Cmd, BaseClass SubClass, BIST Header LatTis, BARs, Cardbus\_CIS\_Ptr, SubID SubVendorID, Exp\_ROM\_BAR, reserved fields, and maxLat minGnt Int. The register at address 7803 4801 is highlighted in red and labeled as '< dev.specific'.

direct select: bus: 2 dev: 0 func: 0

show INT routing highest busnr: 63 E X I T

show Mem Map About

2.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp

DID: x6018 no device name found no

SubVID: x10EE Xilinx

SubID: x0007 no-name

rev.: x00 xA<-INTA#

edit ConfReg: x78034801 hex Nr of ConfRegs: 16 64

Write ConfReg use BIOS int refresh dump: 😊

Config Space Dump: (type 1 xs)

```
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClass
0000 0010 <0C : BIST Header LatTis
D920 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minGnt Int
7803 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
```

rescan write to reset  
PCIbus file bridge

- Navigate the linked list in configuration space to locate the PCIe Capabilities Structure
  - See [UG517](#) for details
- With the Xilinx device selected, select Register 0x40
  - Register 0x40 points to the next structure
  - 0x48 is the address of the next structure

# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices. The right pane shows the configuration details for the selected device (2.00.0). The configuration details include the device ID (VID: x10EE Xilinx Corp), device ID (DID: x6018), and a list of configuration registers. The register at address 0080 with value 6005 and offset <48 is highlighted in red.

direct select: bus: 2 dev: 0 func: 0

show INT routing highest busnr: 63 E X I T

show Mem Map About

2.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp

DID: x6018 no device name found no

SubVID: x10EE Xilinx

SubID: x0007 no-name

rev.: x00 xA<-INTA#

edit ConfReg: x00806005 hex

Nr of ConfRegs: 16 64

Write ConfReg

use BIOS int

refresh dump:

Config Space Dump: (type 1 xs)

7803	4801	<40	: < dev.specific
0000	0008	<44	: < dev.specific
0080	6005	<48	: < dev.specific
0000	0000	<4C	: < dev.specific
0000	0000	<50	: < dev.specific
0000	0000	<54	: < dev.specific
0000	0000	<58	: < dev.specific
0000	0000	<5C	: < dev.specific
0202	0010	<60	: < dev.specific
0000	8FC2	<64	: < dev.specific
0000	2830	<68	: < dev.specific
0003	F481	<6C	: < dev.specific
0081	0001	<70	: < dev.specific
0000	0000	<74	: < dev.specific
0000	0000	<78	: < dev.specific
0000	0000	<7C	: < dev.specific
0000	0000	<80	: < dev.specific

rescan write to reset  
PCIbus file bridge

- **Select Register 0x48**
  - Register 0x48 points to the next structure
  - 0x60 is the address of the next structure

# Running the PCIe x8 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices, with the following entries visible:

- 0.00.0 Host/PCI; Bridge
- 0.01.0 0->1 (1) PCI/PCI;
- 0.03.0 0->2 (2) PCI/PCI;
- 2.00.0 RAM; Memory Controller
- 0.07.0 0->3 (3) PCI/PCI;
- 0.16.0 Generic 8259; P
- 0.16.1 Generic 8259; P
- 0.20.0 Generic 8259; P
- 0.20.1 Generic 8259; P
- 0.20.2 Generic 8259; P
- 0.20.3 Generic 8259; P
- 0.25.0 Ethernet; Netwo
- 0.26.0 Universal Host
- 0.26.1 Universal Host
- 0.26.2 Universal Host
- 0.26.7 o. serial bus D
- 0.27.0 o. Multimedia
- 0.28.0 0->4 (4) PCI/PCI;
- 0.28.1 0->5 (5) PCI/PCI;
- 0.28.4 0->6 (6) PCI/PCI;
- 6.00.0 o. Mass Stora
- 0.29.0 Universal Host
- 0.29.1 Universal Host
- 0.29.2 Universal Host
- 0.29.7 o. serial bus D
- 0.30.0 0->7 (7) Subtracti
- 7.02.0 VGA; PC Comp
- 7.03.0 OpenHCI; IEEE

The right pane shows the configuration details for the selected device (2.0.0):

RAM; Memory Controller  
VID: x10EE Xilinx Corp  
DID: x6018 no device name found no  
SubVID: x10EE Xilinx  
SubID: x0007 no-name  
rev.: x00 xA<-INTA#

edit ConfReg:  hex  
Nr of ConfRegs:  16  64  
 use BIOS int  
Write ConfReg  
 refr after wr.  
refresh dump:

Config Space Dump: (type 1 xs)

7803	4801	<40	: <	dev.specific
0000	0008	<44	: <	dev.specific
0080	6005	<48	: <	dev.specific
0000	0000	<4C	: <	dev.specific
0000	0000	<50	: <	dev.specific
0000	0000	<54	: <	dev.specific
0000	0000	<58	: <	dev.specific
0000	0000	<5C	: <	dev.specific
0202	0010	<60	: <	dev.specific
0000	8FC2	<64	: <	dev.specific
0000	2830	<68	: <	dev.specific
0003	F481	<6C	: <	dev.specific
0081	0001	<70	: <	dev.specific
0000	0000	<74	: <	dev.specific
0000	0000	<78	: <	dev.specific
0000	0000	<7C	: <	dev.specific
0000	0000	<80	: <	dev.specific

## Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure

# Running the PCIe x8 Gen1 Design

direct select: bus: 2 dev: 0 func: 0

show INT routing highest busnr: 63 E X I T

show Mem Map About

2.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp  
DID: x6018 no device name found no  
SubVID: x10EE Xilinx  
SubID: x0007 no-name  
rev.: x00 xA<-INTA#

edit ConfReg: x0003F481 hex Nr of ConfRegs: 16 64

Write ConfReg use BIOS int refresh dump: ☺

Config Space Dump: (type 1 xs)

7803	4801	<40	: <	dev.specific
0000	0008	<44	: <	dev.specific
0080	6005	<48	: <	dev.specific
0000	0000	<4C	: <	dev.specific
0000	0000	<50	: <	dev.specific
0000	0000	<54	: <	dev.specific
0000	0000	<58	: <	dev.specific
0000	0000	<5C	: <	dev.specific
0202	0010	<60	: <	dev.specific
0000	8F02	<64	: <	dev.specific
0000	2800	<68	: <	dev.specific
0003	F481	<6C	: <	dev.specific
0081	0001	<70	: <	dev.specific
0000	0000	<74	: <	dev.specific
0000	0000	<78	: <	dev.specific
0000	0000	<7C	: <	dev.specific
0000	0000	<80	: <	dev.specific

## Register 0x6C

- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
- The value 0x81 shows this is an x8 Gen1 device (1)

## Link Status Register

- 0x70
- Shows the current link status
- This design trained to x8 Gen1 (2)

# Running the PCIe x8 Gen1 Design

The screenshot shows the PCItree application window. The left pane displays a tree view of PCI devices, with the following entries visible:

- 0.00.0 Host/PCI; Bridge
- 0.01.0 0->1 (1) PCI/PCI;
- 0.03.0 0->2 (2) PCI/PCI;
- 2.00.0 RAM; Memory Controller
- 0.07.0 0->3 (3) PCI/PCI;
- 0.16.0 Generic 8259; P
- 0.16.1 Generic 8259; P
- 0.20.0 Generic 8259; P
- 0.20.1 Generic 8259; P
- 0.20.2 Generic 8259; P
- 0.20.3 Generic 8259; P
- 0.25.0 Ethernet; Netwo
- 0.26.0 Universal Host
- 0.26.1 Universal Host
- 0.26.2 Universal Host
- 0.26.7 o. serial bus D
- 0.27.0 o. Multimedia
- 0.28.0 0->4 (4) PCI/PCI;
- 0.28.1 0->5 (5) PCI/PCI;
- 0.28.4 0->6 (6) PCI/PCI;
- 6.00.0 o. Mass Stora
- 0.29.0 Universal Host
- 0.29.1 Universal Host
- 0.29.2 Universal Host
- 0.29.7 o. serial bus D
- 0.30.0 0->7 (7) Subtracti
- 7.02.0 VGA; PC Comp
- 7.03.0 OpenHCI; IEEE

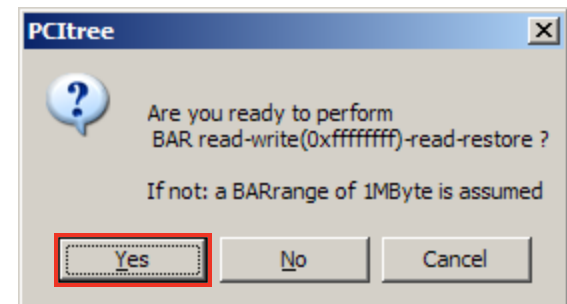
The right pane shows the configuration details for the selected device (2.00.0):

- RAM; Memory Controller
- VID: x10EE Xilinx Corp
- DID: x6018 no device name found no
- SubVID: x10EE Xilinx
- SubID: x0007 no-name
- rev.: x00 xA<-INTA#
- edit ConfReg: xD9200000 hex
- Nr of ConfRegs: 16 (selected) 64
- use BIOS int
- Write ConfReg
- refr after wr.
- refresh dump:
- Config Space Dump: (type 1 xs)

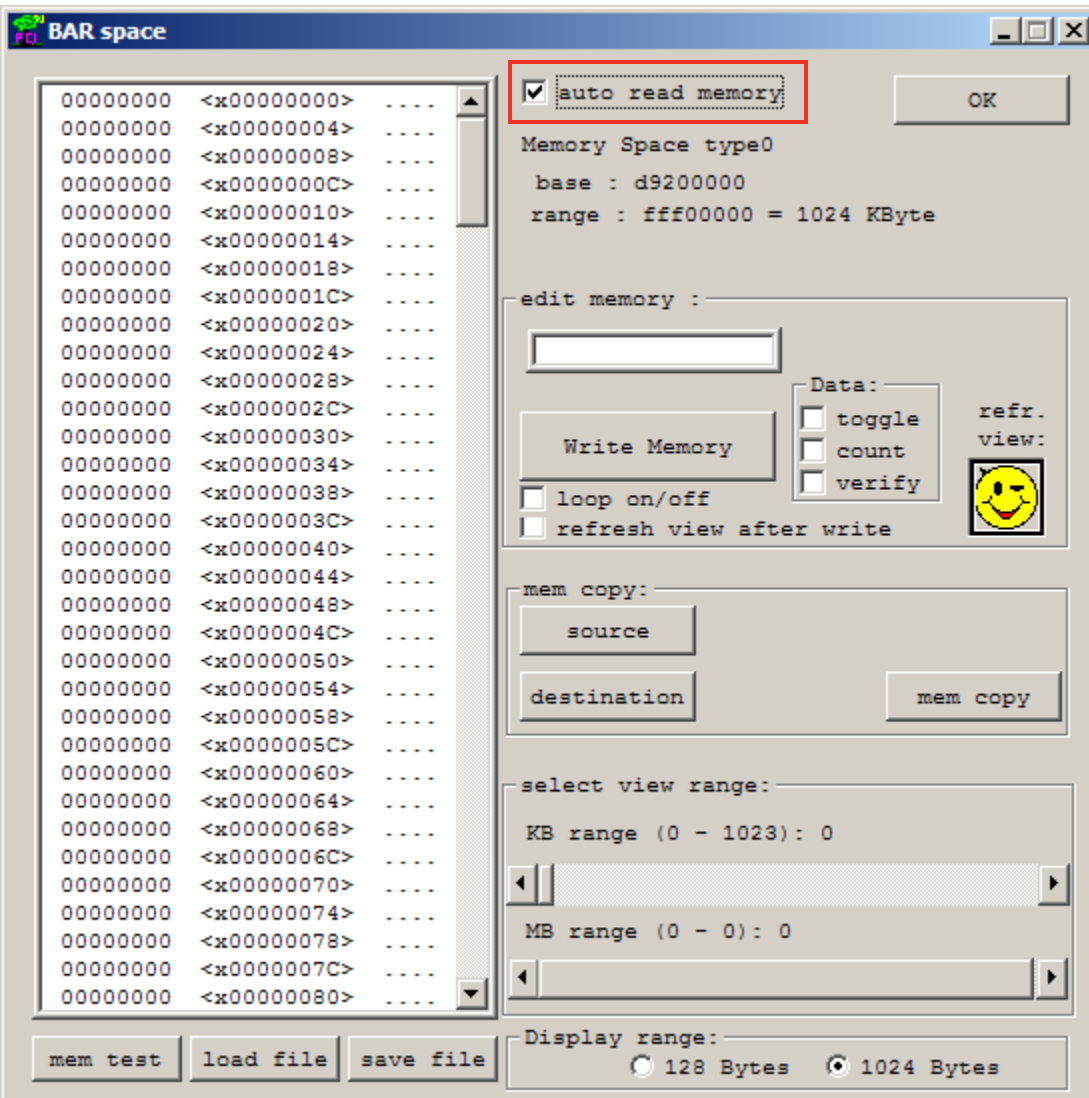
The Config Space Dump shows the following entries:

- 6018 10EE <00 : DID VID
- 0010 0007 <04 : Stat Cmd
- 0500 0000 <08 : BaseClass SubClas
- 0000 0010 <0C : BIST Header LatTi
- D920 0000 <10 : BAR 0 mem 32bit**
- 0000 0000 <14 : BAR 1
- 0000 0000 <18 : BAR 2
- 0000 0000 <1C : BAR 3
- 0000 0000 <20 : BAR 4
- 0000 0000 <24 : BAR 5
- 0000 0000 <28 : Cardbus\_CIS\_Ptr
- 0007 10EE <2C : SubID SubVendorID
- 0000 0000 <30 : Exp\_ROM\_BAR
- 0000 0040 <34 : reserved
- 0000 0000 <38 : reserved
- 0000 010A <3C : maxLat minGnt Int
- 7803 4801 <40 : < dev.specific

- **Double-click on BAR 0**
  - BAR 0 Address is machine dependent
- **Click Yes on the Dialog box seen below**



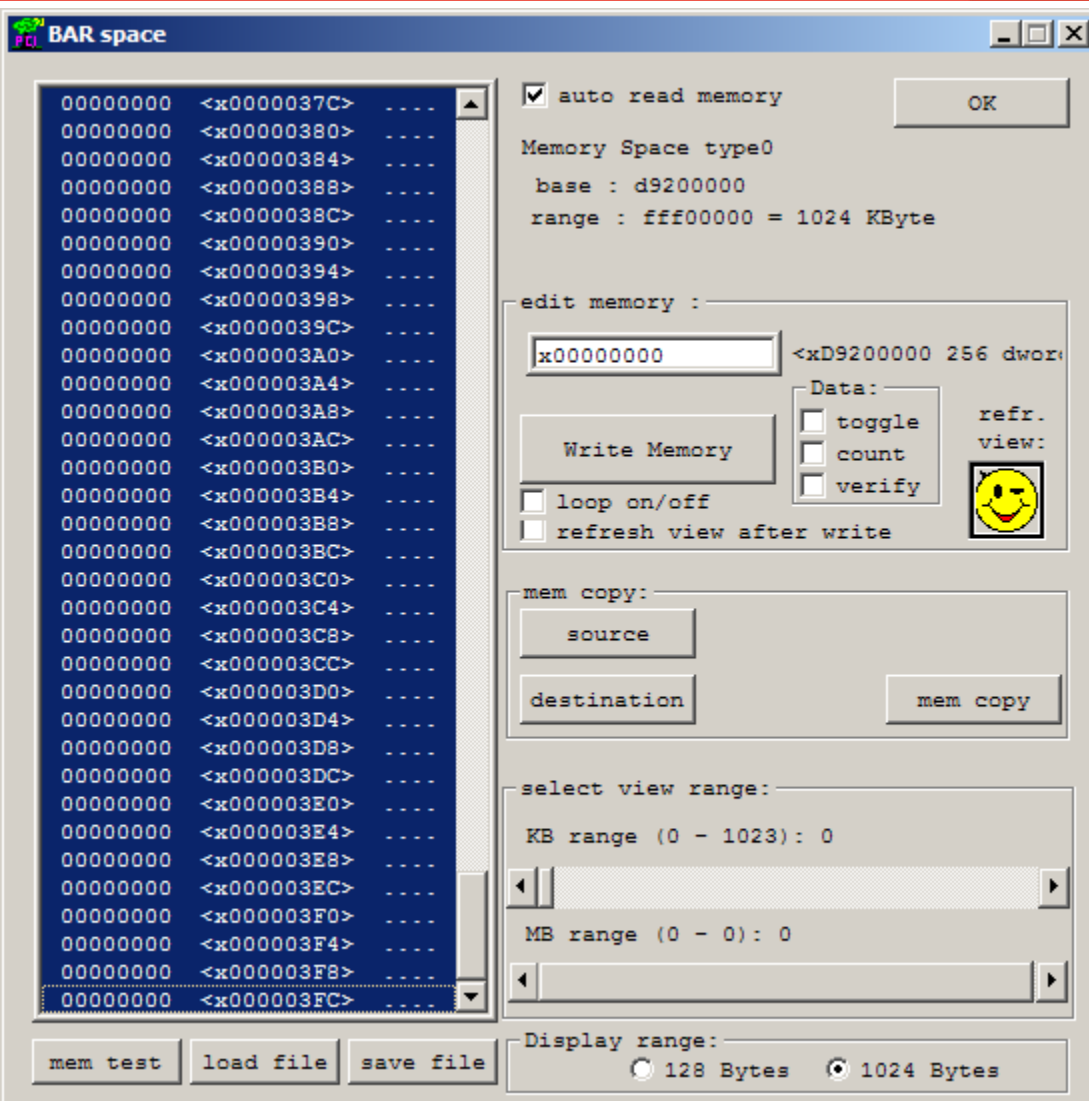
# Running the PCIe x8 Gen1 Design



- Select auto read memory

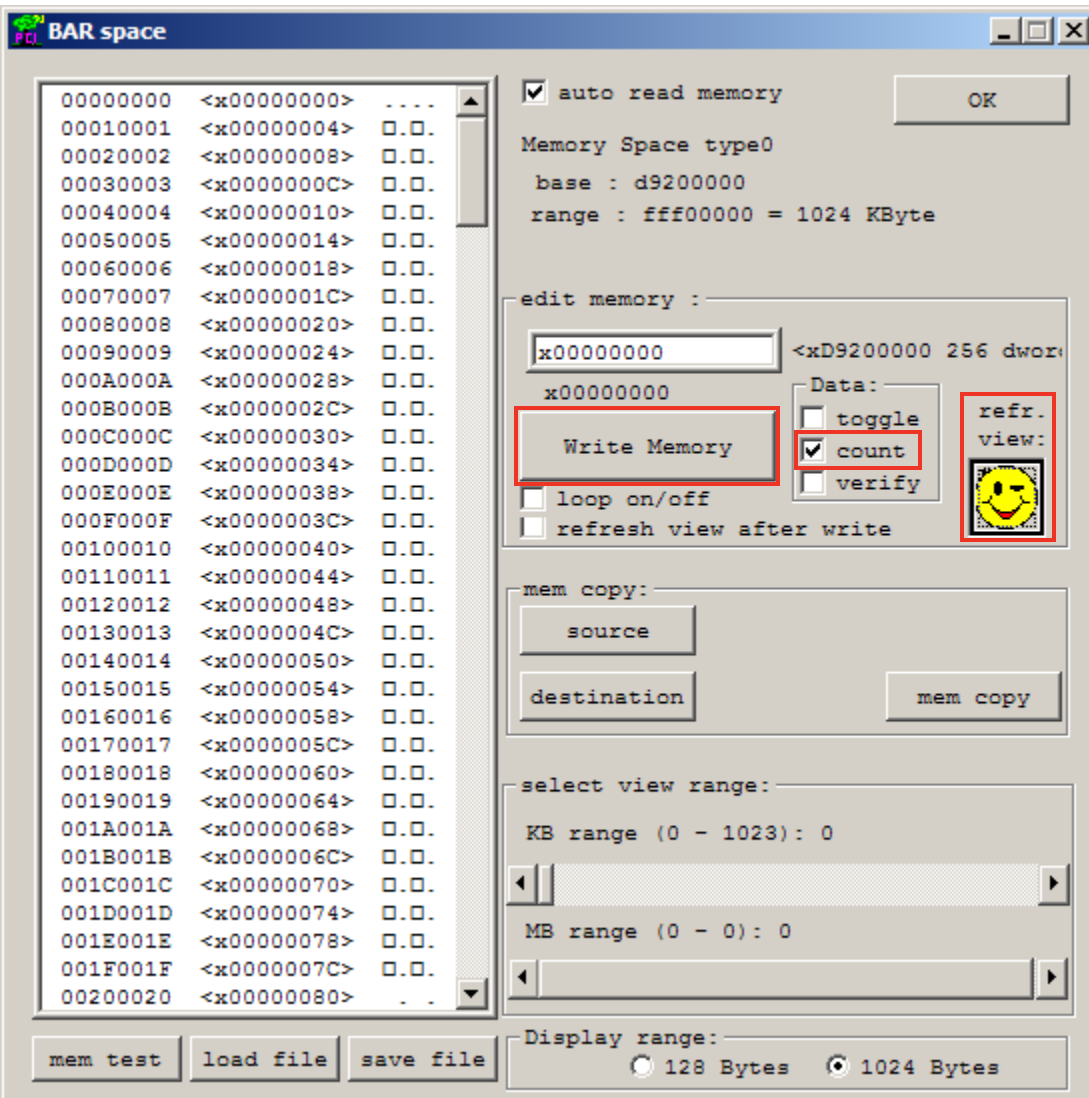


# Running the PCIe x8 Gen1 Design



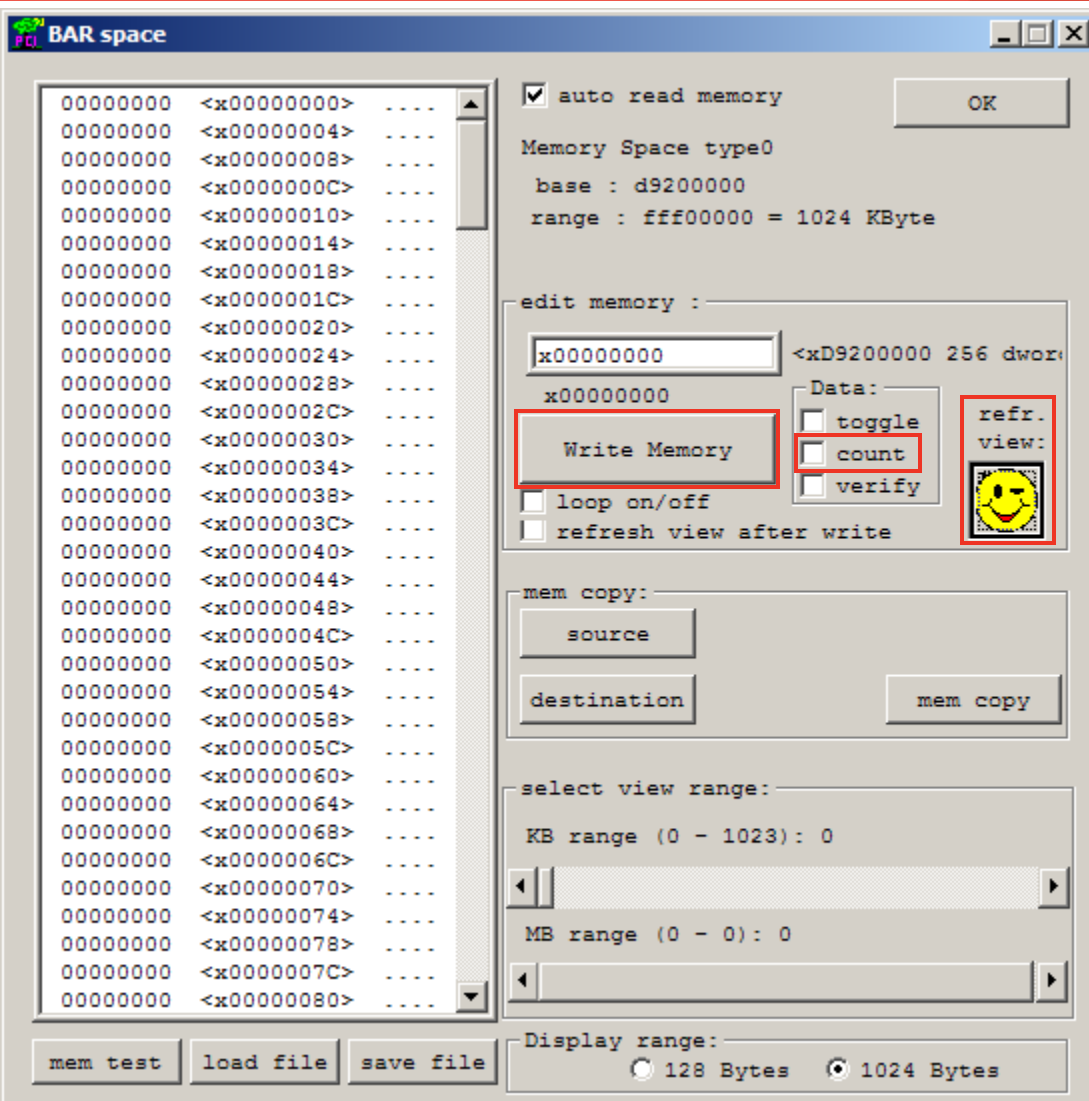
- Click on the first memory location
  - Type <Shift-End> to select 1024 Bytes

# Running the PCIe x8 Gen1 Design



- **Write Memory**
  - Select count
  - Click Write Memory
  - Click refr view
- **View results – counting up to FF**

# Running the PCIe x8 Gen1 Design



- **Restore Memory**
  - Deselect count
  - Click Write Memory
  - Click refr view
- **Memory is reset to zeros**

# Virtex-6 PCIe x8 Gen1 Capability

- **ML605 Supports PCIe Gen1 and Gen2 Capability**
  - x4, x2, or x1 Gen2 lane width
  - x8 Gen2 not supported in -1 parts
- **LogiCORE PIO Example Design**
  - RDF0008.zip
  - Available through <http://www.xilinx.com/ml605>
- **LogiCORE Integrated Block for PCI Express**
  - See [UG517](#) for details

# References

# References

## ▪ PCIe Base Specification

- PCI SIG Web Site

<http://www.pcisig.com/home>

## ▪ Virtex-6 PCIe

- PCIe Product Overview

[http://www.xilinx.com/products/ipcenter/V6\\_PCI\\_Express\\_Block.htm](http://www.xilinx.com/products/ipcenter/V6_PCI_Express_Block.htm)

- Virtex-6 FPGA Integrated Block v1.5 for PCI Express User Guide

[http://www.xilinx.com/support/documentation/ip\\_documentation/v6\\_pcie\\_ug517.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ug517.pdf)

- Virtex-6 FPGA Integrated Block v1.5 for PCI Express Data Sheet

[http://www.xilinx.com/support/documentation/ip\\_documentation/v6\\_pcie\\_ds715.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ds715.pdf)

- IP Release Notes Guide

[http://www.xilinx.com/support/documentation/ip\\_documentation/xtp025.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf)

# Documentation

# Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

<http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

<http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Hardware User Guide

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug534.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf)

- ML605 Reference Design User Guide

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug535.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf)