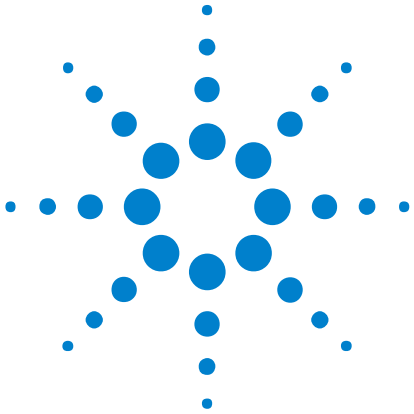

U4301A PCIe Gen3 Analyzer

User Guide

Agilent Technologies

Notices

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www.agilent.com/find/(product-specific information and support, software and documentation updates)

www.agilent.com/find/assist (worldwide contact information for repair and service)

Information on preventing damage to your Agilent equipment can be found at www.agilent.com/find/tips.

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U4301A PCIe Gen3 Analyzer—At a Glance

The U4301A PCIe Gen3 analyzer lets you capture and decode PCI Express 3.0 (PCIe 3.0) data and view it in a Protocol Viewer window. The protocol analyzer supports all PCIe 3.0 speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3), and it supports link widths from x1 to x16.

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2 slot chassis).

When a controller PC is connected to an Agilent Digital Test Console chassis via an external PCIe interface and cable, the *Agilent Logic Analyzer* application (running on the controller PC) lets you connect to the chassis, set up U4301A PCIe Gen3 analyzer data captures, and perform analysis.

The U4301A PCIe Gen3 analyzer provides:

Effective presentation of protocol interactions from physical layer to transaction layer:

- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction.
  - Easy flow columns to better understand the stimulus and response nature of the protocols.
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally.
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for Link Training debug, Config accesses, and general I/O.

Simple and powerful state-based triggering:

- New simple trigger mode makes it easy to setup single event triggers.
- Powerful state-based triggering including:
  - Four states supported in trigger sequencer.
  - Triggering on patterns (ordered set patterns or packet types).
  - Internal counters and timers.
  - Triggering on an ordered set on a specific lane.
- External trigger in/out.

Powerful hardware features ensure capture of important transition events:

- Dual phase lock loops (PLLs) per direction ensuring that the analyzer will lock on speed change events quickly and not miss any critical data.
- Large 4 GB of capture buffer per module (up to 8 GB of capture for x16 analyzer), for long recording sessions.

- PCIe Gen1 x4 link to the host PC, provides up to 10 Gbps of data download.
- LEDs to show lane status and speed for fast understanding of current link status.

See • "Using the PCIe Gen3 Analyzer" on page 5

Using the PCIe Gen3 Analyzer

For an overview and list of features, see: "U4301A PCIe Gen3 Analyzer–At a Glance" on page 3

- Chapter 1, “Hardware and Software Installation,” starting on page 11
- Chapter 2, “Probing Options for PCIe Gen3,” starting on page 13
- Chapter 3, “Specifying the Connection Setup,” starting on page 15
- Chapter 4, “Setting the Capture Options,” starting on page 29
- Chapter 5, “Tuning the Analyzer for a Specific DUT,” starting on page 33
- Chapter 7, “Setting Up Triggers,” starting on page 53
- Chapter 8, “Running/Stopping Captures,” starting on page 63
- Chapter 9, “Viewing PCIe Gen3 Packets,” starting on page 65
- Chapter 10, “Viewing LTSSM States and State Transitions,” starting on page 75
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- Chapter 12, “Viewing Offline Performance Summary,” starting on page 131

See Also

- U4305 PCIe Gen3 exerciser documentation.

Contents

1 Hardware and Software Installation

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2-slot chassis).

The Agilent chassis is connected to a controller PC via a PCI Express interface and cable.

The controller PC runs the *Agilent Logic Analyzer* application software which lets you set up the U4301A PCIe Gen3 analyzer, specify triggers and other data capture options, capture data, and analyze the captured data using Packet Viewer/Protocol Viewer windows.

See the *"Agilent Digital Test Console Installation Guide"* for information on:

- Installing the U4301A PCIe Gen3 analyzer blade into a Digital Test Console chassis.
- Connecting the Digital Test Console chassis to a controller PC via the PCI Express Gen1 x4 interface.
- Installing the *Agilent Logic Analyzer* software on the controller PC.

See the "*Agilent AXIe based Logic Analysis and Protocol Test Modules Installation Guide*" for information on:

- Installing the U4301A PCIe Gen3 analyzer module into an Agilent AXIe chassis.
- Connecting the AXIe chassis to a controller PC via the PCI Express interface.
- Installing the Agilent Logic Analyzer software on the controller PC.

1 Hardware and Software Installation

2 Probing Options for PCIe Gen3

The currently available options for probing a PCIe Gen3 device under test (DUT) are:

- U4321A solid slot interposer
- U4322A midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

Details about these two probing options (and other PCIe Gen3 tools) can be found in the *"PCI Express Gen3 Hardware and Probing Guide"*.

3 Specifying the Connection Setup

Once you have connected the U4301A module, probing hardware, and DUT in the required configuration based on your probing requirements, the next step is to configure the connection setup for the U4301A module in the Agilent Logic Analyzer application. You use the Connection Setup tab of the analyzer's Setup dialog to configure the connection setup.

The connection setup details that you specify in this tab tells the Logic Analyzer software how the U4301A module is connected to the DUT in terms such as the probing option used, the direction of data capture (upstream, downstream, or bidirectional), and the link width needed. For instance, if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the Footprint option, 1 Bidirectional upto x8 as the Link type, and x8 as the Link Width in the Connection Setup tab to reflect the hardware setup that you have configured.

NOTE

- For details on how to set up the hardware and probing connections between the U4301A module and DUT, refer to PCI Express Gen3 Hardware and Probing Guide.
- For details on how to set up the chassis, U4301A module, and host PC, refer to the AXIe based Logic Analysis and Protocol Test Modules Installation Guide.

These guides are installed with the Logic Analyzer software and can also be downloaded from www.agilent.com.

Probing options

While specifying the connection setup, one of the key requirements is to select the probing option that you have used with the U4301A module to probe the DUT and the data capture direction in which you have configured the hardware setup.

Broadly, there are the following four probing options available with the U4301A module:

- U4321A Solid Slot Interposer card
- U4322A Soft Touch Midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

- PCIe Gen2 probes with the U4317A adapter. This adapter is used for conversion between the PCIe Gen2 probes and U4301A PCIe Gen3 Analyzer module. The PCIe Gen2 probes supported are:
  - N5315A Solid Slot Interposer for PCIe Gen2
  - N4241A straight, N4242A swizzled, and N4243A split cable Soft Touch Midbus 2.0 probe for PCIe Gen2
  - N5328A Half Size Midbus probe
  - N4241F/Z Flying Lead probe for PCIe Gen2

For each of the above four probing types, different options are available in the Connection Setup tab reflecting the data direction (upstream, downstream, or bidirectional). Upstream is the data direction towards the root complex. Downstream is the data direction away from the root complex. Based on your probing setup and the data capture direction in which you have configured the hardware setup, you need to select an appropriate probing option in the Connection Setup tab.

U4321A Solid Slot Interposer Card

When used with a U4321A solid slot interposer card, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way.

If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and a U4321A SSI card. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select U4321A Slot Interposer Upstream as the probing option for one of the U4301A modules and U4321A Slot Interposer Downstream as the probing option for the other U4301A module.

if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the probing option.

U4322A Soft Touch Midbus 3.0 probe

The U4322A midbus 3.0 probes require footprints to be designed into the device under test. Each probe requires its own footprint, and there are basically two variations:

- **Bidirectional** – where half the footprint pins are for the upstream data and the other half are for the downstream data.
- **Unidirectional** – where all the pins on the footprint are for the data going in the same direction.

Reversed refers to optional lane reversal which is supported for upstream ports.

Based on how you have designed the footprint for the probe, you need to select an appropriate probing option in the Connection Setup tab. For instance, if you have configured a x4 bidirectional setup using a U4322A midbus probe, then you need to select U4322A Bidirectional Full as the Footprint, 1 Bidirectional upto x8 as the Link type, and x4 as the Link Width in the Connection Setup tab.

U4324A PCIe Gen 3 Flying Lead probe

When used with a U4324A Flying Lead probe, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way. For x1-x8 bidirectional link type, you can use the U4324A Flying Lead probes in a straight or a swizzled configuration.

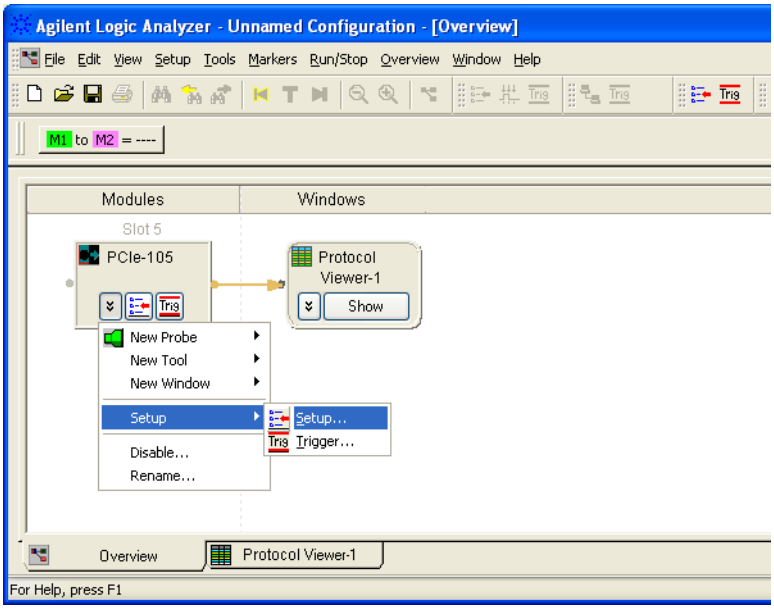
If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and eight U4324A Flying Lead probes. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select the U4324A Flying Lead Probe as the probing option and Unidirectional as the link type for both the U4301A modules.

If you have connected the U4324A Flying Lead probes in a x1 to x8 bidirectional straight setup, then you need to select the U4324A Flying Lead Probe as the probing option and Bidirectional as the link type.

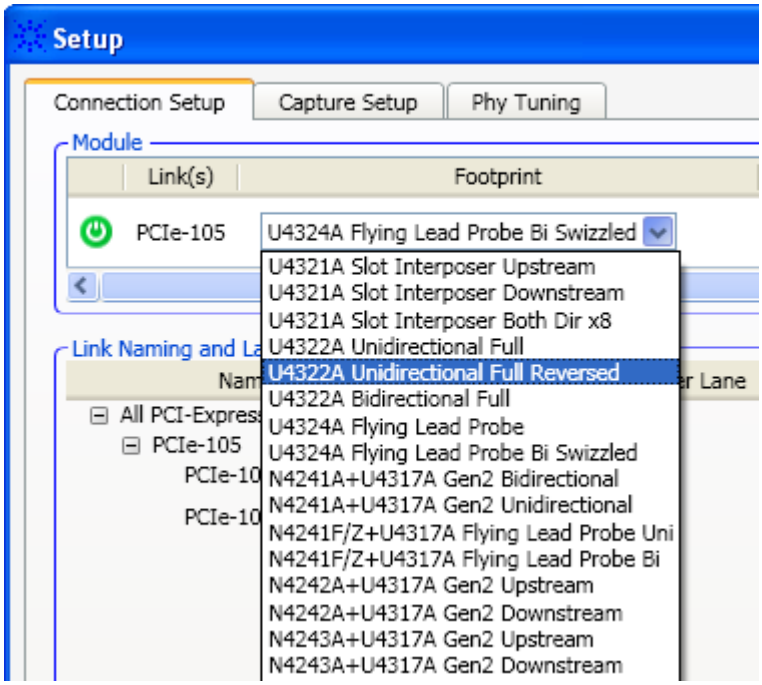
If you have set up a swizzled x1 to x8 bidirectional configuration using the U4324A Flying Lead probes, then you need to select the U4324A Flying Lead Probe Bi Swizzled as the probing option and Bidirectional as the link type.

To specify the connection setup

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Setup...**.

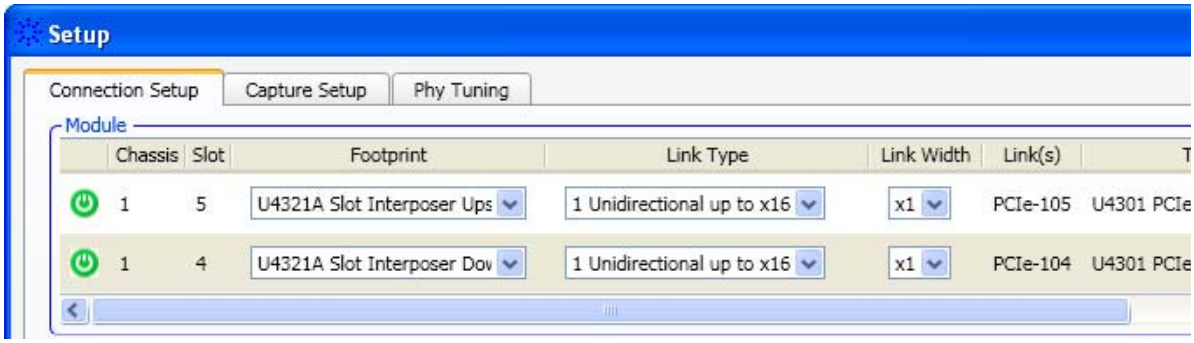


2 From the **Footprint** listbox, select the type of probing that you have set up between the U4301A Analyzer module and DUT. For each of the supported four probing types, different probing options are available in the Footprints listbox based on the data direction (upstream, downstream, or bidirectional). Based on your probing setup and the link type needed, select an appropriate probing option from the Footprint listbox. Refer to the "Probing options" on page 15 to know more about these options.

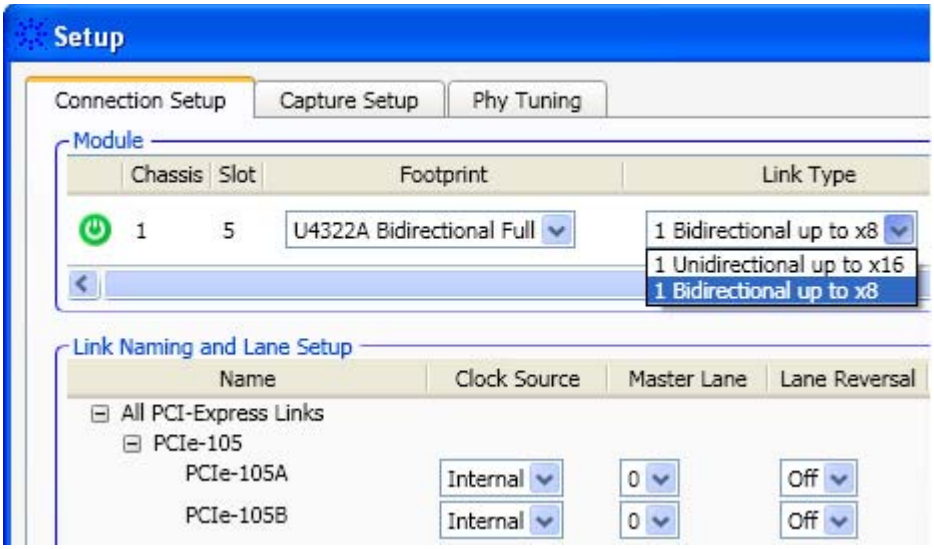


For more information on probing setups, click **Connection diagram...** or refer to the *"PCI Express Gen3 Hardware and Probing Guide"*.

If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the probing option individually for these modules.

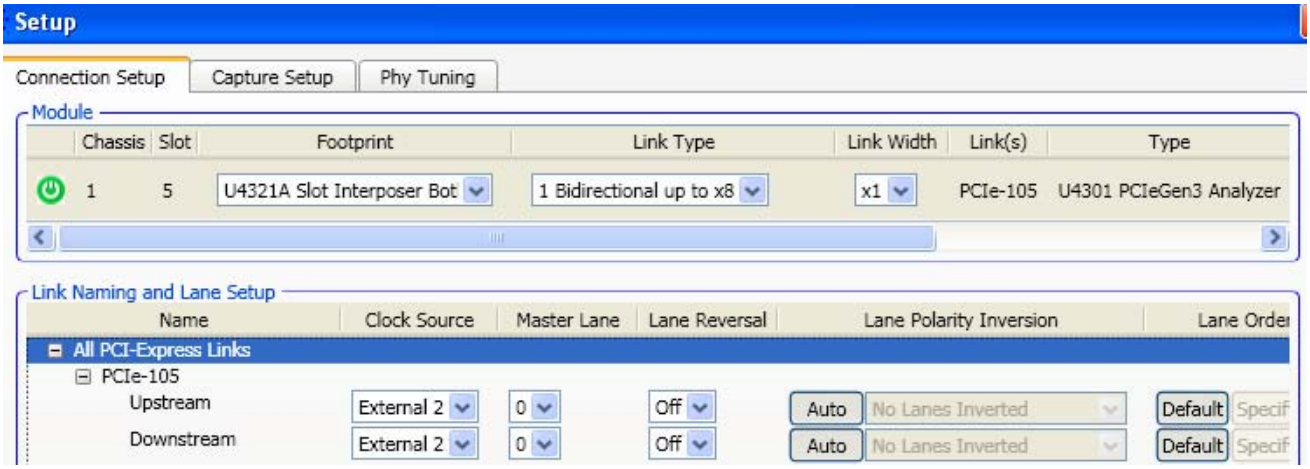


3 Specify the link type.



The **Link Type** refers to the type of link that you want to create between the U4301A module and DUT. You can select the **1 Unidirectional up to x16** link type if you want the U4301A module to probe and capture data in only one direction (upstream or downstream). In the Unidirectional link type, the U4301A module can support a unidirectional link with upto 16 channels in the same direction. You can select the **1 Bidirectional up to x8** link type if you want the same U4301A module to probe and capture data in both directions (upstream as well as downstream). In the bidirectional link type, the U4301A module can support one bidirectional link with upto eight channels for each direction. When you select the bidirectional link type, two sub-links are created for the two directions. You can set the link attributes such as clock source, master lane, and lane ordering separately for these two sub-links. These attributes are available in the **Link Naming and Lane Setup** section.

The following screen displays the sub-links of a x8 bidirectional link. These sub-links have been renamed on the basis of the direction these represent.



If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the link type individually for these modules.

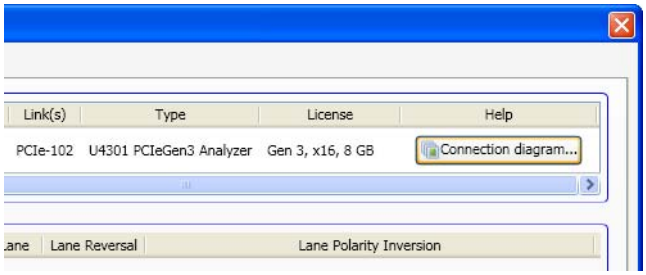
4 Select the link width.

Select the link width that matches the negotiated link width of transmitter and receiver.

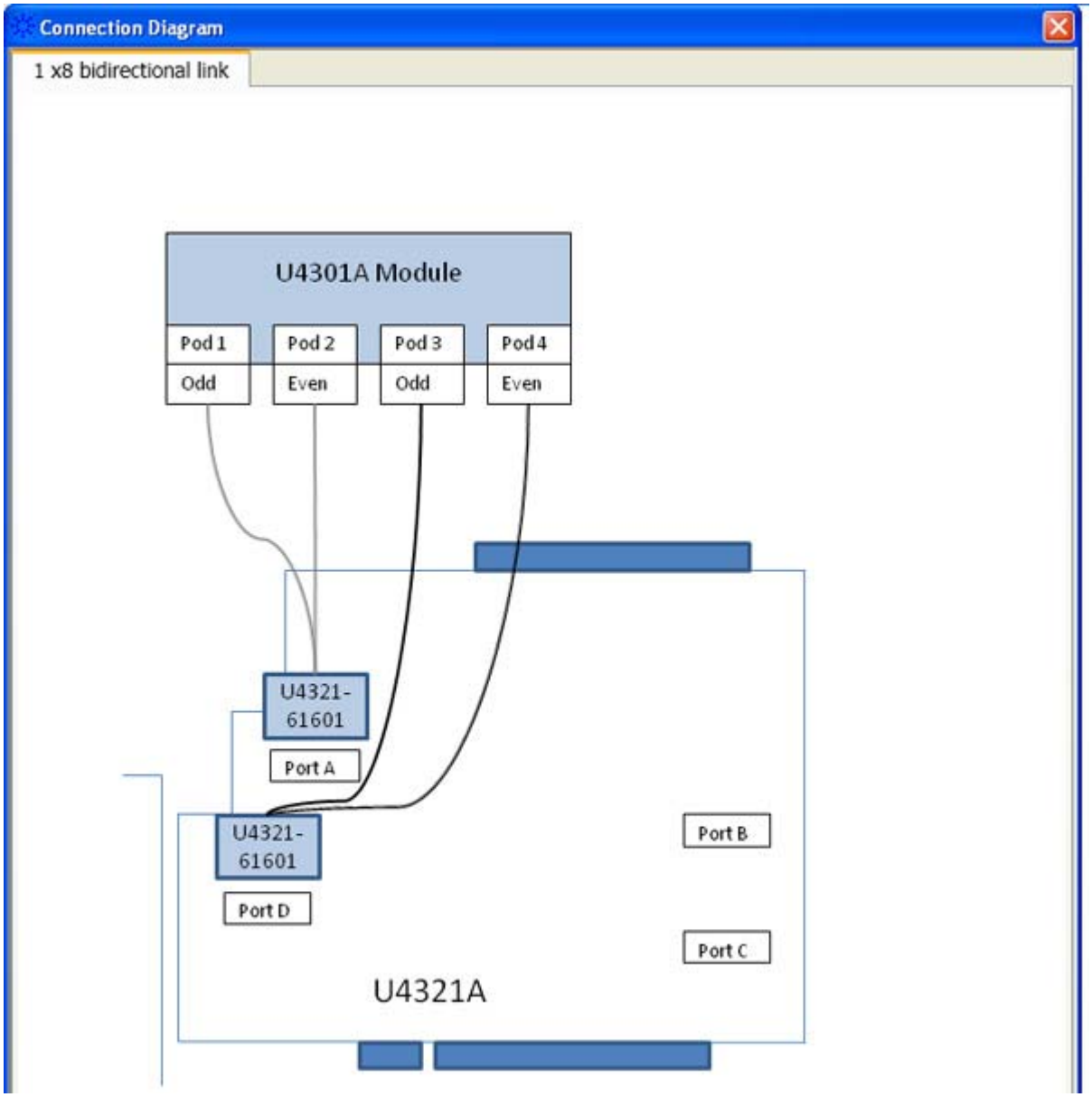
If you select the Link Type as **1 Bidirectional upto x8**, then you can select the Link Width from x1 to x8. The x16 option is disabled in this case because a U4301A Analyzer module can probe and capture data in both directions with upto eight channels in each direction.

5 Verify the connection:

a Click **Connection diagram...**.

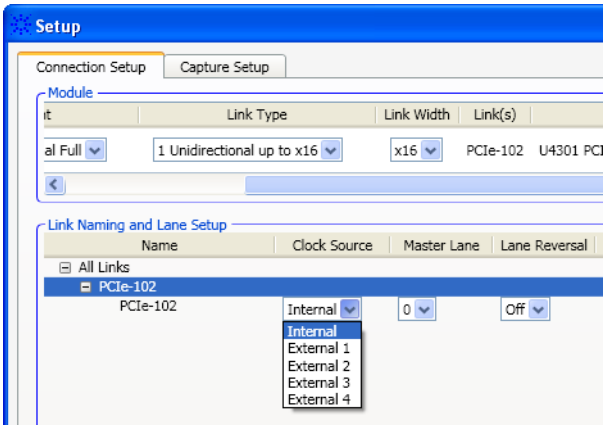


b Use the Connection Diagram dialog to verify that your connection setup specification matches the actual device under test connection.



c Close the Connection Diagram dialog.

6 Select the clock source:



- **Internal** — selects an internal clock source. You should select Internal if the data rate is in the range of 2.5 Gbps or 5 Gbps +/-50 ppm. Note that there is no input clock in this mode.
- **External 1/2/3/4** — selects an external clock source. You should select External if the device under test uses SSC or the data rate is in the range of 2.5 Gbps +/-300 ppm (+0% / -0.5% if using SSC). The clock rate for external mode should be between 100 MHz +/-300 ppm (+0% / -0.5% if using SSC).

Some important points about external reference clock selection

If you plan to use an external clock source, then you must ensure that the reference clock from the DUT is available when you:

- select **External** as the **Clock Source** in the **Setup** dialog and apply the selection by clicking **Apply** or **OK**.
- or load a configuration file that specifies the use of the external clock source.

If the reference clock from the DUT is not available to Analyzer when you apply the external clock source selection, the Analyzer's internal PLL may not be able to attain the initial lock with the DUT's reference clock resulting in an erratic behavior. Just making the DUT's reference clock available at this point does not establish the lock with the reference clock. In such a situation, you can re-establish the lock with the DUT's reference clock by performing the following steps:

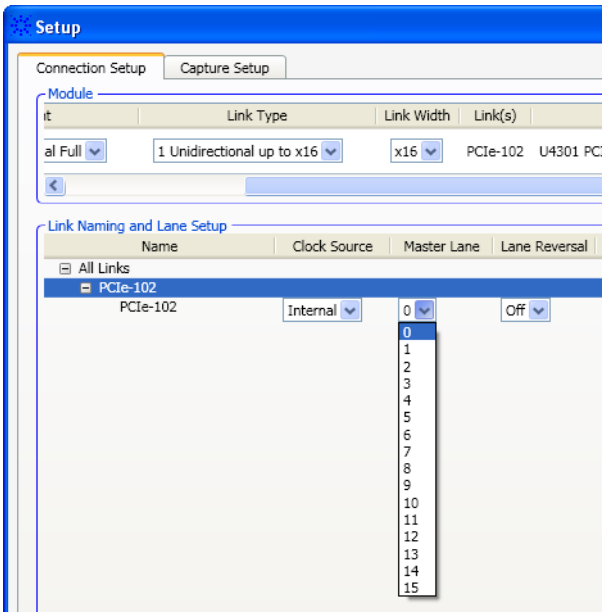
i Ensure that the reference clock of the DUT is available.

ii Then select **Internal** as the **Clock Source** in the **Setup** dialog and click **Apply**.

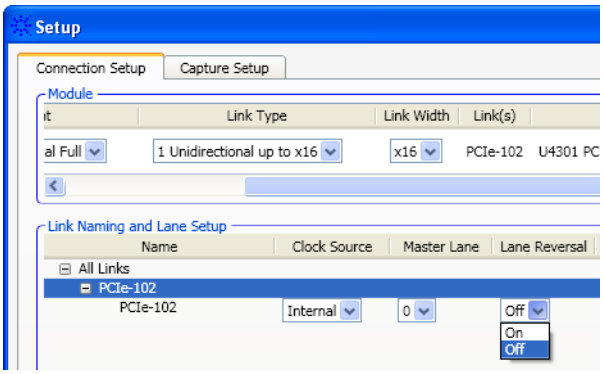
iii Finally, select **External** as the **Clock Source** in the **Setup** dialog and click **Apply**.

Once the initial lock is established, it is maintained. You need not re-establish the lock with the reference clock on subsequent availability/unavailability of the reference clock in the event of DUT power off/on or on any further changes to the Setup dialog except for **Clock Source** or **Link Type**.

7 Select the master lane. You can select any lane as the master lane from the lanes displayed in the Master Lane listbox. The lanes are displayed as per the selected link width. The lane that you select as the master lane is considered the lane for capturing the ordered sets.



8 Specify whether lane reversal is on or off.

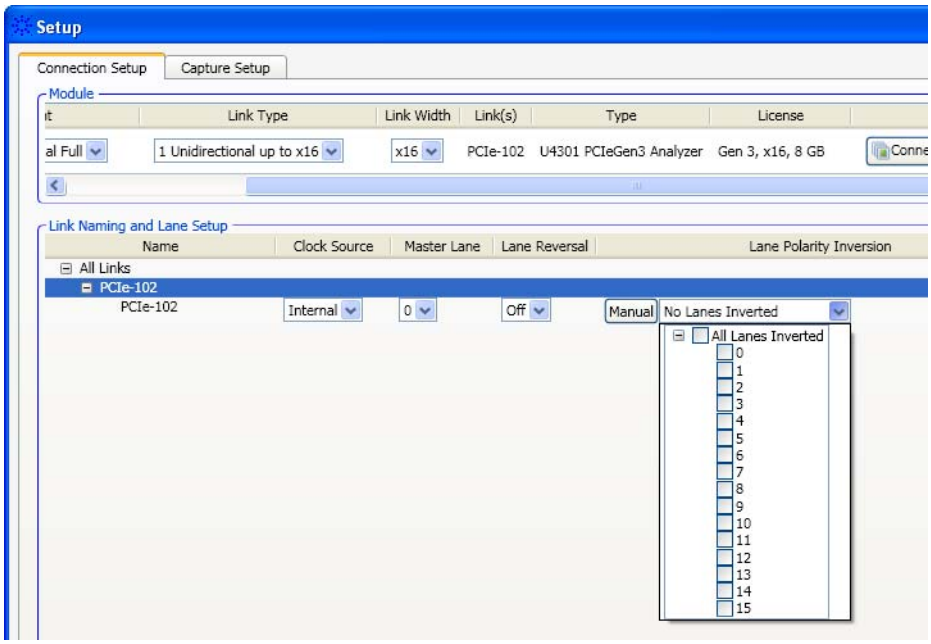


9 Specify any lane polarity inversion:

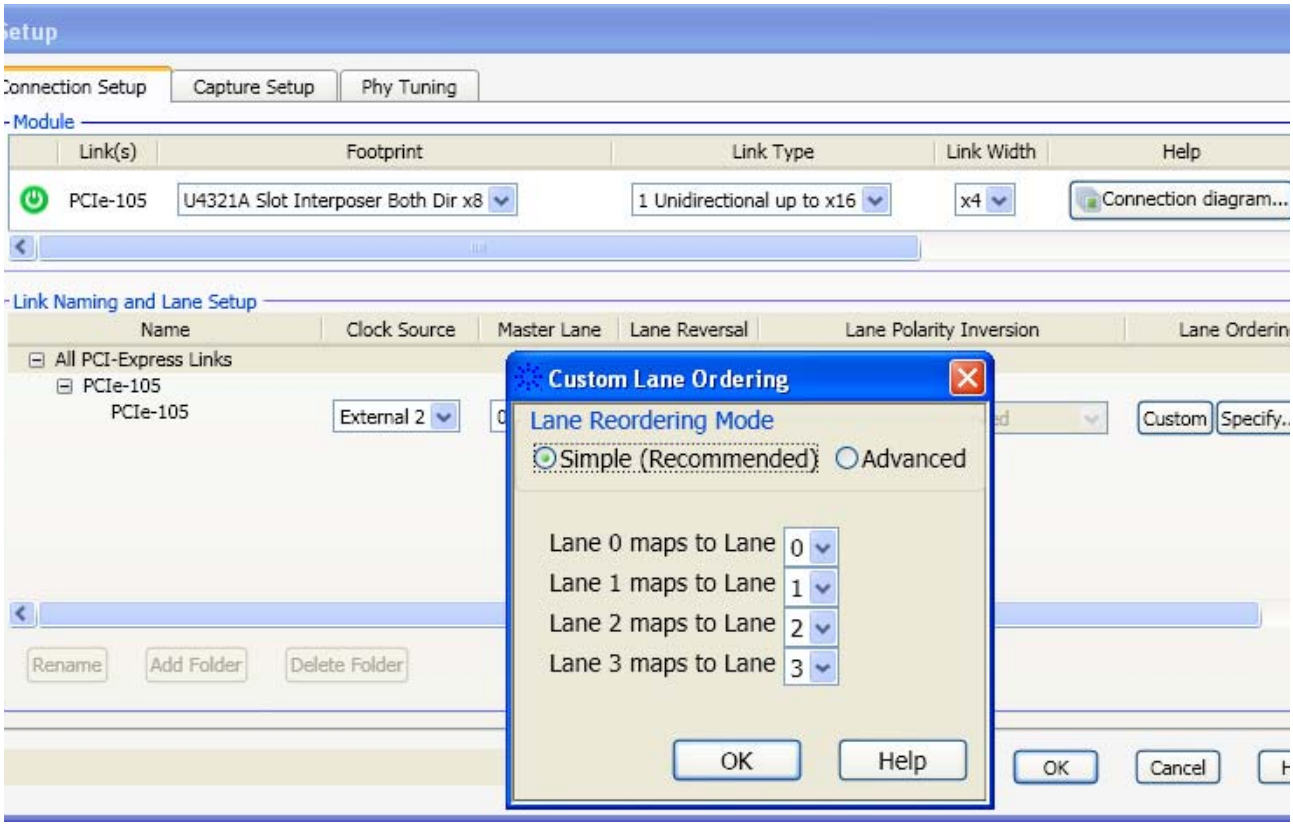
a Click **Auto** or **Manual** to toggle between the types of polarity inversion specification.

When Auto is selected, the polarity of the lanes is set automatically during the initial link training.

b When manual selection is chosen, select the lanes that are inverted.



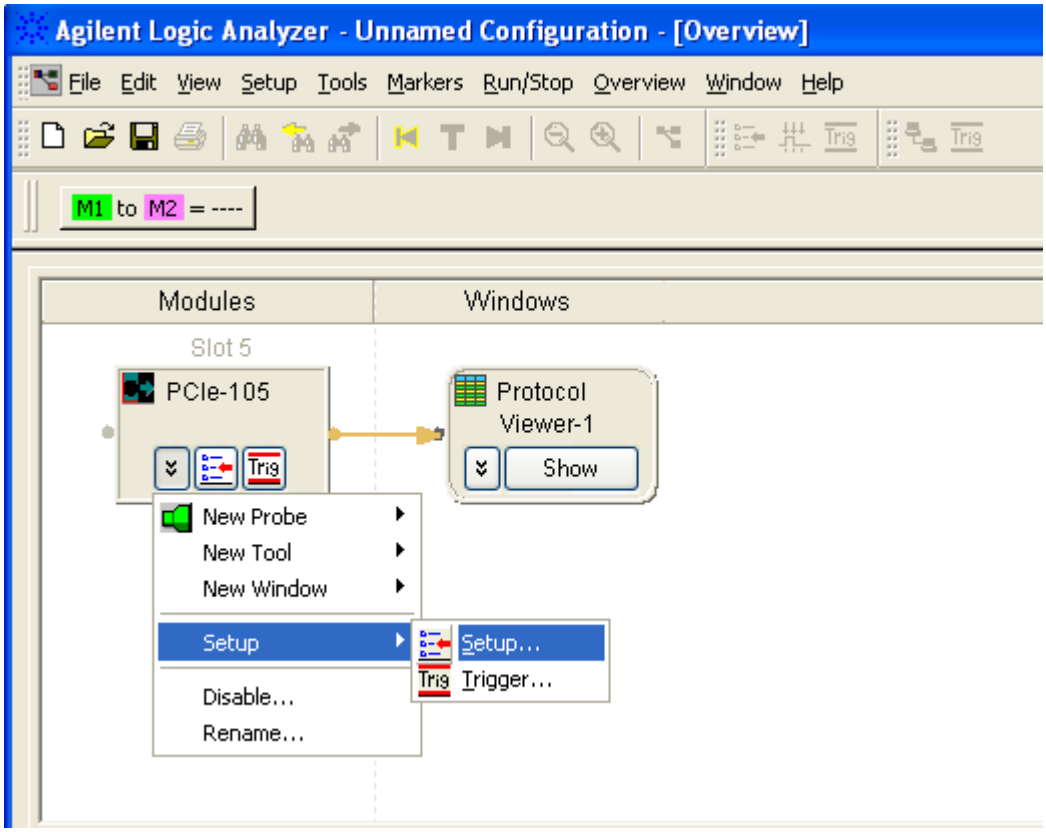
10 The **Lane Ordering** option lets you perform the ordering of the physical lanes of the link with the logical lanes. You can either retain the **Default** lane ordering which means Lane 0 of the link maps to logical Lane 0 and so on. If you want to map Lane 0 of the link to some other Lane, then select **Custom** option from Lane Ordering and click **Specify** to display the **Custom Lane Ordering** dialog box. In this dialog box, select the lane with which you want to map Lane 0. The number of lanes displayed for lane ordering depend on the selected link width. For example, if the link width is selected as x4, then the Lane 0, 1, 2, and 3 are available for lane ordering.


Connection Setup
Capture Setup
Phy Tuning
Module
Link(s)
Footprint
Link Type
Link Width
Help
PCIe-105
U4321A Slot Interposer Both Dir x8
1 Unidirectional up to x16
x4
Connection diagram...
Link Naming and Lane Setup
Name
Clock Source
Master Lane
Lane Reversal
Lane Polarity Inversion
All PCI-Express Links
PCIe-105
PCIe-105
External 2
Custom
Specify...
Rename
Add Folder
Delete Folder
OK
Cancel
Custom Lane Ordering
Lane Reordering Mode
Simple (Recommended)
Advanced
Lane 0 maps to Lane 0
Lane 1 maps to Lane 1
Lane 2 maps to Lane 2
Lane 3 maps to Lane 3
OK
Help

4 Setting the Capture Options

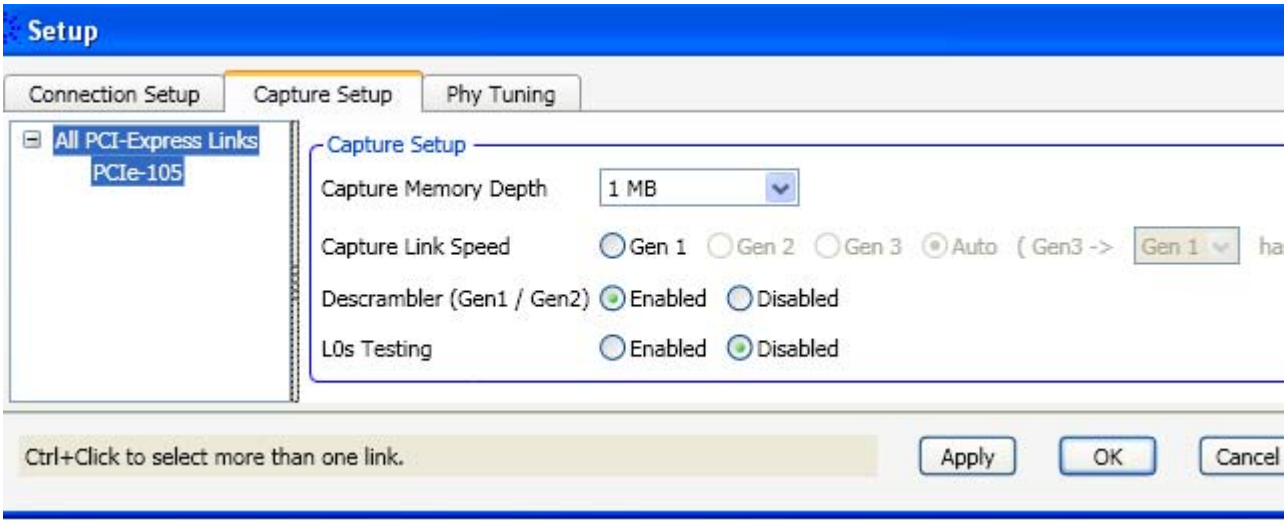
The Capture Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you set basic capture options.

1 In the *Agilent Logic and Protocol Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Capture Setup** tab.

3 In the Capture Setup tab, select the appropriate options.



Capture Memory Depth	Lets you select the trace memory depth. Deeper traces capture more activity but take longer to save and process.
Capture Link Speed	Lets you specify the link speed of the data to be captured: • **Gen 1** — select this when capturing data on 2.5 Gbps links. • **Gen 2** — select this when capturing data on 5 Gbps links. • **Gen 3** — select this when capturing data on 8 Gbps links. • **Auto** – select this option when testing link speed switching scenarios. On selecting this option, analyzer automatically detects the link speed change and accordingly starts capturing data based on the changed link speed. The Auto option also has a drop-down listbox displayed with it. From this listbox, you can select either Gen1 or Gen2. If you select **Gen1** from this listbox, then analyzer prioritizes and captures the Gen 1 ordered sets while switching speed from Gen 3. If you select **Gen2** from this listbox, then analyzer prioritizes and captures the Gen 2 ordered sets while switching speed from Gen 3. Based on the selected link speed, the speed LED of the Analyzer pod on which the logical Lane 0 is present will glow. The following color coding is used to interpret the status of the speed LED. • Off - This means that the system is not configured. • Red - This means that the link speed is not detected or not configured. • Yellow - This means that the link speed is 2.5 Gb/s. • Green - This means that the link speed is 5 Gb/s. • Blue - This means that the link speed is 8 Gb/s. If you selected a fixed speed (Gen1, Gen2, or Gen3), then the speed LED will glow according to the selected speed. If you selected the Auto speed option, then the speed LED will glow according to the detected speed.

Descrambler (Gen1 / Gen2)	Tells the analyzer whether the descrambler algorithm is necessary: • **Enabled** — activates the descrambler algorithm. This algorithm generates the descrambled packet stream from an incoming scrambled packet stream. • **Disabled** — deactivates the descrambler algorithm. Select this option when the DUT is transmitting the non-scrambled data. Garbage data is displayed if this is set incorrectly.

L0s Testing	Lets you select whether or not the U4301A module will capture packets in the L0s state.
	• **Enabled** - When you enable the **L0s Testing** option, the U4301A module captures packets in the L0s state and the power management testing capabilities are enabled and enhanced in terms of :
	  • improvement in locking time
	  • faster data capture while coming out of the electrical idle
	• **Disabled** - When you disable the **L0s Testing** option, the power management testing capabilities are available but not enhanced.

NOTE

When testing L0s/L1, ensure that you:

- set manual lane polarity.

- select a fixed capture link speed instead of the Auto speed.

5
Tuning the Analyzer for a Specific DUT

PCIe Gen3 Tuning Overview

What is Tuning

Tuning is the process of adjusting Agilent's probing system to remove the effects of different driving silicon, termination silicon (or other termination schemes), imperfect transmission paths, and the fact that the probes may not be in the "ideal" location for receiving a high-speed signal (that is, at the end of the transmission path).

Furthermore, a PCIe Gen3 system will negotiate its own TX Linear Equalization, and you would like to have the largest eye possible. Tuning does not affect either the transmitter or the receiver; it is used only to increase the eye as seen by the U4301 Analyzer module. This process involves getting the system/device-under-test to a stable PCIe Gen3 transmission state which the analyzer then optimizes its own equalizations settings for.

How Tuning Works

For tuning, you:

- either use a predefined physical layer tuning (.ptu) file with default tuning values appropriate for your probing and connection setup.
- or create a physical layer tuning (.ptu) file..

The .ptu file contains the information necessary to adjust the probing system for a specific device-under-test (DUT). At the 8 Gbps speed, you then need to load this .ptu file into the U4301 Analyzer module's software to have the best possible eye at the Analyzer.

It is recommended that you first use a predefined .ptu file with default tuning values. If the default tuning values do not provide robust and clean tracing results, you should consider creating your own .ptu file.

From this release of the Agilent PCIe Gen3 software, you can create or fine tune a .ptu file using the Agilent Logic and Protocol Analyzer GUI.

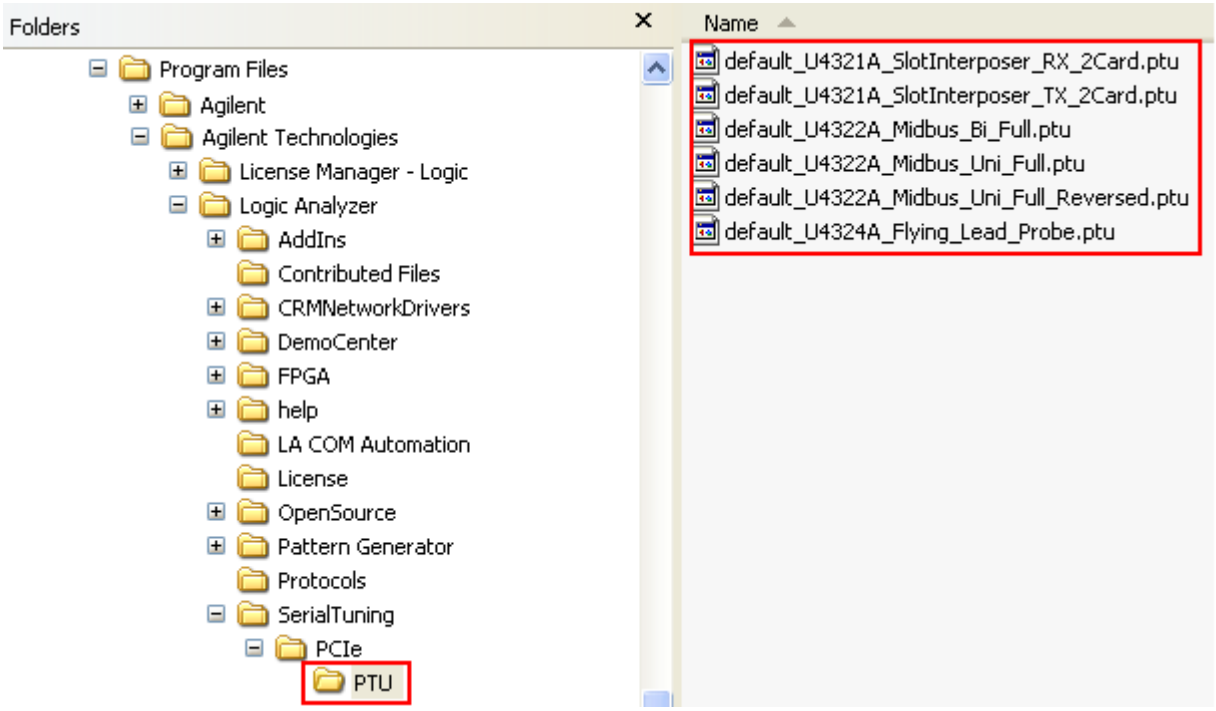
When to Perform Tuning

You should only perform tuning when all of the following conditions are met:

- Poor trace quality which may include red packets, triggers on “Loss of Sync” or “Channel Bonding”.
- No Recovery cycles (that is, cannot Trigger on “Any TS”) on the target.
- When no existing .ptu files are able to provide robust tracing.

Default and User Defined .ptu Files

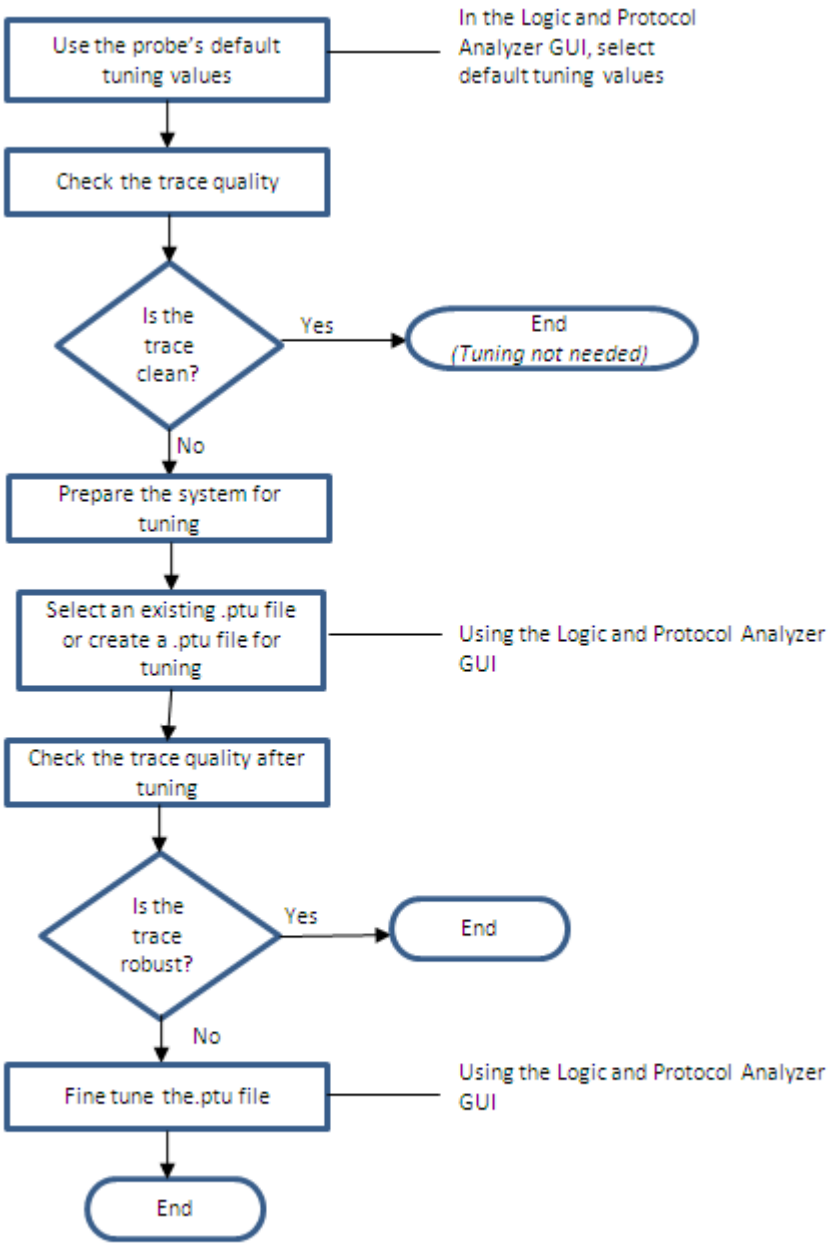
A set of default tuning (.ptu) files are provided with the Agilent Logic and Protocol Analyzer software. These tuning files contain the probe defaults to compensate for the signal impairments associated with the probe. These files are named on the basis of the probe type for which these are created. Based on the probe type you are using, one of these files is used and if the trace quality is clean, you do not need to tune further by creating your own .ptu file. These default .ptu files work fine and support robust tracing in situations where the targets have margin. The following screen displays the location of these default ptu files.



However, if the default .ptu file does not serve the purpose and you find the trace quality to be poor, you can create your own .ptu file with your specific parameters and use it in the Logic and Protocol Analyzer GUI to perform tuning. You can create a .ptu file using the Logic and Protocol Analyzer GUI.

Tuning - Broad steps

The following picture illustrates the broad steps involved in the tuning flow.



All these steps are described in detail in the topics that follow.

Tuning Method

While creating a .ptu file using the Logic and Protocol Analyzer GUI, the **AnalogTune** tuning method is used. This method minimizes the deviations of the observed Vertical Eye characteristics versus the desired Vertical Eye characteristics. From the DUT participation perspective, this method only requires that the DUT must not have transitions to or from Electrical Idle at 8Gbps.

Preparing the U4301A Module and DUT for Tuning

Perform these steps to prepare the setup for tuning:

1 Connect the U4301A Analyzer module to the DUT. Refer to the *PCI Express Gen3 Hardware and Probing Guide* to know how to connect Analyzer to the DUT based on your specific probing situation.

The following Agilent probing options are supported for use with the Analyzer module.

- U4321A solid slot interposer.

  Note that there are four connections on this interposer; the upper two are for the "To Upstream" path (assuming that the card plugged into the top connector of the interposer is the downstream side). The lower two connectors are for the "to Downstream" direction.

- U4322A soft touch midbus 3.0 probe.

  Note that there are several supported footprints that define what lanes are at specific physical connections.

- U4324A PCIe Gen3 flying lead probe.

  Each of these probes provides support for probing one to four channels of a PCIe link making it a total of 16 channels probing support for a set of four probes.

2 If the Resource Bus connector is connecting two Analyzer modules together (the connector at the left of the modules), remove the Resource Bus Connector and do the tuning of one module at a time.

After you have tuned, you can reconnect the Resource Bus Connector without affecting the tuning.

3 Your DUT must enter L0 at Gen3 speed (8 Gbps).

4 The DUT must not transition to or from Electrical Idle at 8Gbps and its TXEQ should have stabilized before tuning. If the DUT is experiencing Recovery cycles, it is likely that it will change its TXEQ to achieve stability.

5 Ensure that the connection settings such as the number of lanes in use and the lanes inverted by the transmitter are correctly set up in the **Connection Setup** tab of the U4301A module's Setup dialog box before starting the tuning. These settings are used in the tuning process and incorrect settings can result in incorrect tuning.

Creating a Physical Layer Tuning File

After you have prepared your system for tuning and configured the connection setup for the U4301A module, you can create a physical layer tuning (.ptu) file. This file stores the information about the test setup (lane inversions, number of lanes, etc) and the tuning parameters that were discovered during tuning. You use this file in the PCIe Analyzer setup in the Logic and Protocol Analyzer GUI to tune the system.

To create a physical layer tuning file

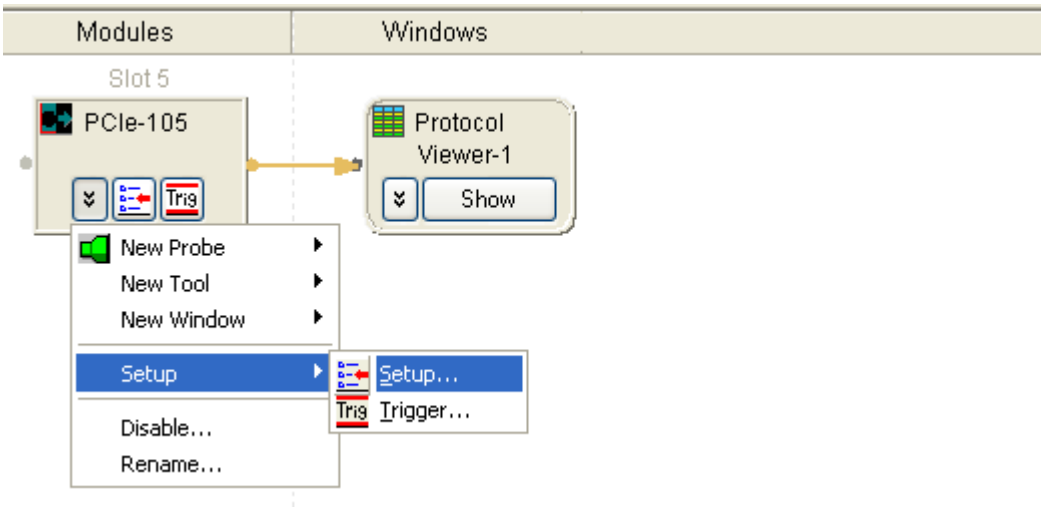
Perform these steps on the host PC that is physically connected to the U4301 Analyzer module.

1 Exit the *Agilent Logic and Protocol Analyzer* application if it is currently active.

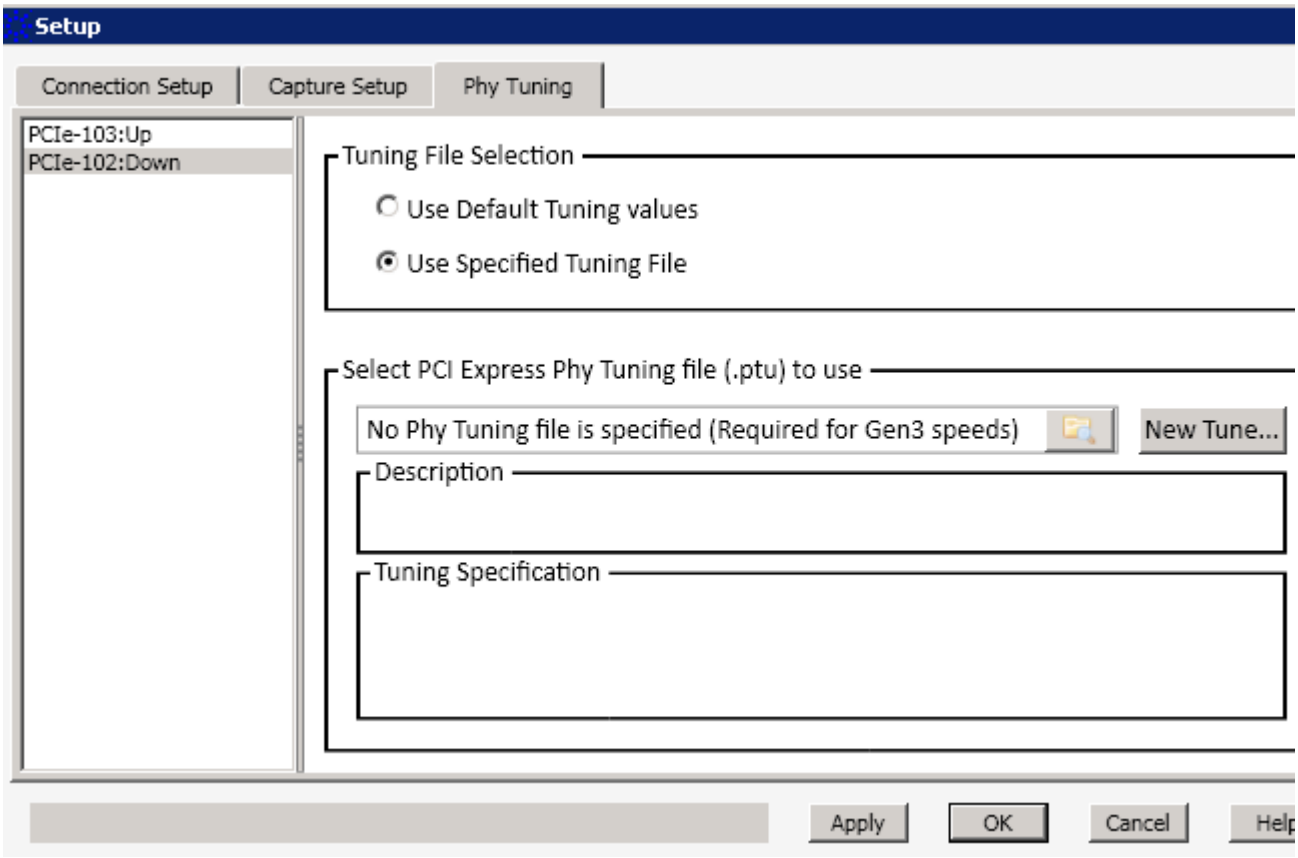
2 Start the *Agilent Logic and Protocol Analyzer* application.

This is done to ensure that all the default settings in the analyzer software are used.

3 In the Logic and Protocol Analyzer GUI's Overview window, select **Setup>Setup...**. from the PCIe analyzer module's drop-down menu to access its Setup dialog box.



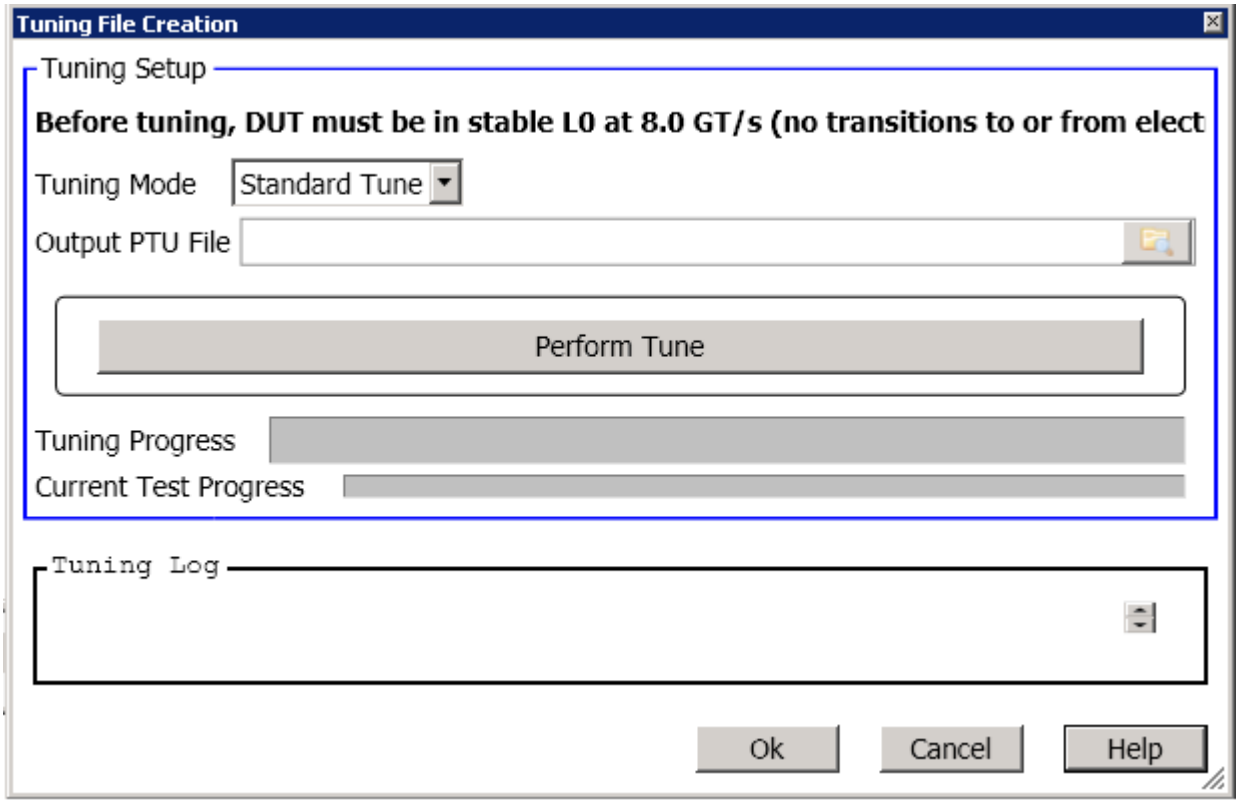
4 Click the **Phy Tuning** tab of the Setup dialog box.



5 The left pane of the Phy Tuning tab displays a list of the currently available PCIe Analyzer modules. From this list, select the module which you want to tune.

6 Select the **Use Specified Tuning File** option from the **Tuning File Selection** section.

7 Click the **New Tune...** button to open the **Tuning File Creation** dialog box.



8 Select one of the following two options from the **Tuning Mode** listbox.

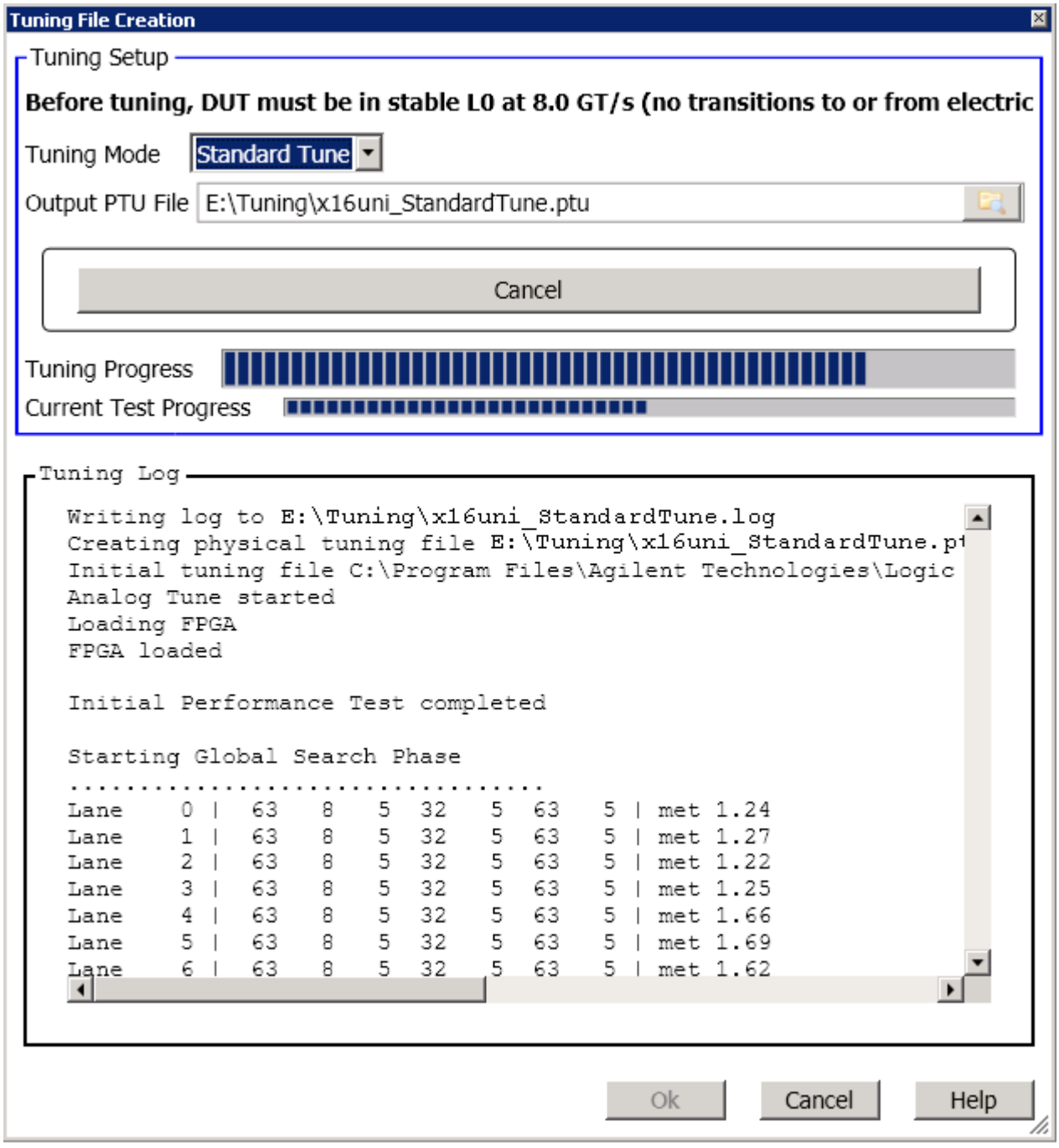
- **Standard Tune** - This option performs an Analog Tune followed by a fine tune. In this option, the number of iterations for a tuning test completion are more than the number of iterations in the Quick Tune option. Standard Tune, therefore takes more time than Quick Tune.
- **Quick Tune** - This option also performs an Analog Tune followed by a fine tune. However, the number of iterations for a test are lesser making this option suitable for performing tuning quickly.

NOTE The third option - **Fine Tune Previous Results** in the Tuning Mode listbox is meant for fine tuning a previously created .ptu file.

9 Click the  icon displayed with the **Output PTU File** field to browse and specify the name and location for the .ptu file.

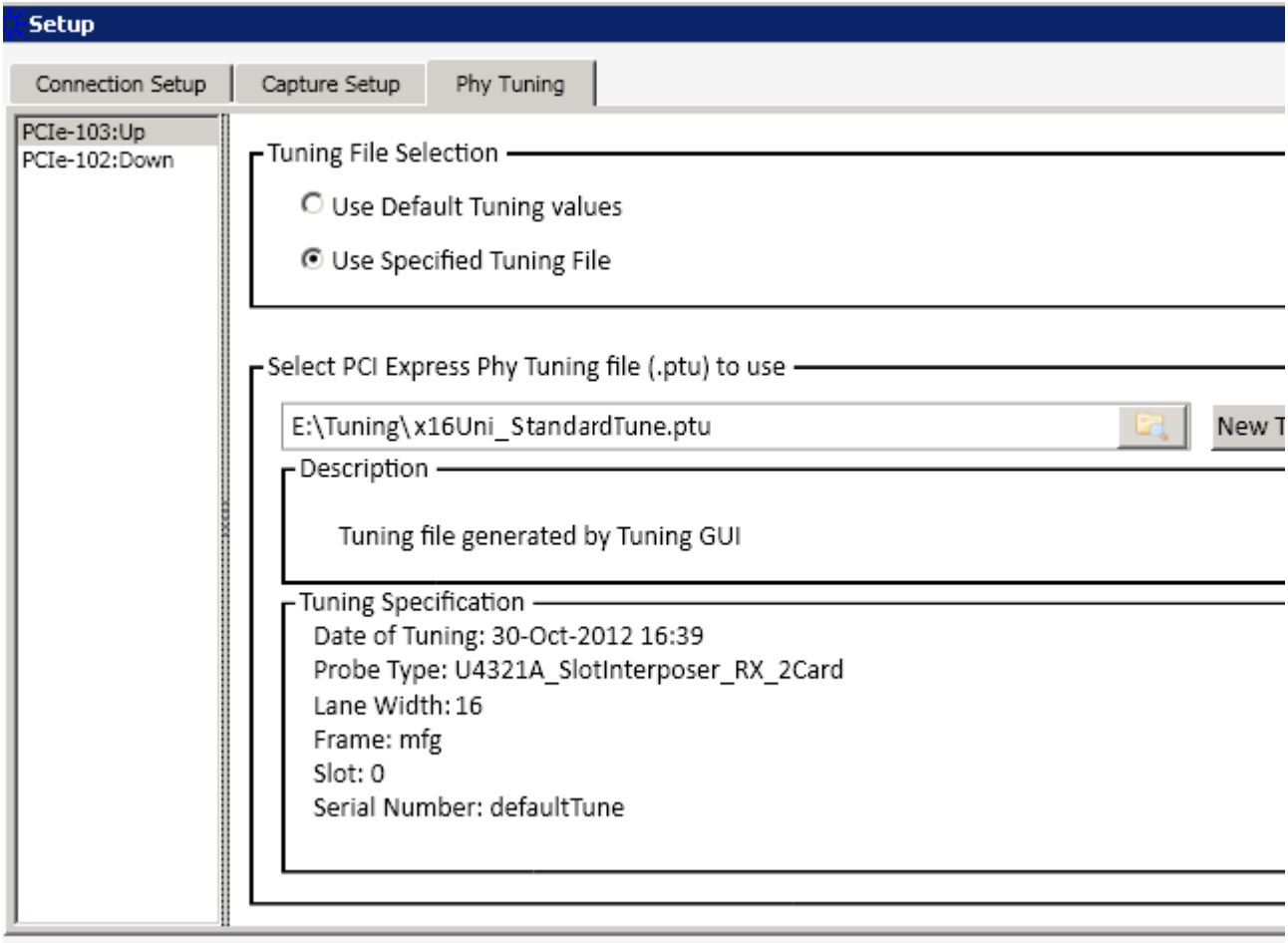
10 Click **Perform Tune**.

The tuning process starts. The **Tuning Log** section displays the results of the tuning process run operation. If the tuning process completes successfully, the specified .ptu file gets created. A tuning log file is also created with the same name and location as the tuning file.



11 Click **OK** to close the Tuning File Creation dialog box.

The newly created tuning file is now loaded for use in the Phy Tuning tab.



LEDs display during BER Based Tuning

The U4301 Analyzer module has 16 channel LEDs and four speed LEDs. The following table lists the interpretation of these LEDs display during BER-based tuning.

Channel LEDs	
Green	Indicates no bit errors on that lane.
Yellow	Indicates loss of sync or "OK"/"ERROR" is toggling quickly. You get "shades of yellow", usually, when there are frequent bit errors.
Red	Indicates bit error on that lane.
Blinking Red / Off	Indicates input FIFO overflow.
Speed LEDs	
Off	Indicates an Idle state.

Channel LEDs	
Blue	Indicates that the data is being taken.

For a general description of the channel and speed LEDs, refer to the *PCI Express Gen3 Hardware and Probing guide*. You can download this guide from www.agilent.com.

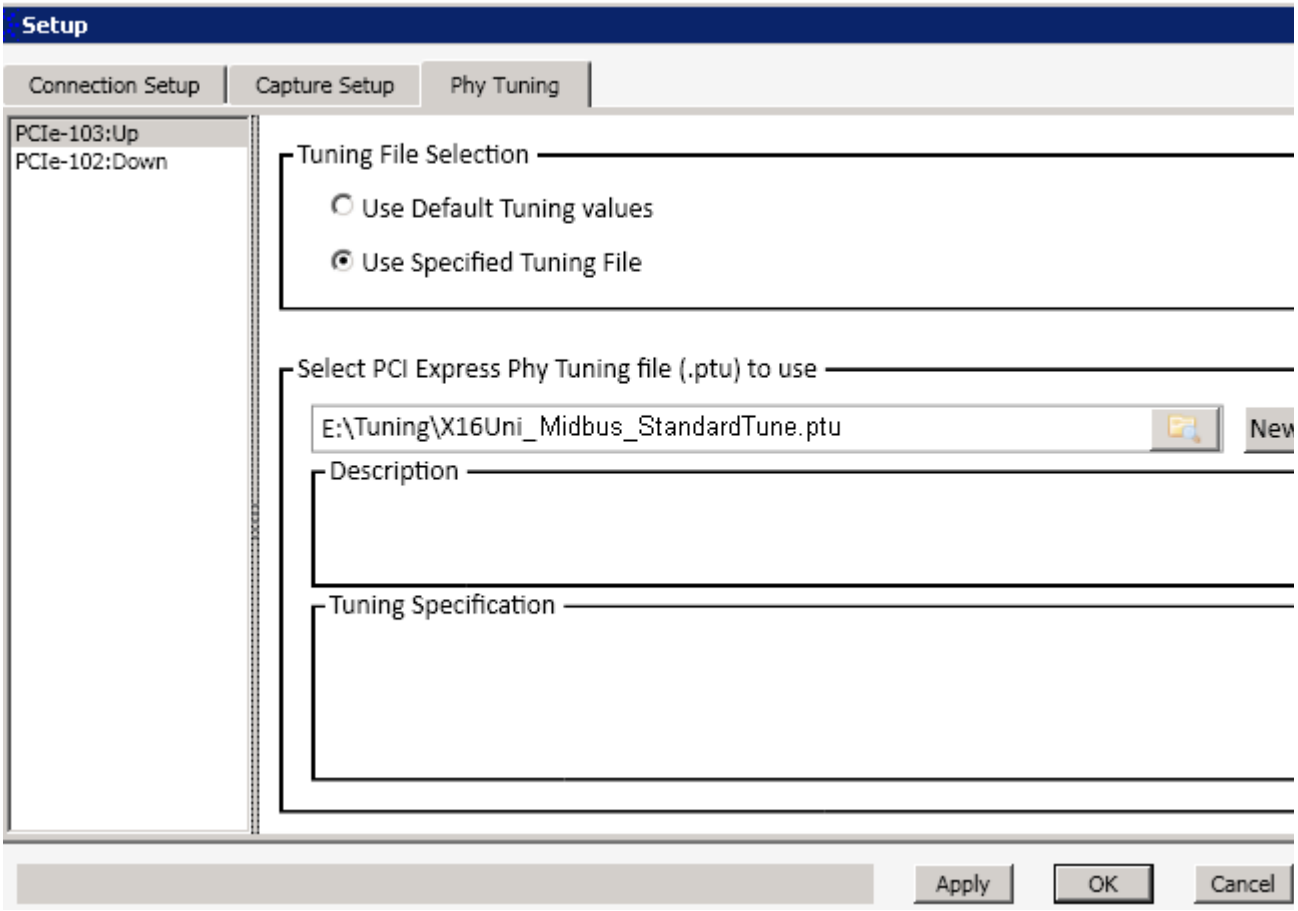
Loading a Tuning File in the Logic and Protocol Analyzer GUI

The Phy Tuning tab lets you load a user-created physical tuning (.ptu) file or the default tuning values from a predefined tuning file.

To load a specified tuning file or default tuning values

1. In the *Agilent Logic and Protocol Analyzer* application's Overview window, select **Setup>Setup...** from the PCIe Gen3 analyzer module's drop-down menu.
2. Click the **Phy Tuning** tab.
3. The left pane of the Phy Tuning tab displays a list of the currently available PCIe Analyzer modules. From this list, select the module for which you want to select a tuning file.
4. To load default tuning values:
   a. Select the **Use Default Tuning Values** option from the **Tuning File Selection** section. On selecting this option, the software automatically uses the default tuning values from the predefined .ptu file applicable for your probing and connection setup. This is the default and recommended option for an initial run. If the default tuning values do not produce robust and clean tracing results, you should load a user-specified PTU file for tuning (described in the next step).
5. To load a user-specified tuning file:
   a. Select the **Use Specified Tuning File** option to load a user-specified tuning file.
   b. Click the  icon displayed with the **Select PCI Express PHY Tuning File (.ptu) to use** section to browse and navigate to the tuning file that you want to load.
   c. Select the tuning file and click **Open** in the Open dialog box.

   The tuning file is now loaded for use.



6 Click **Apply** or **OK**.

Tuning a Bidirectional Setup

A single U4301A module can support a x1 to x8 bidirectional configuration. To tune a U4301A module in a x1 to x8 bidirectional configuration, you just need to tune once. A single tuning file is used to perform tuning for both directions.

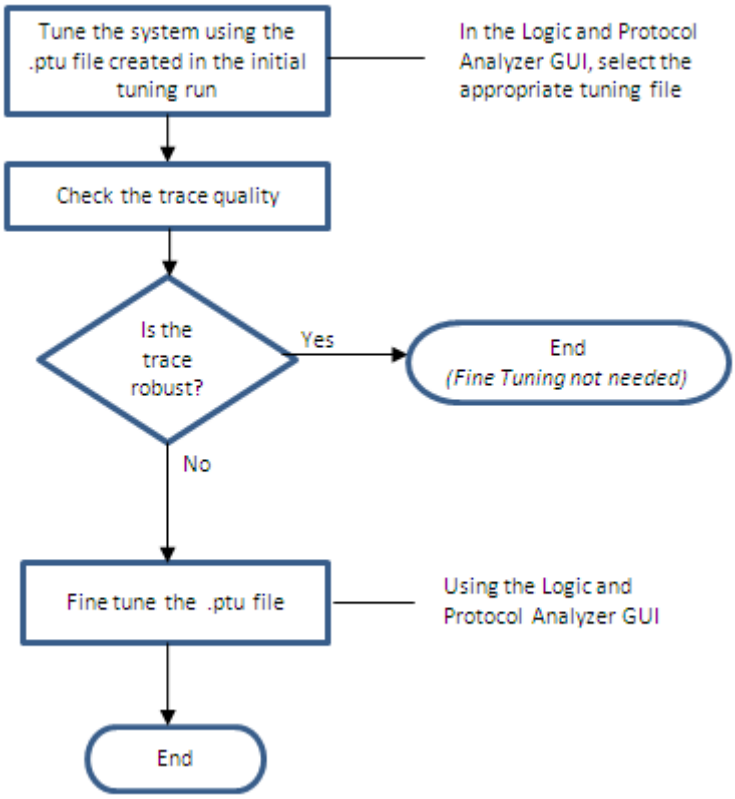
However, for a x16 bidirectional configuration, you need two U4301A modules. Therefore, for such a configuration, you need two separate tuning files, one for each module. Each module is tuned separately using its tuning file.

Fine Tuning a .ptu File

If the .ptu file that you created does not produce robust and clean tracing, then you can fine tune the .ptu file to get the desired results from tuning.

Fine Tuning Flow

The following picture illustrates the fine tuning flow.



To fine tune a .ptu file

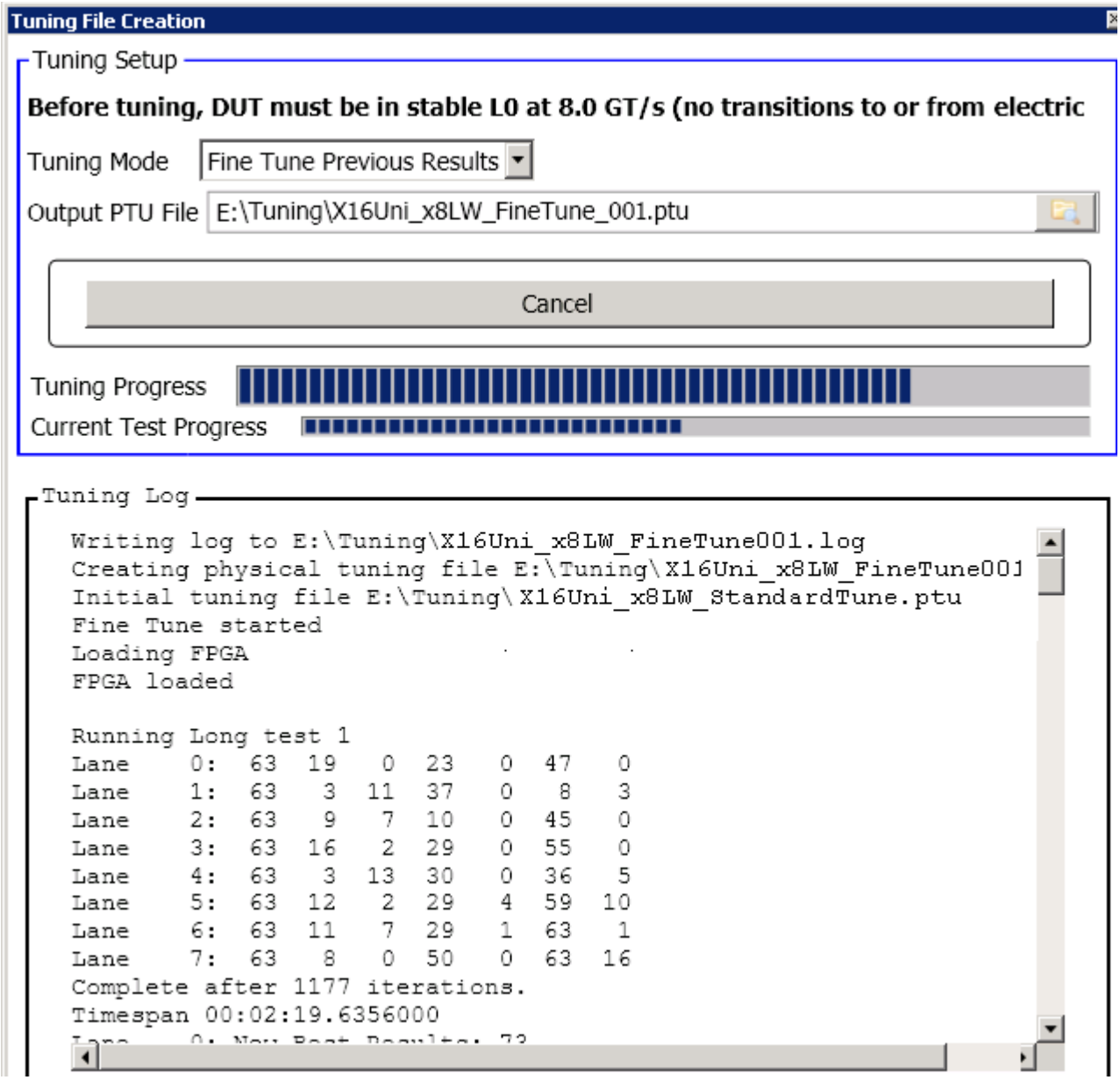
1. In the Setup dialog box of the U4301A Analyzer module, click the **Phy Tuning** tab.
2. Ensure that the **Use Specified Tuning File** option is selected and the .ptu file that you want to fine tune is selected in the **Select PCI Express Phy Tuning File (.ptu) to use** section. If no .ptu file is selected, then the default predefined .ptu file applicable for your probe and connection setup is used for fine tuning.
3. Click **New Tune...**.

4 Select **Fine Tune Previous Results** from the **Tuning Method** listbox in the **Tuning File Creation** dialog box.

5 Click the  icon displayed with the **Output PTU File** field to browse and specify the path and location of the tuning file that will be generated after the fine tuning process.

6 Click **Perform Tune**.

The fine tuning process starts and the fine tuning progress is displayed with a progress bar.



7 When fine tuning completes, click **OK** to close the Tuning File Creation dialog box.

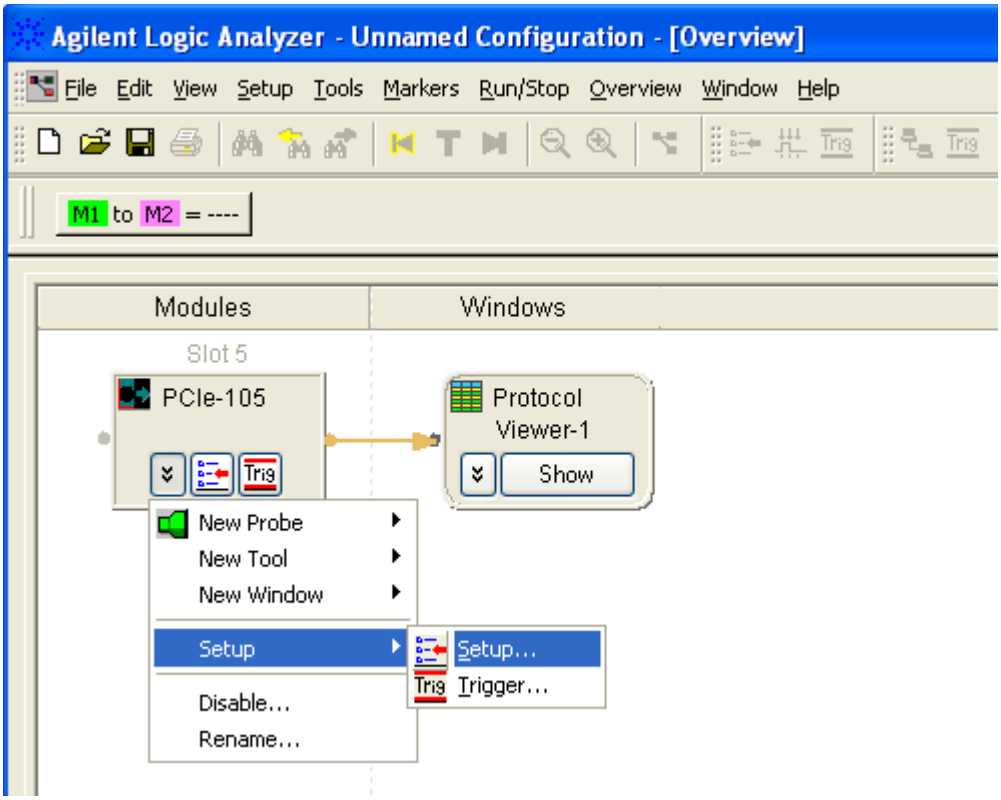
On successful completion, the fine-tuned PTU file is created at the specified location along with a tuning log with the same name as the fine-tuned PTU file.

6 Manually Adjusting the Equalizing Snoop Probe (ESP) Settings

The Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you manually adjust the equalizing snoop probe (ESP) settings.

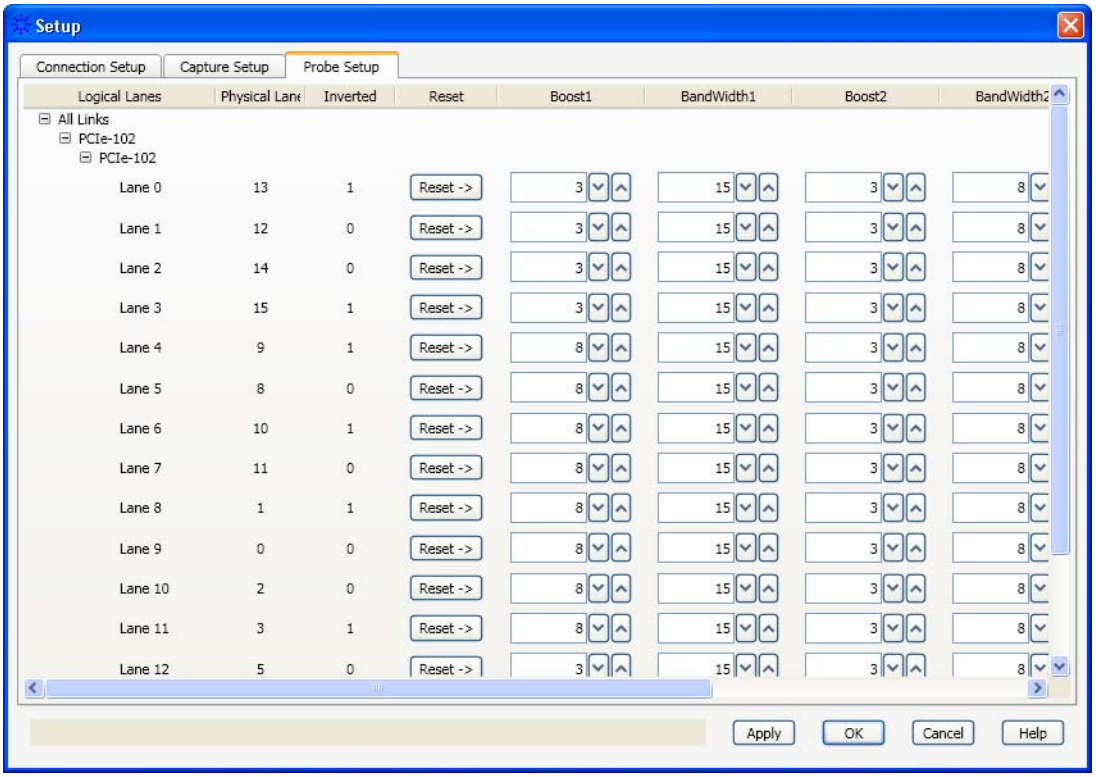
NOTE To enable the Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog, you must check the Enable Advanced Probe Settings (ASP) option in the Options dialog. See "Options Dialog" (in the online help).

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Probe Setup** tab.

3 In the Probe Setup tab, select the appropriate options.



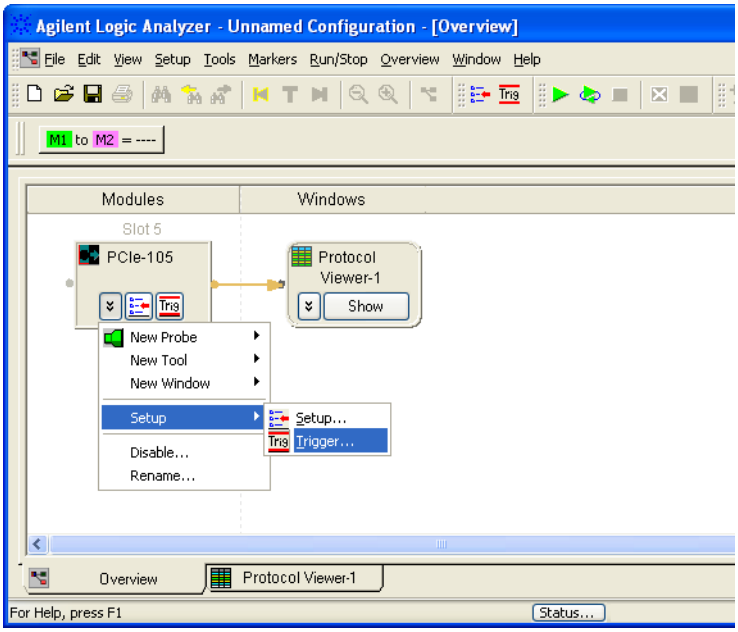
For each lane in the links, you can adjust the boost and bandwith settings. Click **Reset ->** to restore the original settings.

7 Setting Up Triggers

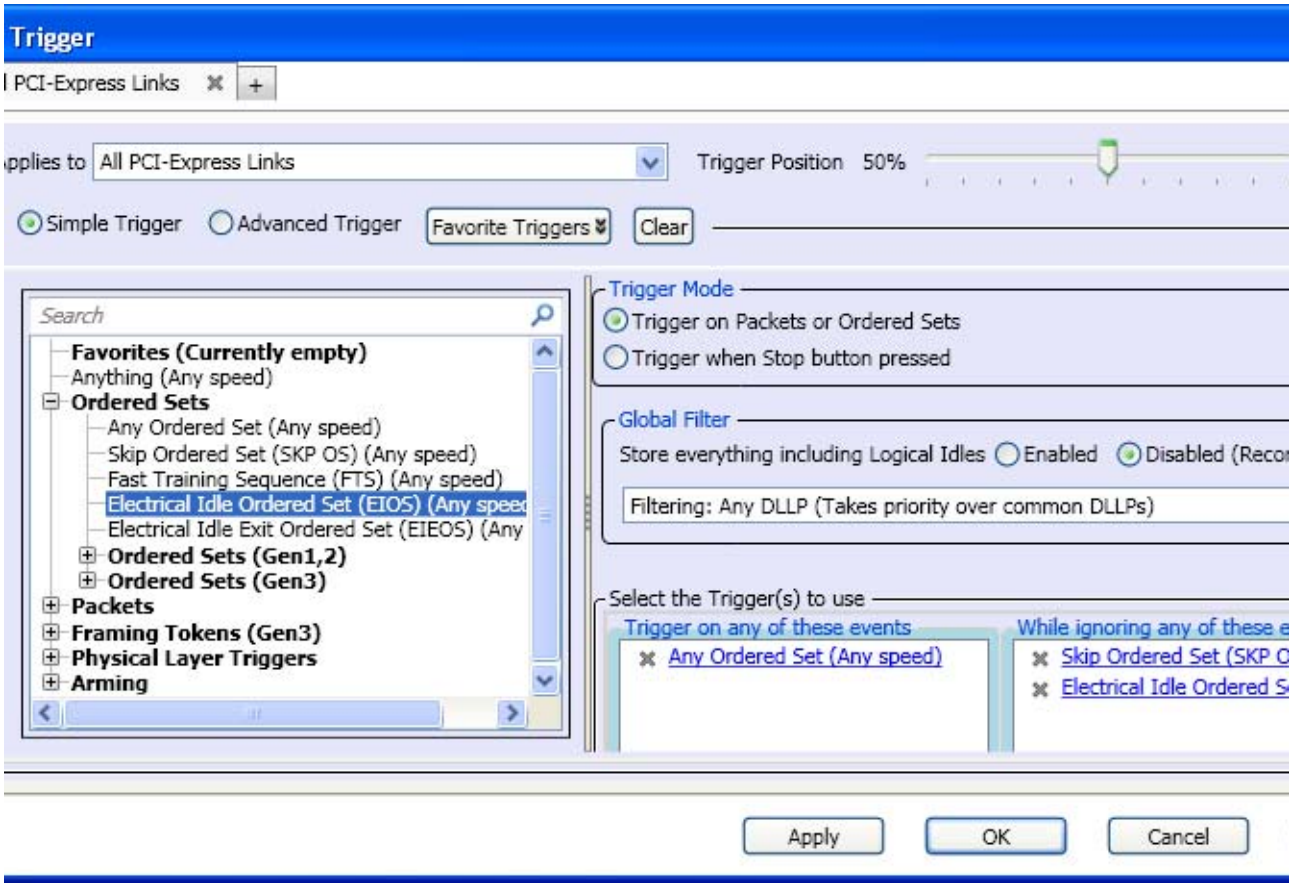
The U4301A PCIe Gen3 analyzer lets you set up triggers (events that specify when to capture a trace) with simple or advanced dialogs.

Setting Up Simple Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Simple Trigger** option.

b Select the **Trigger on Packets or Ordered Sets** Trigger Mode option.

(The **Trigger when Stop button is pressed** Trigger Mode option can be useful, for example, to see the events that lead up to a stop, halt, etc.)

c From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a result, analyzer will keep running and you need to stop it

manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you would like to trigger on from the left-side pane to the **Trigger on any of these events** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed.

To edit events in the trigger box, click the underlined event name.

To remove events from the trigger box, click the "X" to the left of the event name.

d Drag events you'd like to exclude from the trigger to the **While ignoring any of these events** box.

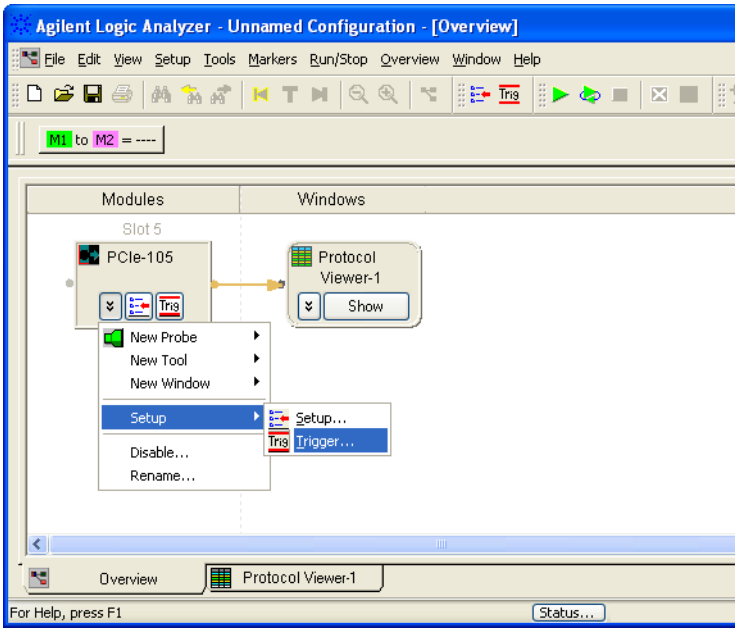
e Click **Apply** or **OK**.

See Also

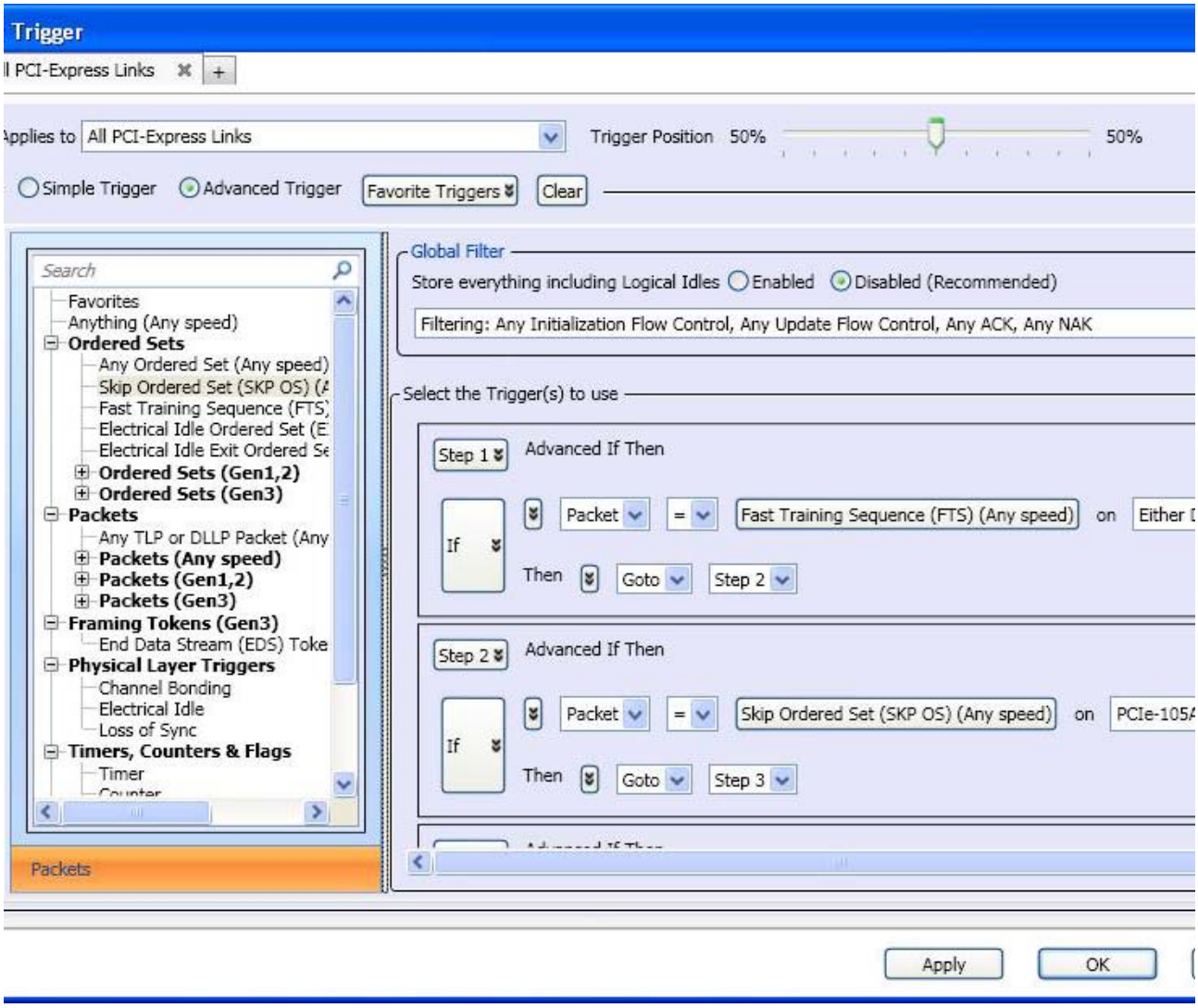
- "To select which links the trigger is for" on page 60
- "To set the trigger position" on page 60
- "To save/recall favorite triggers" on page 61
- "To clear the current trigger" on page 61

Setting Up Advanced Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Advanced Trigger** option.

b From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a

result, analyzer will keep running and you need to stop it manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you'd like to trigger on from the left-side pane to sequence steps in the **Select the Trigger(s) to use** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed. (This is the same event hierarchy displayed in the simple trigger dialog.)

To edit events in the trigger box, click the event button.

To remove events from the trigger box, click the sequence step buttons.

d In the **Select the Trigger(s) to use** box, click buttons, make drop-down selections, and enter values in fields to edit the steps in the trigger sequence:

- The **Step** buttons let you insert or delete steps.
- The **If**/**Else if** buttons let you insert or delete "if" clauses.
- The event chevron buttons let you insert, delete, or logically group (or negate) events.
- The direction drop-down listbox is displayed if you configured the U4301A module's connection setup as a bidirectional setup. It lets you select the direction (upstream or downstream) applicable for the trigger sequence. For a unidirectional data capture setup, this listbox is not displayed.
- The action chevron buttons let you insert or delete actions.
- Use the **Comment** fields to document your advanced triggers.

e Click **Apply** or **OK**.

See Also

- "To select which links the trigger is for" on page 60
- "To set the trigger position" on page 60
- "To save/recall favorite triggers" on page 61
- "To clear the current trigger" on page 61

Setting General Trigger Options

The top part of the Trigger dialog contains general options that apply to both simple and advanced triggers.

To select which links the trigger is for

The top of the Trigger dialog has tabs that let you set up separate triggers for different links. You can add tabs for separate triggers and apply them to the links that are set up in the Connection Setup dialog (see Chapter 3, “Specifying the Connection Setup,” starting on page 15).

To set the trigger position

The top of the Trigger dialog has a slider for setting the trigger position within the capture memory.

Note that the pre-trigger portion of the capture memory is filled before searching for the trigger.

To save/recall favorite triggers

The top of the Trigger dialog has a **Favorite Triggers** drop-down menu for saving trigger setups and recalling previously saved trigger setups.

Do not confuse these "favorite" triggers with the favorites that appear in the left-side pane (which are added using the Event Editor dialog).

To clear the current trigger

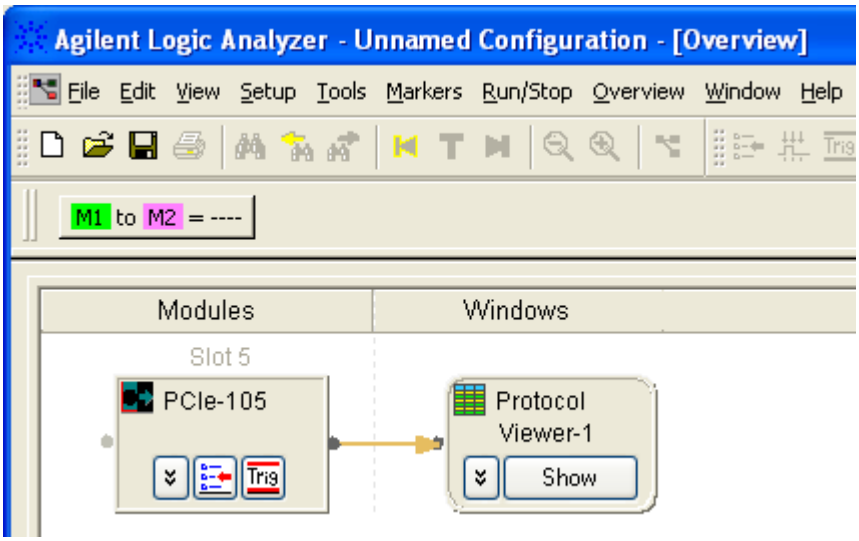
The top of the Trigger dialog has a **Clear** button for erasing the current trigger setup and restoring the default trigger setup.

8 Running/Stopping Captures

Running and stopping the U4301A PCIe Gen3 analyzer is just like running and stopping any other analyzer. See "Running/Stopping Measurements" (in the online help).

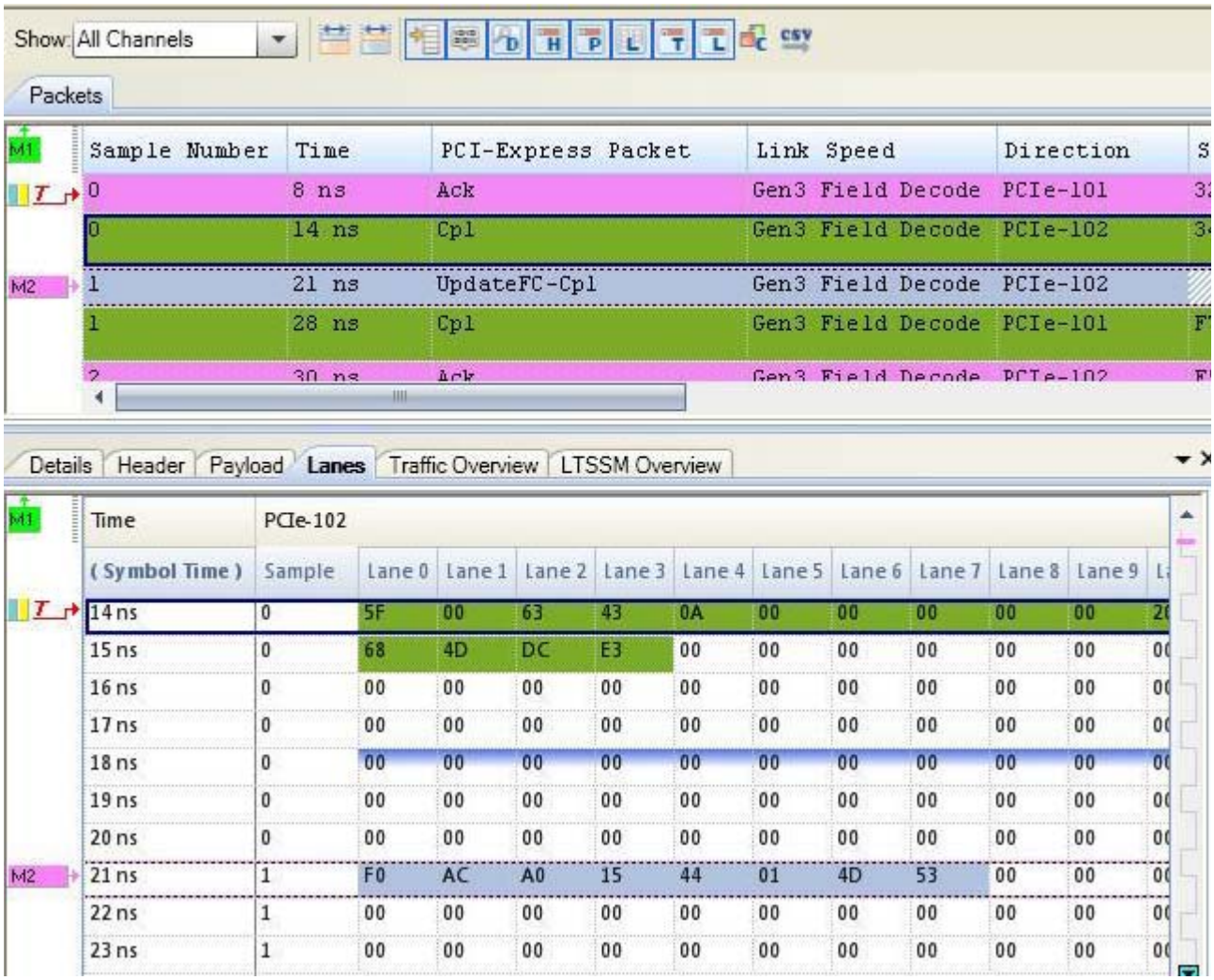
9 Viewing PCIe Gen3 Packets

You can view the data captured by the U4301A PCIe Gen3 analyzer using the Protocol Viewer window. See “Analyzing Packet Data” (in the Agilent Logic and Protocol Analyzer online help). A Protocol Viewer is automatically added for a U4301A PCIe Gen3 analyzer module in the Logic Analyzer GUI.



The Protocol Viewer window displays the summarized and detailed packet information at the same time within two panes. The upper pane lists the packets. On selecting a packet, the details of that packet are displayed in the lower pane.

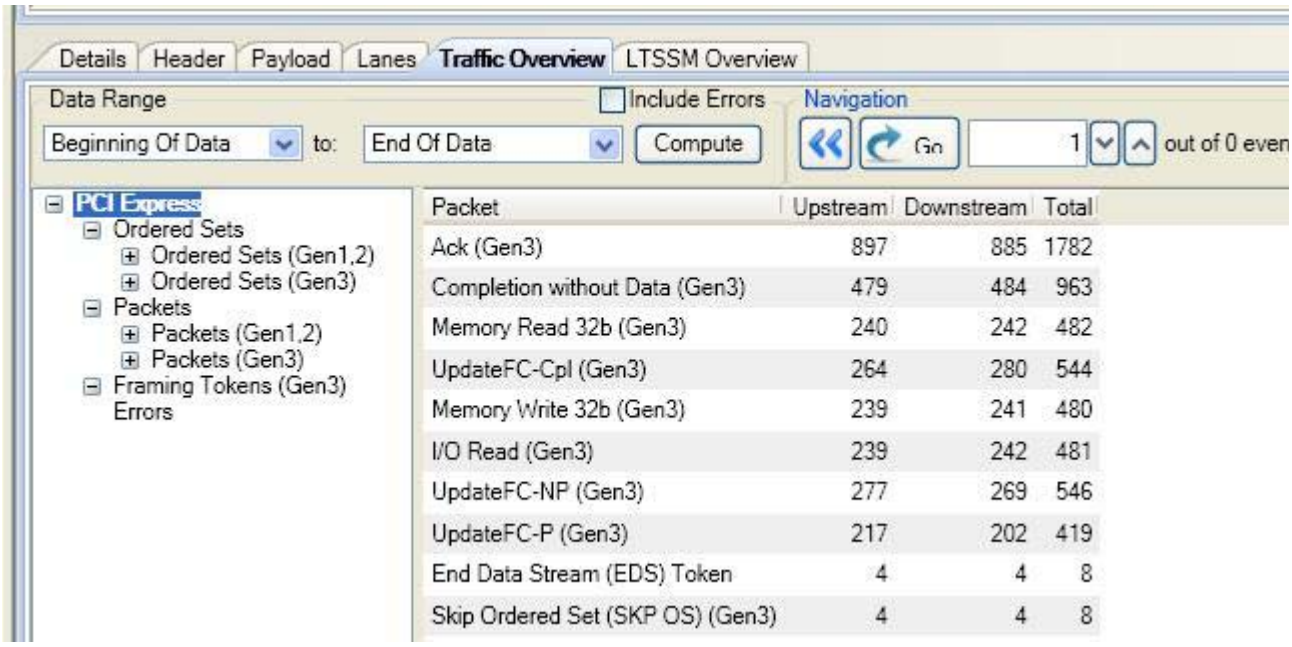
The following screen displays a sample view of the captured PCIe data in the Protocol Viewer window. In this screen, the Lanes tab of the Protocol Viewer window is displayed. The Lanes viewer displays not just the selected packet data across lanes but also the post packet data represented by colors matching the selected packet color in the upper pane.


Show: All Channels
Packets
Sample Number | Time | PCI-Express Packet | Link Speed | Direction
0 | 8 ns | Ack | Gen3 Field Decode | PCIe-101
0 | 14 ns | Cpl | Gen3 Field Decode | PCIe-102
1 | 21 ns | UpdateFC-Cpl | Gen3 Field Decode | PCIe-102
1 | 28 ns | Cpl | Gen3 Field Decode | PCIe-101
Details | Header | Payload | Lanes | Traffic Overview | LTSSM Overview
Time | PCIe-102
(Symbol Time) | Sample | Lane 0 | Lane 1 | Lane 2 | Lane 3 | Lane 4 | Lane 5 | Lane 6 | Lane 7 | Lane 8 | Lane 9
14 ns | 0 | 5F | 00 | 63 | 43 | 0A | 00 | 00 | 00 | 00 | 00
15 ns | 0 | 68 | 4D | DC | E3 | 00 | 00 | 00 | 00 | 00 | 00
16 ns | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
17 ns | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
18 ns | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
19 ns | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
20 ns | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
21 ns | 1 | F0 | AC | A0 | 15 | 44 | 01 | 4D | 53 | 00 | 00
22 ns | 1 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00
23 ns | 1 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00

Viewing the Captured PCIe Traffic Statistics

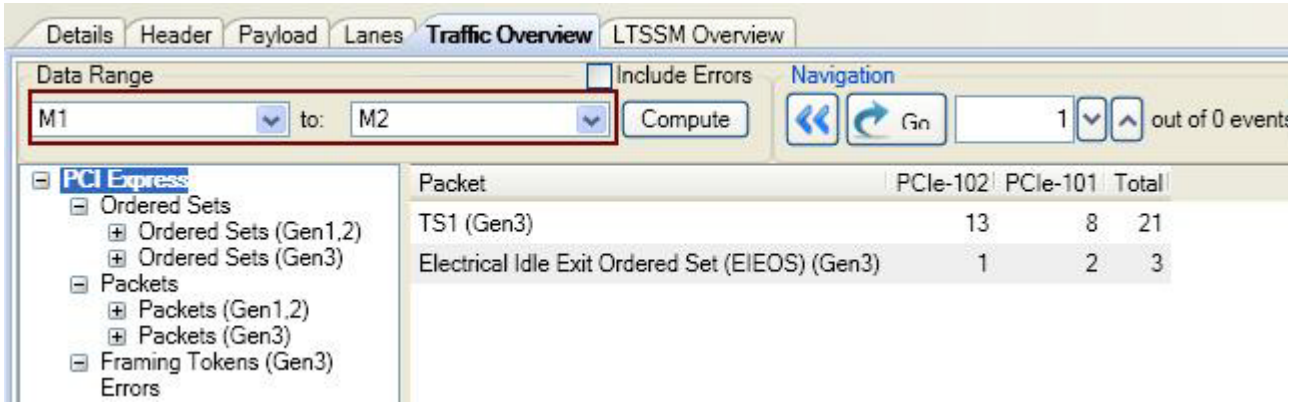
You can use the **Traffic Overview** tab in the lower pane of Protocol Viewer to get an overview of the PCIe traffic that is displayed in the upper pane of Protocol Viewer. This tab provides a count of various PCIe packet types captured and displayed in the upper pane. The count of packets is categorized on the basis of packet types.

For each packet type, the count of packets is further segregated based on the direction (upstream or downstream). The following screen displays the traffic statistics in the lower pane. Notice that for each packet type, the count of packets is displayed for upstream as well as downstream direction along with a sum of packets in both directions.



Packet	Upstream	Downstream	Total
Ack (Gen3)	897	885	1782
Completion without Data (Gen3)	479	484	963
Memory Read 32b (Gen3)	240	242	482
UpdateFC-Cpl (Gen3)	264	280	544
Memory Write 32b (Gen3)	239	241	480
I/O Read (Gen3)	239	242	481
UpdateFC-NP (Gen3)	277	269	546
UpdateFC-P (Gen3)	217	202	419
End Data Stream (EDS) Token	4	4	8
Skip Ordered Set (SKP OS) (Gen3)	4	4	8

You can specify the data range based on which the traffic statistics get computed in the Traffic Overview tab. For instance, you might want to view the traffic statistics only for the PCIe packets between the markers M1 and M2. In such a situation, you can select M1 as the start point and M2 as the end point in the **Data Range** group box and then click **Compute**. Then Protocol Viewer displays the traffic statistics of only the packets that fall in the specified data range and not for all the PCIe packets displayed in the upper pane. The following screen displays the traffic statistics for the data range starting from M1 and ending at M2 markers.

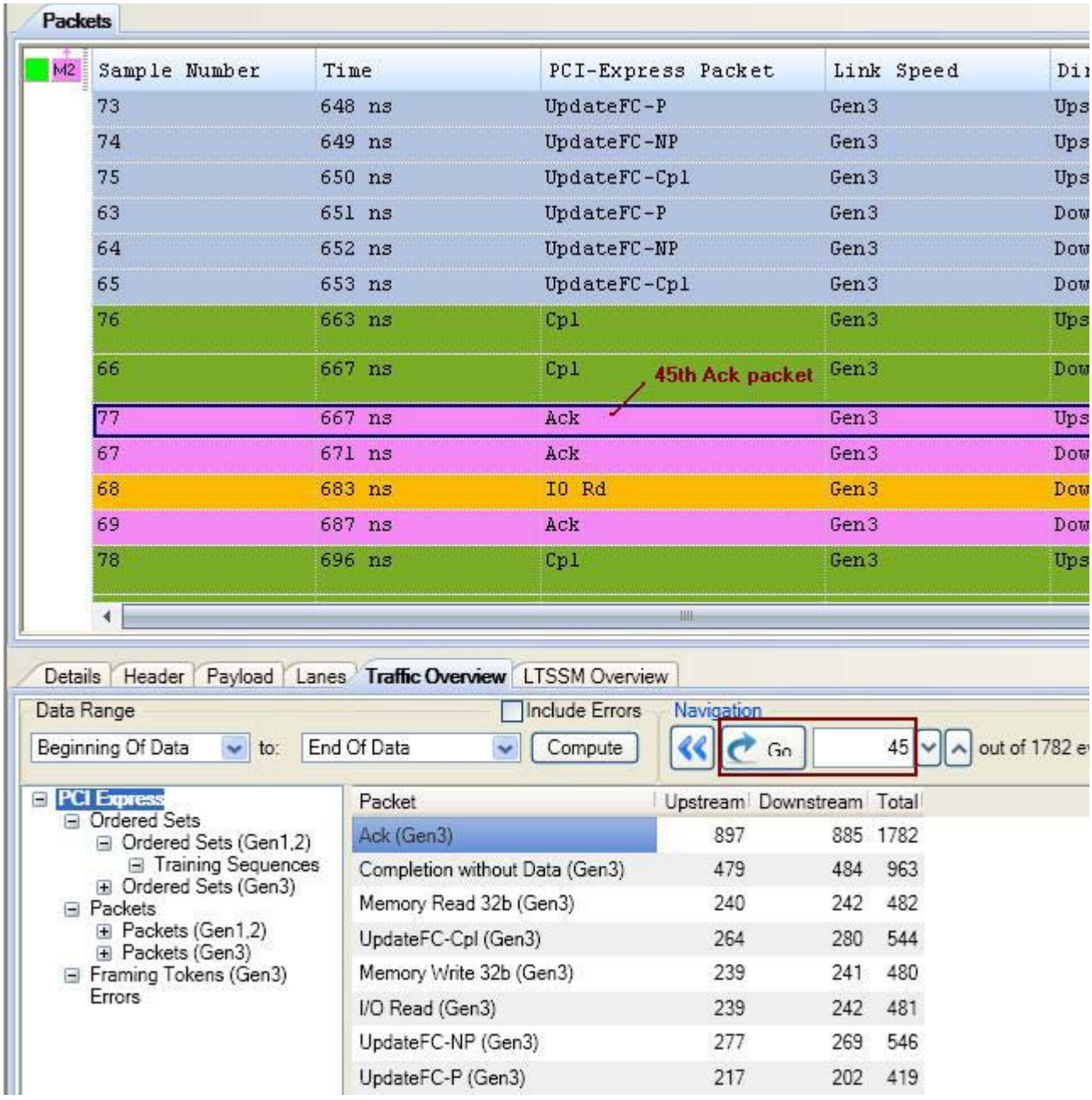


The Compute button is disabled when U4301A PCIe Analyzer module is capturing data. It becomes enabled when the capture has stopped.

Navigating through the captured PCIe packets

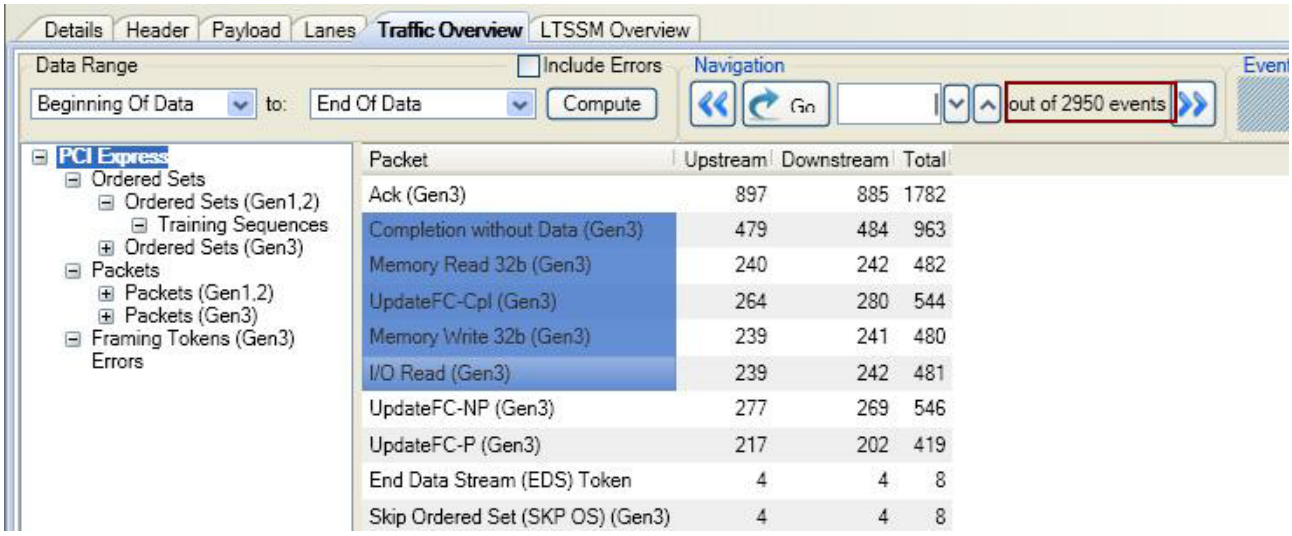
From the displayed traffic overview statistics, you can select a particular packet type and then navigate through the packets displayed in the upper pane for that packet type. For instance, there are total 1782 packets of the type Ack and you want to view the details of the 45th Ack packet out of these 1782 Ack packets. To go directly to the 45th Ack packet out of the total Ack packets, you can select this packet type in the Traffic Overview

results and then type 45 in the Navigation text box and click Go. This takes you directly to the 45th Ack packet in the upper pane of Protocol Viewer.



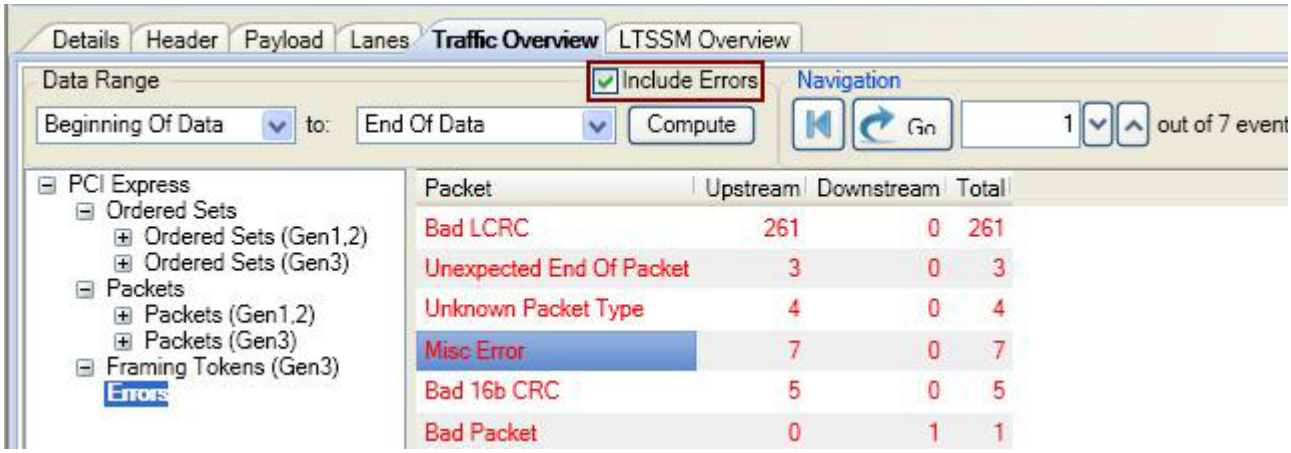
You can also navigate through the PCIe packets of a particular direction (upstream or downstream). To do this, select a particular packet type in the displayed traffic statistics and then select the count column for the required direction. Then specify the packet number in the Navigation text box to reach directly to that packet.

You can also select multiple packet types in the Traffic Overview tab by clicking a packet type and then dragging the mouse over to the other packet types that you want to select. When you select multiple packet types, the Navigation section displays the total packet count for all the selected packet types.



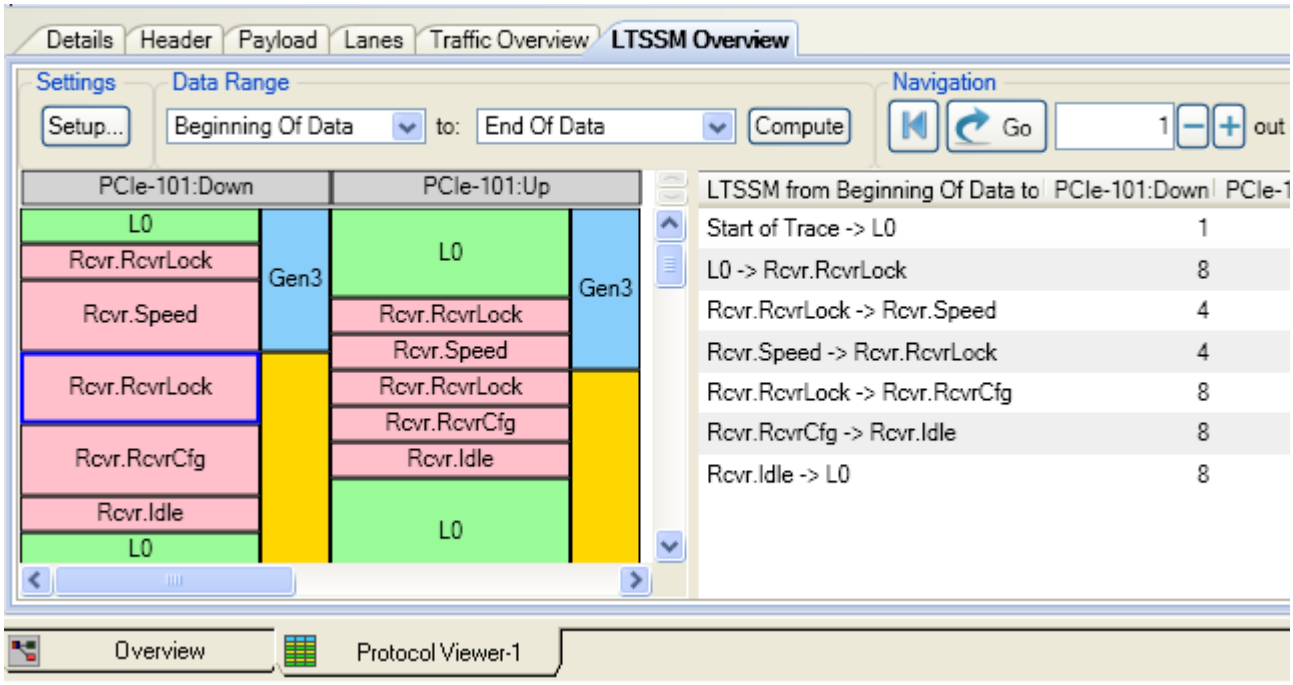
Viewing Errored Packets Statistics

If you want to include the count of errored packets in the traffic overview, then select the **Include Errors** check box. You can then click the Errors option in the left panel of Traffic Overview tab. This displays the count of errored packets categorized based on different error types and direction.



Viewing LTSSM State Transitions

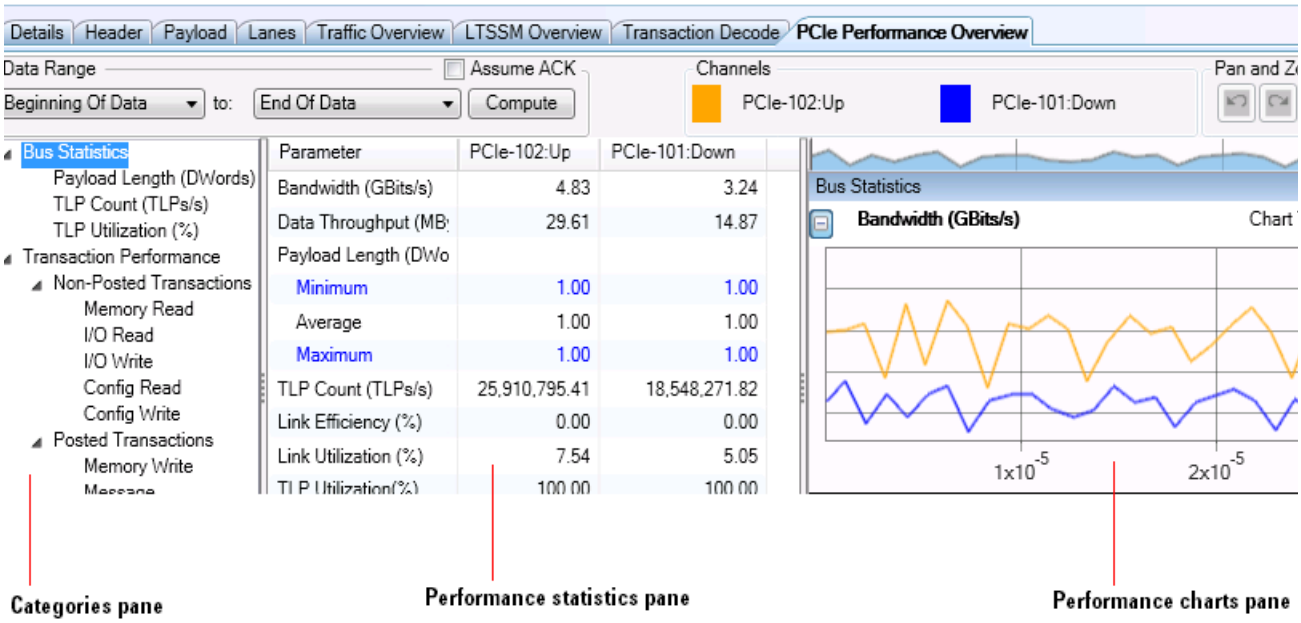
You can use the **LTSSM Overview** tab in the lower pane of Protocol Viewer to get an overview of the LTSSM state transitions that occurred in the PCIe data captured by U4301A module in a trace. This pane provides an overview of the link training process by displaying a sequential list of the LTSSM states and their transitions and the packets exchanged during each state. You can use this information to verify the link training process and find out reasons for any failure in this process.



To get detailed information on how to use Protocol Viewer's LTSSM Overview pane, refer to the chapter "Viewing LTSSM States and State Transitions" on page 75.

Viewing Offline Performance Summary

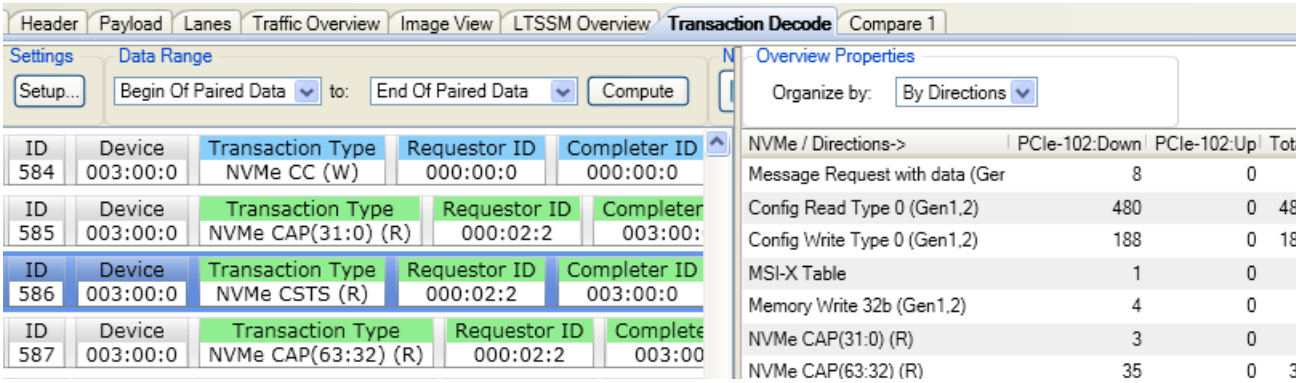
You can use the **PCIe Performance Overview** tab in the lower pane of Protocol Viewer to perform post processing on the captured PCIe traffic and generate an offline performance summary of bus utilization.



To get detailed information on how to use Protocol Viewer's PCIe Performance Overview pane, refer to the chapter "Viewing Offline Performance Summary" on page 131.

Viewing Decoded Transactions

You can use the **Transaction Decode** tab in the lower pane of Protocol Viewer to compute and view transactions decoded from the captured PCIe traffic.



To get detailed information on how to use Protocol Viewer's Transaction Decode pane, refer to the chapter "Computing and Viewing Decoded Transactions" on page 85.

Exporting Captured PCIe Data to a .csv File

You can export the captured PCIe packet information from the Protocol Viewer window to a specified .csv file and use it later in other analysis tools. You do this by clicking the  toolbar button in the Protocol Viewer window. On clicking this toolbar button, the **Protocol Export** dialog box is displayed in which you can specify the details of export such as the range of packet data that you want to export and the delimiter that you want to use to delimit the exported data in the specified .csv file.

For details on how to export data to a .csv file, click the Help button in the Protocol Export dialog box.

10 Viewing LTSSM States and State Transitions

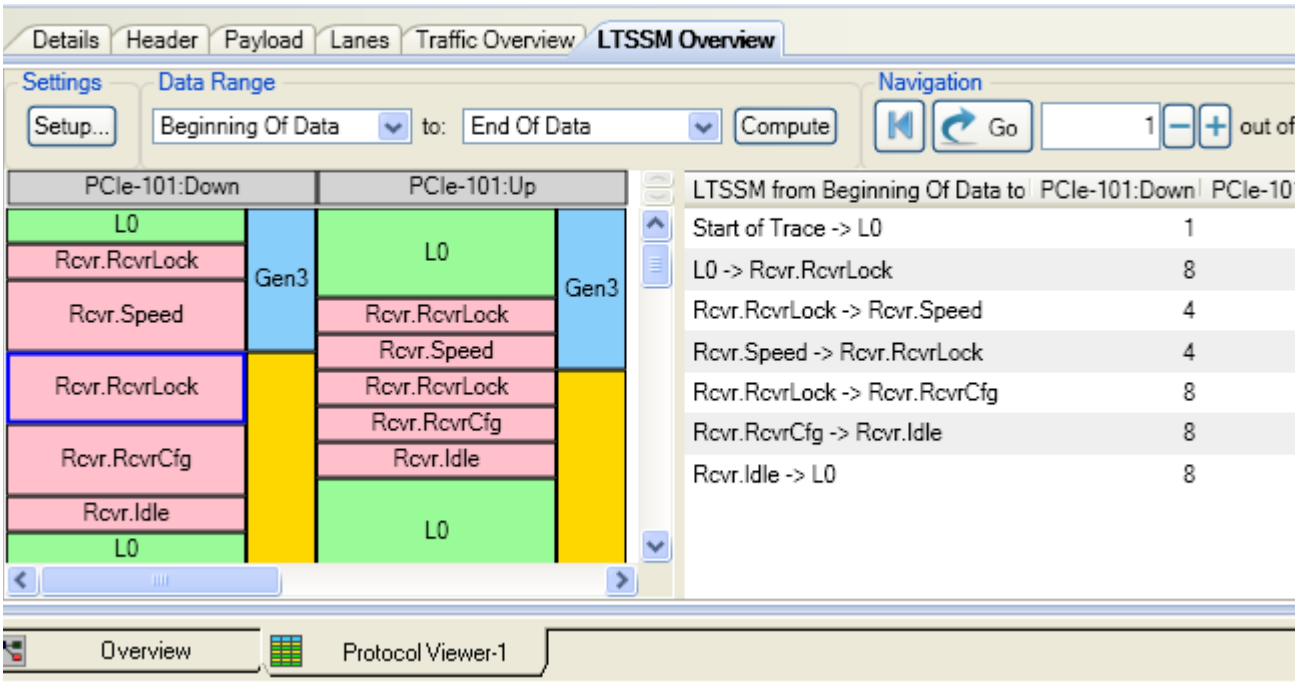
The U4301A PCIe Gen3 analyzer lets you view LTSSM states and their transitions as detected in the data captured in a trace to help you test or debug the DUT's LTSSM functions. This chapter describes how you can view these LTSSM states.

LTSSM Overview

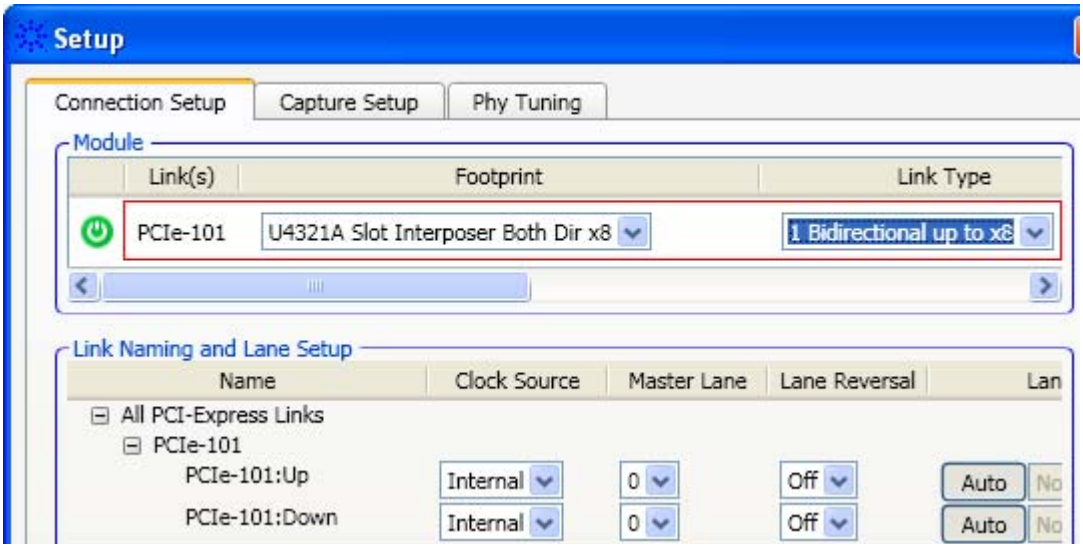
Link Training and Status State Machine (LTSSM) drives and controls the link initialization and training process for a PCIe device to enable the normal data exchange between the two PCIe devices over the link. LTSSM operates at the physical layer level and transits through various states and substates during link initialization, training, and management. During each of these states, appropriate physical layer packets (training sequences) are exchanged between the link partners to initialize, train, and manage the link.

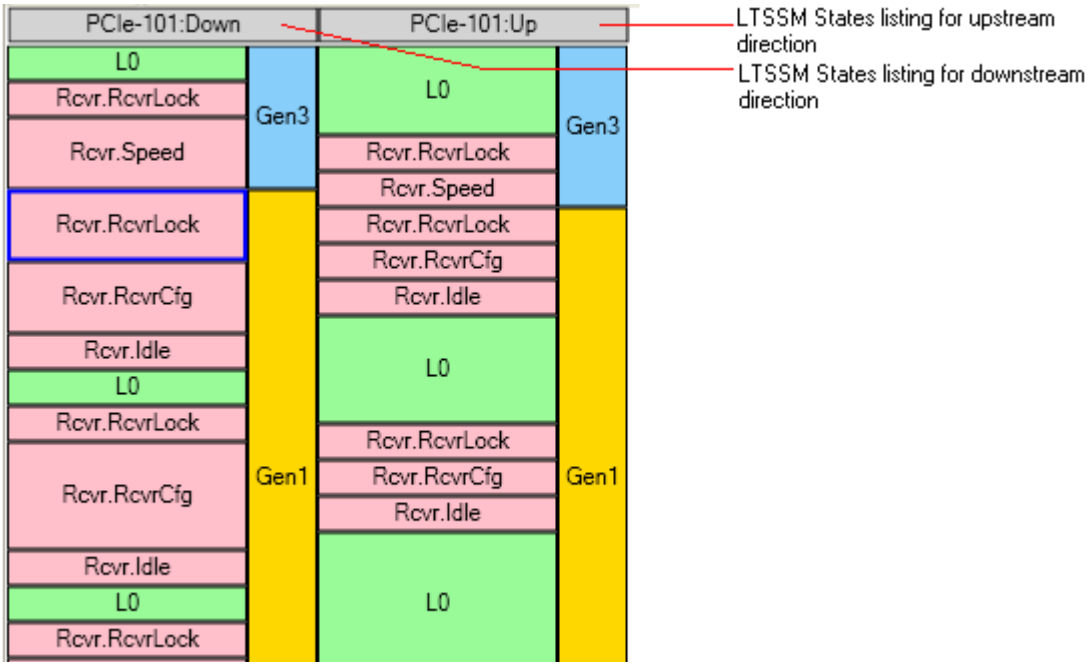
To begin communication with a PCIe device, the link training process must complete successfully. This makes link training one of the most crucial process in testing and validating a DUT. With so many states/substates and training sequences exchange involved in link training, it can be a challenging task to verify and debug this process.

The ***LTSSM Overview*** pane in the Protocol Viewer window of the Logic Analyzer GUI helps you in verifying the link training process and finding out reasons for any failure in this process. This pane provides an overview of the link training process by displaying a sequential list of the LTSSM states and their transitions and the packets exchanged during each state. To display these states and transitions, it analyzes a user-specified data range or the entire data captured in a trace and presents the list of states/transitions from that trace.



The LTSSM Overview pane can display LTSSM states and transitions for both upstream as well as downstream link directions. However, this display depends on how you configured the direction of data capture (upstream, downstream, or bidirectional) in the Connection Setup tab of the Setup dialog box of the U4301A module. For instance, if you configured a bidirectional data capture using U4301A, then LTSSM states are displayed for both directions.





Using the LTSSM Overview pane, you can view the LTSSM states and their transitions during events such as:

- Link initialization and configuration to bring the link to an operational state.
- Link recovery or retraining in situations such as speed changes, power management, or recovering from a link error.
- Downgrading or upgrading the link speed in response to a link speed change request.
- Performing the Equalization procedure before reaching the Gen3 (8.0 GT/s) speed during the link training or retraining.

Prerequisites

Before you can view LTSSM states and transitions, you need to ensure that:

- You have the appropriate node/server software license available and installed for the LTSSM Overview feature.
- You have set up the U4301A analyzer module and captured the PCIe data for the required direction(s).
- You have configured the LTSSM setup to get the data display in the LTSSM overview pane according to your requirements. (Described in the next section)

Configuring and Computing LTSSM States

To view LTSSM states in the LTSSM Overview pane, you need to configure the pane settings and initiate computation of the LTSSM states display based on these settings.

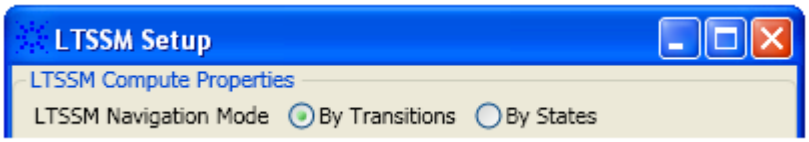
1 Access the captured data along with the U4301A setup details in the Logic Analyzer GUI.

2 Click the **Protocol Viewer** node connected to the U4301A module in the Overview window of the Logic Analyzer GUI.

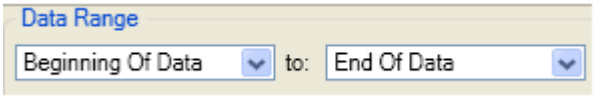
3 Click the **LTSSM Overview** tab in the lower pane of the Protocol Viewer window.

4 Configure the LTSSM setup to get a display of LTSSM states as per your requirements.

   a To configure how the states are displayed in the LTSSM Overview's navigation pane, click **Setup** and then select the appropriate LTSSM navigation mode - **By Transitions** or **By States** from the **LTSSM Setup** dialog box. '*By Transitions*' displays the LTSSM states transitions in the results for navigating through the occurrences of the state transition events in the analyzed data. 'By States' displays the LTSSM states in the results for navigating through the occurrences of the state entry events in the analyzed data.



   b In the **Data Range** groupbox, specify the start and end range for the captured data in the trace for which you want to display the LTSSM states and transitions. Only the specified range of data is analyzed to detect the LTSSM states. The default selections in the Data Range group box ensure that the LTSSM states are displayed for the entire trace. However, you can set markers in the packets listing in the upper pane and then specify the data range using these markers so that LTSSM states are displayed only for that specific range of packets.

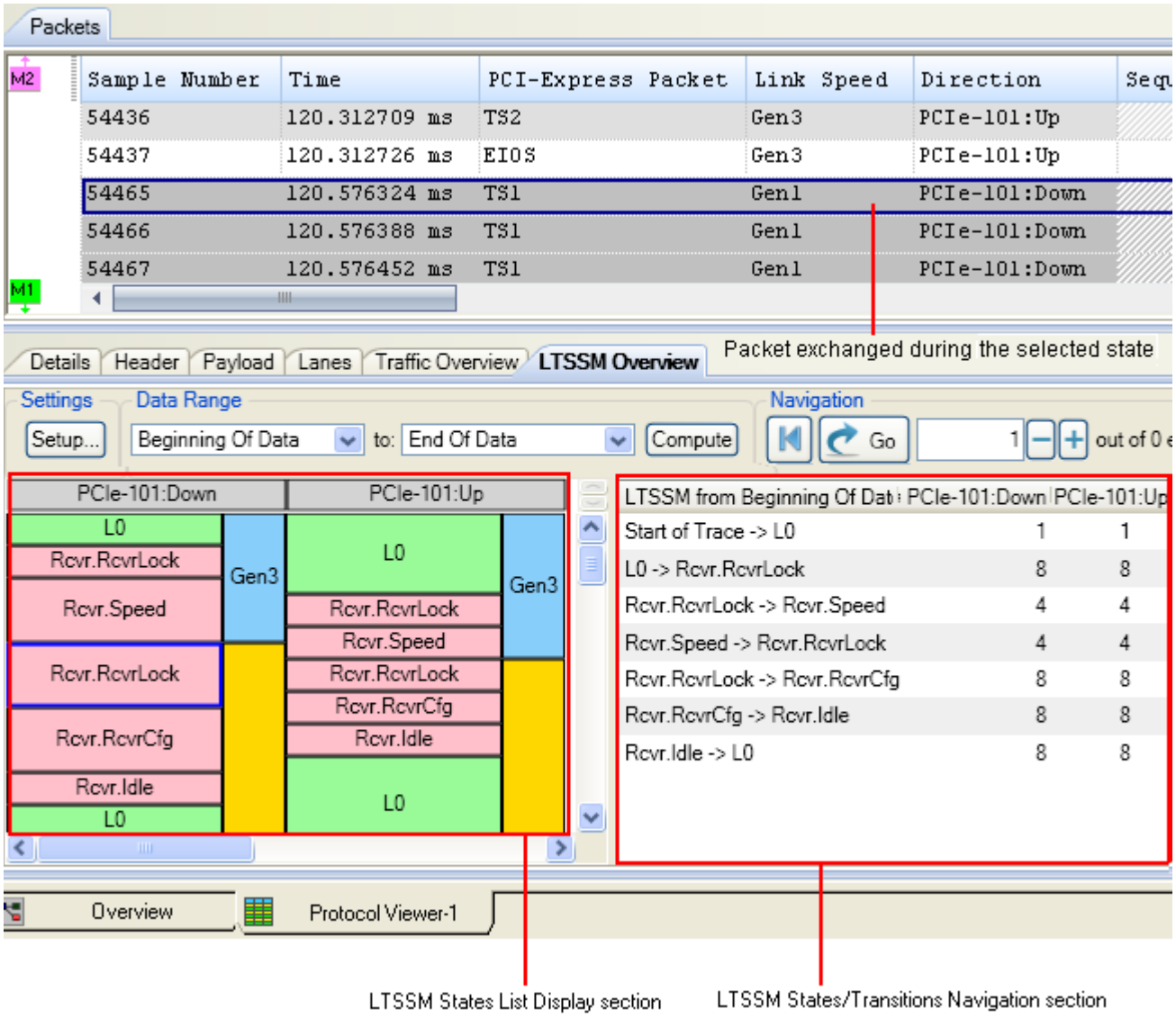


5 Click the **Compute** button displayed with the Data Range fields.

   The LTSSM states are computed and displayed for the specified data range and configured link direction.

Viewing LTSSM States/Transitions

The screen below displays the results of a compute operation for LTSSM states followed by a description of these results.



The LTSSM states results are displayed in the following two sections of the pane as highlighted in the above screen.

LTSSM States List Display section	This section displays a list of the LTSSM states in the sequence in which these occurred in the trace or the specified part of the trace. The states are grouped and listed for a link direction. In the above screen, LTSSM states are displayed for both upstream and downstream directions. For each state in this list, the applicable link speed during the state is also displayed. Clicking a speed in this list highlights the packet representing the transition to that speed in the upper pane of the Protocol Viewer. When you click a state in the list, the packet that is exchanged as the first packet for that state occurrence is highlighted in the upper pane of the Protocol Viewer. This provides you a quick start point for viewing and navigating through the packets exchanged during a particular state. Moving the mouse pointer to a state presents a tool tip with useful information about the state such as the time tag for the state and the packet exchanged at the state change.
LTSSM States/Transitions Navigation section	This section displays a list of the applicable LTSSM states or state transition names. The display of states or transitions in this section depends on whether you selected **By Transitions** or **By States** navigation mode in the LTSSM Setup dialog box. In the above screen, the display in the navigation section is as per the *By transitions* mode. For each of these states/transitions, the section displays the number of events representing the number of occurrences of these states or transitions in the analyzed data. For instance, in the above screen, the transition from Rcvr.Idle to L0 state occurred 8 times in each upstream and downstream direction making the total occurrences of this transition 16. Using this section, you can easily navigate through these occurrences of LTSSM states or transitions and the packets exchanged during these occurrences.

NOTE

You need to recompute the LTSSM states display results if you want to change:

- the data range for which results are to be displayed.
- the LTSSM navigation mode for the navigation pane.
- the link direction for which results are to be displayed.

You can hide or display the LTSSM Overview pane using the  toolbar button in the upper pane of the Protocol Viewer window.

Navigating Through the LTSSM States/Transitions Occurrences

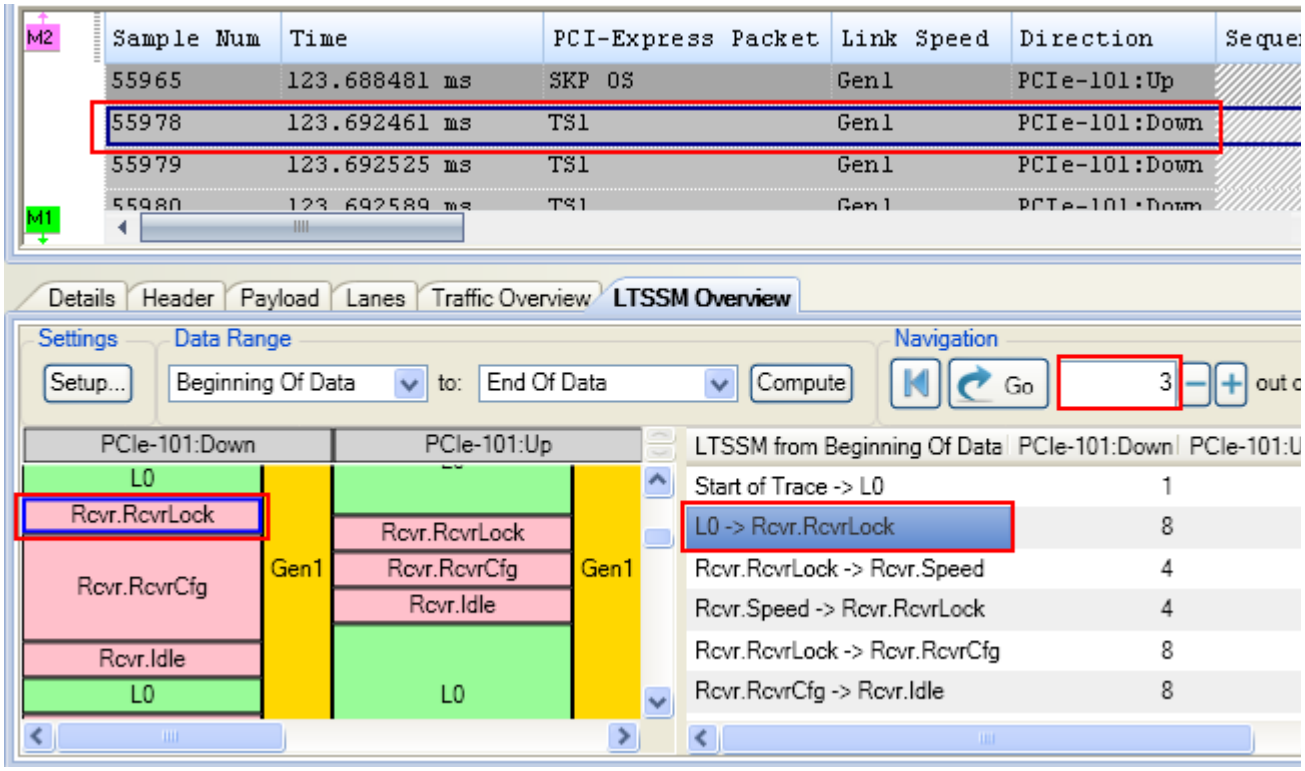
You use the Navigation groupbox in the LTSSM Overview pane to navigate through LTSSM states / transitions occurrences.

1 To navigate through the occurrences of a state for both the directions, select the particular state / transition name in the navigation section. To navigate through the occurrences of a state for a specific direction,

select the number of events displayed for that direction in front of the state / transition name in the navigation section.

2 Either type the number of occurrence to which you want to navigate in the Navigation groupbox and click **Go** or click the + or - buttons in the groupbox to sequentially move to next or previous occurrence of the state/transition.

The specified occurrence of the selected state/transition is highlighted in the state list display and the packet representing the state transition is highlighted in the upper pane of the Protocol Viewer window. For instance, in the following screen, the third occurrence of the transition from L0 to Rcvr.RcvrLock is highlighted in the states list along with the TS1 packet representing the beginning of the third occurrence of Rcvr.RcvrLock state.



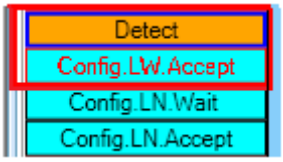
3 Click  toolbar button to navigate to the first packet of the first occurrence of the selected state/transition.

4 Click  toolbar button to navigate to the packet representing the transition to the last occurrence of the selected state/transition.

Interpreting LTSSM Overview Results

Following are some important points about interpreting the states and transitions displayed in the LTSSM Overview pane:

- **Errored LTSSM states** - If an LTSSM state is listed in red colored text, it indicates an erroneous state transition. Following is an example of an erroneous state transition from Detect to Config.LW.Accept. There should have been a transition to the Polling state after Detect.



- The following background color coding is used to represent the three speed in the speed column of the states listing.
  - Yellow - Gen1 (2.5 Gbps)
  - Green - Gen2 (5 Gbps)
  - Blue - Gen3 (8 Gbps)
- The pane displays LTSSM states as detected from the trace. If some events are not represented in the captured data in the trace, then these events will not be part of the LTSSM state transitions list in the LTSSM Overview pane.
- Except for the Configuration and Recovery states, the substates are not displayed for any other state. For instance, the substates of Polling such as Polling.Active, Polling.Compliance and Polling.Configuration are not displayed. Only the Polling state is listed in the pane.

11 Computing and Viewing Decoded Transactions

The U4301A Analyzer module can decode storage protocols over PCI Express such as NVMe and AHCI to display decoded transactions from the captured PCIe data. This chapter describes how you can compute and view these decoded transactions.

Transaction Decoding - Overview

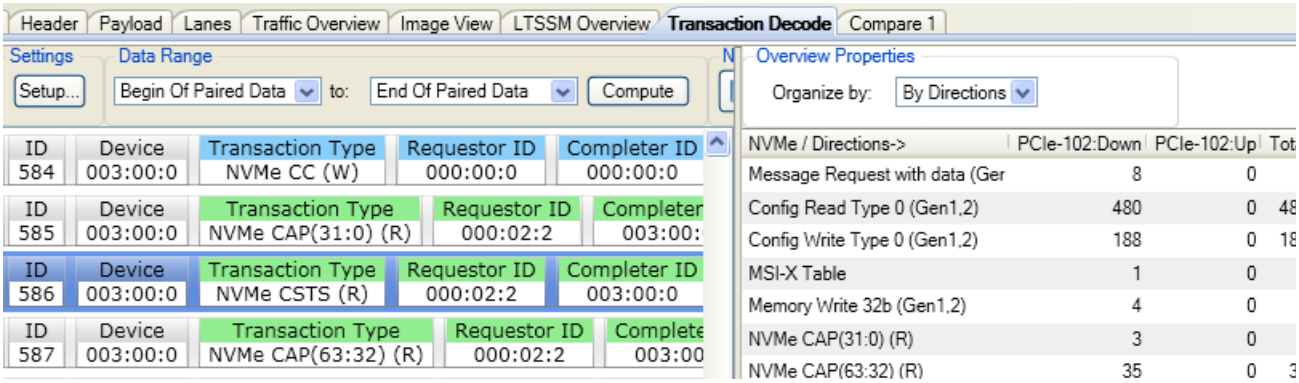
The ***Transaction Decode*** tab in the Protocol Viewer window allows you to compute and view transactions decoded from the captured PCIe traffic. The decoding and display of transactions is done as per the relevant storage protocol specifications to help you easily correlate the decoded data to the protocol specifications and evaluate DUT's compliance to these specifications.

Types of Protocols Supported

In this release, decoding of NVMe, AHCI, and PCIe transactions are supported.

Transaction Decode Tab

You use the ***Transaction Decode*** tab displayed in the lower pane of the Protocol Viewer to compute and view decoded transactions.



This tab consist of two panes. The left pane displays a list of transactions. The right pane displays the number of occurrences of these transactions.

Configuring and Computing Decoded Transactions

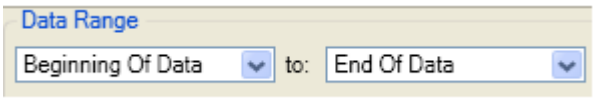
Before you Start

- You should have purchased and installed the U4301 *Transaction Decoder* license for computing decoded transactions.

  On purchasing the license, you receive an entitlement certificate. Follow the instructions in this certificate to install the license.
- Ensure that the data in the required direction(s) is already captured and available in the Logic and Protocol Analyzer GUI for transaction decoding. You may save the captured data in a Logic Analyzer configuration (.ala) file and access this data offline for transaction decoding.
- It is recommended that you capture the device's complete boot process data so that the required device setup details such as AHCI base address and port addresses in case of an AHCI device are available for decoding transactions accurately.

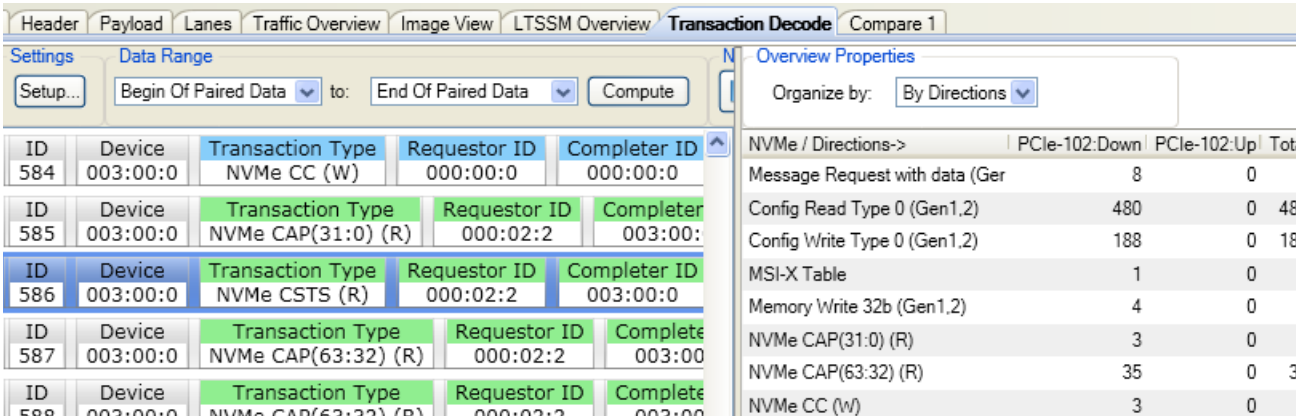
Computing Transactions from the Captured Data

1. Click the **Transaction Decode** tab in the Protocol Viewer window.
2. In the **Data Range** groupbox, specify the start and end points of the captured PCIe data for which you want to compute decoded transactions. Only the specified range of data is analyzed to compute transactions. Following options are available for setting the data range.
   - **Beginning and End of data** - This data range selection ensures that transactions are computed for the entire trace.
   - **Trigger** - Selecting Trigger in the data range ensures that transactions are computed from the point where the U4301 module's trigger condition was met.
   - **Markers** - Selecting markers in the data range ensures that transactions are computed for the specific portion of PCIe traffic defined by markers. Refer to "Defining Markers for Setting the Computation Range" on page 88 to know more.



3. Click the **Compute** button displayed with the Data Range fields.

   Transactions are computed and displayed for the specified data range.



NOTE

You need to recompute the decoded transaction results if you want to change:

- the data range for which transactions are to be displayed.
- the storage protocol for which transactions are to be displayed.
- the device setup such as base address, size, or the number of queues.

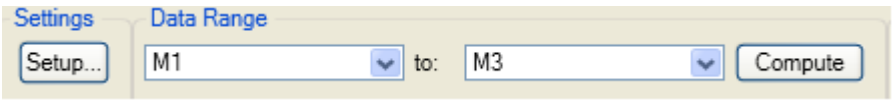
Defining Markers for Setting the Computation Range

If the captured PCIe traffic is too large and you want to view decoded transactions from a specific portion of this traffic, then you can limit the computation range by defining start and end markers in the PCIe traffic.

To define markers

1. From the upper pane of the Protocol Viewer, right-click the row in the captured PCIe traffic that should act as the starting point for transaction decode.
2. Select **Place Marker** from the displayed context menu and then select an existing marker or click **New Marker** to define a new marker at this point.

Once markers are defined, these are available for selection in the **Data Range** group box of the **Transaction Decode** tab.



Defining / Verifying the Device Setup

While computing decoded transactions, the Logic and Protocol Analyzer software automatically discovers the required device details such as device ID, type, and base address from the captured data. You can view this device related data in the ***Transaction Decode Setup*** dialog box.

NOTE

At times, the required device details are not available in the captured data and therefore cannot be autodiscovered from the captured data. In such situations, it becomes mandatory for you to specify these details. To avoid such a situation, you can ensure that device details are available by capturing the device's complete boot process.

There may also be situations when you want to rectify the autodiscovered device details or add details of multiple devices or queues (in case of NVMe).

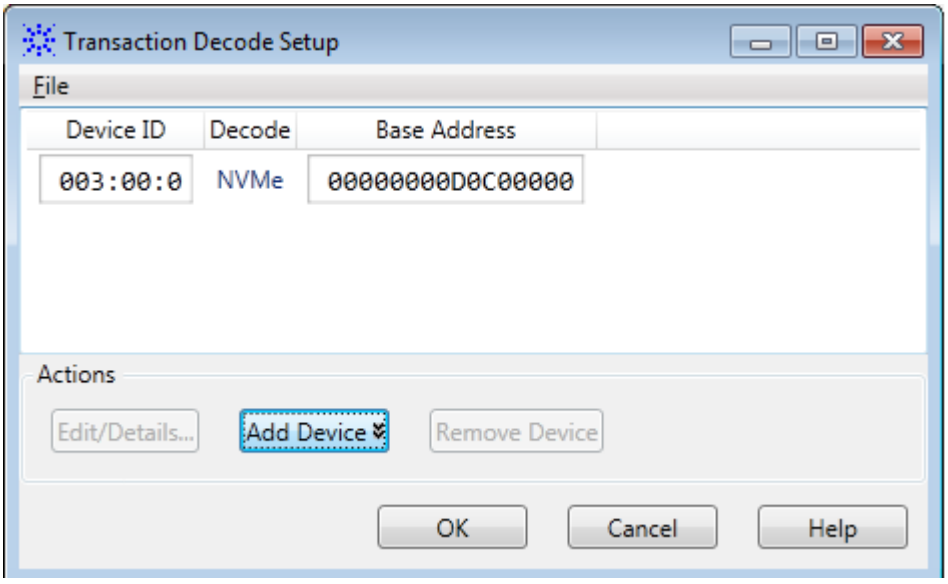
It is recommended that you verify and modify device details (if needed) for accurate transaction decode computation.

You use the ***Transaction Decode Setup*** dialog box to define/modify/verify the information about the device being tested. The types of information displayed in this dialog box differ based on the storage protocol decode applicable for the device.

To verify/modify device details

1 Click **Setup** in the **Transaction Decode** tab of the Protocol Viewer.

The **Transaction Decode Setup** dialog box is displayed with the autodiscovered device details from the captured PCIe data.



2 Modify **Device ID** and **Base Address**, if needed.

3 You can also add a new device details by clicking **Add Device** and then selecting the appropriate device type applicable for the DUT.

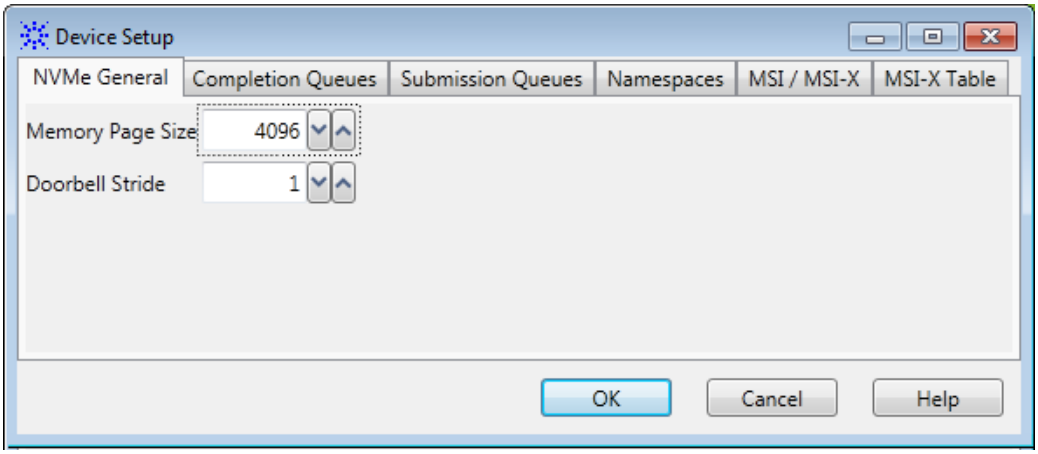
4 To delete the setup details of an existing device, click **Remove Device**.

5 Double-click the device row to view/edit its details. Alternatively, select the device row and click **Edit Details...**

The **Device Setup** dialog box is displayed. The tabs and fields in this dialog box differ based on the storage protocol decode applicable for the device. The following steps describe these device-type specific fields.

To view/edit details of an NVMe device

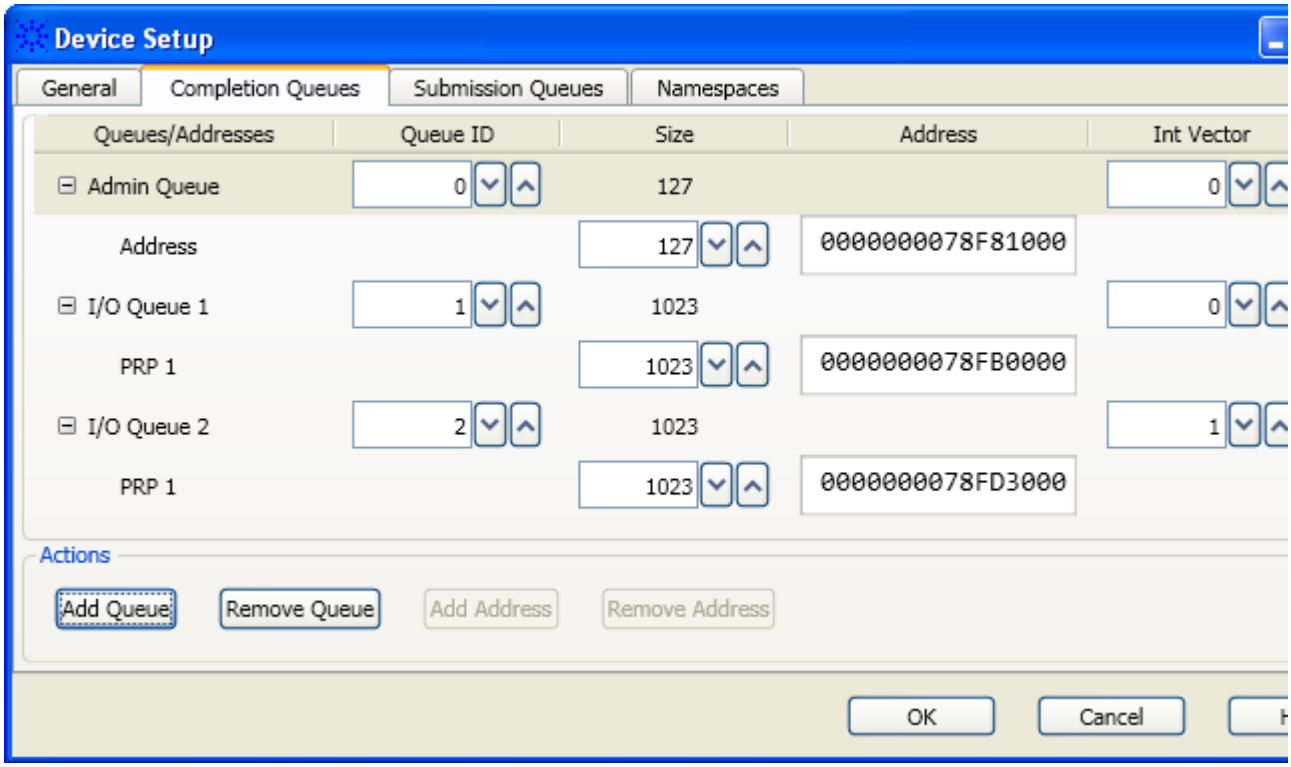
All device details such as its submission and completion queues and namespaces are autodiscovered while computing decoded transactions. If needed, you can add, remove, or edit these details of an NVMe device in the Device Setup dialog box.



1 The **Memory Page Size** field indicates the size of the physical memory page configured by the host software. The Memory Page Size value is a part of the controller configurations that the host can set and modify. This value is used to set the size of PRP entries.

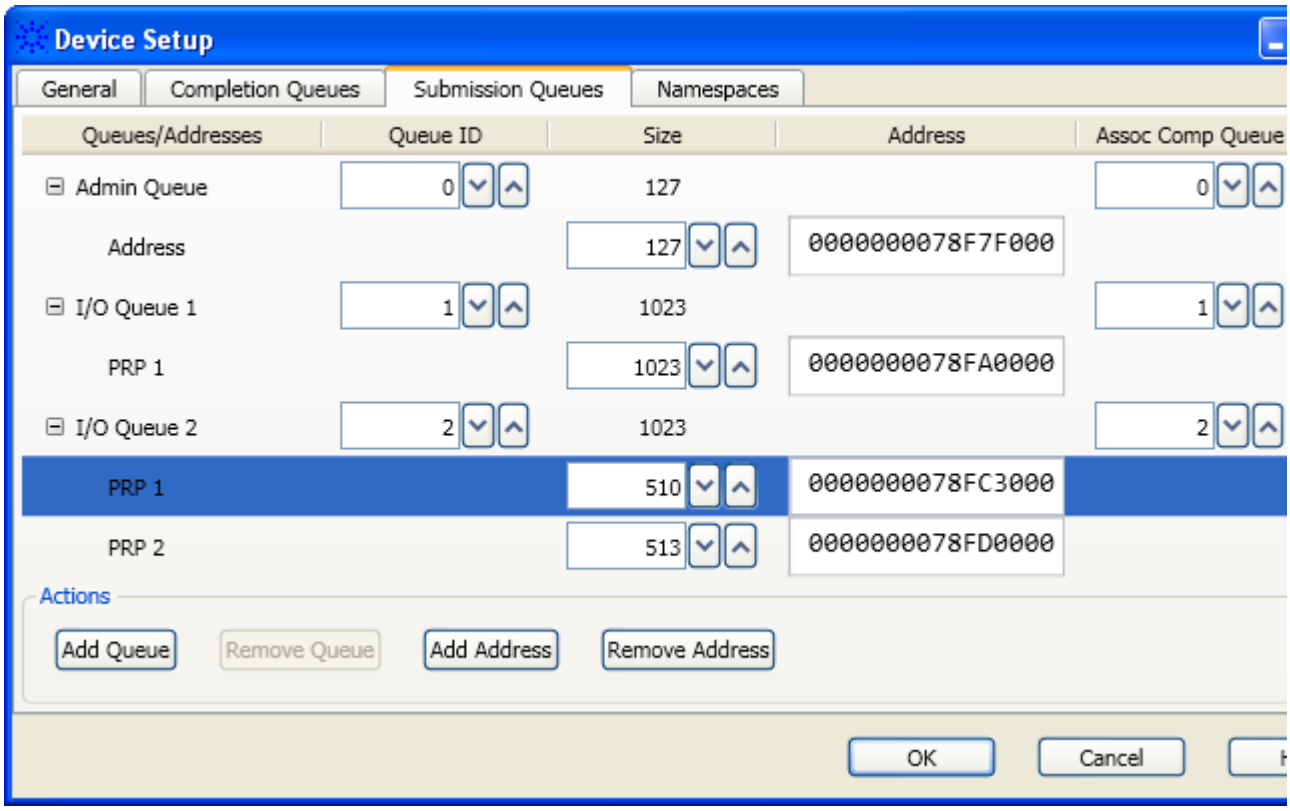
2 The **Doorbell Stride** field indicates the number of bytes to be used in memory space to separate doorbell registers. This value is a part of the controller capabilities.

3 Click the **Completion Queue** tab. The details of Admin and I/O completion queue(s) autodiscovered by the software from the captured data are displayed. If these are not autodiscovered, you can add a new queue by clicking **Add Queue** and specifying its ID, size, base address, and the unique MSI-X vector that the controller allocated to this queue to respond back.



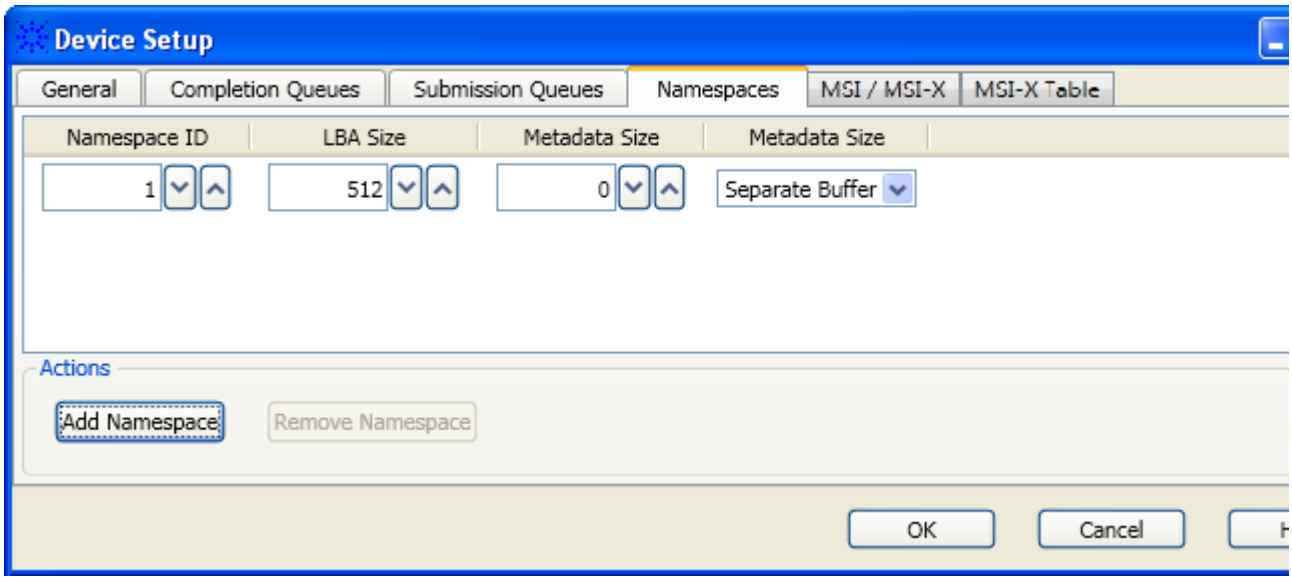
4 Click the **Submission Queue** tab. The details of Admin and I/O submission queue(s) autodiscovered by the software from the captured data are displayed. The completion queue associated with a submission queue is also displayed. A queue ID is used to display this association. If a queue's details are not autodiscovered, you can add a new queue by clicking **Add Queue** and specifying its ID, size, and base PRP address(es).

5 If a queue is physically non-contiguous, multiple PRP addresses are displayed for the queue representing multiple memory chunks. For a non-contiguous queue, you can add multiple PRP addresses by selecting a PRP address entry of the queue and clicking **Add Address**.



6 Click the **Namespaces** tab. The details of the controller's namespace(s) autodiscovered by the software from the captured data are displayed. If these are not autodiscovered, you can add a new namespace by clicking **Add Namespace** and specifying the following details.

- **LBA Size** - The Logical Block Address (LBA) data size (in bytes) that the namespace supports.
- **Metadata Size** - The number of metadata bytes provided per LBA.
- **Metadata Transfer Mode** - The metadata may be transferred either as part of the LBA by creating an extended LBA or as a separate contiguous buffer of data. When this field is set to **End of data LBA**, it indicates that the metadata is transferred at the end of the data LBA. When this field is set to **Separate Buffer**, it indicates that all the metadata for a command is transferred as a separate contiguous buffer of data.



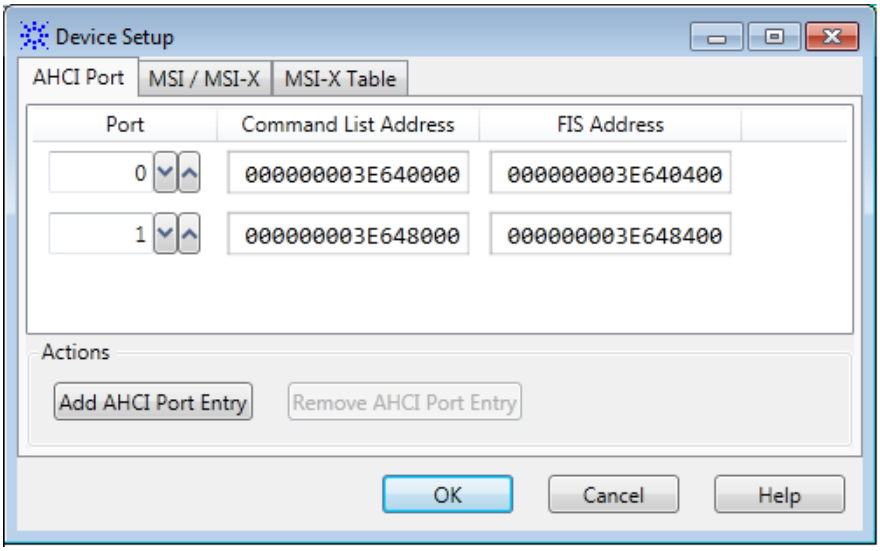
7 Click the **MSI / MSI-X** tab to view/modify the MSI / MSI-X capabilities that were discovered for the NVMe device.

8 Click the **MSI-X** tab to view/add/modify the MSI-X table entries that were discovered for the NVMe device.

9 Click **OK** to confirm and apply these settings.

To view/edit details of an AHCI device

An AHCI device's details such as the ports that it supports are autodiscovered while computing decoded transactions. If needed, you can add, remove, or edit these details of an AHCI device in the Device Setup dialog box.



1. In the **AHCI Port** tab, click the **Add AHCI Port Entry** button if you want to add an AHCI port that the device supports. This tab displays the autodiscovered ports of the AHCI device.
2. In the **Port** field, view/modify the port number.
3. In the **Command List Address** field, view/modify the base physical address of the Command List of the selected AHCI port. A command list refers to the list of commands that the HBA fetches from the command list base address to execute. The base address of the command list is as per the *PxFB* and *PxFBU* port registers.
4. In the **FIS Address** field, view/modify the base address of the FISes (Frame Information Structure) received for the selected AHCI port. An FIS refers to the frame of information exchanged between the host and device. The base address of the FIS is as per the *PxFB* and *PxFBU* port registers.
5. Click the **MSI / MSI-X** tab to view/modify the MSI / MSI-X capabilities that were discovered for the AHCI device.
6. Click the **MSI-X** tab to view/add/modify the MSI-X table entries that were discovered for the AHCI device.
7. Click **OK** to confirm and apply these settings.

Saving the Device Setup Details

You can save the device, its queues, and namespace details (specified using the Transaction Decode Setup dialog box) in a Transaction decode (.tdprop) file. Once saved, you can open this file later in the Transaction Decode Setup dialog box to quickly access and set up the device details for a transaction decode computation.

To save device details

1. Click **Setup** in the **Transaction Decode** tab of the Protocol Viewer.

   The **Transaction Decode Setup** dialog box is displayed. Modify the device details as needed.
2. Click **File** > **Save As...**
3. Specify a name for the Transaction Decode setup file and click **Save**.

To open a previously saved setup file for transaction computation

1. Click **Setup** in the **Transaction Decode** tab.

   The **Transaction Decode Setup** dialog box is displayed.
2. Click **File** > **Open**.
3. In the **Open** dialog box, select the Transaction decode (.tdprop) file that contains the device setup details.
4. Click **Open**.

You can edit a saved .tdprop file by opening it in an XML Editor or the Transaction Decode Setup dialog box.

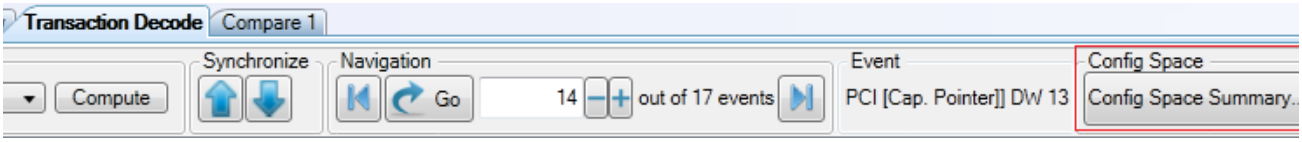
Viewing the Configuration Space of a DUT

While computing decoded transactions, the Logic and Protocol Analyzer software automatically discovers and reads details from various PCIe configuration registers in the DUT's configuration space. It displays register values for DUT's capabilities such as PCI, PCIe, Power Management, MSI, MSI-X, Advanced Error Reporting, and any Vendor-specific capabilities.

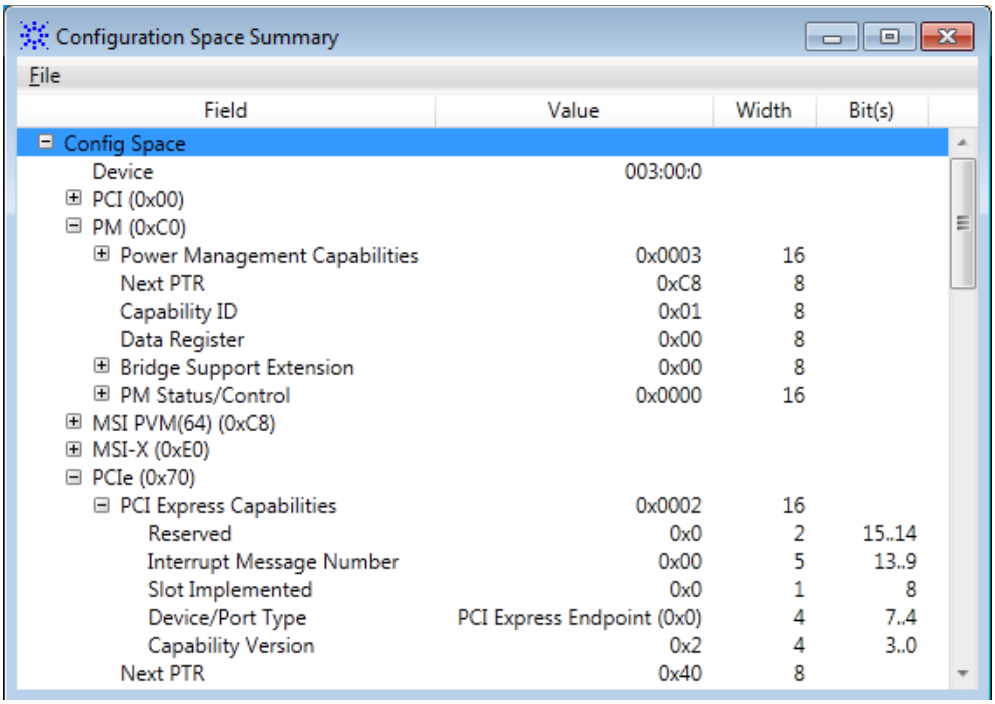
To view the configuration space of a DUT

1 Compute decoded transactions in the **Transaction Decode** tab.

2 Click the **Config Space Summary** button displayed in the top panel of the Transaction Decode tab.



The configuration space summary of the DUT is displayed.



Configuring Timestamps Displayed in the Computed Transactions

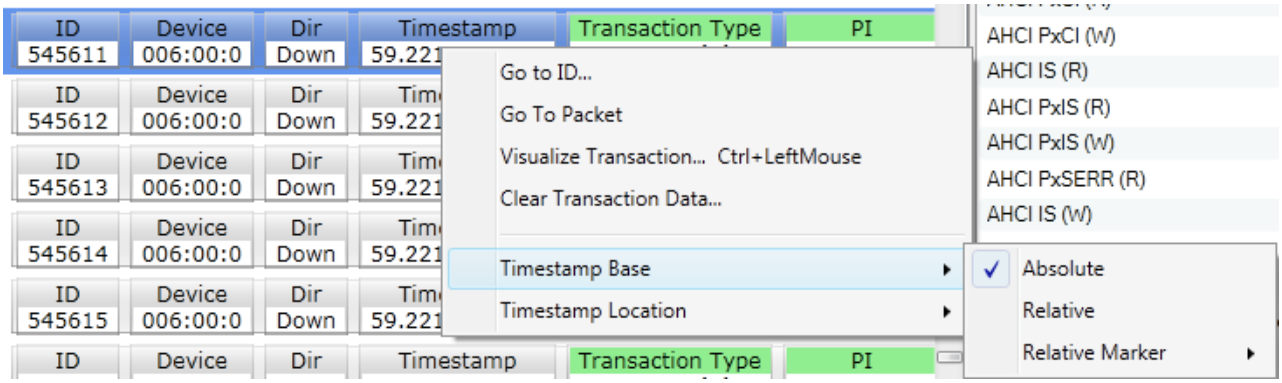
Each computed transaction has a timestamp displayed for it. You can configure:

- where you want the timestamp field to be located for the computed transactions.
- the base to be used for the calculation of timestamps of transactions.

To configure timestamp settings

1 Right-click the **Timestamp** field displayed for a computed transaction.

2 Select **Timestamp Base** from the context-menu.



3 From the displayed submenu, you can select:

- **Absolute** - Timestamp for a transaction is calculated on the basis of the absolute time of the first PCIe packet applicable for that transaction. This is the default selection.
- **Relative** - Timestamp for a transaction is calculated relative to the time of the first packet applicable for the previous transaction in the list.
- **Relative Marker** - Timestamps are calculated relative to the marker that you select from the displayed submenu.

Changing the timestamp base recalculates the displayed timestamps based on the selected base.

4 Right-click the **Timestamp** field displayed for a computed transaction and then select **Timestamp Location** from the context-menu.

5 By default, timestamps are displayed in the front of transactions data. If required, you can move the display of timestamps to the back of transactions data.

Saving the Computed Transaction Data

Once you computed the transaction data, you can save it in a logic analyzer .ala configuration file. The transaction data is saved along with the captured PCIe traffic, device setup details, and any other configurations that you made in the Protocol Viewer window.

NOTE You do not need the Transaction Decoder software license to view the saved transaction data. However, if you want to recompute transactions from the saved PCIe trace, then you need the Transaction Decoder software license.

To save the computed transaction data

1 Click **File** > **Save as**.

2 In the **Save As** dialog box, specify the name of the file.

3 Ensure that the **Standard Configuration (*.ala)** option is selected as the file type and **All Data and Setup** is selected in the **File Options** group box.

4 Click **Save**.

To access and view previously saved transaction data

1 Click **File** > **Open**.

2 In the **Open** dialog box, navigate to the **Standard Configuration (*.ala)** file in which you saved the transaction data.

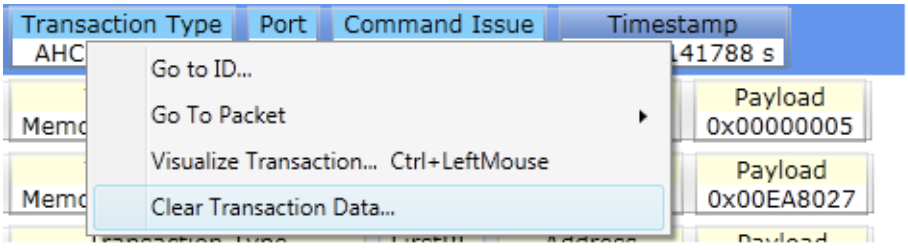
3 Click **Open**.

Clearing the Computed Transaction Data

You can clear the computed transaction data displayed in the Transaction Decode tab.

1 Right-click a transaction displayed in the Transaction Decode tab.

2 Click **Clear Transaction Data...** from the right-click context menu.



3 Click **Yes** to confirm.

The computed transactions display is cleared.

If the transactions data was previously saved in an .ala file, then reloading the .ala file redisplays the transactions data after it has been cleared. If the transactions data was not previously saved, you can specify the data range and then click **Compute** again to redisplay the transactions data.

Interpreting and Navigating Through the Transaction Decode Results

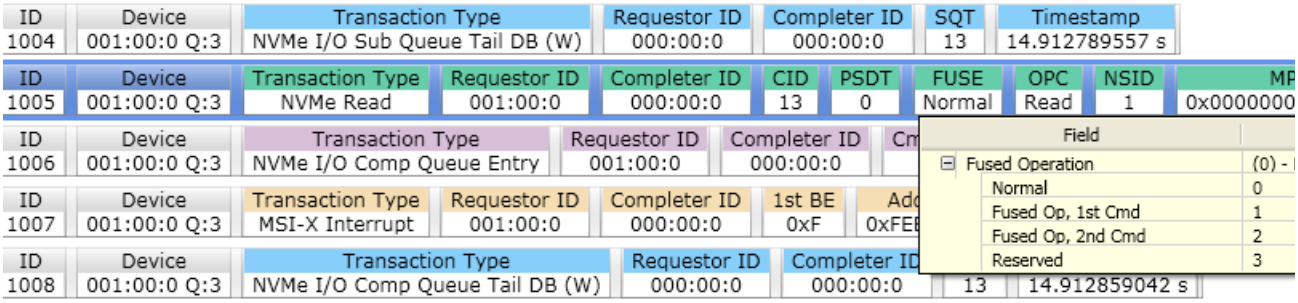
Transactions are decoded and computed from a set of captured PCIe packets that contain the storage protocol information associated with that transaction.

Decoded transactions are displayed in the *Transaction Decode* tab in an order based on the timestamp of the first packet associated with a transaction. One or many PCIe packets may be associated with a transaction.

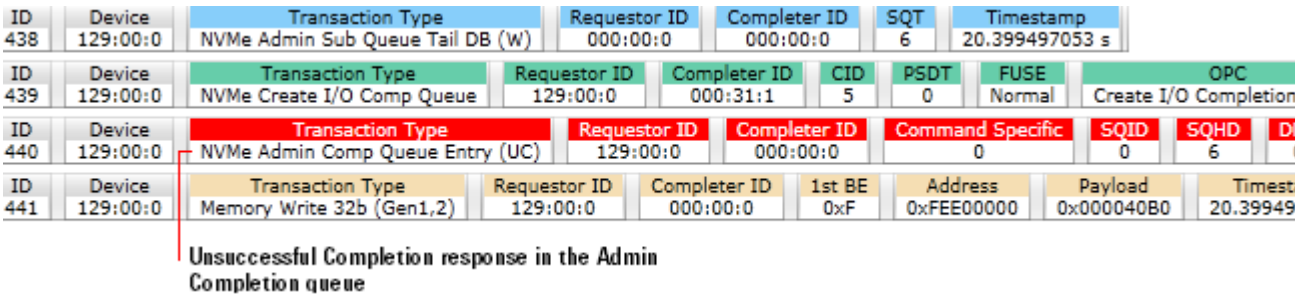
Transaction Details Pane

In the left pane of the Transaction Decode tab, transactions with their details are displayed. In this pane, a transaction is uniquely identified by a Transaction ID.

The details displayed for transactions vary based on their type and the applicable storage protocol. Moving the mouse pointer to a field of a transaction presents a tool tip with information about that field.



A color coding scheme is used to clearly indicate transactions of different types. Errored transactions are displayed in red.



NOTE

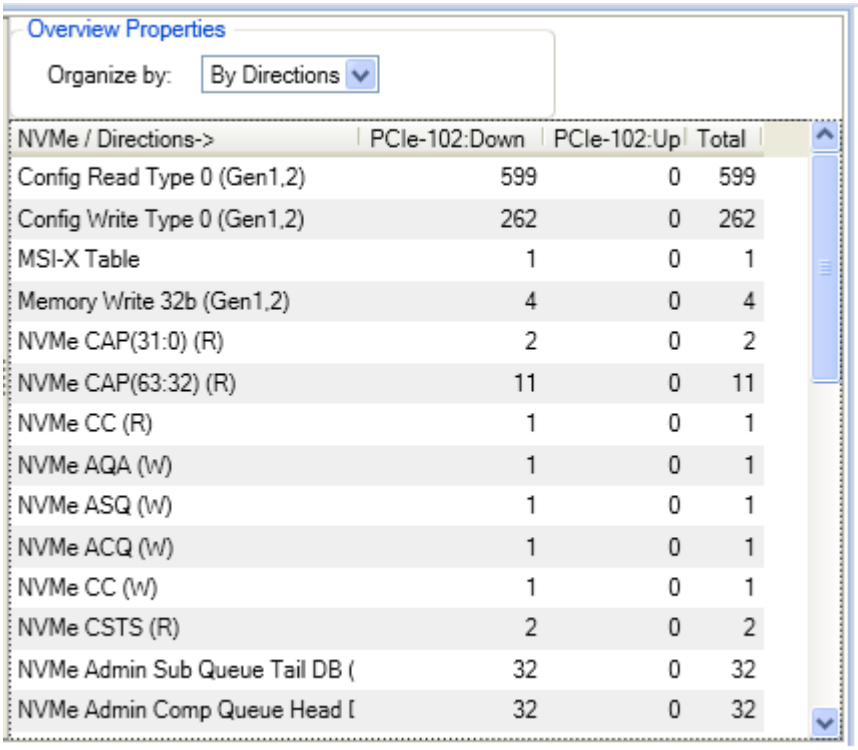
If you are displaying data captured from multiple U4301A modules in a single Protocol Viewer instance, then transactions from these multiple modules will be interleaved based on the timestamp of the first packet in the transaction.

To display transactions for each module separately, you can add a Protocol Viewer instance to each module in the Overview pane of the Logic and Protocol Analyzer GUI.

Refer to the topic "Viewing NVMe Transactions" on page 109 and "Viewing AHCI Transactions" on page 119 to get an understanding of how NVMe and AHCI transactions are decoded and displayed.

Transaction Overview Pane

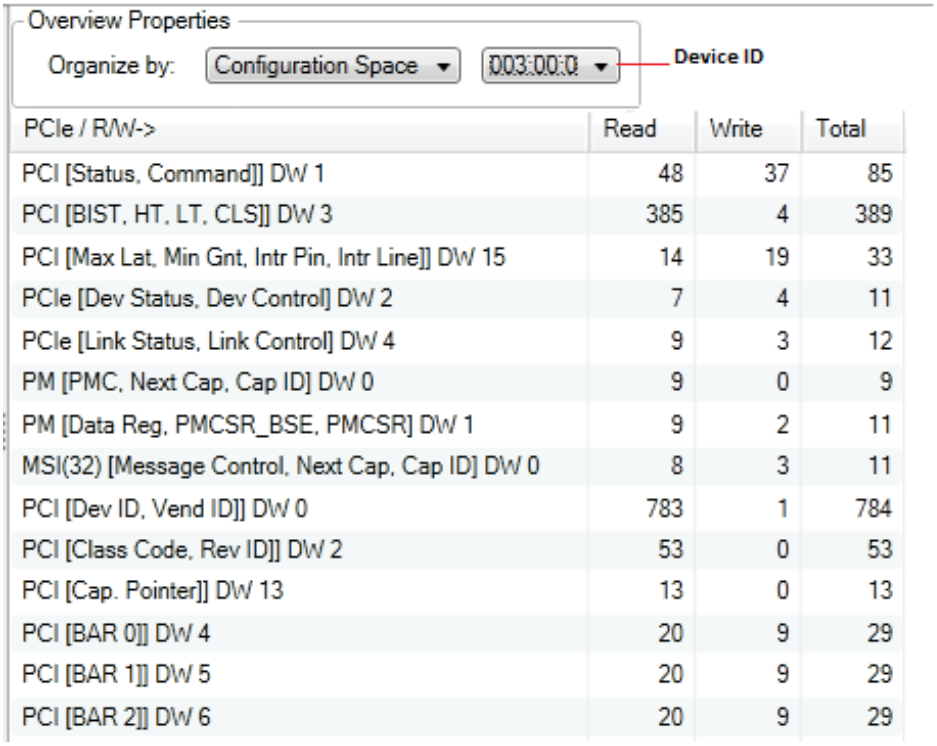
The right pane of the Transaction Decode tab displays statistics for the computed transactions. This pane lists the transaction types applicable for the computed transaction data and the number of events/occurrences for each transaction type in the computed data.



NVMe / Directions->	PCIe-102:Down	PCIe-102:Up	Total
Config Read Type 0 (Gen1,2)	599	0	599
Config Write Type 0 (Gen1,2)	262	0	262
MSI-X Table	1	0	1
Memory Write 32b (Gen1,2)	4	0	4
NVMe CAP(31:0) (R)	2	0	2
NVMe CAP(63:32) (R)	11	0	11
NVMe CC (R)	1	0	1
NVMe AQA (W)	1	0	1
NVMe ASQ (W)	1	0	1
NVMe ACQ (W)	1	0	1
NVMe CC (W)	1	0	1
NVMe CSTS (R)	2	0	2
NVMe Admin Sub Queue Tail DB (	32	0	32
NVMe Admin Comp Queue Head [	32	0	32

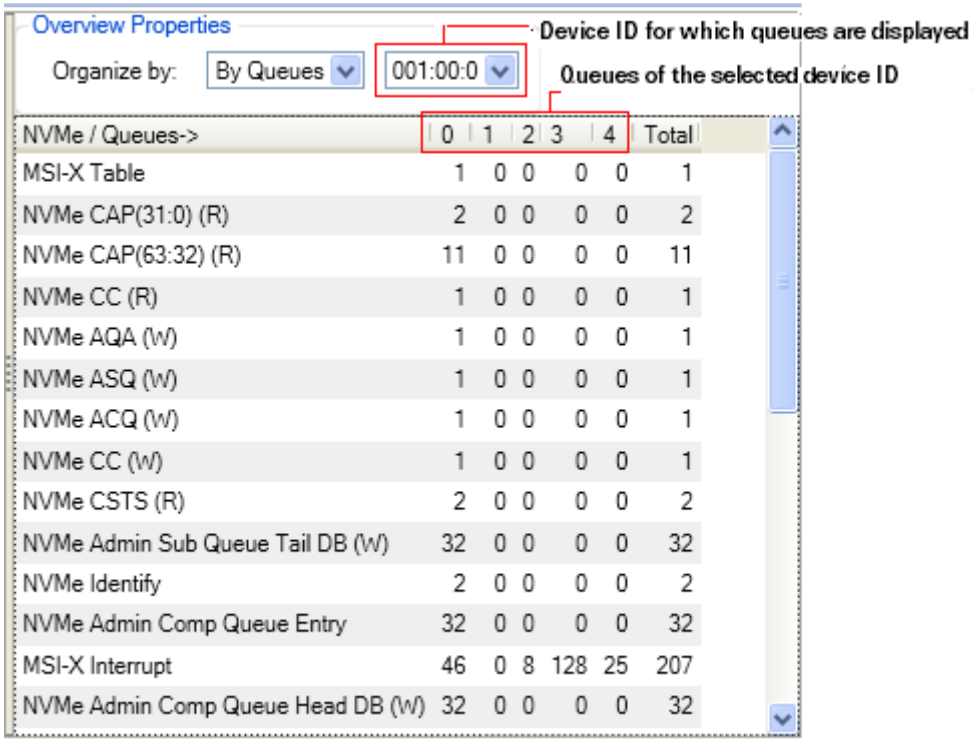
In this pane, you can organize the number of transaction occurrences/events on the basis of the organization types described in the following table.

Organized by	Description
Directions	Transaction occurrences are organized on the basis of the Uplink and Downlink directions in the captured data. If the captured data is unidirectional, then this view displays occurrences for one direction only.
Configuration Space	Selecting this option displays the number of occurrences of only PCIe config space transactions organized on the basis of reads and writes to PCIe configuration registers in the DUT's configuration space.



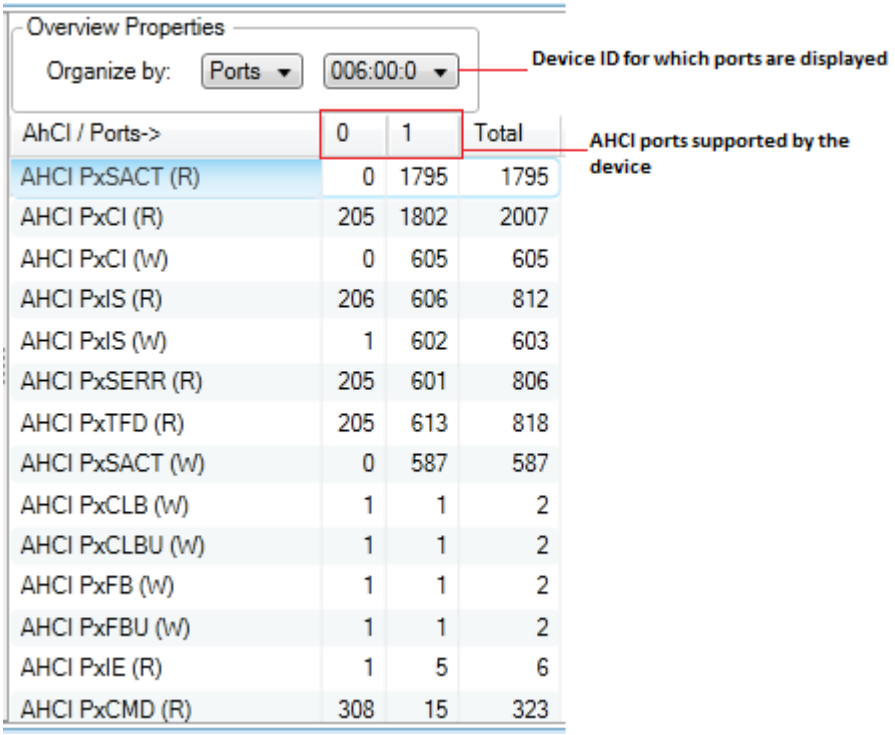
PCIe / R/W->	Read	Write	Total
PCI [Status, Command]] DW 1	48	37	85
PCI [BIST, HT, LT, CLS]] DW 3	385	4	389
PCI [Max Lat, Min Gnt, Intr Pin, Intr Line]] DW 15	14	19	33
PCIe [Dev Status, Dev Control] DW 2	7	4	11
PCIe [Link Status, Link Control] DW 4	9	3	12
PM [PMC, Next Cap, Cap ID] DW 0	9	0	9
PM [Data Reg, PMCSR_BSE, PMCSR] DW 1	9	2	11
MSI(32) [Message Control, Next Cap, Cap ID] DW 0	8	3	11
PCI [Dev ID, Vend ID]] DW 0	783	1	784
PCI [Class Code, Rev ID]] DW 2	53	0	53
PCI [Cap. Pointer]] DW 13	13	0	13
PCI [BAR 0]] DW 4	20	9	29
PCI [BAR 1]] DW 5	20	9	29
PCI [BAR 2]] DW 6	20	9	29

Organized by	Description
Queues *(Applicable only for NVMe decoded transactions)*	Transaction occurrences are organized on the basis of the NVMe submission/completion queues applicable for transactions. Ensure that you select **By Queues** in the **Organize by** field to organize occurrences by queues. The field next to Organize by listbox displays the device ID for which the displayed queues are applicable. If multiple devices are involved, then this field provides you multiple options representing device IDs of multiple devices. The following screen displays organization by five queues (0 to 4) of the device with device ID (001:00:0).



NVMe / Queues->	0	1	2	3	4	Total
MSI-X Table	1	0	0	0	0	1
NVMe CAP(31:0) (R)	2	0	0	0	0	2
NVMe CAP(63:32) (R)	11	0	0	0	0	11
NVMe CC (R)	1	0	0	0	0	1
NVMe AQA (W)	1	0	0	0	0	1
NVMe ASQ (W)	1	0	0	0	0	1
NVMe ACQ (W)	1	0	0	0	0	1
NVMe CC (W)	1	0	0	0	0	1
NVMe CSTS (R)	2	0	0	0	0	2
NVMe Admin Sub Queue Tail DB (W)	32	0	0	0	0	32
NVMe Identify	2	0	0	0	0	2
NVMe Admin Comp Queue Entry	32	0	0	0	0	32
MSI-X Interrupt	46	0	8	128	25	207
NVMe Admin Comp Queue Head DB (W)	32	0	0	0	0	32

Organized by	Description
Ports *(Applicable only for AHCI decoded transactions)*	Selecting this option displays the number of occurrences of only AHCI port-specific register transactions organized on the basis of reads and writes to AHCI port registers of the DUT. The field next to Organize by listbox displays the AHCI device ID for which the displayed ports are applicable. If multiple devices are involved, then this field provides you multiple options representing device IDs of multiple devices. The following screen displays organization by two ports (0 and 1) of the device with device ID (006:00:0).



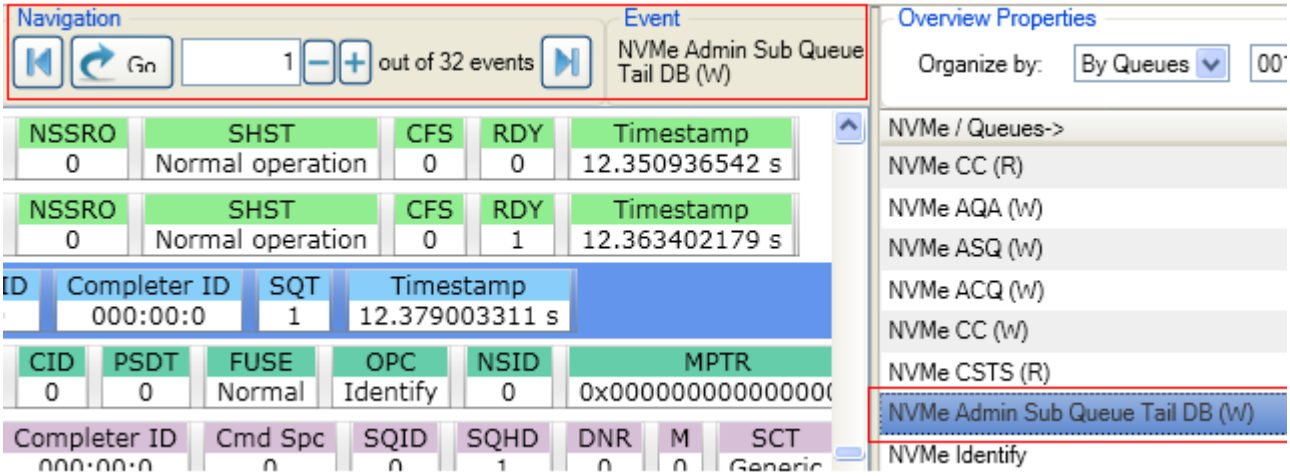
AhCI / Ports->	0	1	Total
AHCI PxSACT (R)	0	1795	1795
AHCI PxCI (R)	205	1802	2007
AHCI PxCI (W)	0	605	605
AHCI PxIS (R)	206	606	812
AHCI PxIS (W)	1	602	603
AHCI PxSERR (R)	205	601	806
AHCI PxTFD (R)	205	613	818
AHCI PxSACT (W)	0	587	587
AHCI PxCLB (W)	1	1	2
AHCI PxCLBU (W)	1	1	2
AHCI PxFB (W)	1	1	2
AHCI PxFBU (W)	1	1	2
AHCI PxIE (R)	1	5	6
AHCI PxCMD (R)	308	15	323

Navigating Through Transactions

You can easily navigate through the occurrences of a particular type of transaction in the computed transaction data.

1 From the Transaction Overview pane on the lower-right, select a transaction type whose occurrences you want to navigate and view.

The navigation bar in the Transaction Decode tab now displays the total number of occurrences found for the selected transaction type.

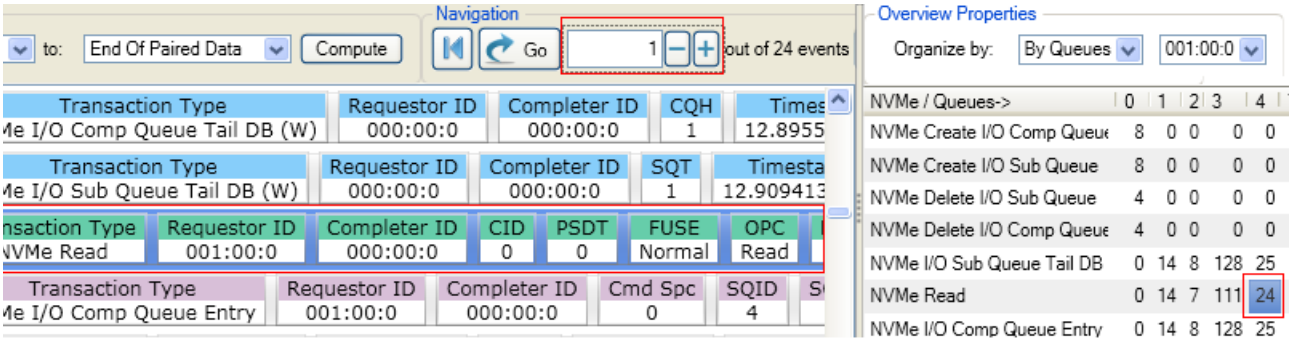


2 To view the first occurrence of that transaction type in the computed data, click button in the navigation bar. Click to go to the last occurrence of the selected transaction type.

3 To sequentially move through the occurrences of a transaction type, use the buttons in the navigation bar.

4 To go to a specific occurrence of a transaction type, specify the event/occurrence number in the text box displayed in the navigation bar and click **Go**.

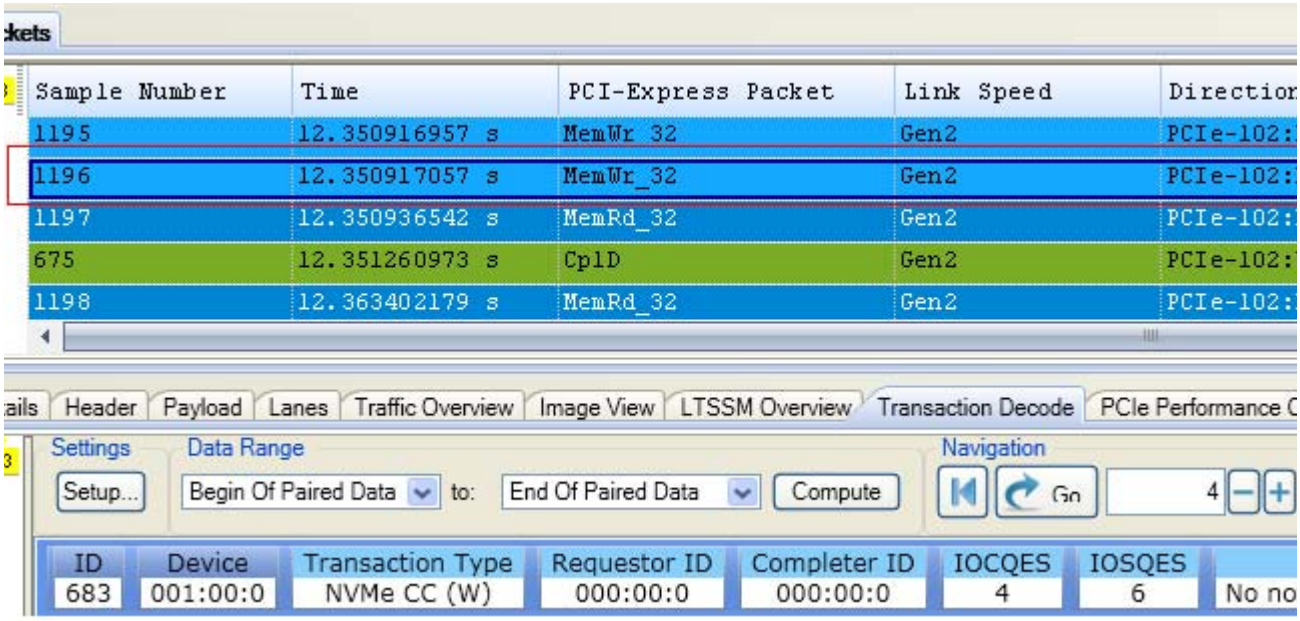
You can also double-click a particular occurrence number in the right pane to navigate to the first transaction mapped to that occurrence number. For instance, in the following screen, the first occurrence of an *NVMe Read* transaction for Queue 4 is highlighted on double-clicking its occurrence number in the right pane.



Navigating Between Transactions and their Associated Packets

From a transaction listed in the Transaction Decode tab, you can quickly navigate to the PCIe packet(s) exchanged for that particular transaction. To accomplish this, you need to double-click a transaction in the Transaction Decode tab. Doing so, highlights the packet exchanged as the first packet for that transaction in the upper pane of the Protocol Viewer. You can also use the **Synchronize** button in the Transaction Decode tab to synchronize the display of packets data with the selected transaction.

In the following screen, double-clicking the transaction for modifying controller settings highlights the memory write packet for this modification.



NOTE

You can also quickly navigate from a PCIe packet displayed in the upper pane to its applicable transaction in the Transaction Decode tab. To accomplish this, you select the packet and then click the **Synchronize** button displayed in the Transaction Decode tab. This synchronizes the display of transactions with the selected packet.

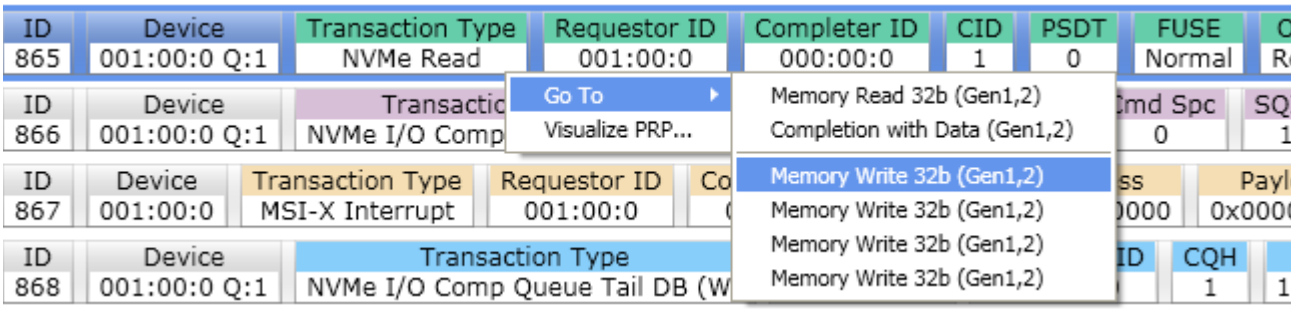
Navigating to a specific packet of a transaction

A transaction may have multiple packets associated with it. For such transactions, you can directly navigate to any packet of the transaction. To do this,

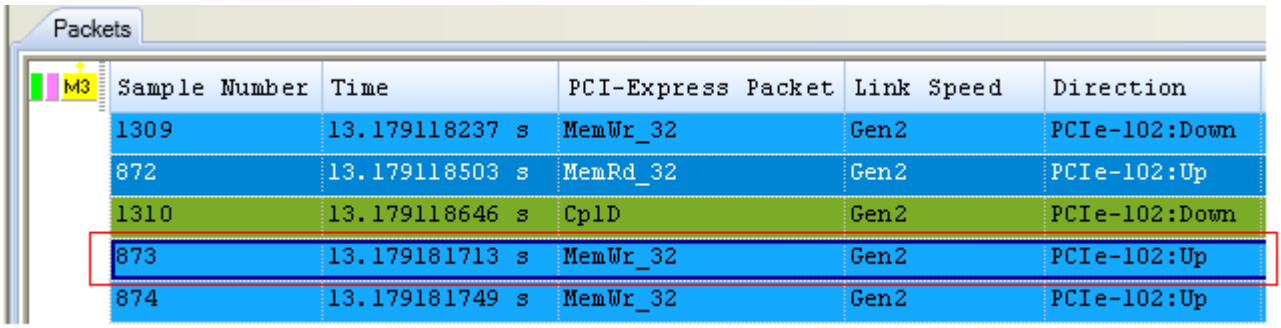
1 Right-click a transaction.

2 Select **Go To**.

A list of packets applicable for that transaction are displayed in a sequential order.



3 Select a packet from this list. The packet that you selected gets highlighted in the upper pane of the Protocol Viewer.



Visualizing a Transaction Set (Super Transaction)

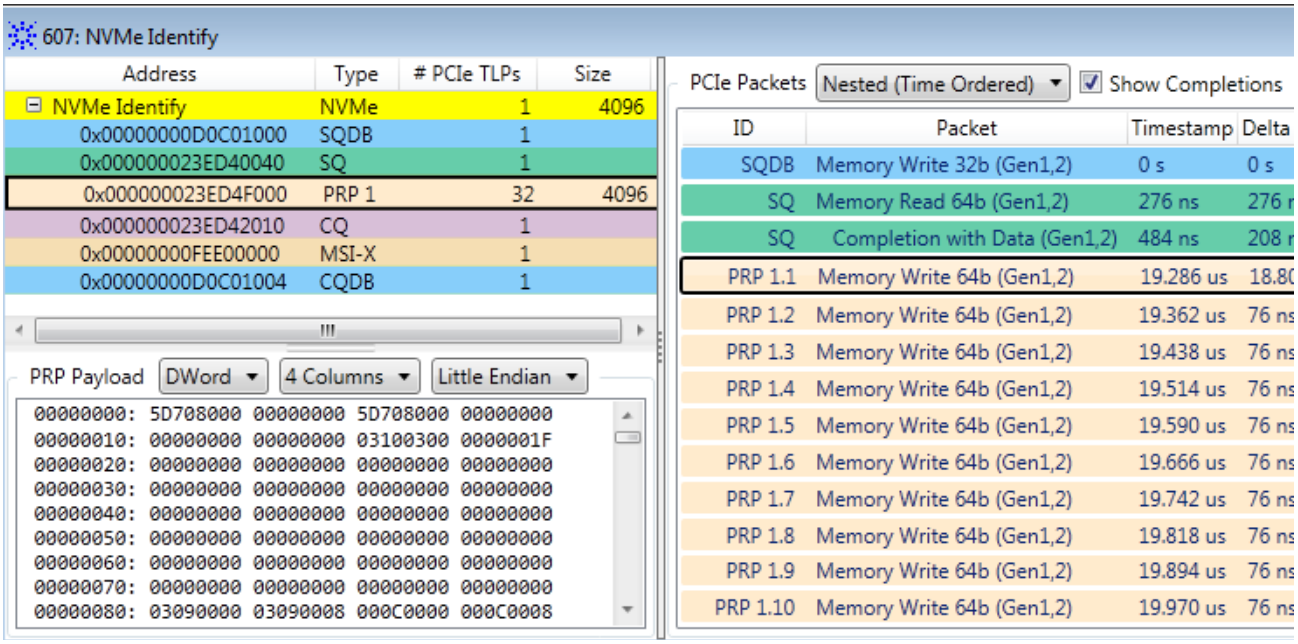
At times, you may want to visualize a decoded transaction as a super transaction with all its related transactions forming a complete set. This provides a visual sequential flow of transactions that were related to a particular transaction.

To visualize a transaction set

1 Right-click a decoded transaction.

2 Select **Visualize Transaction...** from the context menu.

For instance, in the following screen, the *NVMe Identify* transaction has been visualized as a complete set of transactions.



In the above screen, the transaction set for the NVMe Identify transaction:

- begins with the SQDB (Submission Queue Doorbell) transaction.
- followed by the SQ (memory read and completion with data) transaction and then the PRP entries used for the Identify command.
- then the Command Completion entry to the Completion Queue (CQ) transaction.
- then the MSI-X interrupt generation transaction.
- finally the CQDB (Completion Queue Doorbell) transaction.

For each of these related transactions in a set, you can view:

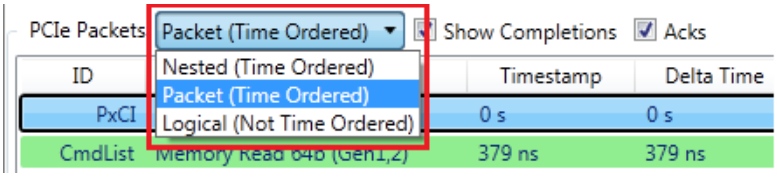
- the associated raw payload in the lower pane.
- the applicable PCIe packet(s) in the right pane.

NOTE Clicking a super transaction displays the combined payload for the complete set of transactions.

PCIe Packets applicable for a Transaction Set

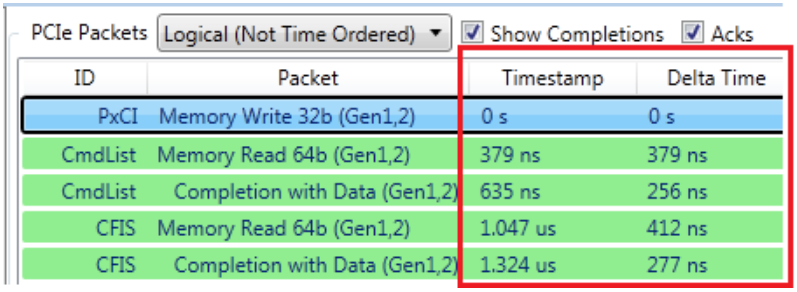
In the right pane of the Visualize Transaction dialog box, by default, PCIe packets are listed as per the *Nested (Time Ordered)* option. This means packets are listed in a time based sequence with the completion packets nested within the applicable Read packets. If required, you can change this display to:

- list the packets in a logical sequence instead of time based sequence - *Logical (Not Time Ordered)* option.
- list the packets without nesting the completions within the read packets - *Packets (Time Ordered)* option.



For each of the listed packets, the following time related fields are displayed:

- **Timestamp** - This field is relative to the timestamp of the first packet displayed for the transaction set. (The first packet timestamp is taken as 0s.).
- **Delta Time** - This field displays the difference between the timestamp of the currently selected packet and the previous packet in the list of packets for the transaction set.



You can enable or disable the display of Completions and Acks packets from the packets list in the right pane using the **Show Completions** and **Acks** checkboxes respectively.

To get visualize transaction information specific to storage protocols, refer to "Viewing a Complete Set of Transactions for a Command Submission and Completion" on page 113 and "Visualizing a Complete Set of AHCI Transactions" on page 123.

Viewing NVMe Transactions

Previous help topics described how you can configure and compute transactions in the Transaction Decode tab. This topic is specific to NVMe transactions and provides examples of how you can interpret NVMe transactions that are computed and displayed in the Transaction Decode tab.

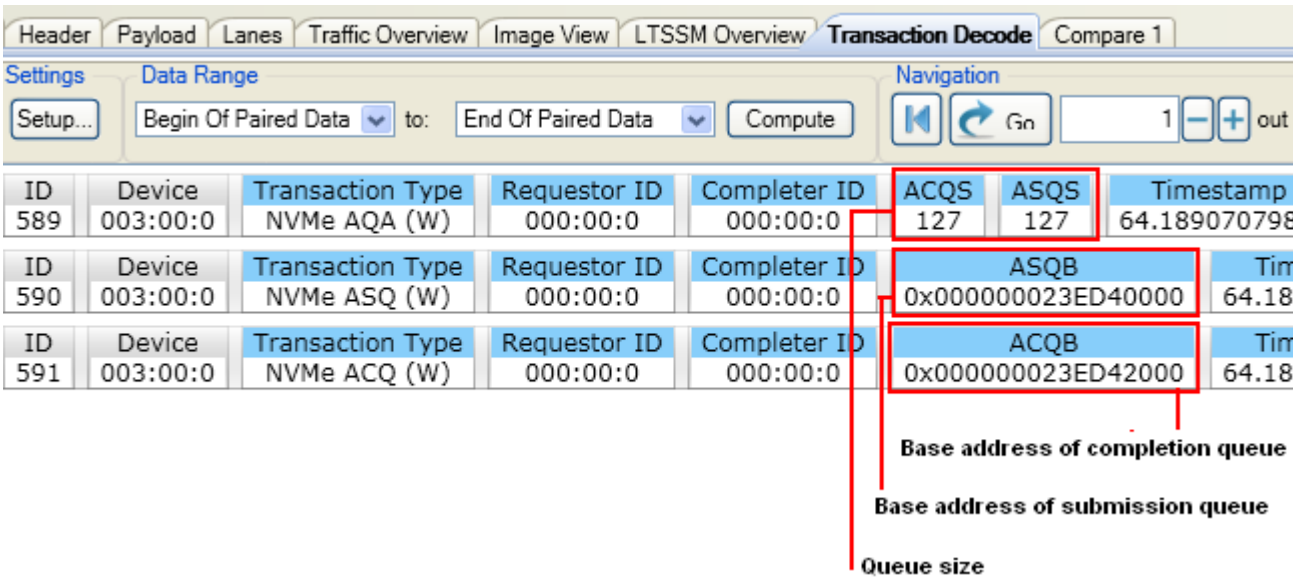
The decoded NVMe transactions provide you a sequential view of the communication cycle between the host software and NVMe controller for various requests placed by the host software in queues. You can check how the NVMe controller responds to and completes these requests. At the administrative management level, you can verify how the NVMe controller handles admin requests such as queue management requests.

For NVMe, the Transaction Decode tab displays transactions for:

- NVMe controller initialization such as Admin queue configuration
- NVMe Admin and I/O commands submission and their responses (completions).
- MSI-X interrupts initiations by controller
- NVMe I/O submission and completion queues management

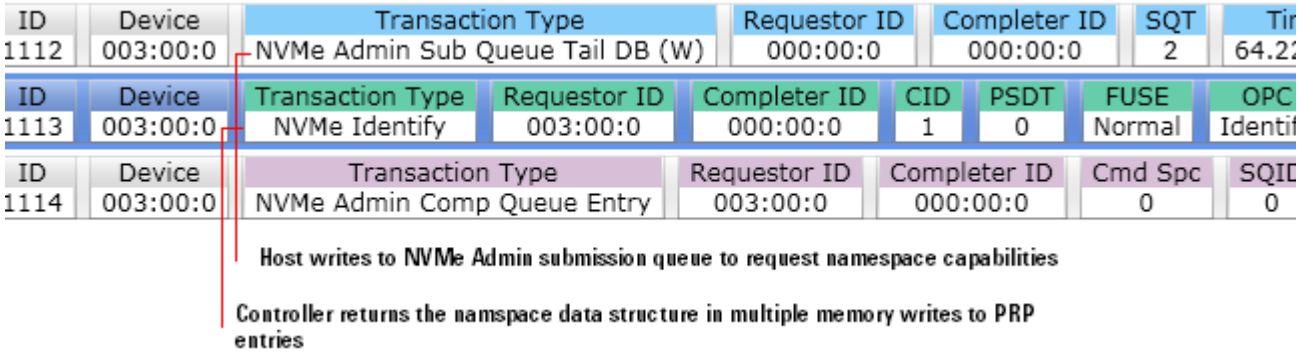
Viewing Transactions for NVMe Controller Initialization

The following screen displays a set of transactions for NVMe controller initialization. The *AQA*, *ASQ*, and *ACQ* registers are modified to define the Admin Submission Queue and its corresponding Admin Completion Queue. The transactions display the Admin queue attributes in terms of size (128 entries) and the base address (64-bit physical address) to be used for Admin submission queue and completion queue.

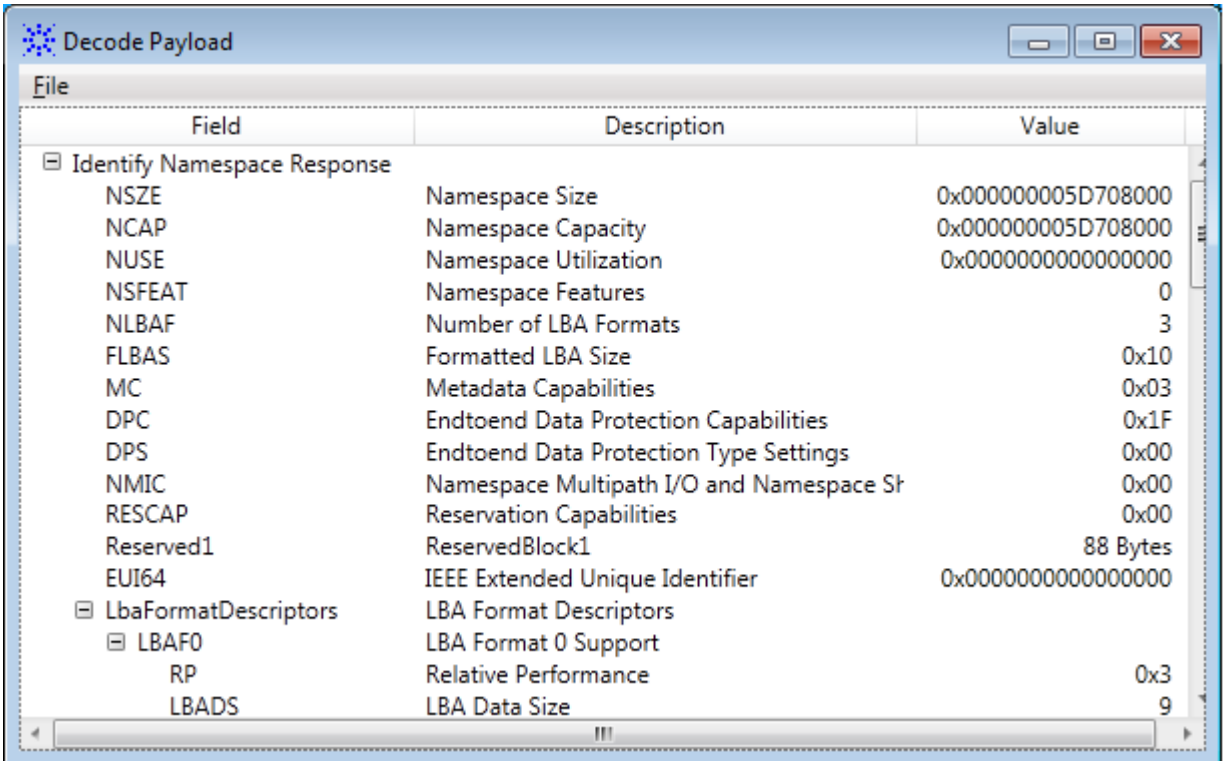


Viewing Admin Command Transactions

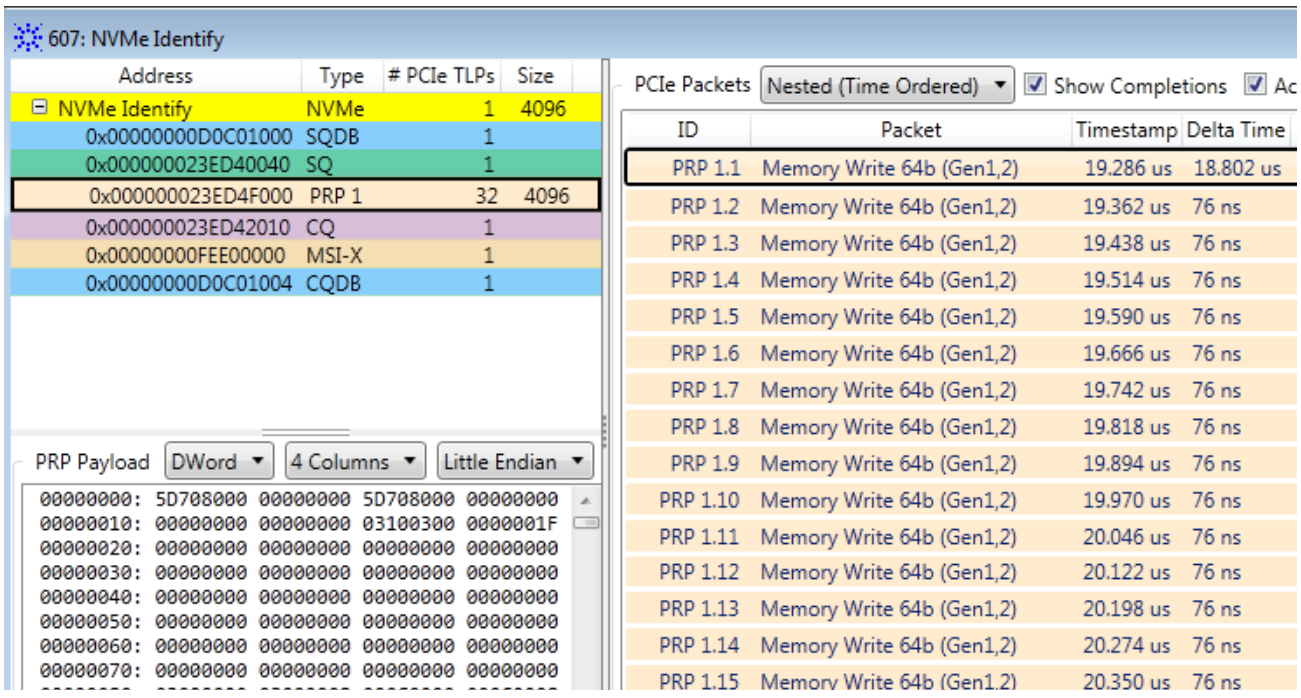
The following screen displays transactions related to the ***Identify*** command submission and completion to return capabilities and status of a specific namespace.



You can further view the namespace capabilities returned by the Identify command by right-clicking the NVMe Identify transaction and selecting **Decode Payload**.

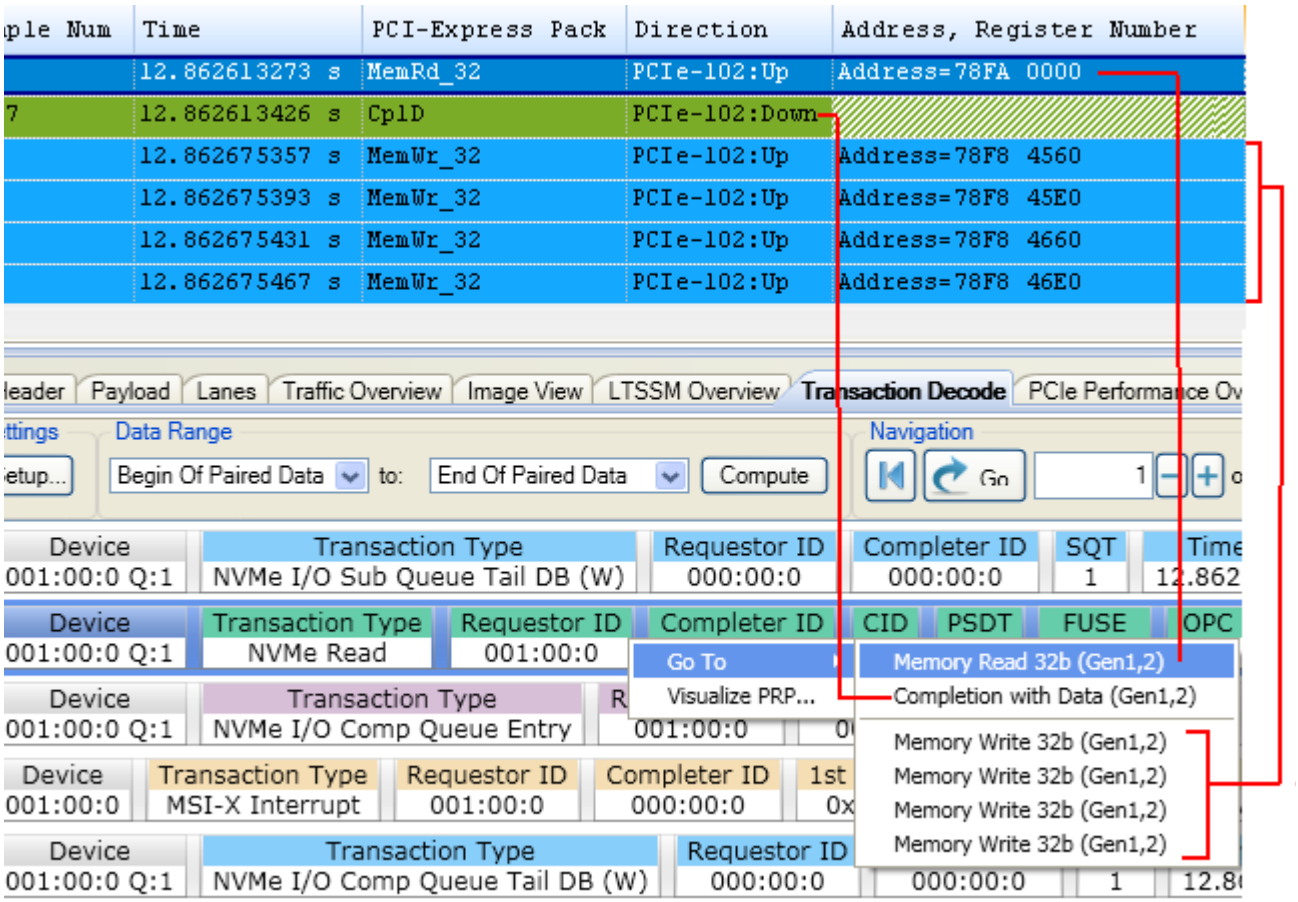


You can also visualize how the data returned by the Identify command is stored in specific PRP entries by right-clicking the transaction and selecting **Visualize Transaction...** (see page 115 for details).



Viewing NVMe I/O Command Transactions

The following screen displays an *NVMe Read* transaction to read data from the starting LBA specified in the Read command.



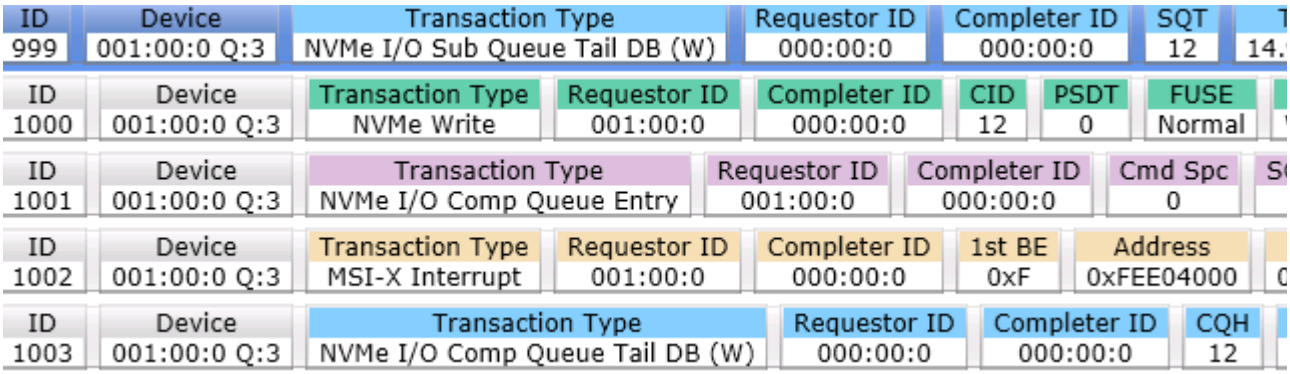
For this transaction, the controller:

- first performs a *Memory Read* to read the request entry from the base address of submission queue 1.
- then fetches the requested data from system memory
- then performs multiple Memory Writes to write this data to the applicable PRP entries for data transfer to host.

In the transaction following the NVMe Read transaction, the controller updates the completion queue 1 with the status of the Read command completion.

Viewing a Complete Set of Transactions for a Command Submission and Completion

The following screen displays a complete set of NVMe transactions between the host and controller. This set of five transactions represents the steps involved in the *NVMe Write* command submission and completion process.



ID	Device	Transaction Type	Requestor ID	Completer ID	SQT	T
999	001:00:0 Q:3	NVMe I/O Sub Queue Tail DB (W)	000:00:0	000:00:0	12	14.

ID	Device	Transaction Type	Requestor ID	Completer ID	CID	PSDT	FUSE	
1000	001:00:0 Q:3	NVMe Write	001:00:0	000:00:0	12	0	Normal	

ID	Device	Transaction Type	Requestor ID	Completer ID	Cmd Spc	S
1001	001:00:0 Q:3	NVMe I/O Comp Queue Entry	001:00:0	000:00:0	0	

ID	Device	Transaction Type	Requestor ID	Completer ID	1st BE	Address	
1002	001:00:0 Q:3	MSI-X Interrupt	001:00:0	000:00:0	0xF	0xFEE04000	0

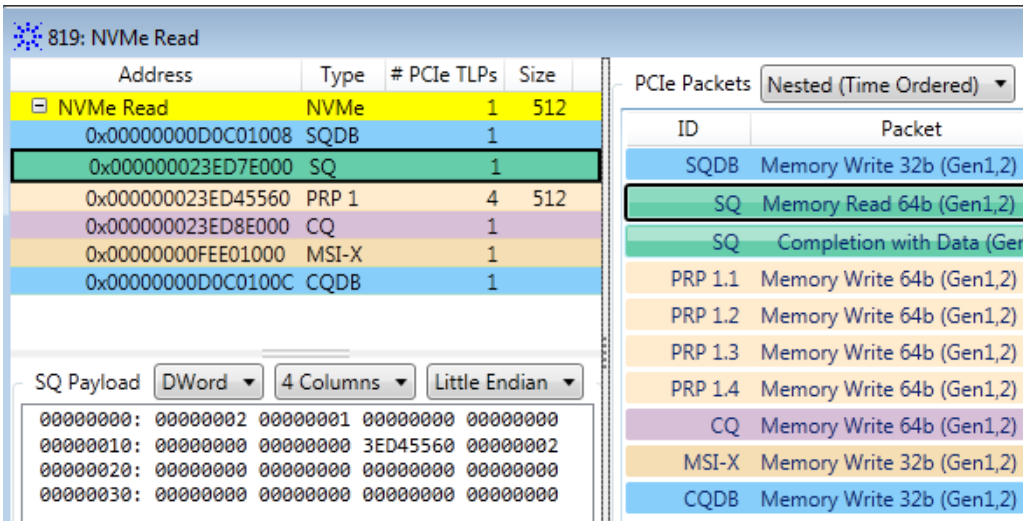
ID	Device	Transaction Type	Requestor ID	Completer ID	CQH	
1003	001:00:0 Q:3	NVMe I/O Comp Queue Tail DB (W)	000:00:0	000:00:0	12	

The following list describes the set of five transactions displayed above.

1. The first transaction indicates to the controller that a command is submitted for processing.
2. The second transaction represents the NVMe Write command that the host created in the submission queue. The controller reads this command from the submission queue for execution and executes the command.
3. The third transaction represents the command completion entry that the controller writes to the completion queue.
4. The fourth transaction represents the MSI-X interrupt generated by the controller to indicate that a completion entry has been added to the completion queue.
5. The fifth transaction indicates to the controller that the host has processed the completion entry that the controller added to the completion queue.

NOTE

You can also visualize a complete set of related transactions (as a super transaction) by right-clicking the transaction and selecting **Visualize Transaction...**. See page 106 for details on this feature. The following is an example of how the set of transactions for an *NVMe Read* command has been sequentially visualized.



Viewing Decoded Payload for NVMe Commands

For NVMe commands that retrieve information from NVMe registers in a specific data structure format, you can view the returned data structure in the same format as defined in the NVMe protocol specifications. For instance, the *Identify* command or the *Get Features* command returns information in a specific data structure format defined in NVMe specifications. The Transaction Decode tab displays the decoded payload for such commands to present the data structure for such commands as per the defined format.

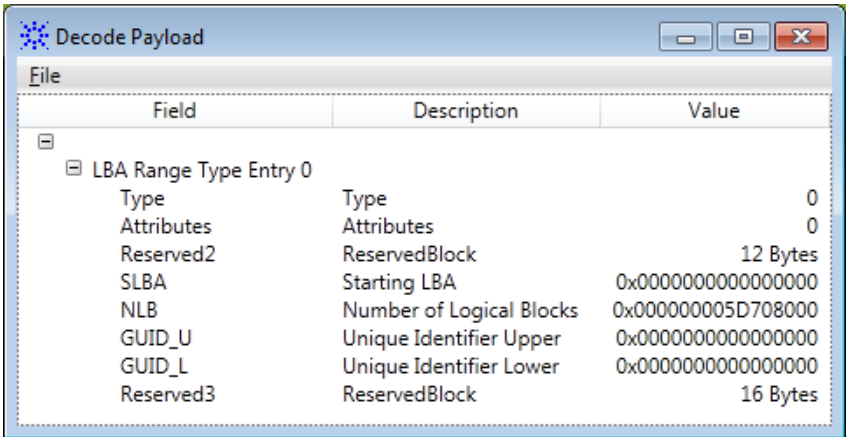
To view the decoded payload of an NVMe command

1 Right-click the transaction displayed for the command in the Transaction Decode tab.

2 Select **Decode Payload...**

The **Decode Payload** dialog box is displayed with the payload fields matching the fields specified in NVMe specifications.

The following screen displays the payload details of the ***NVMe Get Features*** command. The feature for which the information is retrieved is ***LBA Range Type***. The displayed payload is as per the data structure format defined for LBA Range Type in NVMe specifications.



Viewing Decoded PRPs for NVMe Commands

Physical Region Page (PRP) entries are used in read/write transactions to indicate the physical memory locations in system memory. These memory locations are used by controller for data transfers to and from system memory. For a Read request, the PRP entry indicates the memory location where the controller should transfer the data read from system memory. For a Write request, the PRP entry indicates the memory location from where the controller has to gather the data to be written to the system memory.

These addresses can be directly a memory location or a pointer to a location that provides a set of addresses of contiguous memory to perform large read/write operations.

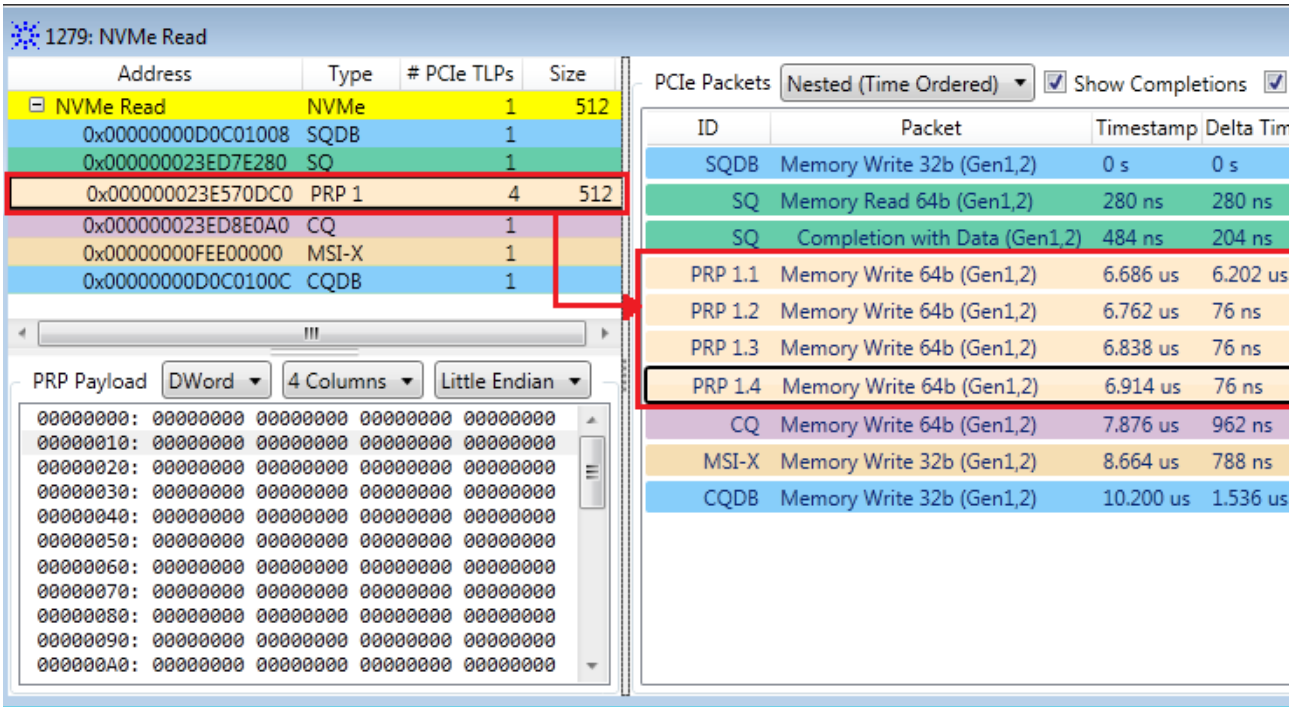
In the Transaction Decode tab, you can view the PRP entries associated with a command that utilizes PRP entries such as an NVMe Read or Write command.

To view the decoded PRPs of an NVMe command

1 Right-click the transaction displayed for the command in the Transaction Decode tab.

2 Select **Visualize Transaction...**

A dialog box is displayed with PRPs and other related transactions associated with the command.



In this dialog box, you can find the following PRP related information.

Component displayed	Description
PRPs applicable for the NVMe command	The displayed PRPs include: • a PRP entry representing an actual physical memory page. • a PRP representing a pointer to a page that defines a PRP List. For such a PRP, a set of PRP entries in a single page of contiguous memory are also displayed underneath. • multiple PRP lists for commands that require multiple PRP Lists for larger read/writes. The last PRP entry in the first list points to the next PRP list used.
Raw payload for each PRP entry	Clicking a PRP entry in the left displays the raw payload for that PRP entry in the lower pane of the dialog box.
Packets associated with each PRP entry	Clicking a PRP entry in the left displays a list of its associated PCIe packets in the right pane of the dialog box. You can click a packet from this list to navigate directly to that specific packet in the upper pane of Protocol Viewer. This can help you view the complete address range associated with a PRP entry.

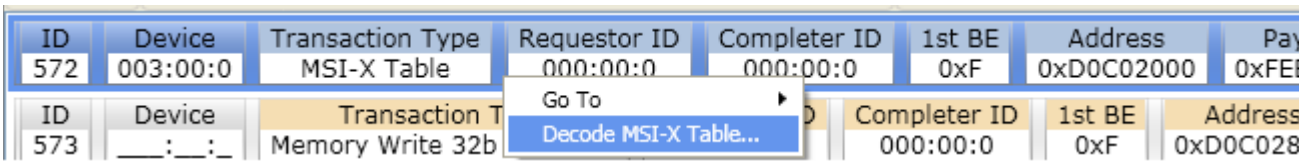
Viewing Decoded MSI-X Table

From the decoded **MSI-X Table** transaction, you can view the index entries of the MSI-X table in a decoded readable format.

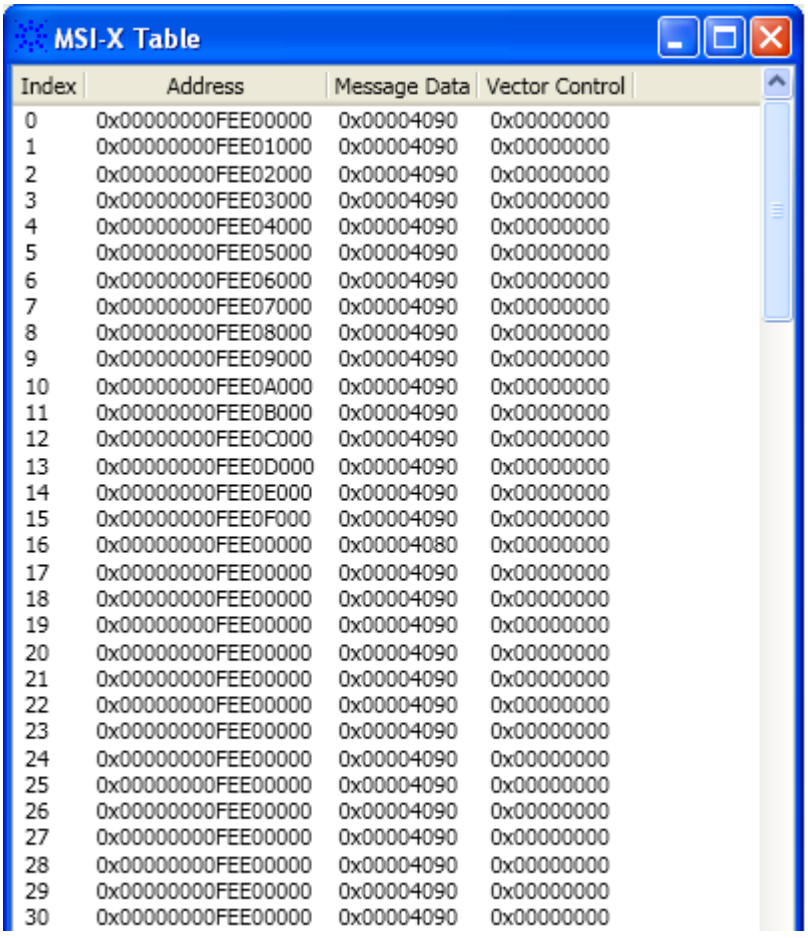
To view index entries of the MSI-X table

1 In the Transaction Decode tab, navigate to the MSI-X Table transaction by double-clicking the **MSI-X Table** transaction type from the right pane.

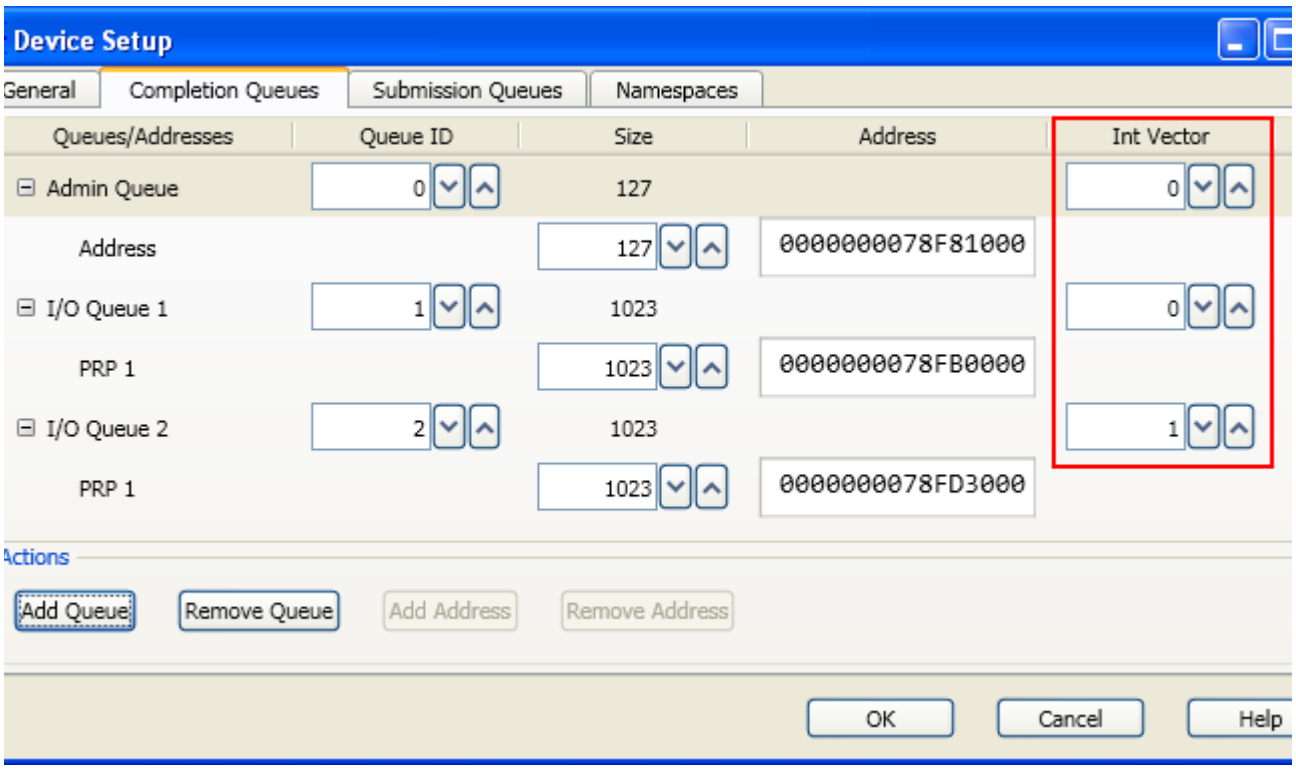
2 Right-click the highlighted **MSI-X Table** transaction in the left pane of the Transaction Decode tab and then select **Decode MSI-X Table**.



The decoded **MSI-X Table** is displayed.



An MSI-X index entry is associated to a completion queue at the time of creation of the queue. You can view details about the MSI-X index entry associated to a completion queue in the **Completion Queues** tab of the **Setup** dialog box.



Each MSI-X index entry in the MSI-X table has a base address associated to it. This is the address at which the controller writes the MSI-X interrupt for the associated completion queue.

The following screen displays one such MSI-X Interrupt transaction for the completion queue 1.

Viewing AHCI Transactions

This topic is specific to AHCI transactions and provides examples of how you can interpret AHCI transactions that are computed and displayed in the **Transaction Decode** tab. To get information on how you can configure and compute AHCI transactions in the Transaction Decode tab, refer to the following previous topics in this chapter.

- "Transaction Decoding - Overview" on page 86
- "Configuring and Computing Decoded Transactions" on page 87
- "Defining / Verifying the Device Setup" on page 89
- "Interpreting and Navigating Through the Transaction Decode Results" on page 99

For AHCI, the Transaction Decode tab displays transactions for:

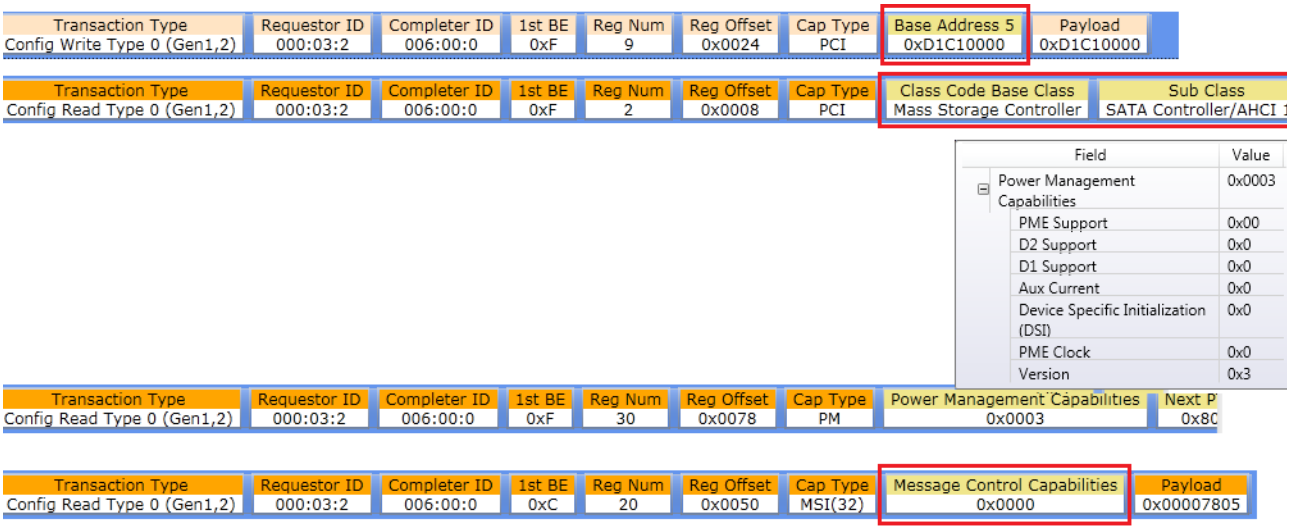
- PCIe Config space registers
- Generic host control registers
- Port specific registers
- SATA commands

The following sections provide examples of these decoded AHCI transactions.

PCIe Configuration Space Registers Transactions - Examples

These transactions are PCIe Config Read and Write requests to various configurations registers in the DUT's config space. You can view the PCI Header and PCI Capabilities for an AHCI device in these transactions. Some examples of the registers that these transactions map to are:

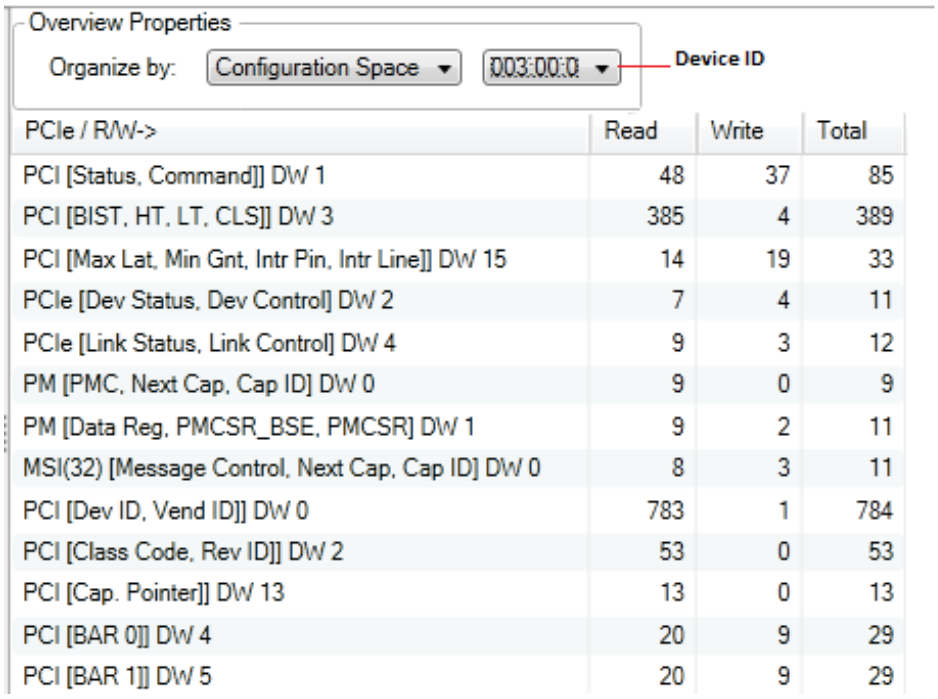
- PCI Header registers such as *Identifier (Device ID), Class Codes, AHCI Base Address <BAR5>, and Capabilities Pointer (CAP).*
- PCI Power Management Capability registers such as *PMCAP*
- Message Signaled Interrupt Capability registers such as *MSICAP*



NOTE

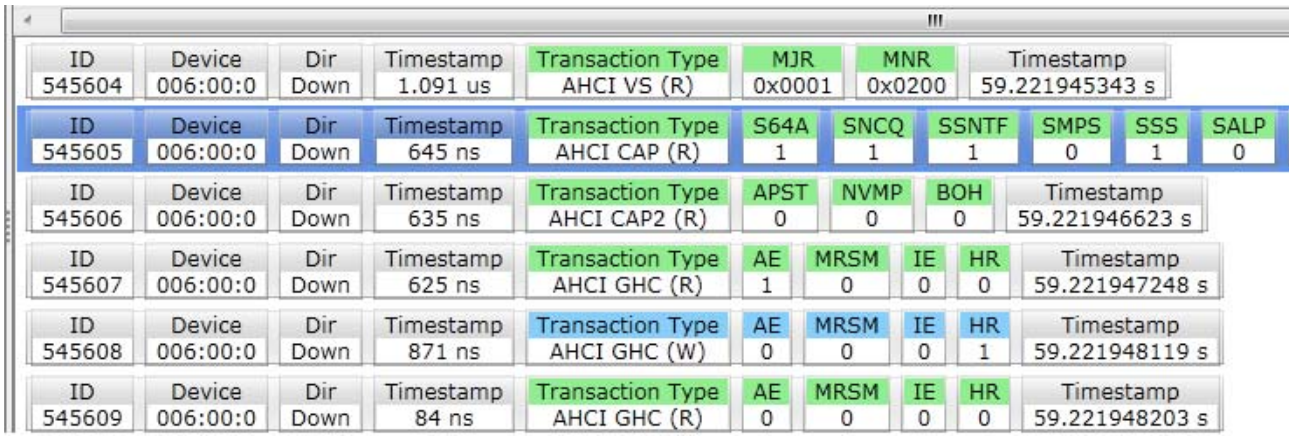
The decoded transactions are a mix of PCIe Config, generic host control, port-specific and SATA commands transactions. If you are looking for specific PCIe config space transactions, you may want to use the Overview pane on the right. In this pane, you can choose to organize the registers listing by **Configuration Space**. Doing so, displays the list of PCIe configuration space registers in this pane. You can then double-click the desired register from this list to navigate to the transaction for this register in the left pane.

PCIe config space registers are not displayed in the Overview pane if you have organized this pane by **Directions** or **Ports**.



Generic Host Control Registers Transactions - Examples

Generic host control registers such as *AHCI CAP (Host Capabilities)* and *GHC (Global Host Control)* are global HBA registers that are applicable for the entire HBA. The Transaction Decode tab displays decoded transactions for these registers. The following screen shows some such transactions for generic host control registers.



ID	Device	Dir	Timestamp	Transaction Type	MJR	MNR	Timestamp
545604	006:00:0	Down	1.091 us	AHCI VS (R)	0x0001	0x0200	59.221945343 s

ID	Device	Dir	Timestamp	Transaction Type	S64A	SNCQ	SSNTF	SMPS	SSS	SALP
545605	006:00:0	Down	645 ns	AHCI CAP (R)	1	1	1	0	1	0

ID	Device	Dir	Timestamp	Transaction Type	APST	NVMP	BOH	Timestamp
545606	006:00:0	Down	635 ns	AHCI CAP2 (R)	0	0	0	59.221946623 s

ID	Device	Dir	Timestamp	Transaction Type	AE	MRSM	IE	HR	Timestamp
545607	006:00:0	Down	625 ns	AHCI GHC (R)	1	0	0	0	59.221947248 s
545608	006:00:0	Down	871 ns	AHCI GHC (W)	0	0	0	1	59.221948119 s
545609	006:00:0	Down	84 ns	AHCI GHC (R)	0	0	0	0	59.221948203 s

Port Specific Registers Transactions - Examples

AHCI port specific registers such as *PcCLB, PxIS, PxSACT* and *PxCDM* are applicable for each port supported by an AHCI device. The read and write transactions to these port registers are also displayed in the Transaction Decode tab. The following screen displays some examples of such ports register accesses.

ID	Device	Dir	Timestamp	Transaction Type	Port	Command Issue	Timestamp
547898	006:00:0	Down	675 ns	AHCI PxCI (R)	1	0x00000000	62.812769603 s

ID	Device	Dir	Timestamp	Transaction Type	Port	Device Status	Timestamp
547899	006:00:0	Down	163.849 us	AHCI PxSACT (R)	1	0x00000000	62.812933452 s

ID	Device	Dir	Timestamp	Transaction Type	Port	Command Issue	Timestamp
547900	006:00:0	Down	632 ns	AHCI PxCI (R)	1	0x00000000	62.812934084 s

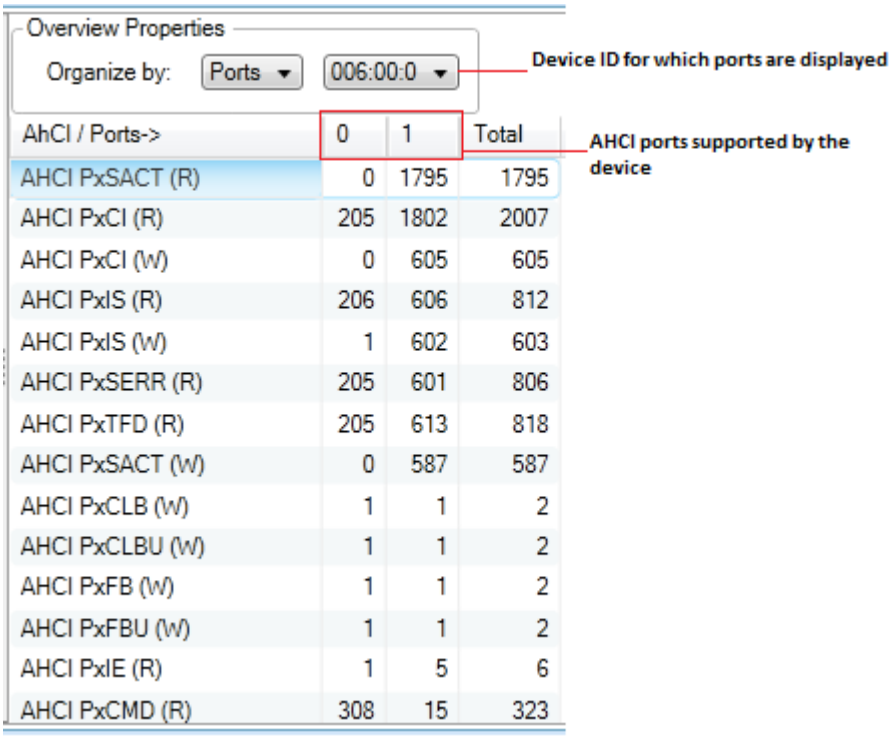
ID	Device	Dir	Timestamp	Transaction Type	Port	Device Status	Timestamp
547901	006:00:0	Down	648 ns	AHCI PxSACT (W)	1	0x00000020	62.812934732 s

ID	Device	Dir	Timestamp	Transaction Type	Port	Command Issue	Timestamp
547902	006:00:0	Down	451 ns	AHCI PxCI (W)	1	0x00000020	62.812935183 s

NOTE

The decoded transactions are a mix of PCIe Config, generic host control, port-specific and SATA commands transactions. If you are looking for a particular type of port specific transactions, you may want to use the Overview pane on the right. In this pane, you can choose to organize the registers listing by **Ports**. Doing so, displays the list of port registers in this pane and organize the transaction occurrences by ports. You can then double-click the desired register from this list to navigate to the transaction for this register in the left pane.

Port registers are not displayed in the Overview pane if you have organized this pane by **Configuration Space**.



AhCI / Ports->	0	1	Total
AHCI PxSACT (R)	0	1795	1795
AHCI PxCI (R)	205	1802	2007
AHCI PxCI (W)	0	605	605
AHCI PxIS (R)	206	606	812
AHCI PxIS (W)	1	602	603
AHCI PxSERR (R)	205	601	806
AHCI PxTFD (R)	205	613	818
AHCI PxSACT (W)	0	587	587
AHCI PxCLB (W)	1	1	2
AHCI PxCLBU (W)	1	1	2
AHCI PxFB (W)	1	1	2
AHCI PxFBU (W)	1	1	2
AHCI PxIE (R)	1	5	6
AHCI PxCMD (R)	308	15	323

SATA Commands Transactions - Examples

The decoded AHCI transactions also include transactions for SATA Commands such as *Identify Device*, *Set Features*, *Read FPDMA Queued*, *Write FPDMA Queued*, and *NOP*.

The following screens display some examples of decoded SATA Commands transactions.

Transaction Type	Port	Command Header	Address	Features	Command	C	R
AHCI ATA Command SetFeature (R)	1	4	0x13E64ED00	Enable write cache	SET FEATURES	1	0

Transaction Type	Port	Command Header	Address	Features	Command	C	R
AHCI ATA Command RDMA_NCQ (R)	1	28	0x13E64D800	0x00	READ FPDMA QUEUED	1	0

Transaction Type	Port	Command Header	Address	Features	Command	C	R	R1	R
AHCI ATA Command Identify (R)	1	1	0x13E64D800	0x00	IDENTIFY DEVICE	1	0	0	

Transaction Type	Port	Command Header	Address	Features	Command	C	R
AHCI ATA Command WRMA_NCQ (R)	1	16	0x13E64D800	0x08	WRITE FPDMA QUEUED	1	0

Visualizing a Complete Set of AHCI Transactions

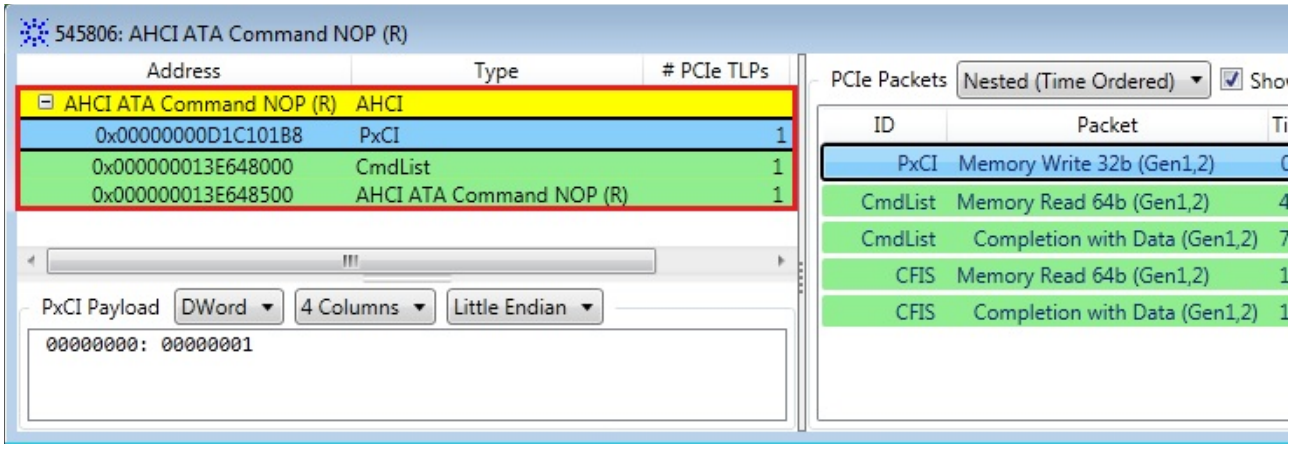
You can view each AHCI transaction displayed in the Transaction Decode tab as a super transaction to visualize its complete set of related transactions. To visualize the transaction set for an AHCI transaction, right-click the transaction and select **Visualize Transaction...**.

NOTE

For a SATA command transaction such as Read FPDMA Queued that has a number of related transactions, the Visualize Transaction feature is particularly useful.

For PCIe config space or AHCI (generic/port) register transactions, the Visualize Transaction feature displays the read/write access transaction to the register.

Example 1 - Visualize the transaction set for a NOP command transaction



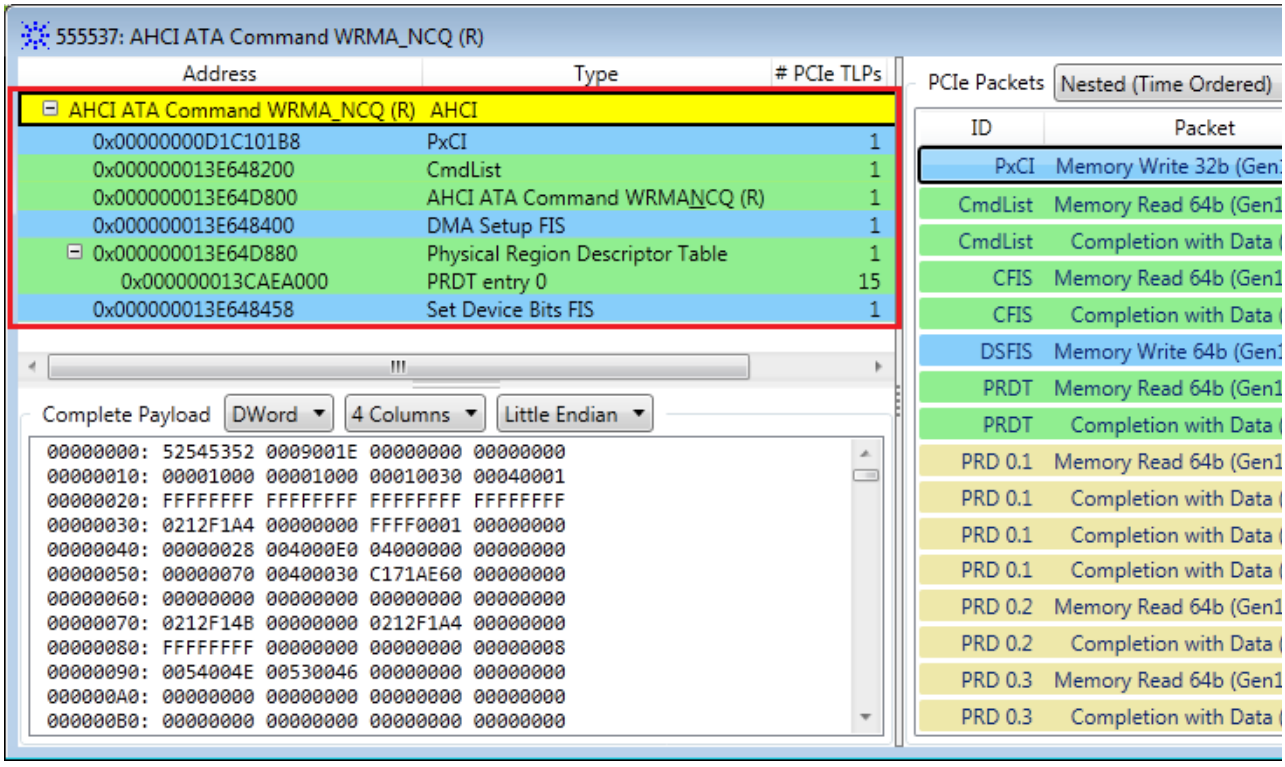
In the above example, the following transactions are a part of the *ATA Command NOP* super transaction.

1 The first transaction is a memory write to the PxCI (Port x Command Issue) register to indicate that a command has been built in memory for a command slot.

2 The second transaction is a memory read for the added command list entry.

3 The third transaction is a memory read of the NOP command from the command table.

Example 2 - Visualize the transaction set for a Write FPDMA Queued command transaction



In the above example, the following transactions are a part of the *ATA Command Write FPDMA Queued* super transaction.

1 The first transaction is a memory write to the PxCI (Port x Command Issue) register to indicate that a command has been built in memory for a command slot.

2 The second transaction is a memory read for the added command list entry.

3 The third transaction is a memory read of the Write FPDMA Queued command from the command table.

4 The fourth transactions is a DMA Setup FIS (DSFIS) memory write to transfer data for the Write FPDMA Queued command in the appropriate slot.

5 The fifth transaction is a PRD Table read transaction. This transaction further expands to display the PRDT entry used for reading the transferred data.

6 The last transaction in the set is a memory write for updating the Set Device Bits FIS. This indicates the completion of the Write FPDMA Queued command.

For more information on visualize transaction, refer to "Visualizing a Transaction Set (Super Transaction)" on page 106.

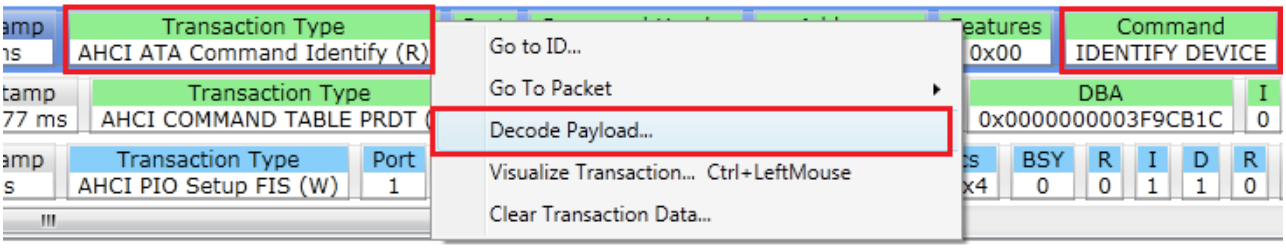
Viewing Decoded Payload for AHCI Commands

For ***AHCI ATA IDENTIFY DEVICE*** and ***IDENTIFY (PACKET) DEVICE*** commands that retrieve information in a specific data structure format, you can view the returned data structure in the same format as defined in the Serial ATA specifications. The Transaction Decode tab displays the decoded payload (all 256 words) for these commands to present their data structure as per the defined format.

To view the decoded payload of an AHCI ATA IDENTIFY DEVICE command

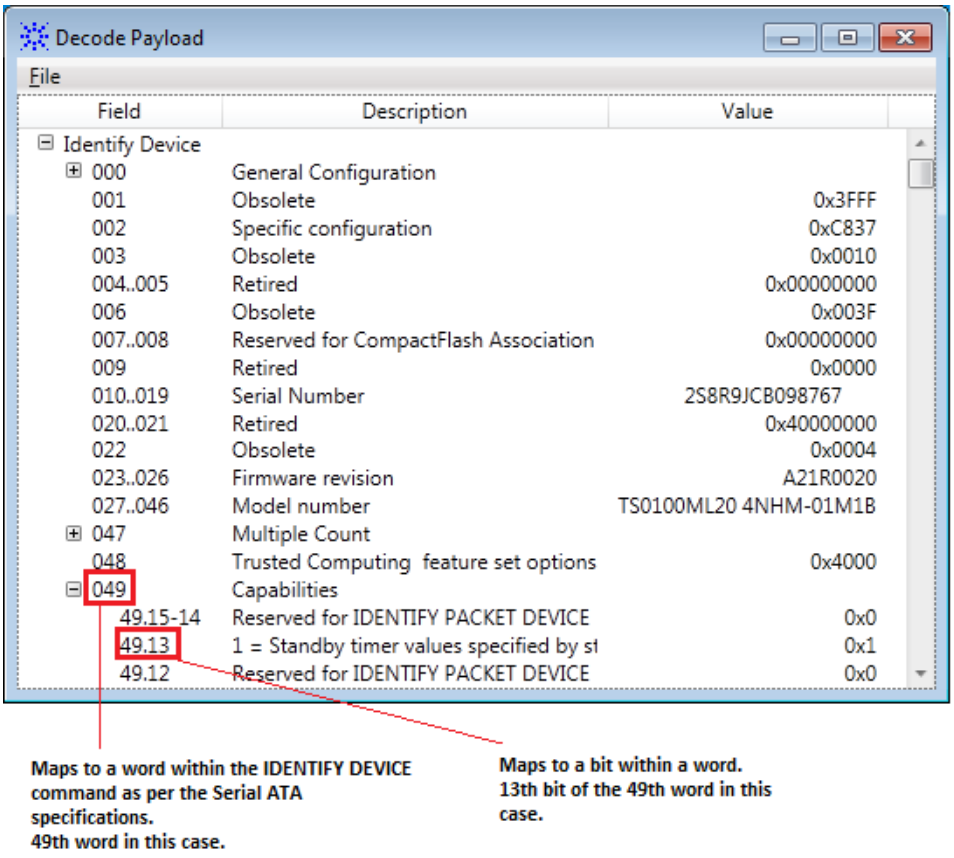
1 Right-click an AHCI ATA IDENTIFY DEVICE transaction in the Transaction Decode tab.

2 Select **Decode Payload...**



The **Decode Payload** dialog box is displayed with the payload fields matching the information structure specified for the IDENTIFY DEVICE command in Serial ATA specifications.

The following screen displays the payload details of the ***IDENTIFY DEVICE*** command.



Viewing PRDT Entries for an ATA Command

Physical Region Descriptor Table (PRDT) is a table of scatter/gather list. It has zero to many entries. Each entry has a base address and byte counts in system memory where the device reads or writes the actual data transfer if the ATA command is a data transfer command.

In the Transaction Decode tab, you can view the PRDT entries associated to an ATA command that utilizes PRDT entries such as an *AHCI ATA Identify command* or *AHCI Read FPDMA Queued command*.

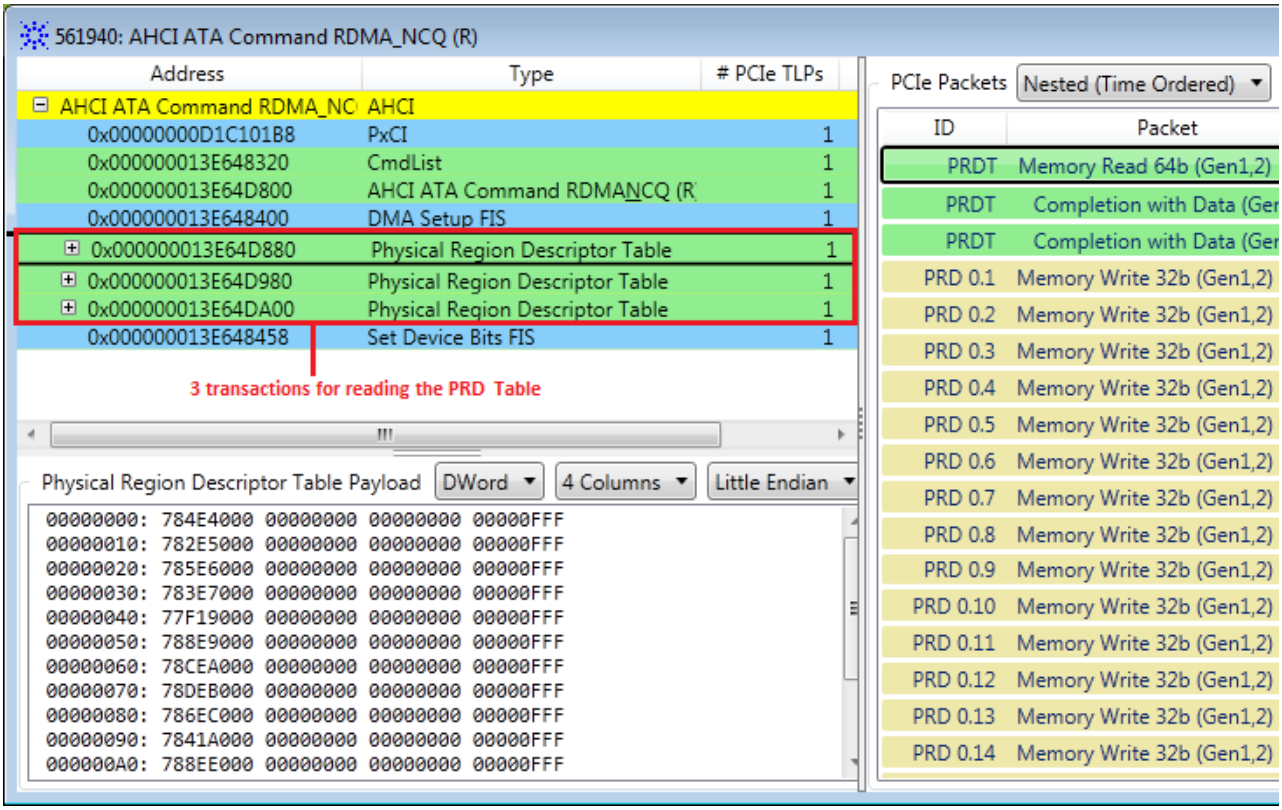
To view the decoded PRDT entries of an ATA command

1 Right-click the transaction displayed for the command in the Transaction Decode tab.

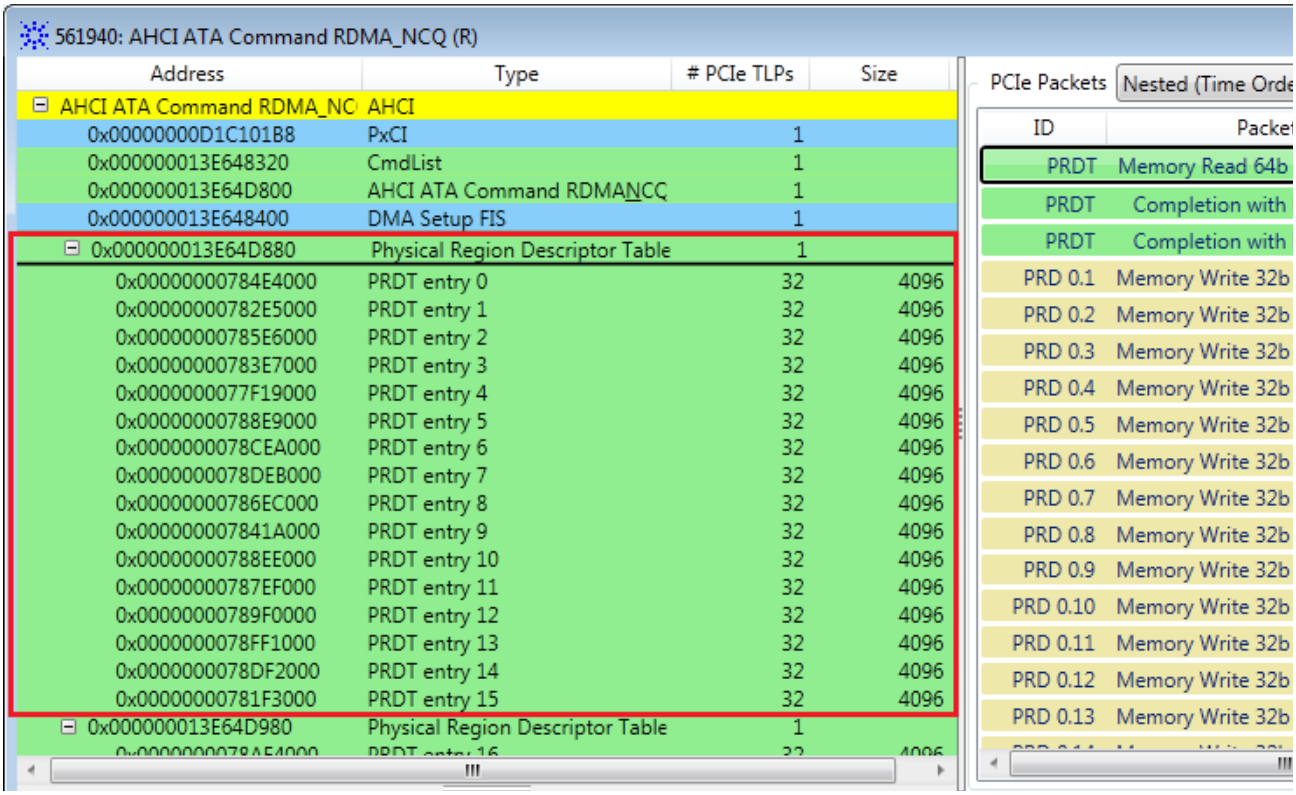
2 Select **Visualize Transaction...**

A dialog box is displayed with applicable PRDT transactions and other related transactions for the ATA command. In the following example, the three transactions for reading the PRD table for the Read FPDMA

Queued command are highlighted. Clicking one of these PRDT transactions displays the raw payload for that PRDT Read transaction in the lower pane.

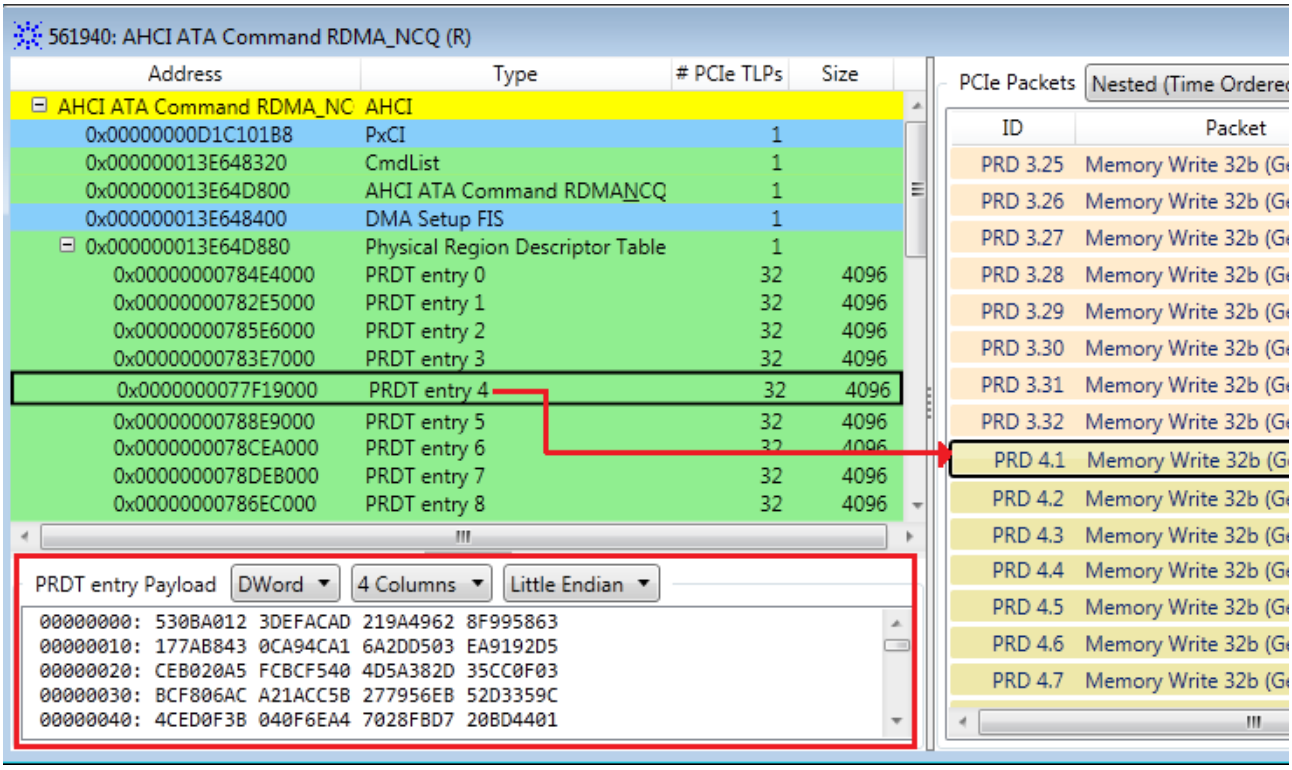


3 Expand each of the displayed PRDT read transactions in the left to view the PRDT entries used for the data transfer. In the following example, the 16 PRDT entries applicable for the first PRDT read transaction are highlighted. With each PRDT entry, its base address, bytes count, and the number of PCIe TLPs utilized for data transfer are also displayed.



4 Clicking a PRDT entry:

- displays the raw payload for the data transfer for the memory pointed to by that PRDT entry.
- highlights the first PCIe packet utilized for data transfer for the memory pointed to by that PRDT entry.


561940: AHCI ATA Command RDMA_NCQ (R)
Address
Type
PCIe TLPs
Size
AHCI ATA Command RDMA_NC
AHCI
0x00000000D1C101B8
PxCI
1
0x000000013E648320
CmdList
1
0x000000013E64D800
AHCI ATA Command RDMANCQ
1
0x000000013E648400
DMA Setup FIS
1
0x000000013E64D880
Physical Region Descriptor Table
1
0x00000000784E4000
PRDT entry 0
32
4096
0x00000000782E5000
PRDT entry 1
32
4096
0x00000000785E6000
PRDT entry 2
32
4096
0x00000000783E7000
PRDT entry 3
32
4096
0x0000000077F19000
PRDT entry 4
32
4096
0x00000000788E9000
PRDT entry 5
32
4096
0x0000000078CEA000
PRDT entry 6
0x0000000078DEB000
PRDT entry 7
32
4096
0x00000000786EC000
PRDT entry 8
32
4096
PRDT entry Payload
DWord
4 Columns
Little Endian
00000000: 530BA012 3DEFACAD 219A4962 8F995863
00000010: 177AB843 0CA94CA1 6A2DD503 EA9192D5
00000020: CEB020A5 FCBCF540 4D5A382D 35CC0F03
00000030: BCF806AC A21ACC5B 277956EB 52D3359C
00000040: 4CED0F3B 040F6EA4 7028FBD7 20BD4401
PCIe Packets
Nested (Time Ordere
ID
Packet
PRD 3.25
Memory Write 32b (Ge
PRD 3.26
Memory Write 32b (Ge
PRD 3.27
Memory Write 32b (Ge
PRD 3.28
Memory Write 32b (Ge
PRD 3.29
Memory Write 32b (Ge
PRD 3.30
Memory Write 32b (Ge
PRD 3.31
Memory Write 32b (Ge
PRD 3.32
Memory Write 32b (Ge
PRD 4.1
Memory Write 32b (G
PRD 4.2
Memory Write 32b (Ge
PRD 4.3
Memory Write 32b (Ge
PRD 4.4
Memory Write 32b (Ge
PRD 4.5
Memory Write 32b (Ge
PRD 4.6
Memory Write 32b (Ge
PRD 4.7
Memory Write 32b (Ge

12 Viewing Offline Performance Summary

In the Protocol Viewer window, you can generate and view the performance summary from a PCIe trace that you captured using the U4301A Analyzer module. This chapter describes how you can compute and view offline performance summary from the captured PCIe data.

Offline Performance Summary - Overview

The ***PCIe Performance Overview*** tab in the Protocol Viewer window allows you to perform post processing on the captured PCIe traffic to generate an offline performance summary of bus utilization. This tab presents statistics for various performance parameters in tabular as well as charts form.

In this tab, you define the range of captured data for which performance summary is to be generated. The software decodes transactions from this specified range of data and then computes performance statistics and charts from the decoded transactions. The specified range of trace data is sampled and statistics is computed from these samples to generate charts for each performance parameter.

Performance statistics are displayed separately for upstream and downstream link directions.

NOTE You do not need connectivity to the U4301 hardware module to generate performance summary from a captured PCIe trace.

PCIe Performance Overview Tab

You use the ***PCIe Performance Overview*** tab displayed in the lower pane of the Protocol Viewer to compute and view performance summary.

This tab displays the performance data in the following two panes.

Pane	Description
Performance Statistics pane	This is the left pane that displays a list of categories and the performance parameters for each of the categories for which statistics will be generated and displayed. For each of the parameters that you select, statistics are displayed based on the link directions (upstream as well as downstream).
Performance Charts pane	This is the right pane and displays a performance chart for selected performance parameters listed under the category.

NOTE If the PCIe Performance Overview tab is not visible, click the button displayed at the top of the Protocol Viewer window.

The Overlay View - At a Glance

The information in the PCIe Performance Overview tab is presented using the Overlay view. The Overlay view allows you to select the series that you want to be displayed in the chart area. You can select the series by clicking the required performance parameter check box listed under Statistics tree/table on the left. This view displays graphs for the selected series in a single chart with a black background. It displays the Band Chart area where you can view the MSI Write, Msg Assert_INT and Msg Deassert_INT and error packets occurrence plotted in the chart. It also displays multiple Y-axis which you select in the **Setup** dialog box. To know more about how to select and interpret multiple Y-axis, see "Showing/Hiding multiple Y-axis" on page 138. Following screen displays the Overlay view after you select and compute a range:

In the above screen, graphs for the Update_FC_P series (represented by dotted lines) in both directions are displayed. The blue dotted line represents the graph for Update_FC_P series in upstream, whereas, the red dotted line represents the graph for Update_FC_P series in the downstream direction.

Configuring and Computing Offline Performance Summary

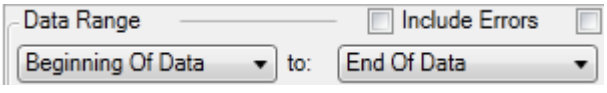
Before you Start

- You should have purchased and installed the *Offline Performance Summary* license for computing performance summary.

  On purchasing the license, you receive an entitlement certificate. Follow the instructions in this certificate to install the license.
- Ensure that the data in the required direction(s) is already captured and available in the Logic and Protocol Analyzer GUI for performance summary computation. You may save the captured data in a Logic Analyzer configuration (.ala) file and access this data offline for performance summary computation.

Computing Offline Performance Summary

1. Click the **PCIe Performance Overview** tab in the Protocol Viewer window.
2. In the **Data Range** groupbox, specify the start and end points of the captured PCIe data for which you want to compute performance summary. Only the specified range of data is analyzed to compute performance. Following options are available for setting this data range.
   - **Beginning and End of data** - This data range selection ensures that performance summary is computed for the entire trace.
   - **Begin Extent and End Extent** - This data range selection ensures that performance summary is computed only for the data that has been marked by extent markers. The software automatically places extent markers on the beginning and end of the current pan/zoom extents defined in charts. When you change the pan/zoom extents in charts, the extent markers are automatically moved to changed extents.
   - **Trigger** - Selecting Trigger in the data range ensures that performance summary is computed from the point where the U4301 module's trigger condition was met.
   - **Markers** - Selecting markers in the data range ensures that performance summary is computed for the specific portion of PCIe traffic defined by markers. Refer to "Defining Markers for Setting the Computation Range" on page 136 to know more.



3. For generating performance statistics, only complete transactions from the captured trace are used. Select the **Assume ACK** checkbox to instruct the software to assume ACKs for the transactions in which only ACK is

missing. Assuming ACKs, therefore ensures that the transactions with missing ACK are considered complete and used in performance summary computation. You may want to use this Assume ACK option in situations such as when you have filtered ACKs while data capture to make more memory available to TLPs.

4 For producing the performance statistics, transaction of only error free packets from the captured trace are taken into account. The packets containing error are ignored while generating the performance statistics. Select the **Include Errors** check-box to let the software include error packets and compute the performance statistics including these packets. Selecting Include Errors checkbox increases the computation time of PCIe performance Overview. It creates a series that is displayed in the Band Chart with an element for each packet containing error in the list.

5 Click the **Compute** button displayed with the Data Range fields.

On clicking Compute, first the transactions are decoded from the specified data range of PCIe trace. Then, statistics and charts are computed from these decoded transactions and results are displayed.

Defining Markers for Setting the Computation Range

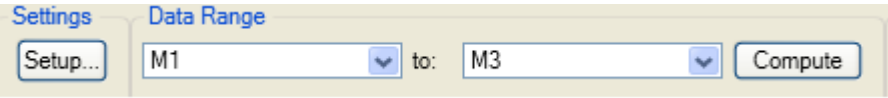
If the captured PCIe traffic is too large and you want to view performance summary for a specific portion of this traffic, then you can limit the computation range by defining start and end markers in the PCIe traffic.

To define markers

1 From the upper pane of the Protocol Viewer, right-click the row in the captured PCIe traffic that should act as the starting point for performance summary computation.

2 Select **Place Marker** from the displayed context menu and then select an existing marker or click **New Marker** to define a new marker at this point.

Once markers are defined, these are available for selection in the **Data Range** group box of the **PCIe Performance Overview** tab.



Saving the Computed Performance Summary Data

Once you computed the performance summary data, you can save the performance configurations along with the captured PCIe traffic in a logic analyzer .ala configuration file. On saving, the settings such as zoom, pan, sample rate, markers, chart type, and chart order that you configured in

the PCIe Performance Overview tab are also saved in the .ala file along with the PCIe trace data. Loading this .ala file retrieves these settings and computes and displays performance summary based on the saved settings.

NOTE

You do not need the *Offline Performance Summary* software license to resample charts from the computed performance summary. However, if you want to recompute performance summary from the saved PCIe trace, then you need the *Offline Performance Summary* software license.

To save the performance summary settings

1 Click **File** > **Save as**.

2 In the **Save As** dialog box, specify the name of the file.

3 Ensure that the **Standard Configuration (*.ala)** option is selected as the file type and **All Data and Setup** is selected in the **File Options** group box.

4 Click **Save**.

To access and view previously saved performance summary settings

1 Click **File** > **Open**.

2 In the **Open** dialog box, navigate to the **Standard Configuration (*.ala)** file in which you saved the data.

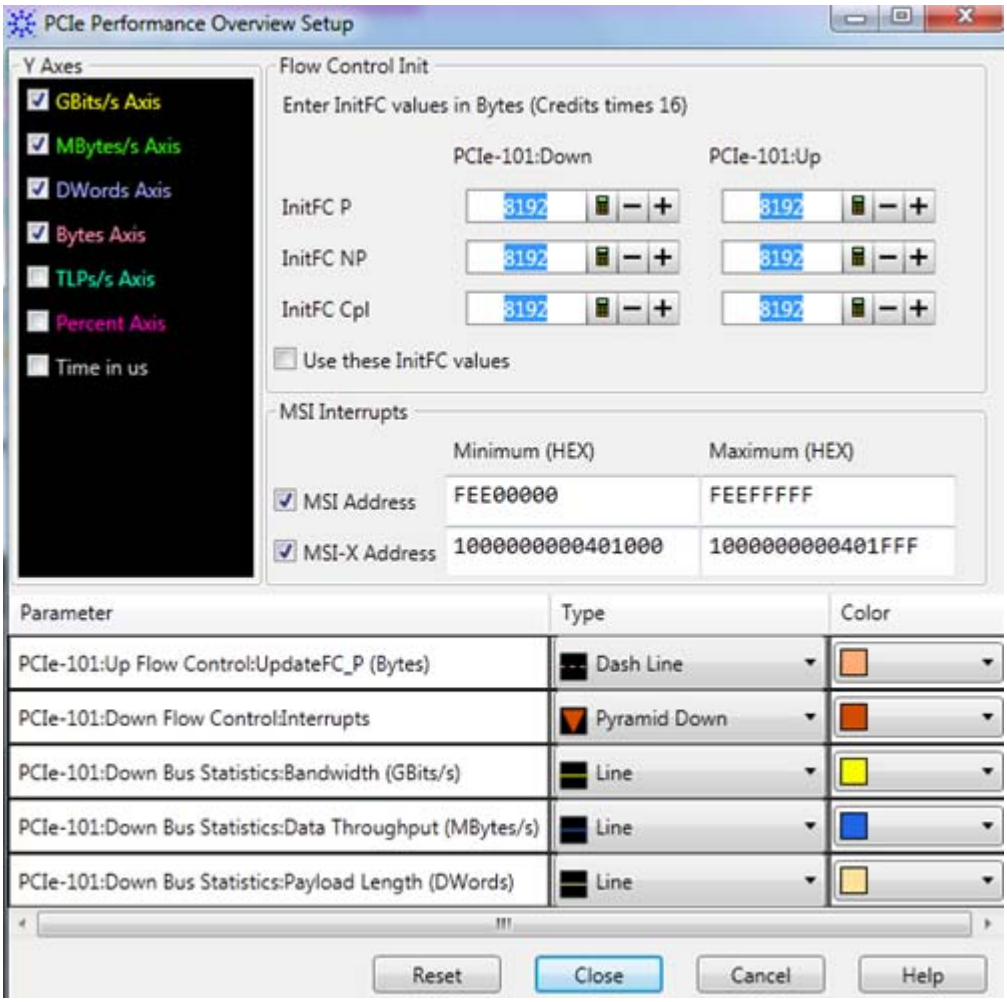
3 Click **Open**.

Defining Chart Settings

You can define settings for the overlay chart in the **Setup...** tab of the **Settings** section and change the appearance of the displayed chart.

To access the Setup dialog box

Click the **Setup...** button under the **Settings** section. The Setup dialog box appears as shown below.

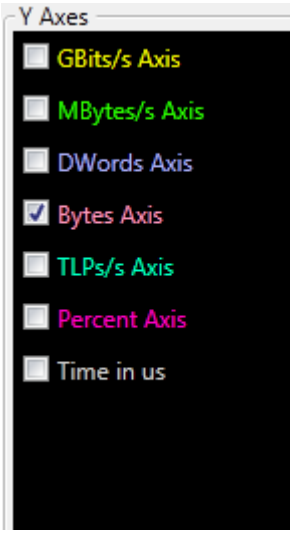


The setup details that you specify in this dialog box helps you change the way series and axes are displayed in the overlay graph. For example- you can change the graph display type and color of the displayed series or you can show or hide the Y-axis by selecting or de-selecting the respective Y-axis checkbox.

The following is the list of tasks that you can do using the **Setup** dialog box:

Showing/Hiding multiple Y-axis

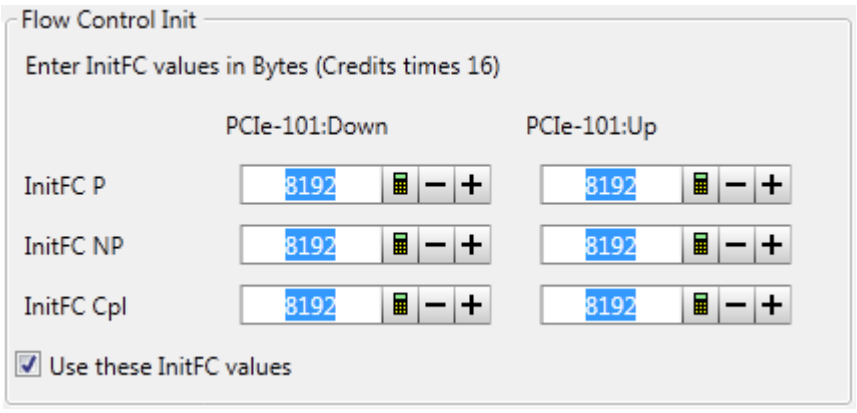
Select or de-select the Y-axis checkbox to show or hide the Y-axis displayed in the chart.



NOTE Showing or hiding a particular Y-axis does not affect how series are computed or displayed in the chart.

Specifying InitFC values

You can initially define the maximum flow control credit limits by entering InitFC values for posted, non-posted, and completion transactions in both directions (Upstream and Downstream).



Click button displayed with the InitFC_P, InitFC_NP, and InitFC_Cpl fields to open the calculator and input values. Select the checkbox '**Use these InitFC values**' to use the InitFC values defined by you when you are computing and interpreting offline performance summary. In case InitFC values are not defined or '**Use these InitFC values**' field is not selected, the minimum and maximum credit levels for the captured trace is

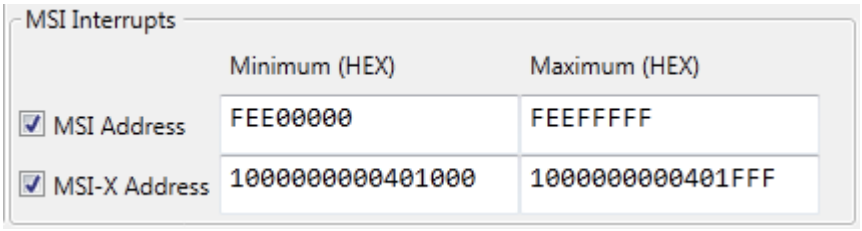
automatically computed and flow control mechanism works on the basis of those calculated values. The minimum and maximum credit levels varies from one trace to other depending upon the size of the trace.

NOTE InitFC values are applicable only for Flow Control performance statistics category. You can use InitFC values for posted, non-posted and completions transactions only when you are computing flow control credits.

Specifying Min/Max value for MSI and MSI-X Address

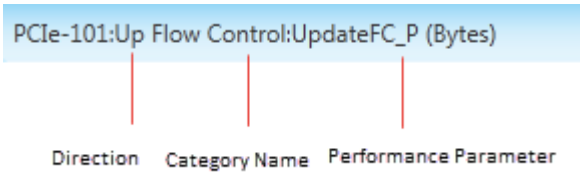
You can specify the minimum and maximum values for the Message Signaled Interrupt (MSI/MSI-X) address in the **MSI and MSI-X Address** row for which you want Interrupt to be generated and plotted in the Band Chart.

Selecting this checkbox will generate interrupts for the specified address which you can view in the Band Chart.



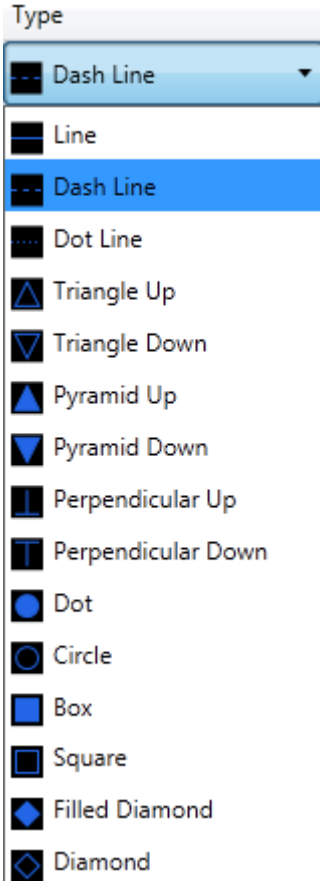
Understanding Parameter Column

The series which you select by clicking their respective check-box in the Statistics Tree/Table of the Performance Overview Tab is displayed here in the **Parameter** column of the **Setup** dialog box. The Parameter is the full name of the series and is comprised of the Direction (Up or Down), the Category name picked from the Performance Statistics tree/table, and the checked Series name.



Changing the appearance of the graph

You can change the appearance of the graph representing the respective series listed in the **Parameter** column of the **Setup** dialog box. To do so, click the drop-down in the **Type** column and select the graph type you want to change with.



Changing the color of the Graph Line

You can also change the color of the graph line by picking color of your choice from the color palette. To do so, click the **Color** drop-down to display the color combo box consisting of different colors, and select the color of your choice.

- Once all the settings are defined in the Setup dialog box, click the **Close** button to apply those settings and exit from the dialog box.
- Click the **Reset** button to restore the last settings done previously when you opened the Setup dialog box. This resets the Axis, Types and Colors to their previous state.
- Clicking the **Cancel** button allows you to exit from the dialog box without making any changes.

Interpreting the Performance Summary Results

Performance Statistics panes

The **Performance Statistics** pane displays a hierarchical list in which various performance statistics are categorized in groups and sub-groups.

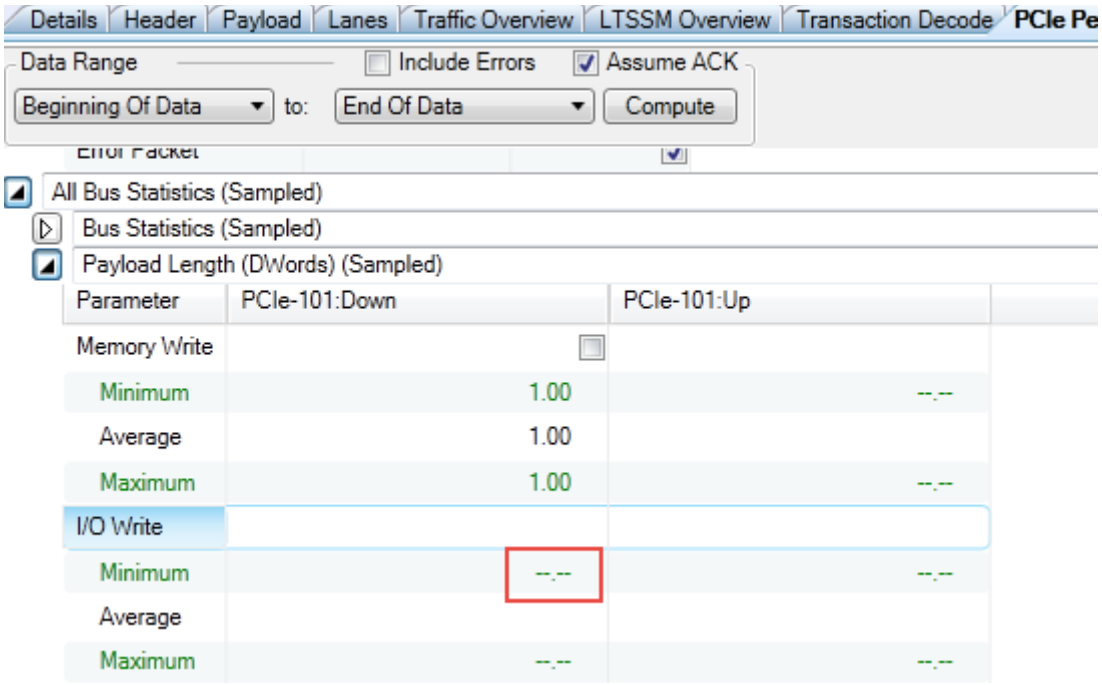
Clicking a group or category in this pane displays the link-wise statistics for associated performance parameters. The following table briefly describes the performance statistics displayed for categories.

Category	Performance Statistics Displayed
Flow Control	Tracks and computes the available flow control credits for a bidirectional data trace and helps in analyzing the flow of data. To know more refer to the topic Flow Control.
Bus Statistics	• **Bandwidth (GBits/s):** Shows the number of non- idle symbol bits transferred per second. • **Data Throughput (MBytes/s)**: Shows the number of TLP payload bytes transferred per second. • **Payload Length (DWords):** Shows the minimum, maximum, as well as average payload size for TLPs. • **TLP Count (TLPs/s)**: Shows the number of TLPs transferred per second. • **Link Efficiency (%):** Shows the efficiency of the link. It is calculated as Symbol time for payload / (Symbol time for all DLLP + Symbol time for all TLP + Symbol time for OS). • **Link Utilization (%)**: Shows the percentage of non- idle symbols in total number of symbols transferred. • **TLP Utilization (%):** Shows the percentage of TLP symbols in total number of symbols transferred.

Transaction Performance	• **Non- Posted Transactions**: Shows the minimum, maximum, and average values of the following performance parameters for all non- posted transactions.
	  • **Response Time (ns)**: It is same as the duration of the transaction.
	  • **Latency (us)**: It is the time duration between the end of a request transaction and the arrival of its first completion.
	  • **Throughput (MBytes/s)**: It is the length of complete data divided by the response time.
	• **Posted Transactions**: Shows the minimum, maximum, and average values of the following performance parameters for all posted transactions.
	  • **Response Time (ns)**: It is same as the duration of the transaction.
	  • **Throughput (MBytes/s)**: It is the length of complete data divided by the response time.

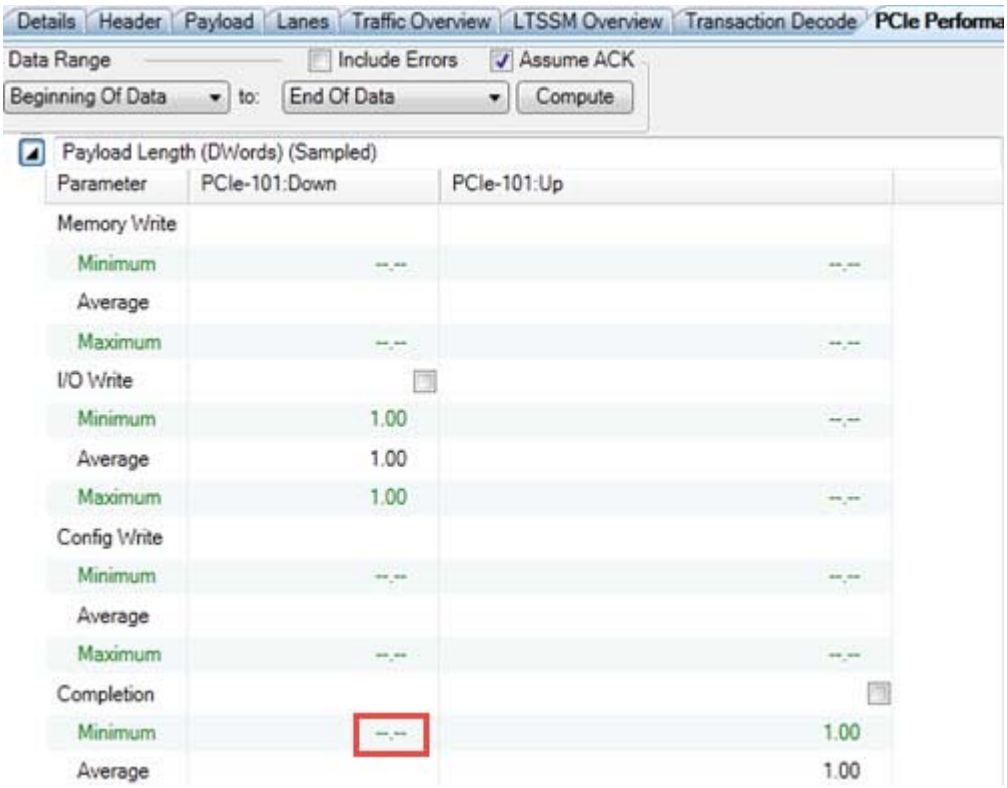
Some important points while viewing and interpreting performance summary:

- A --.-- value displayed in a statistics tree/table for a performance parameter indicates that the packet(s) required to generate that statistics is not found in the trace. It signifies 'no data' received for generating the statistics. Consequently, the chart corresponding to such a performance parameter contains no data and is therefore not displayed in the charts pane. Such a chart gets displayed only when the required packets are found while computing performance summary to generate data for the chart.



- For calculating the statistics for the **Completion** parameter, only *Completions with Data* packets are included. Any *Completions without Data packets* found in the trace are ignored for this parameter's statistics calculations.

  For instance, in the following screen, the *Completion with Data* packets are used for calculating the *minimum*, *maximum*, and *average* payload size for Completions. In the absence of *Completion with Data* packets in the trace, the *Completion* statistics is shown --.--.



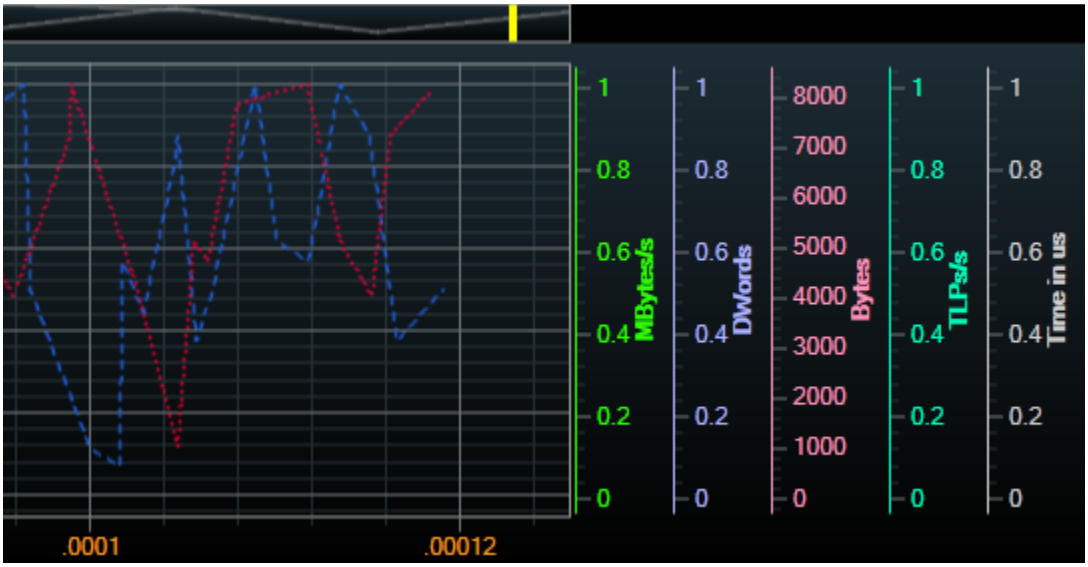
- Some performance parameters are displayed in blue color. This indicates that the navigation to the associated PCIe packet is applicable for that performance parameter. To know more, refer to "From the Performance Statistics pane" on page 156.

Charts pane

This pane displays charts for all the selected performance parameters listed in the statistics tree table.

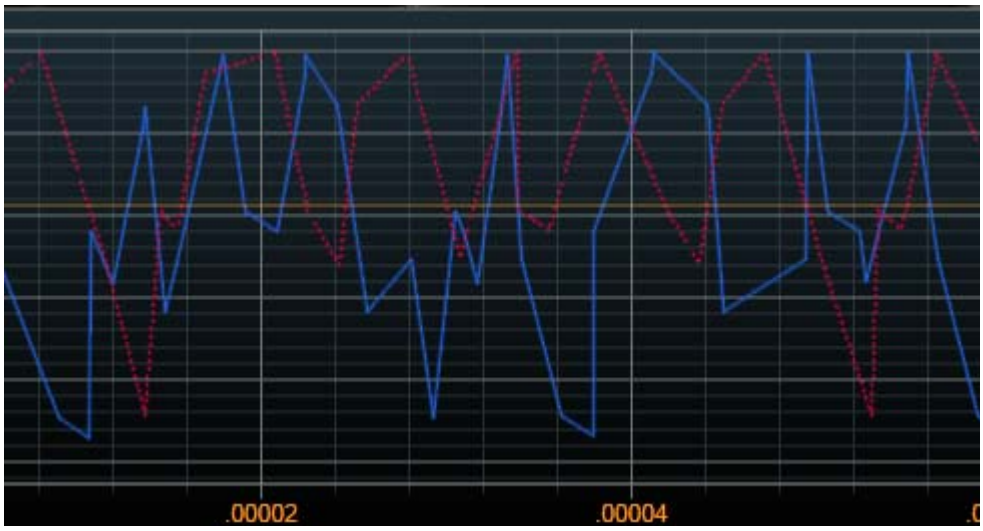
Viewing Multiple Y-axis in the Chart Pane

The chart pane displays multiple Y-axis if you select multiple Y-axis checkbox in the **Setup...** dialog box. To know more, see "Showing/Hiding multiple Y-axis" on page 138.



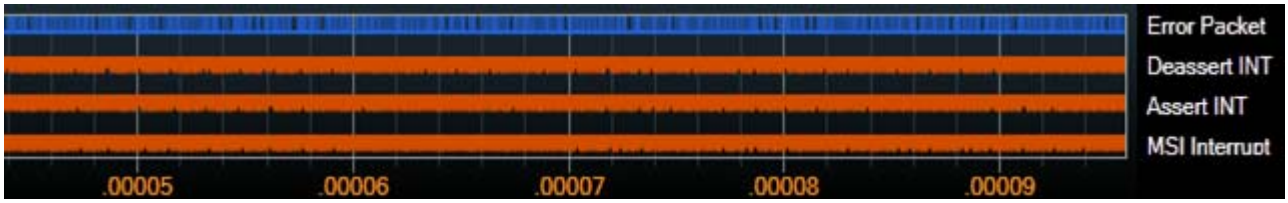
Viewing Overlay Charts and defining Color code for graphs

The Chart pane displays Overlay chart for selected performance parameters listed in the categories pane. You can define different color codes to display the performance data for downstream and upstream directions in charts. To accomplish this, click the **Setup...** button under the **Settings** section. Then, click the **Color** drop-down to select the color from the color palette. To know more, refer "Changing the color of the Graph Line" on page 141.



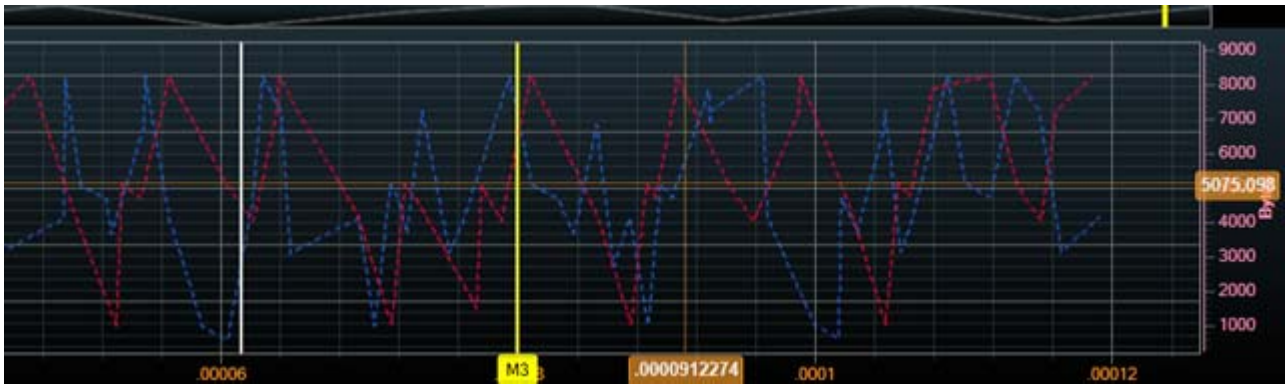
Viewing Band Chart

The lower section of the Chart pane displays the Band Chart. You can view MSI Write, Msg Assert_INT and Msg Deassert_INT and error packets in the Band chart area of the Chart pane.



Viewing X and Y axes values in a chart

Hovering the mouse over a chart location displays the applicable values of X-axis and Y-axis for that location.



Flow Control

Flow Control computes and displays the available flow control credits from the data trace that has a bidirectional traffic. It presents flow control statistics and graphs and helps in analyzing the flow of data. Flow control credit level is determined by the Writes and Completions in one direction and the UpdateFC packets in the other direction. The data series created for the flow control charts contain a point for every packet that is a part of that series. This is in contrast to all other charts which represent a group of packets in a sample period. Flow control credit levels are represented by UpdateFC series. The performance parameters for the Flow Control are explained below:

- **UpdateFC_P (Bytes)** - Shows the minimum, maximum, as well as average flow control credit levels for posted transactions.
- **UpdateFC_NP (Bytes)** - Shows the minimum, maximum, as well as average flow control credit levels for non-posted transactions.

- **UpdateFC_Cpl (Bytes)** - Shows the minimum, maximum, as well as average flow control credit levels for Completions data.
- **Memory Read (Bytes)** - Charts the size of Memory Read requests in each direction (X and Y axes).
- **Memory Write (Bytes)** - Maps the size of Memory Write and MsgD packets in each direction.
- **Memory_CplD (Bytes)** - Charts the size of Memory completion with data packets in each direction.
- **Inst. CplD and Inst. Write (Mbytes/s)** - The instantaneous completion with data (Inst. CplD) and instantaneous write (Inst. Write) show Instantaneous Bandwidth in each direction. Instantaneous Bandwidth is defined as the number of data bytes (in MegaBytes) in the packet divided by the time (in seconds) since the end of the previous data carrying packet to the end time of the current data carrying packet.

  Each packet carrying data is represented by a point in these series.
- **Interrupts**- Shows the location in the graph where MSI Write, Msg Assert_INT and Msg Deassert_INT occurred. This is displayed in the Band chart area of the chart pane.
- **Error Packet**- Shows the location in the graph where packets with any error occurred. This is displayed in the Band chart only when the Include Errors checkbox is enabled under Data Range heading.

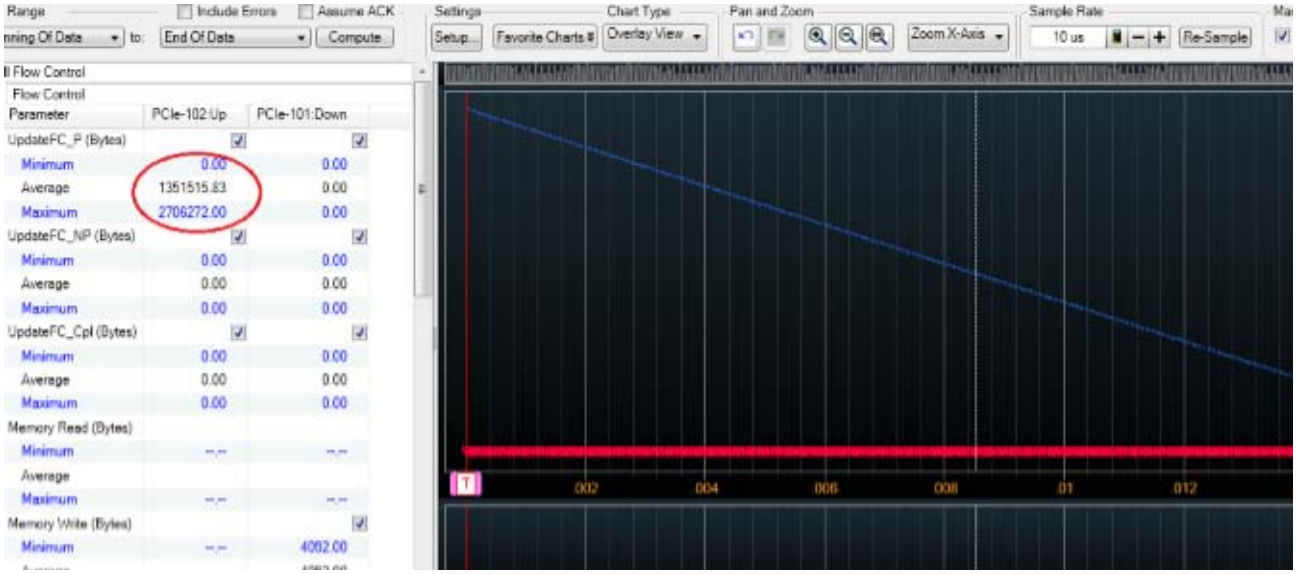
Flow Control- Examples

The following examples elaborate the usage of Flow Control feature:

Example-1

The flow control charts represent the computed flow control credit level, which is meant for how many bytes the receiver is ready to receive. When the data is sent in a higher volume than the receiving capacity of the receiver, there will be a continuous slow movement of data from transmitter to receiver. This sometimes also leads to data loss. In such scenarios, you can use the Flow Control feature to display the credit limits of the data to be sent and the data received by the receiver.

In this example, 4092B (1023 DW) packets of data are being sent in the downstream direction and the link partner is updating credits in increments of 4096B. In the following screen, a steep decline in the blue line clearly indicates the situation that FC credit is being updated at higher rate than the rate at which data is being posted. The blue line represents the computed UpdateFC_P regulating against the red line representing the corresponding Memory Write packets in the trace.

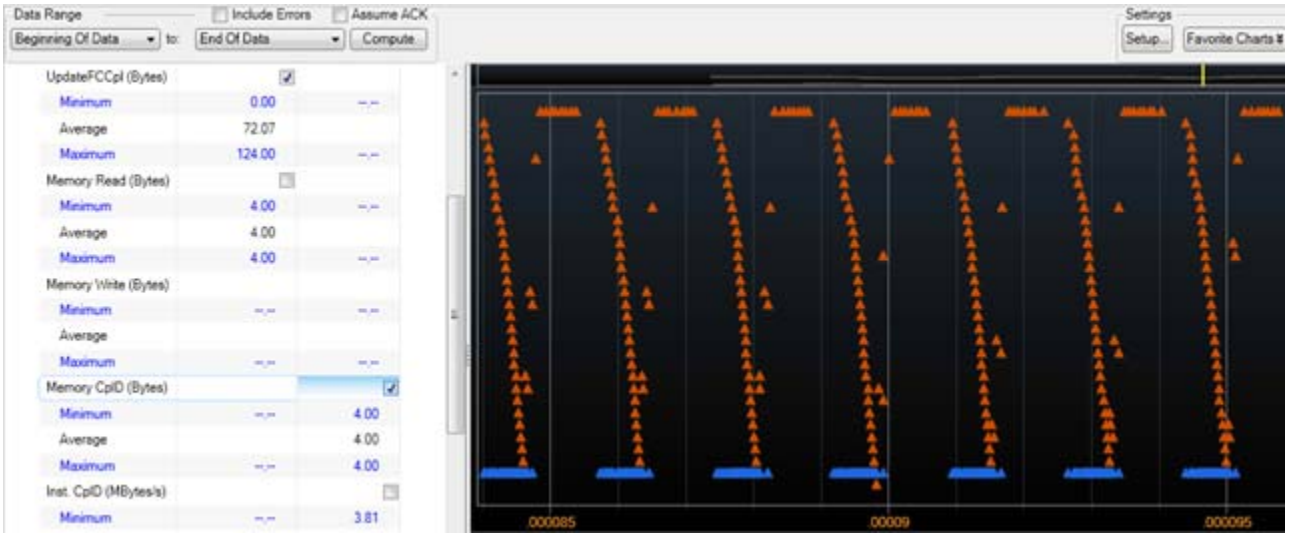


The UpdateFC_P Flow Control credit level is reduced by Memory Write packets coming from the root occurred in the trace. As displayed in the above graph, the Maximum is near the beginning of the trace and the Flow Control credit level continuously drops down and reaches zero on the right side of the trace.

This too many credits difference may indicate problem in the credit update behavior of the DUT.

Example-2

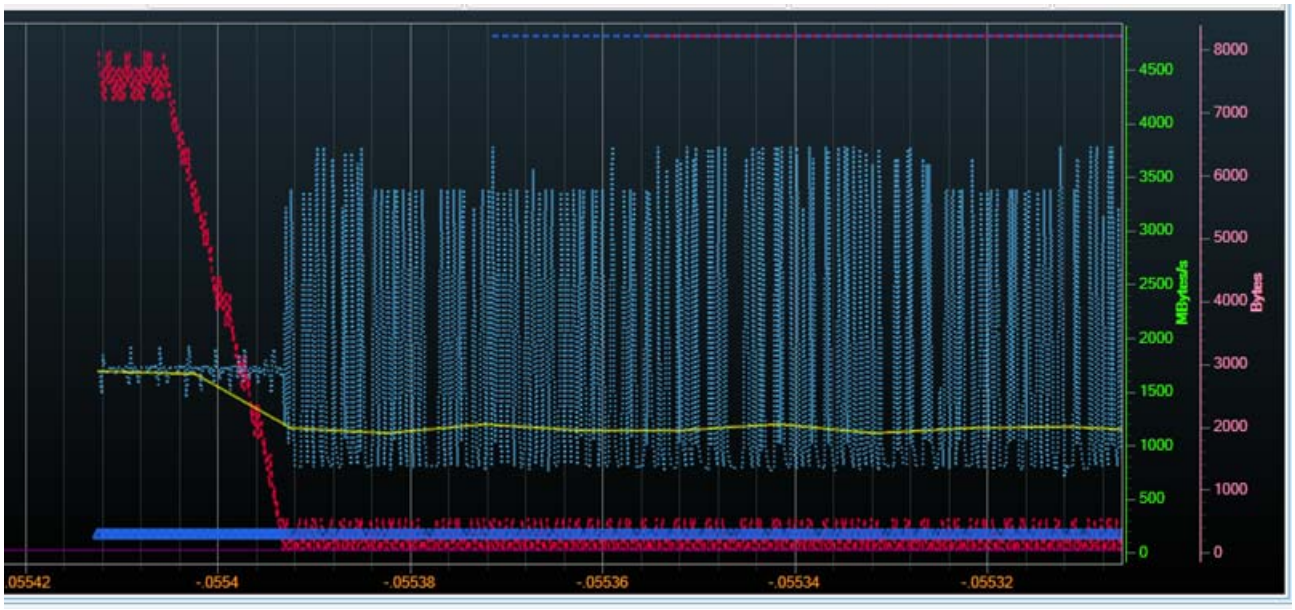
In the following screen, when memory completion data (Memory CplD) is being sent, the UpdateFC_Cpl performance parameter computes and displays minimum, maximum, as well as average flow control credit levels for Completions data. The blue and orange Pyramid Up chart line represents Memory CplD and UpdateFC_Cpl respectively. The UpdateFC_Cpl credit starts from an initial counter value and keeps on updating its credit limit till all the packets are sent and received.



As displayed in the above graph, the UpdateFC_Cpl graph line keeps showing the credit fluctuation regulating against the corresponding Memory Completion packets coming from root that occurred in the trace. The drop in credit level shows how many packets are left to be transmitted and helps in regulating the flow of data packets. When all packets are transmitted and received, the FC level changes to zero counter value. It remains constant till any further credits are added into account. Once the FC level is incremented with some value, the same mechanism is repeated till all the packets are transmitted and received and FC level again comes to a zero value.

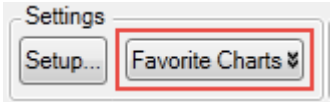
Example-3

In the start of the DMA buffer transfer, the link credits are quickly exhausted and reaches to zero counter value because the buffer transfer runs at a higher rate in comparison to the rest of the data transfer. The quick drop in credit level is caused by the chain of link buffering. In the start, the data write or completion capacity remains higher than the sink capacity but lower than the link capacity. The data transfer at higher rate only happens while the link buffering capacity can sustain it.



Saving the Favorite Overlay Chart

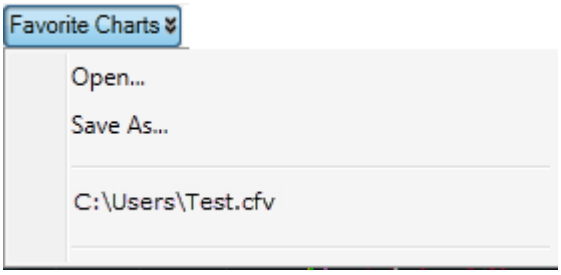
In the PCIe Performance Overview tab, the **Settings** section has a **Favorite Charts** button which allows you to save your favorite charts and open the previously saved overlay charts.



The overlay chart is saved along with all the settings that you made to the graph displayed in the chart pane of PCIe performance tab (such as selecting or deselecting various performance parameters in the Categories pane, zooming or panning the chart, making changes in the Setup dialog box etc.).

To save the Overlay Chart

1 Click **Favorite Charts** button> **Save as**.



2 In the Save As dialog box, specify the name of the chart. Ensure that ***.cfv** (Chart Favorite) option is selected as the file type.

3 Click **Save**.

To view previously saved Overlay chart

1 Click **Favorite Charts** button> **Open**.

2 In the Open dialog box, navigate to the *.cfv file name by which you saved the Overlay chart.

3 Click Open.

Navigating Through the Performance Summary Results

Navigating Through a Chart

By Using Pan option

To navigate through a chart horizontally, that is X-axis, click the **Pan X-Axis** button displayed at the top of the charts pane.

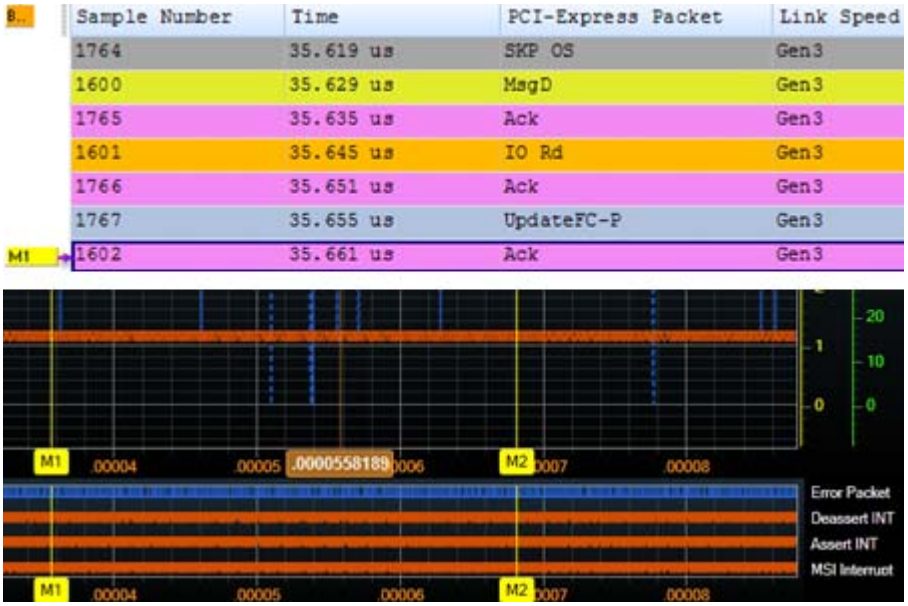
To navigate through a chart horizontally and vertically, that is both axis, click the **Pan Both Axis** button displayed at the top of the Charts pane. You can then drag the chart up, down, left, and right.

Navigating Between Performance Statistics and Associated PCIe Data

By placing markers in charts

You can place markers in charts and use these markers to navigate to the PCIe packet associated with the chart location at which you placed a marker. Markers placed in charts are correlated to markers displayed in the trace data in the upper pane of the Protocol Viewer.

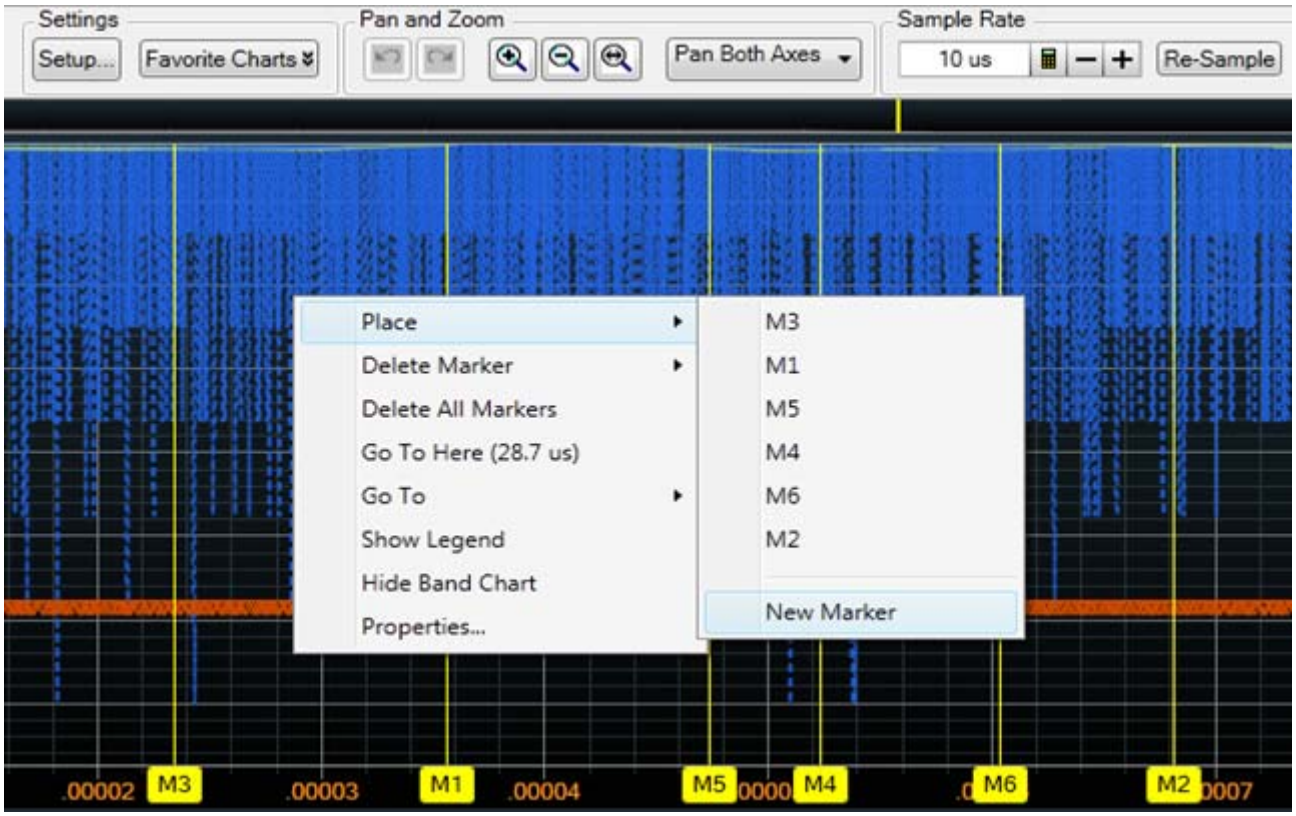
This type of navigation is particularly useful when you notice a sudden variation in a chart and want to navigate to the exact trace position that corresponds to that chart location.



To place a marker in charts

1 Double-click the location in the chart at which you want to place a marker. A new marker is added to that chart location and the corresponding trace location in the upper pane (trace view).

Alternatively, right-click the chart location where you want to place a marker. Then select **Place** > **New Marker** or select an existing marker to place that marker at the current location.

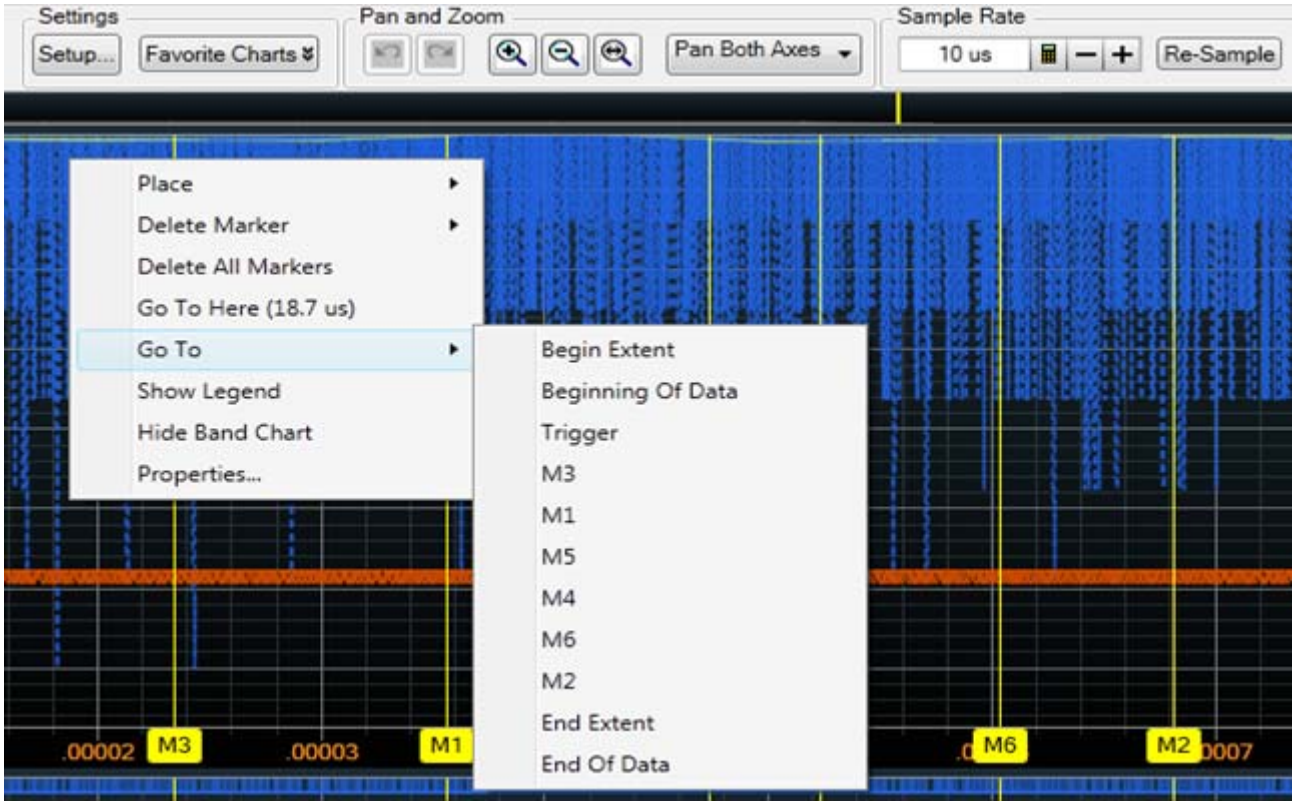


To navigate to a particular marker placed in charts

In situations when you have placed multiple markers in charts, you may want to navigate to a particular marker and its associated trace position in the upper pane. To do so, right-click anywhere in a chart, select **Go To** and then select the marker to which you want to navigate.

On doing so, the chart display moves to the point at which the selected marker is located. Also, the trace position corresponding to the selected marker is highlighted in the upper pane.

NOTE If the markers are not displayed in charts, click the Show Markers button at the top of the charts pane.



By using Extent Markers

When you pan/zoom a defined area in charts, Extent Markers are automatically placed at the beginning and end of this defined pan/zoom extent in charts. On changing the pan/zoom area, these markers are automatically moved. There may be situations when you zoom a specific area in charts and then want to navigate to the PCIe data associated with the chart's zoomed area in a Waveform Viewer or a Listing. To accomplish this, you can navigate using Extent Markers.

To navigate using Extent markers:

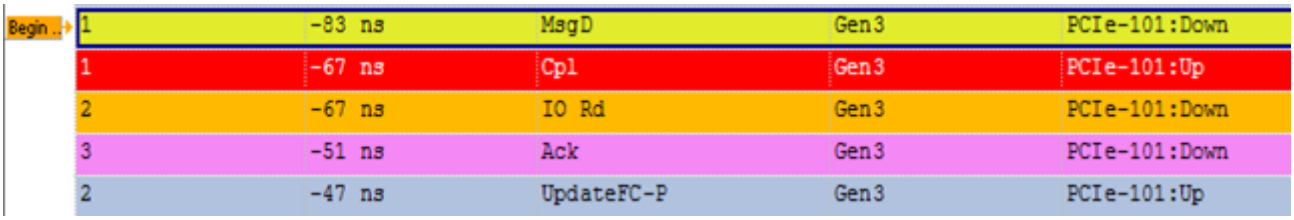
1 Right-click anywhere in the zoomed area in a chart and select **Go To**.

2 Then select **Begin Extent** or **End Extent** to navigate to the PCIe data associated with the beginning or end of the zoomed area.

The applicable PCIe data is highlighted in the upper pane of Protocol Viewer as well as in Waveform and Listing viewers.

NOTE

If the Extent Markers are not visible, then click the **Extent Markers** button at the top of the charts panes to display these markers in trace view as well as other viewers in Logic and Protocol Analyzer application.

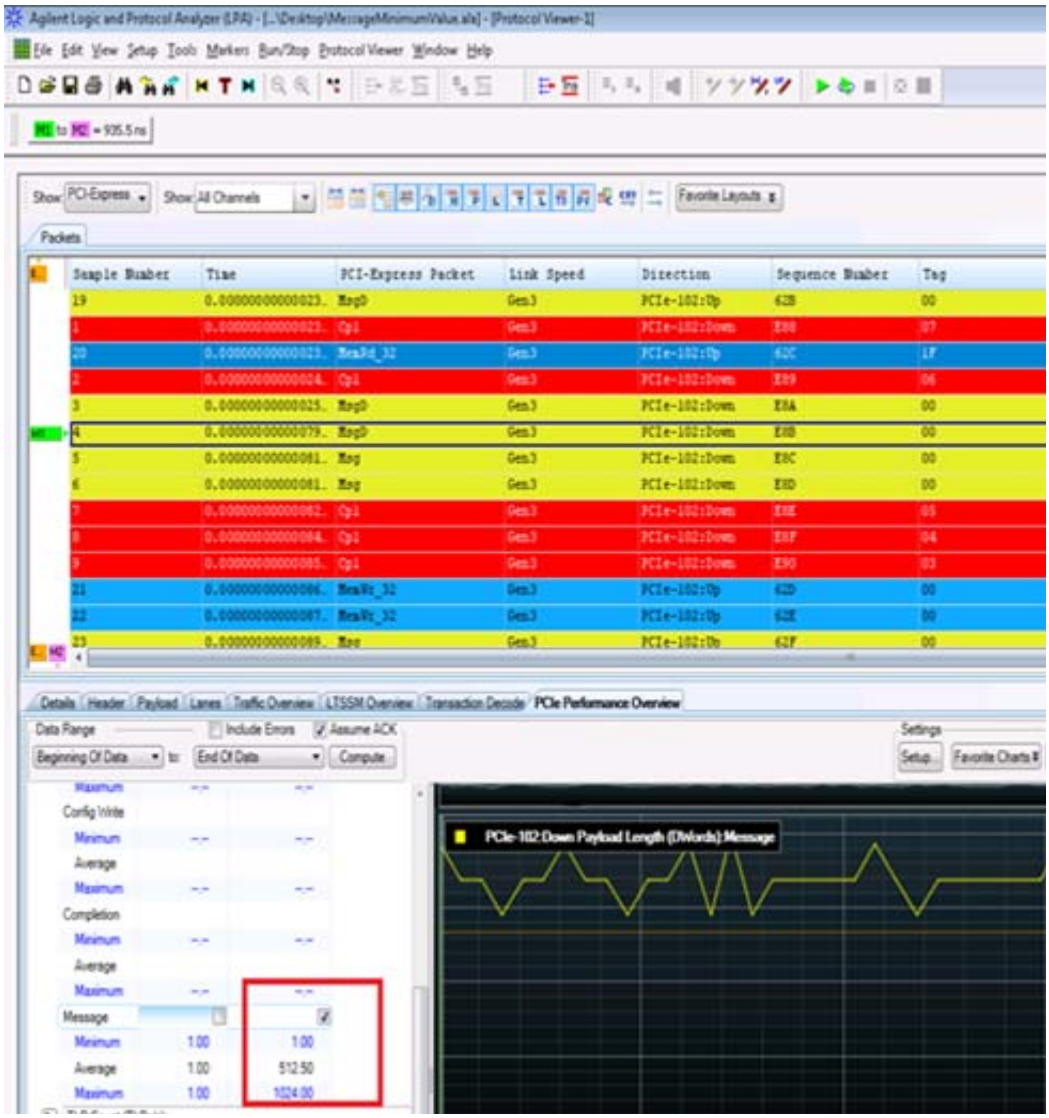


From the Performance Statistics pane

For some performance parameters such as **Minimum** and **Maximum**, it is possible to navigate directly to the PCIe packet that accounted for the generation of a particular statistical value of that performance parameter.

Such performance parameters for which navigation to the PCIe packet is applicable are displayed in blue color.

In the following screen the “Message” parameter in the downstream direction has a Min of 1.0 and Max of 1024 displayed in blue color. Clicking these numbers, navigate you to MsgD packets with lengths of 1 and 1024 (DWords) that is accounted for the minimum and maximum value respectively in the upper pane.



NOTE The chart pane does not show the exact value of the data packets as displayed in the upper pane of the Protocol Viewer window. This is because the chart pane displays the graph of sampled series that represents an average value of all the packets transmitted during a particular micro second as defined in the sample rate field.

Customizing Charts

Changing the Sampling Rate and Re-sampling the Chart

Sampling is a process by which captured data trace is sampled on the basis of specified time period to create charts. The trace data is sampled to compute statistics from these samples for charts generation. This sampling is done as per the *Sample Rate* set for charts. By default, the sample rate is set to 10 microseconds. You can change this sample rate and can re-sample the data trace by specifying time slices. By resampling the data you can regenerate charts based on the changed sampling rate.

To change the sample rate of charts

1 Access the **PCIe Performance Overview** tab.

2 Click the  button displayed with the **Sample Rate** field in the Charts pane on the right.

3 In the **Time** dialog box, specify the value and unit for the sample rate. The permissible range for sample rate is 1 us to 100 ms.

4 Click **OK**.

To regenerate charts based on the new sample rate

1 Click the **Re-Sample** button displayed with the **Sample Rate** field at the top of the Charts pane.

NOTE Sampling is done on the basis of specified time period defined as per the sample rate. It is not applicable for Flow Control category because Flow Control statistics is not time dependent and is based on the flow control credits of the data transmitted and received, The series listed under the Flow Control category have packet granularity whereas sampling is significant for all other categories listed in the Statistics tree/table of the PCIe Performance Overview tab.

When you capture a data trace and sample it at defined sample rate to generate charts, there may be repeated scenarios when no message packets are received during a particular slice of time while sampling the entire trace. Such scenarios are represented in the graph by plotting glyphs at zero entry. The glyphs plotted at zero, which you see in the chart, signifies no data packet received at that time.

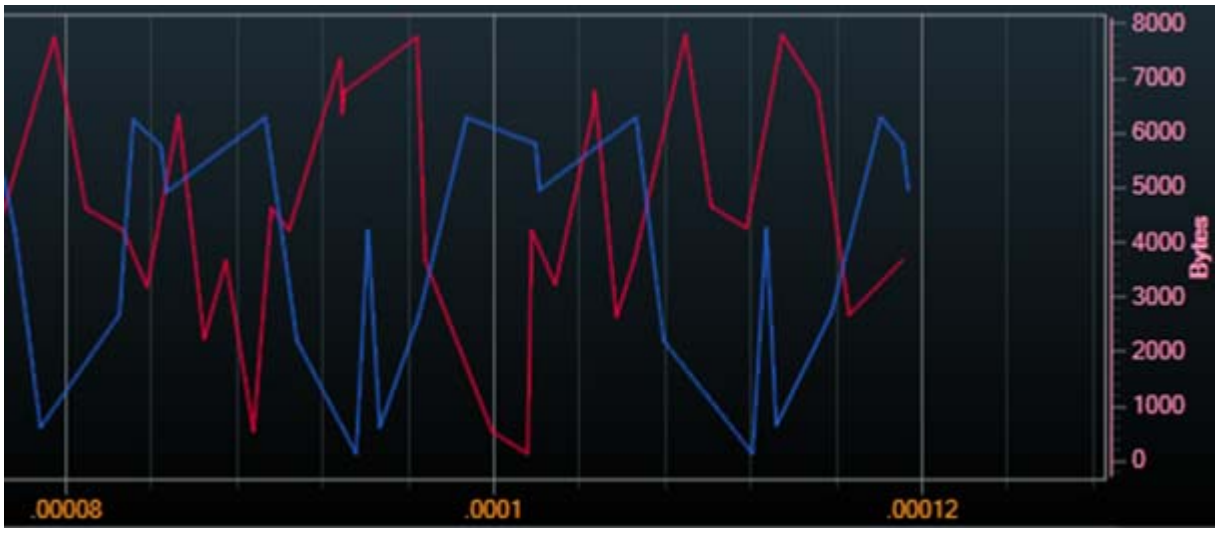
NOTE Message packet displaying a zero/hyphen value in the chart does not mean it has zero value, rather it means no relevant data received at that time.

Changing the Chart Display

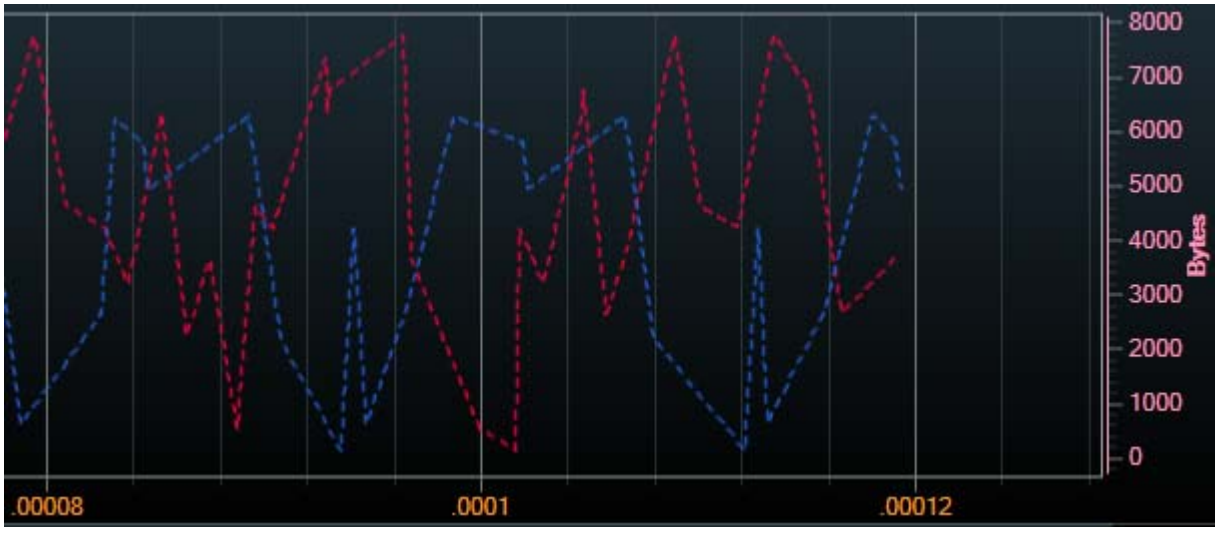
You can change how data is presented in a performance chart. To know, how to change the chart display, see "Changing the appearance of the graph" on page 141.

By default, data is presented as Dash Line chart type. The following chart type options are available.

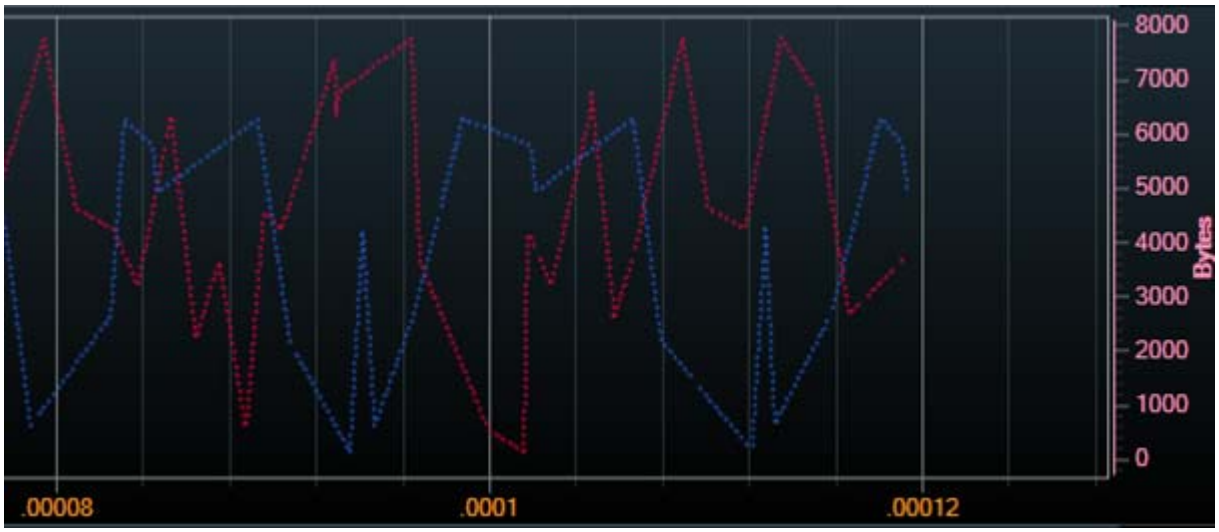
- Line -



- Dash Line-

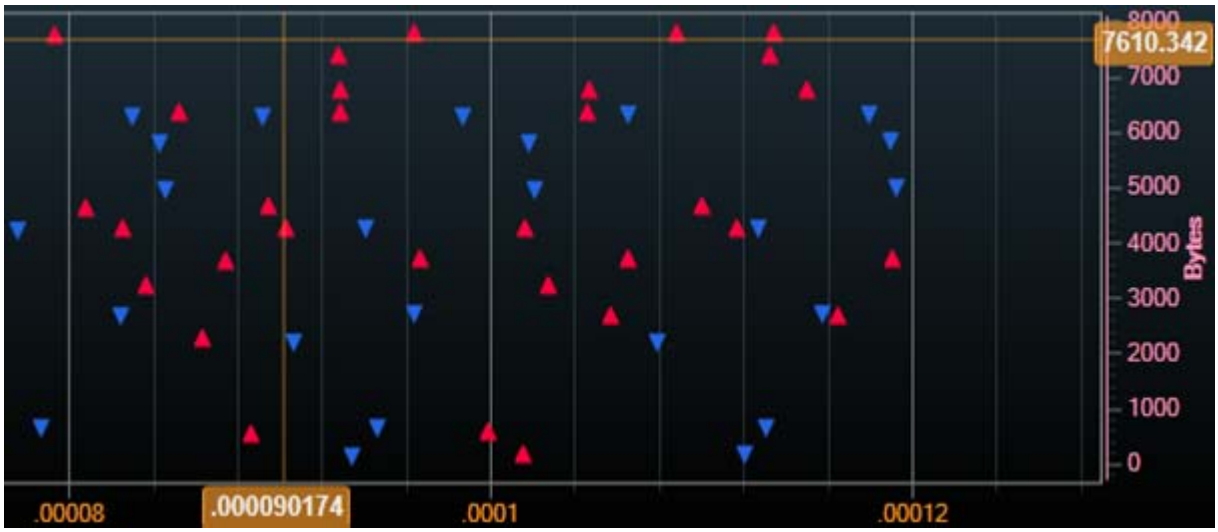


- Dot Line -

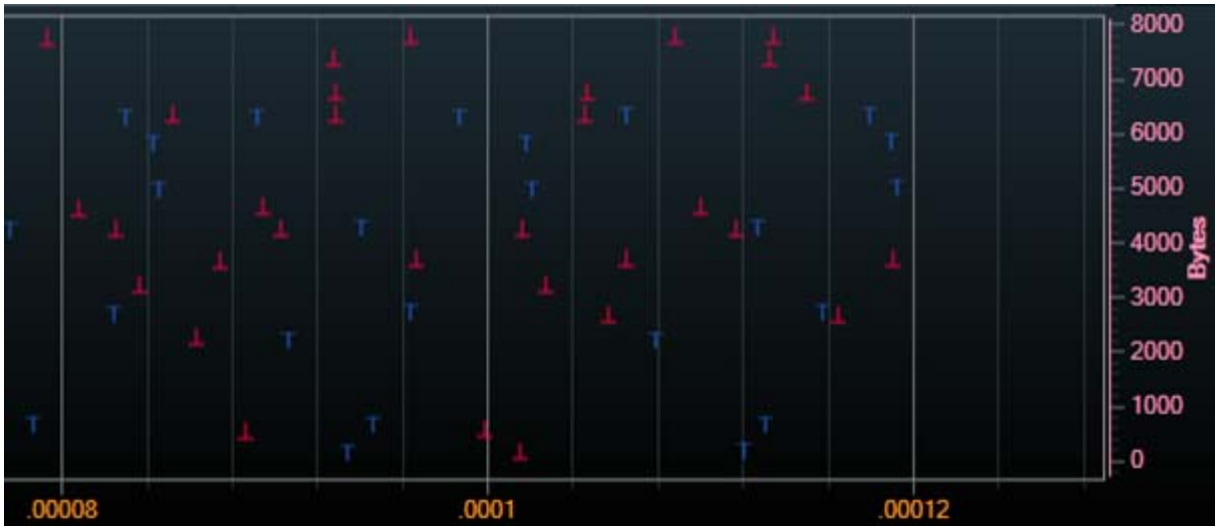


- Triangle Up/Down -

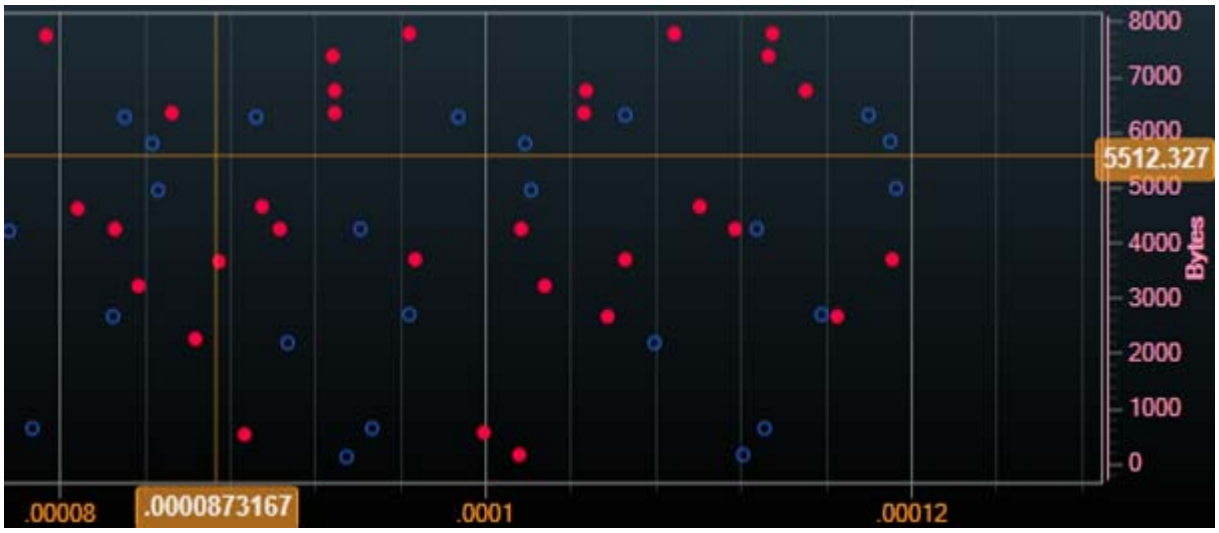
- Pyramid Up/Down -



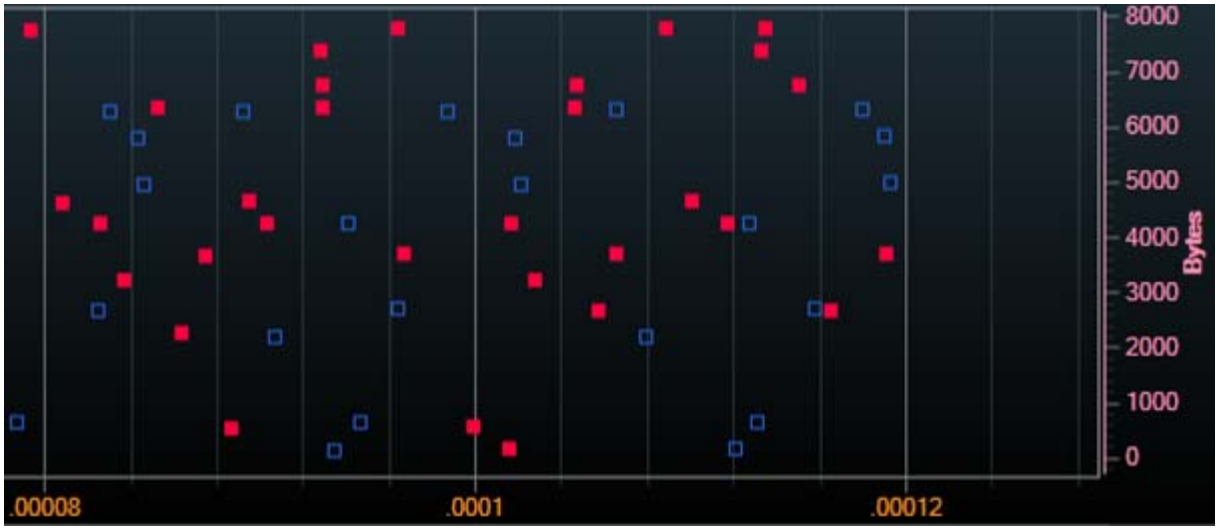
- Perpendicular Up/Down-



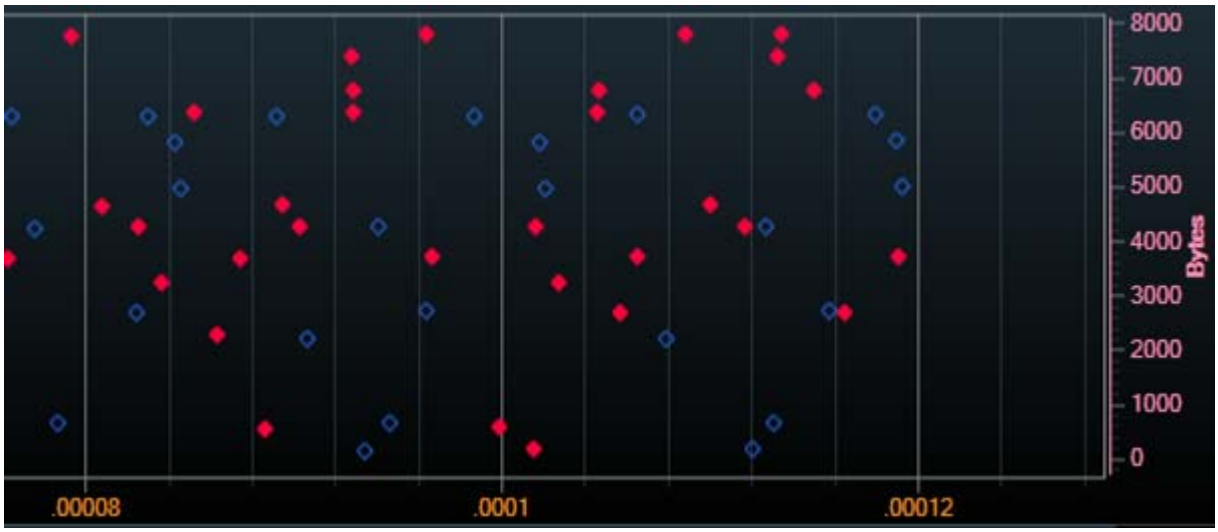
- Dot/Circle -



- Box/Square -



- Diamond/Filled Diamond -



To change chart type for a performance chart

Click the drop-down in the **Type** column from the **Setup...** dialog box and select the type you want to change with.

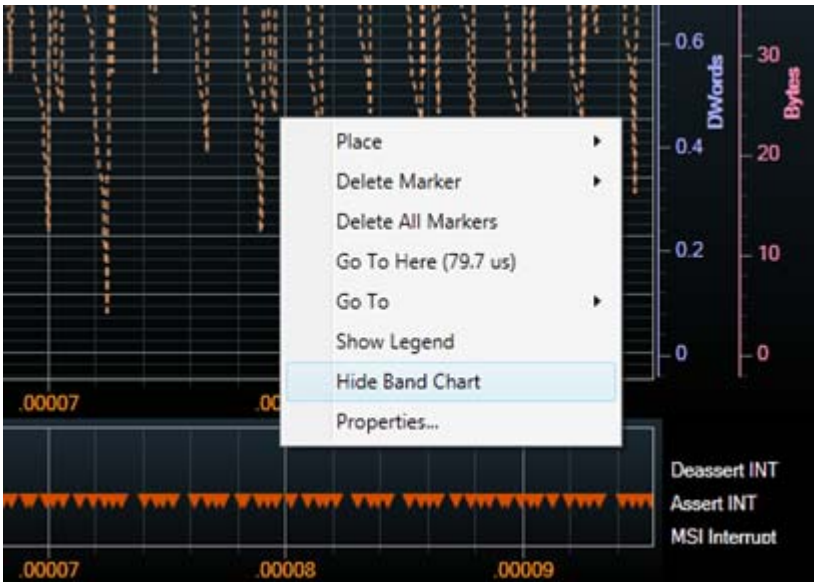
The chart is displayed as per the changed chart type.

Showing/Hiding the Band Chart

You can show or hide the Band Chart displayed in the lower pane of the chart area.

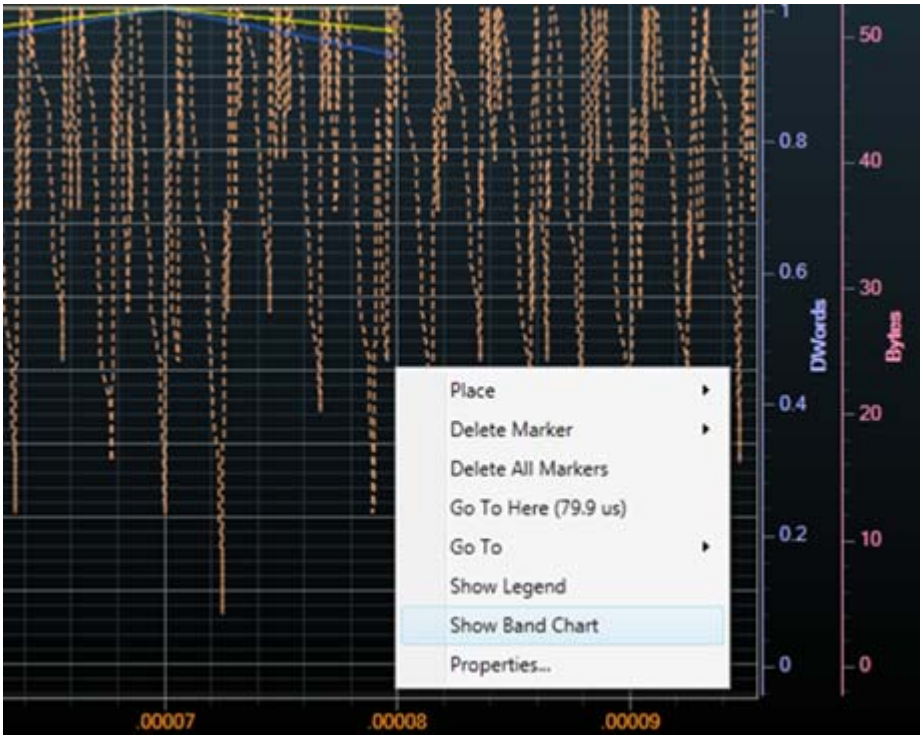
To hide the Band Chart

Right-click anywhere in the chart location and then select **Hide Band Chart**.



To show the Band Chart

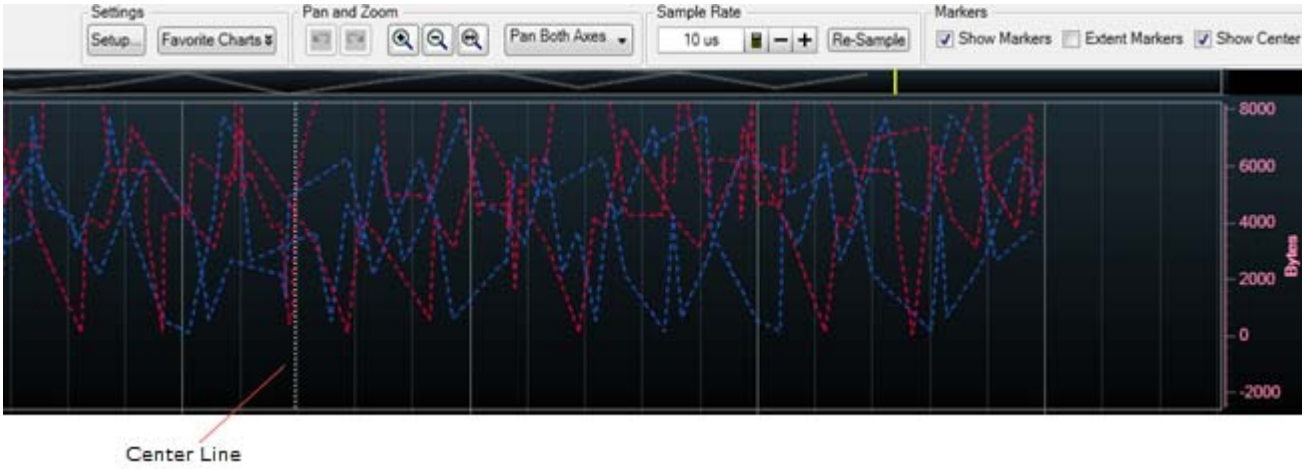
Right-click anywhere in the chart location and then select **Show Band Chart**.



Viewing the Center of the Chart

If the captured PCie traffic is too large and defined pan/zoom extent in the overlay chart is outsized, there may be situations when you want to view where the center of the chart's zoomed area lies. You can do so by using **Show Center** check-box.

To view the center of the chart's zoomed area, click the checkbox **Show Center**. Selecting this checkbox displays a white colored vertical dotted line at the center of the Overlay Chart. It makes the center of the chart apparent as displayed in the following screen:

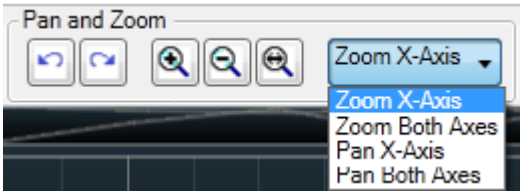


Zooming In/Out Charts

You can zoom in or zoom out a defined area in the chart or the complete chart.

To zoom X-Axis for a defined area in the chart

1 Click the **Zoom X-Axis** option from the combo box displayed in the **Pan and Zoom** section of the charts pane to make it active.

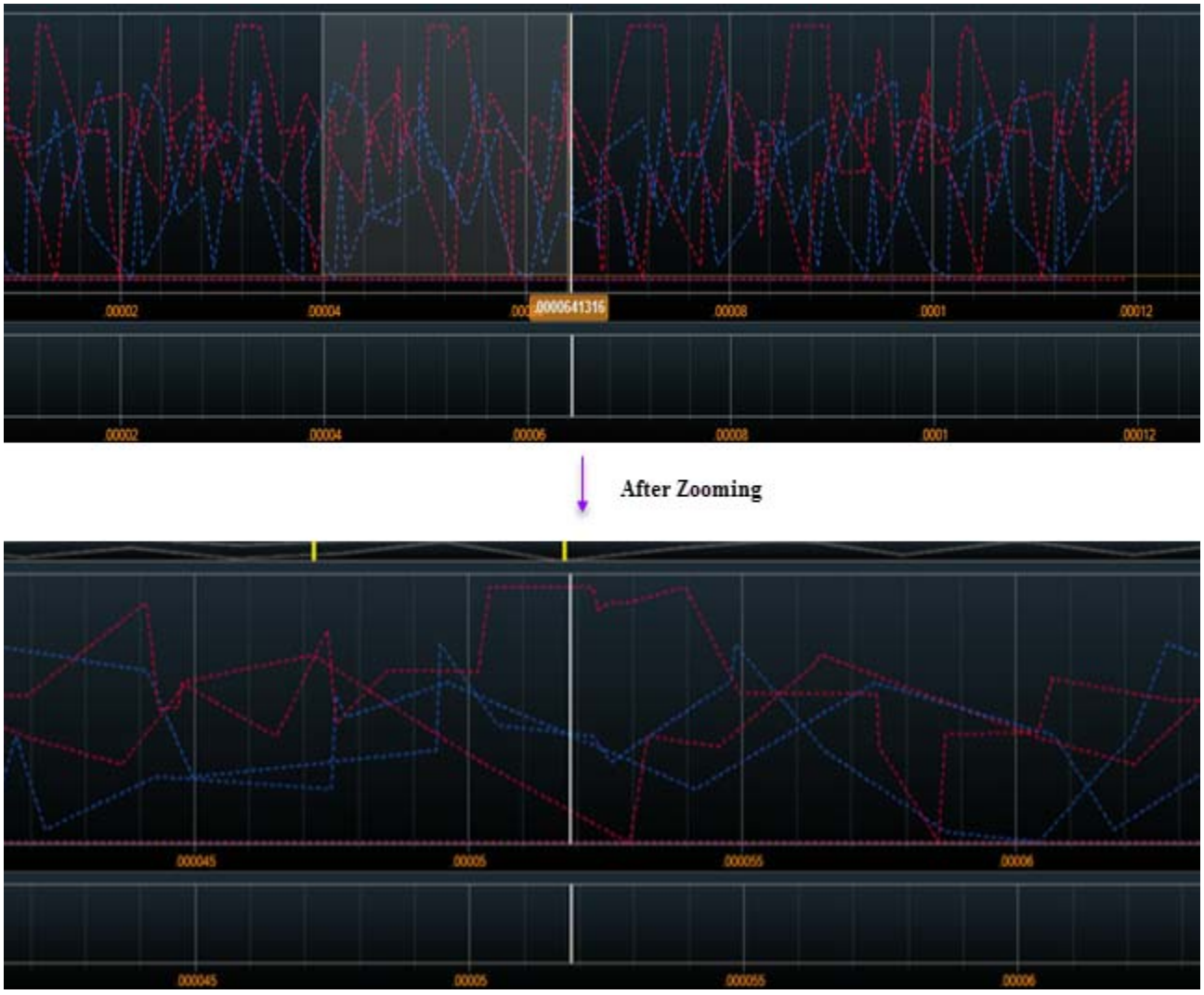


2 Move the mouse pointer to the chart location from which you want to begin zooming.

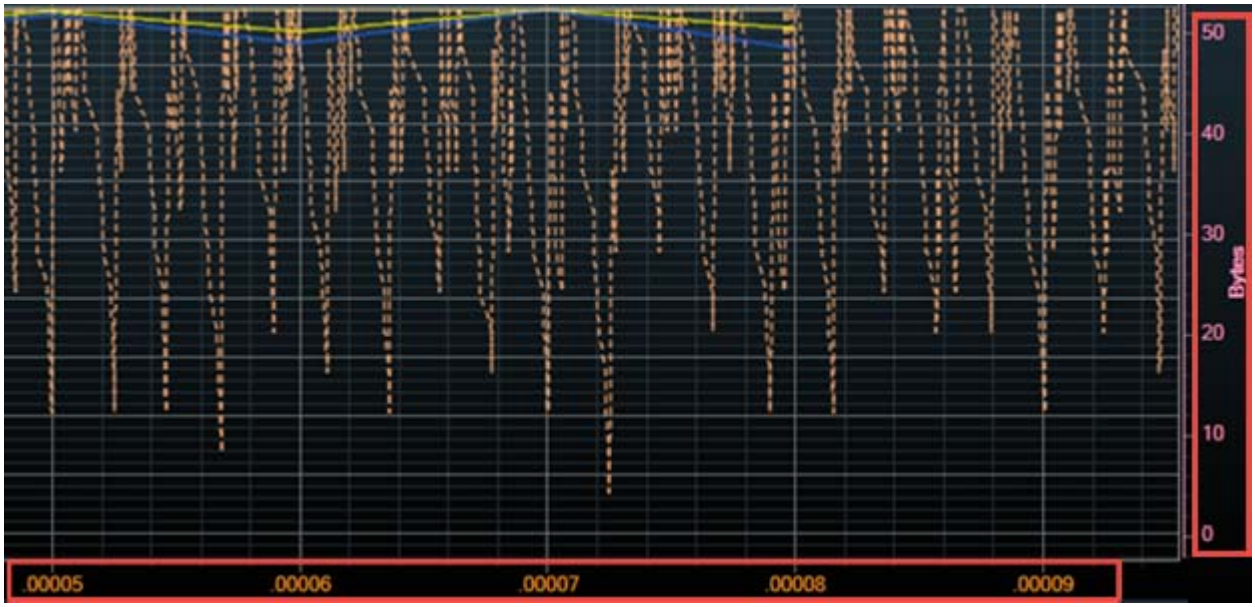
3 Left-click at this location and while keeping the left mouse button pressed, drag the mouse to the chart location till which you want to

zoom the display. As you move the mouse, the zooming extent is defined in chart and highlighted with grey.

When you release the left mouse button, the defined X-axis area is zoomed for all the displayed charts. Following screen displays the chart before and after zooming in Overlay view:



Similarly, you can zoom both X and Y axes of the defined area in the chart by selecting the **Zoom Both Axes** option from the combo box displayed in the **Pan and Zoom** section of the performance charts pane.



NOTE The X-axis zoom applies to all the displayed charts where as the Y-axis zoom (in both axis zoom) applies only to the chart in which you define the area to zoom.

You can also zoom in or zoom out complete charts. To do this, use the following buttons in the **Pan and Zoom** section of the charts pane.

- - **Zoom In** magnifies the center 50% of the chart to the full width of the chart.
- - **Zoom Out** doubles the time displayed in the full width of the chart.
- - **Zoom Out Full** displays the entire range of Computed data across the full width of the chart.

NOTE You can undo and redo zooms by clicking the and buttons in the **Pan and Zoom** section of the charts pane.

Glossary

D

DUT Device Under Test.

I

interposer Describes a probing method where the probe is located between a slot and the PCI Express device under test.

M

midbus probe Describes a probing method where Soft Touch footprints are designed into a DUT board between the controller and the device under test.

13 Glossary

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U

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Z