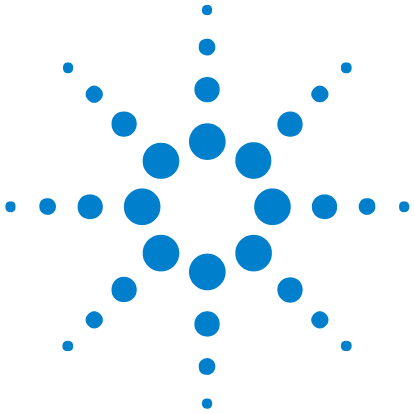

U4301A PCIe Gen3 Analyzer

User Guide

Agilent Technologies

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U4301A PCIe Gen3 Analyzer—At a Glance

The U4301A PCIe Gen3 analyzer lets you capture and decode PCI Express 3.0 (PCIe 3.0) data and view it in a Packet Viewer/Protocol Viewer window. The protocol analyzer supports all PCIe 3.0 speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3), and it supports link widths from x1 to x16.

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2 slot chassis).

When a controller PC is connected to an Agilent Digital Test Console chassis via an external PCIe interface and cable, the *Agilent Logic Analyzer* application (running on the controller PC) lets you connect to the chassis, set up U4301A PCIe Gen3 analyzer data captures, and perform analysis.

The U4301A PCIe Gen3 analyzer provides:

Effective presentation of protocol interactions from physical layer to transaction layer:

- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction.
  - Easy flow columns to better understand the stimulus and response nature of the protocols.
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally.
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for Link Training debug, Config accesses, and general I/O.

Simple and powerful state-based triggering:

- New simple trigger mode makes it easy to setup single event triggers.
- Powerful state-based triggering including:
  - Four states supported in trigger sequencer.
  - Triggering on patterns (ordered set patterns or packet types).
  - Internal counters and timers.
  - Triggering on an ordered set on a specific lane.
- External trigger in/out.

Powerful hardware features ensure capture of important transition events:

- Dual phase lock loops (PLLs) per direction ensuring that the analyzer will lock on speed change events quickly and not miss any critical data.
- Large 4 GB of capture buffer per module (up to 8 GB of capture for x16 analyzer), for long recording sessions.

- PCIe Gen1 x4 link to the host PC, provides up to 10 Gbps of data download.
- LEDs to show lane status and speed for fast understanding of current link status.

See • "Using the PCIe Gen3 Analyzer" on page 5

Using the PCIe Gen3 Analyzer

For an overview and list of features, see: "U4301A PCIe Gen3 Analyzer–At a Glance" on page 3

- Chapter 1, “Hardware and Software Installation,” starting on page 9
- Chapter 2, “Probing Options for PCIe Gen3,” starting on page 11
- Chapter 3, “Specifying the Connection Setup,” starting on page 13
- Chapter 4, “Setting the Capture Options,” starting on page 27
- Chapter 5, “Tuning the Analyzer for a Specific DUT,” starting on page 31
- Chapter 7, “Setting Up Triggers,” starting on page 51
- Chapter 8, “Running/Stopping Captures,” starting on page 61
- Chapter 9, “Viewing PCIe Gen3 Packets,” starting on page 63

See Also

- U4305 PCIe Gen3 exerciser documentation.

Contents

1 Hardware and Software Installation

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2-slot chassis).

The Agilent chassis is connected to a controller PC via a PCI Express interface and cable.

The controller PC runs the *Agilent Logic Analyzer* application software which lets you set up the U4301A PCIe Gen3 analyzer, specify triggers and other data capture options, capture data, and analyze the captured data using Packet Viewer/Protocol Viewer windows.

See the *"Agilent Digital Test Console Installation Guide"* for information on:

- Installing the U4301A PCIe Gen3 analyzer blade into a Digital Test Console chassis.
- Connecting the Digital Test Console chassis to a controller PC via the PCI Express Gen1 x4 interface.
- Installing the *Agilent Logic Analyzer* software on the controller PC.

See the "*Agilent AXIe based Logic Analysis and Protocol Test Modules Installation Guide*" for information on:

- Installing the U4301A PCIe Gen3 analyzer module into an Agilent AXIe chassis.
- Connecting the AXIe chassis to a controller PC via the PCI Express interface.
- Installing the Agilent Logic Analyzer software on the controller PC.

2 Probing Options for PCIe Gen3

The currently available options for probing a PCIe Gen3 device under test (DUT) are:

- U4321A solid slot interposer
- U4322A midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

Details about these two probing options (and other PCIe Gen3 tools) can be found in the *"PCI Express Gen3 Hardware and Probing Guide"*.

3 Specifying the Connection Setup

Once you have connected the U4301A module, probing hardware, and DUT in the required configuration based on your probing requirements, the next step is to configure the connection setup for the U4301A module in the Agilent Logic Analyzer application. You use the Connection Setup tab of the analyzer's Setup dialog to configure the connection setup.

The connection setup details that you specify in this tab tells the Logic Analyzer software how the U4301A module is connected to the DUT in terms such as the probing option used, the direction of data capture (upstream, downstream, or bidirectional), and the link width needed. For instance, if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the Footprint option, 1 Bidirectional upto x8 as the Link type, and x8 as the Link Width in the Connection Setup tab to reflect the hardware setup that you have configured.

NOTE

- For details on how to set up the hardware and probing connections between the U4301A module and DUT, refer to PCI Express Gen3 Hardware and Probing Guide.
- For details on how to set up the chassis, U4301A module, and host PC, refer to the AXIe based Logic Analysis and Protocol Test Modules Installation Guide.

These guides are installed with the Logic Analyzer software and can also be downloaded from www.agilent.com.

Probing options

While specifying the connection setup, one of the key requirements is to select the probing option that you have used with the U4301A module to probe the DUT and the data capture direction in which you have configured the hardware setup.

Broadly, there are the following four probing options available with the U4301A module:

- U4321A Solid Slot Interposer card
- U4322A Soft Touch Midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

- PCIe Gen2 probes with the U4317A adapter. This adapter is used for conversion between the PCIe Gen2 probes and U4301A PCIe Gen3 Analyzer module. The PCIe Gen2 probes supported are:
  - N5315A Solid Slot Interposer for PCIe Gen2
  - N4241A straight, N4242A swizzled, and N4243A split cable Soft Touch Midbus 2.0 probe for PCIe Gen2
  - N5328A Half Size Midbus probe
  - N4241F/Z Flying Lead probe for PCIe Gen2

For each of the above four probing types, different options are available in the Connection Setup tab reflecting the data direction (upstream, downstream, or bidirectional). Upstream is the data direction towards the root complex. Downstream is the data direction away from the root complex. Based on your probing setup and the data capture direction in which you have configured the hardware setup, you need to select an appropriate probing option in the Connection Setup tab.

U4321A Solid Slot Interposer Card

When used with a U4321A solid slot interposer card, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way.

If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and a U4321A SSI card. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select U4321A Slot Interposer Upstream as the probing option for one of the U4301A modules and U4321A Slot Interposer Downstream as the probing option for the other U4301A module.

if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the probing option.

U4322A Soft Touch Midbus 3.0 probe

The U4322A midbus 3.0 probes require footprints to be designed into the device under test. Each probe requires its own footprint, and there are basically two variations:

- **Bidirectional** – where half the footprint pins are for the upstream data and the other half are for the downstream data.
- **Unidirectional** – where all the pins on the footprint are for the data going in the same direction.

Reversed refers to optional lane reversal which is supported for upstream ports.

Based on how you have designed the footprint for the probe, you need to select an appropriate probing option in the Connection Setup tab. For instance, if you have configured a x4 bidirectional setup using a U4322A midbus probe, then you need to select U4322A Bidirectional Full as the Footprint, 1 Bidirectional upto x8 as the Link type, and x4 as the Link Width in the Connection Setup tab.

U4324A PCIe Gen 3 Flying Lead probe

When used with a U4324A Flying Lead probe, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way. For x1-x8 bidirectional link type, you can use the U4324A Flying Lead probes in a straight or a swizzled configuration.

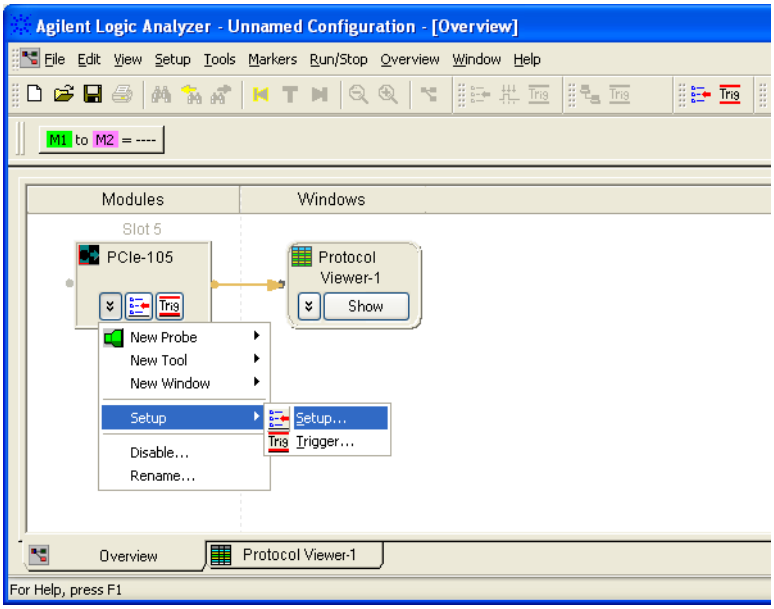
If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and eight U4324A Flying Lead probes. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select the U4324A Flying Lead Probe as the probing option and Unidirectional as the link type for both the U4301A modules.

If you have connected the U4324A Flying Lead probes in a x1 to x8 bidirectional straight setup, then you need to select the U4324A Flying Lead Probe as the probing option and Bidirectional as the link type.

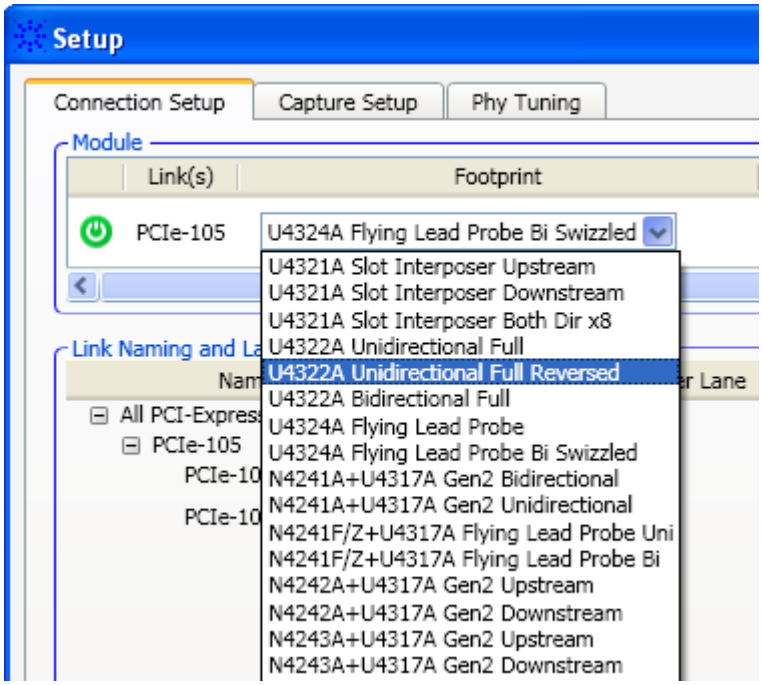
If you have set up a swizzled x1 to x8 bidirectional configuration using the U4324A Flying Lead probes, then you need to select the U4324A Flying Lead Probe Bi Swizzled as the probing option and Bidirectional as the link type.

To specify the connection setup

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Setup...**.

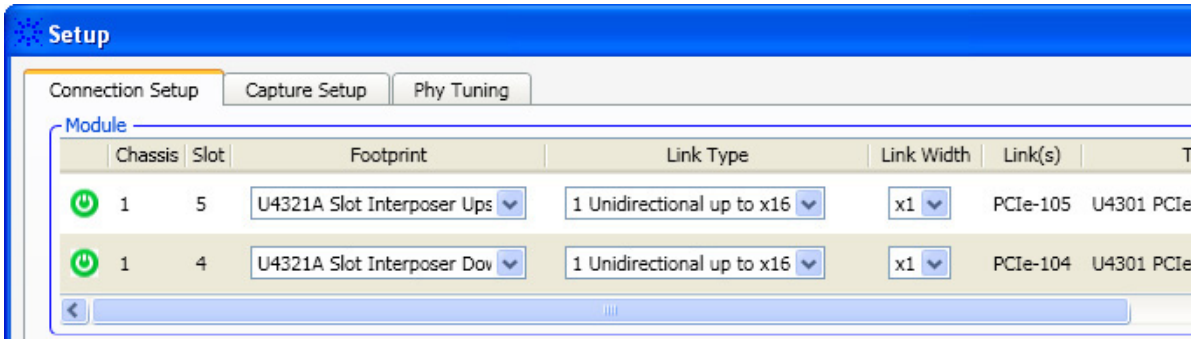


2 From the **Footprint** listbox, select the type of probing that you have set up between the U4301A Analyzer module and DUT. For each of the supported four probing types, different probing options are available in the Footprints listbox based on the data direction (upstream, downstream, or bidirectional). Based on your probing setup and the link type needed, select an appropriate probing option from the Footprint listbox. Refer to the "Probing options" on page 13 to know more about these options.

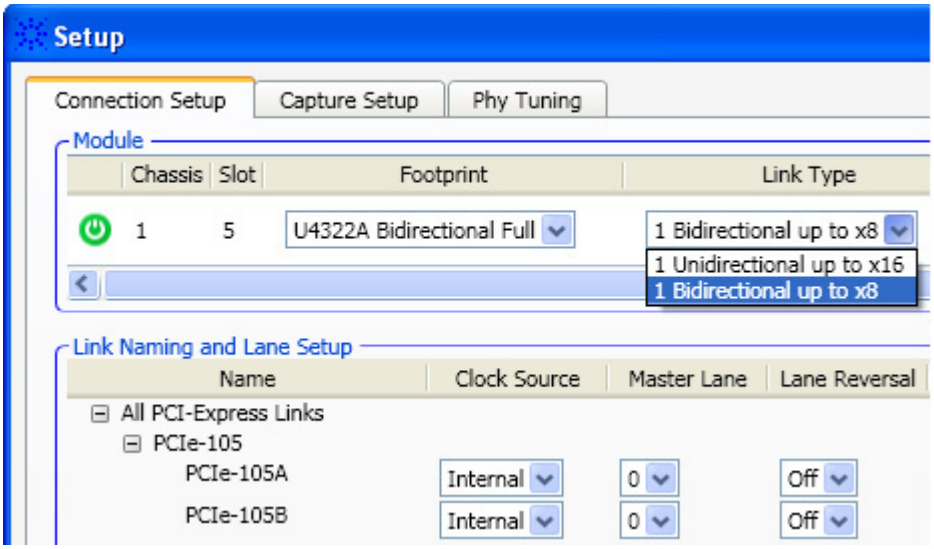


For more information on probing setups, click **Connection diagram...** or refer to the *"PCI Express Gen3 Hardware and Probing Guide"*.

If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the probing option individually for these modules.

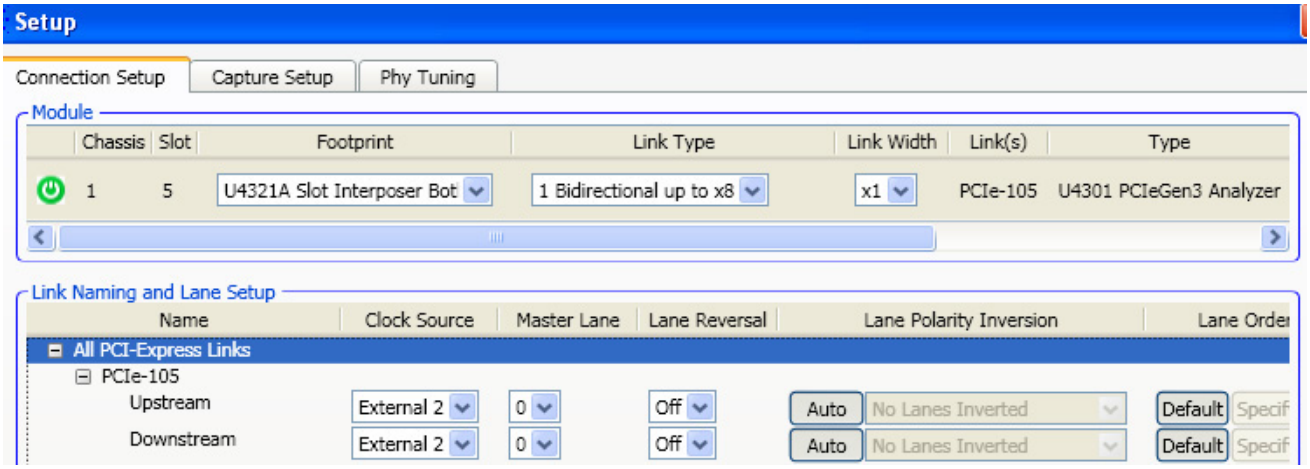


3 Specify the link type.



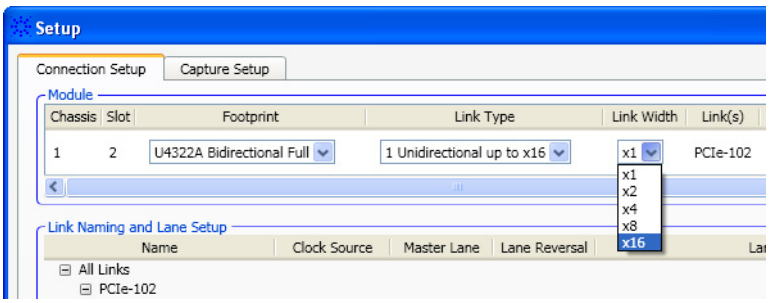
The **Link Type** refers to the type of link that you want to create between the U4301A module and DUT. You can select the **1 Unidirectional up to x16** link type if you want the U4301A module to probe and capture data in only one direction (upstream or downstream). In the Unidirectional link type, the U4301A module can support a unidirectional link with upto 16 channels in the same direction. You can select the **1 Bidirectional up to x8** link type if you want the same U4301A module to probe and capture data in both directions (upstream as well as downstream). In the bidirectional link type, the U4301A module can support one bidirectional link with upto eight channels for each direction. When you select the bidirectional link type, two sub-links are created for the two directions. You can set the link attributes such as clock source, master lane, and lane ordering separately for these two sub-links. These attributes are available in the **Link Naming and Lane Setup** section.

The following screen displays the sub-links of a x8 bidirectional link. These sub-links have been renamed on the basis of the direction these represent.



If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the link type individually for these modules.

4 Select the link width.

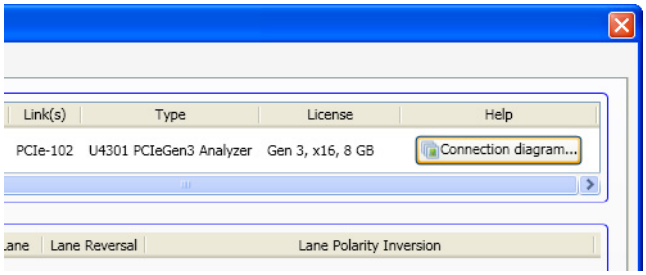


Select the link width that matches the negotiated link width of transmitter and receiver.

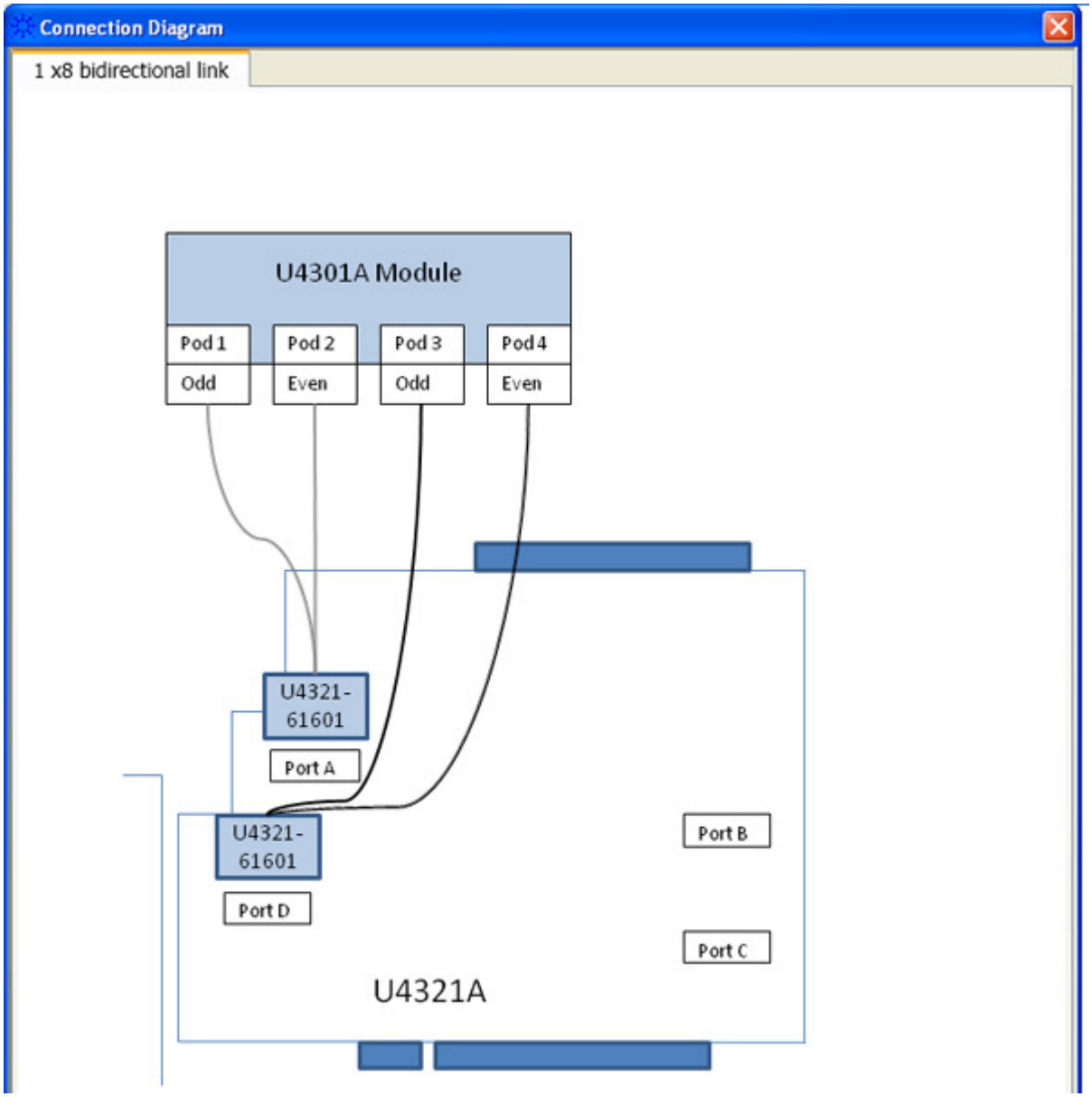
If you select the Link Type as **1 Bidirectional upto x8**, then you can select the Link Width from x1 to x8. The x16 option is disabled in this case because a U4301A Analyzer module can probe and capture data in both directions with upto eight channels in each direction.

5 Verify the connection:

a Click **Connection diagram...**.

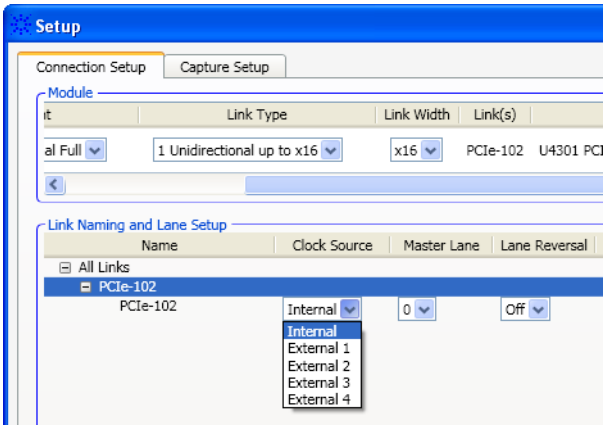


b Use the Connection Diagram dialog to verify that your connection setup specification matches the actual device under test connection.



c Close the Connection Diagram dialog.

6 Select the clock source:



- **Internal** — selects an internal clock source. You should select Internal if the data rate is in the range of 2.5 Gbps or 5 Gbps +/-50 ppm. Note that there is no input clock in this mode.
- **External 1/2/3/4** — selects an external clock source. You should select External if the device under test uses SSC or the data rate is in the range of 2.5 Gbps +/-300 ppm (+0% / -0.5% if using SSC). The clock rate for external mode should be between 100 MHz +/-300 ppm (+0% / -0.5% if using SSC).

Some important points about external reference clock selection

If you plan to use an external clock source, then you must ensure that the reference clock from the DUT is available when you:

- select **External** as the **Clock Source** in the **Setup** dialog and apply the selection by clicking **Apply** or **OK**.
- or load a configuration file that specifies the use of the external clock source.

If the reference clock from the DUT is not available to Analyzer when you apply the external clock source selection, the Analyzer's internal PLL may not be able to attain the initial lock with the DUT's reference clock resulting in an erratic behavior. Just making the DUT's reference clock available at this point does not establish the lock with the reference clock. In such a situation, you can re-establish the lock with the DUT's reference clock by performing the following steps:

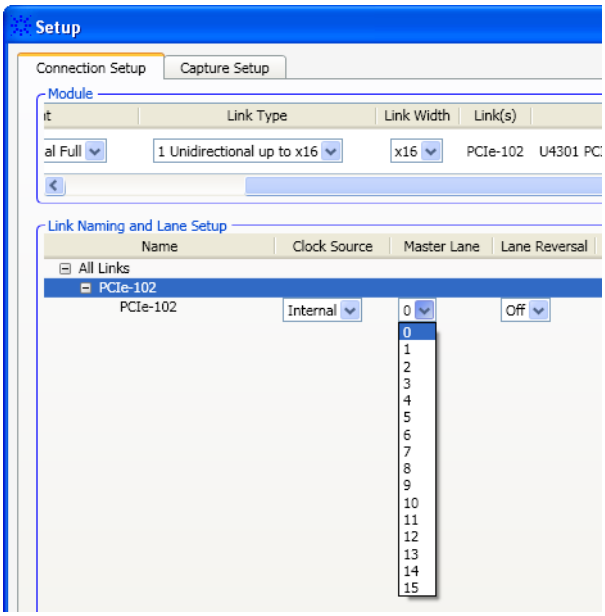
i Ensure that the reference clock of the DUT is available.

ii Then select **Internal** as the **Clock Source** in the **Setup** dialog and click **Apply**.

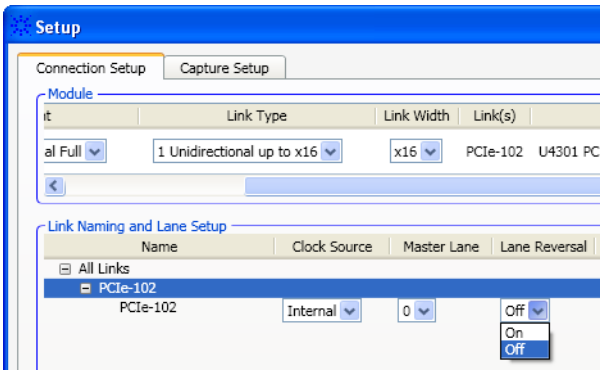
iii Finally, select **External** as the **Clock Source** in the **Setup** dialog and click **Apply**.

Once the initial lock is established, it is maintained. You need not re-establish the lock with the reference clock on subsequent availability/unavailability of the reference clock in the event of DUT power off/on or on any further changes to the Setup dialog except for **Clock Source** or **Link Type**.

7 Select the master lane. You can select any lane as the master lane from the lanes displayed in the Master Lane listbox. The lanes are displayed as per the selected link width. The lane that you select as the master lane is considered the lane for capturing the ordered sets.



8 Specify whether lane reversal is on or off.

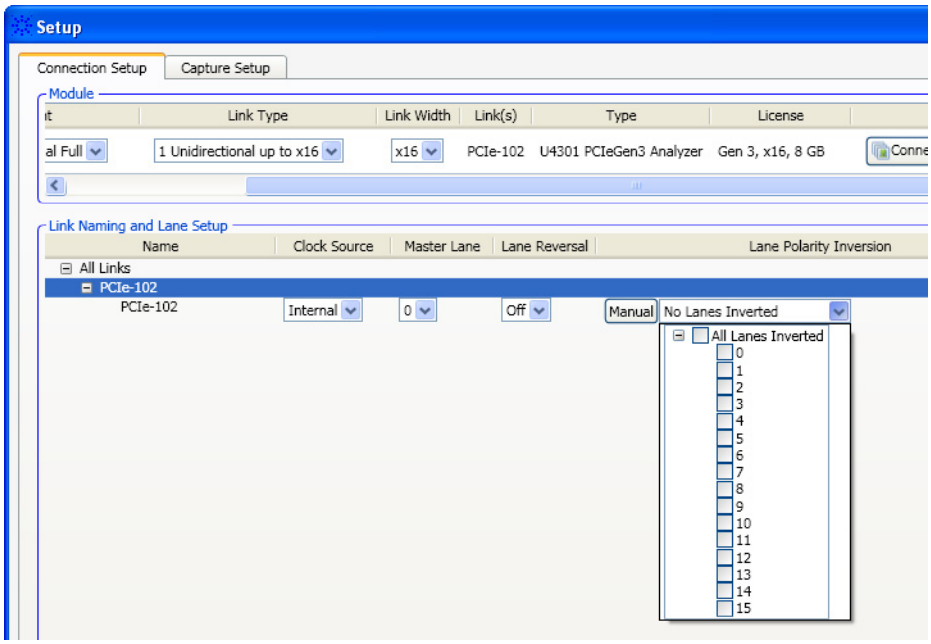


9 Specify any lane polarity inversion:

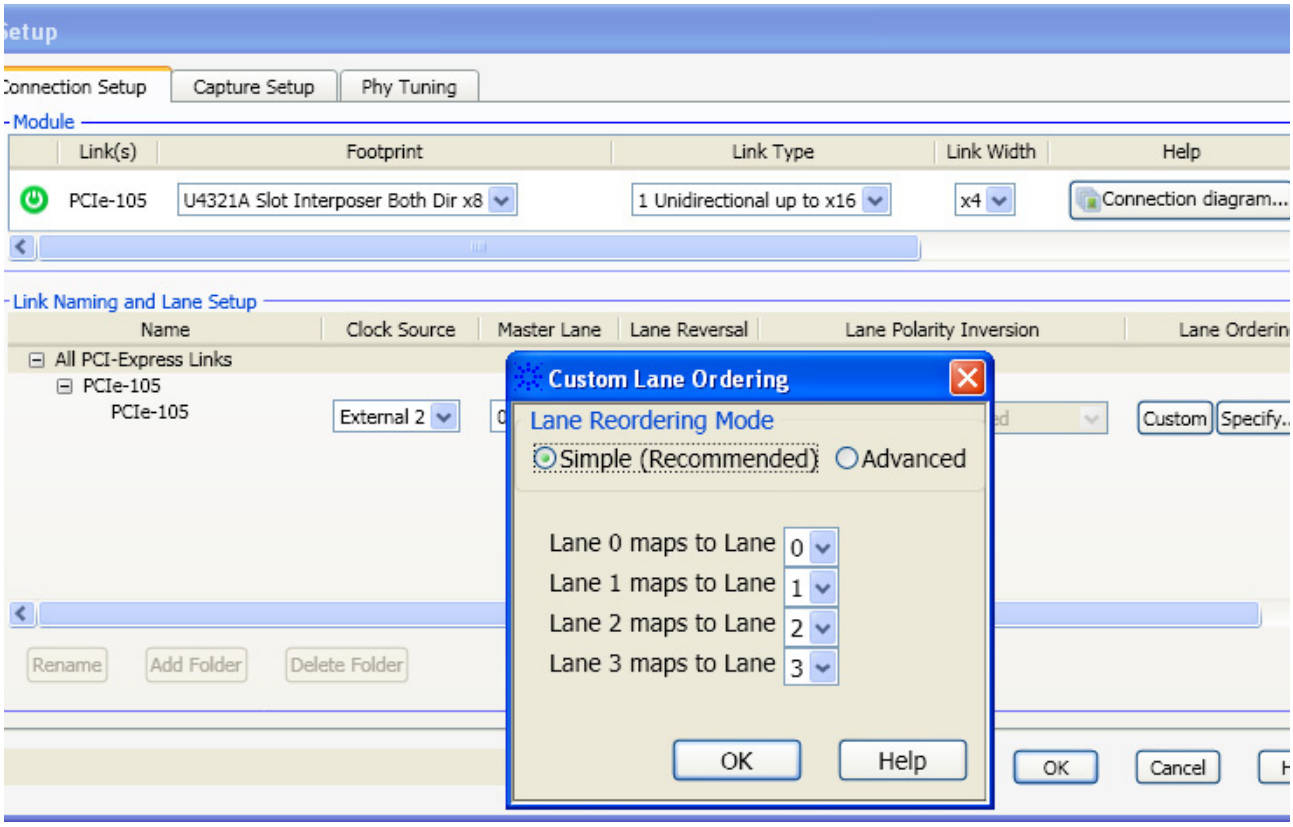
a Click **Auto** or **Manual** to toggle between the types of polarity inversion specification.

When Auto is selected, the polarity of the lanes is set automatically during the initial link training.

b When manual selection is chosen, select the lanes that are inverted.



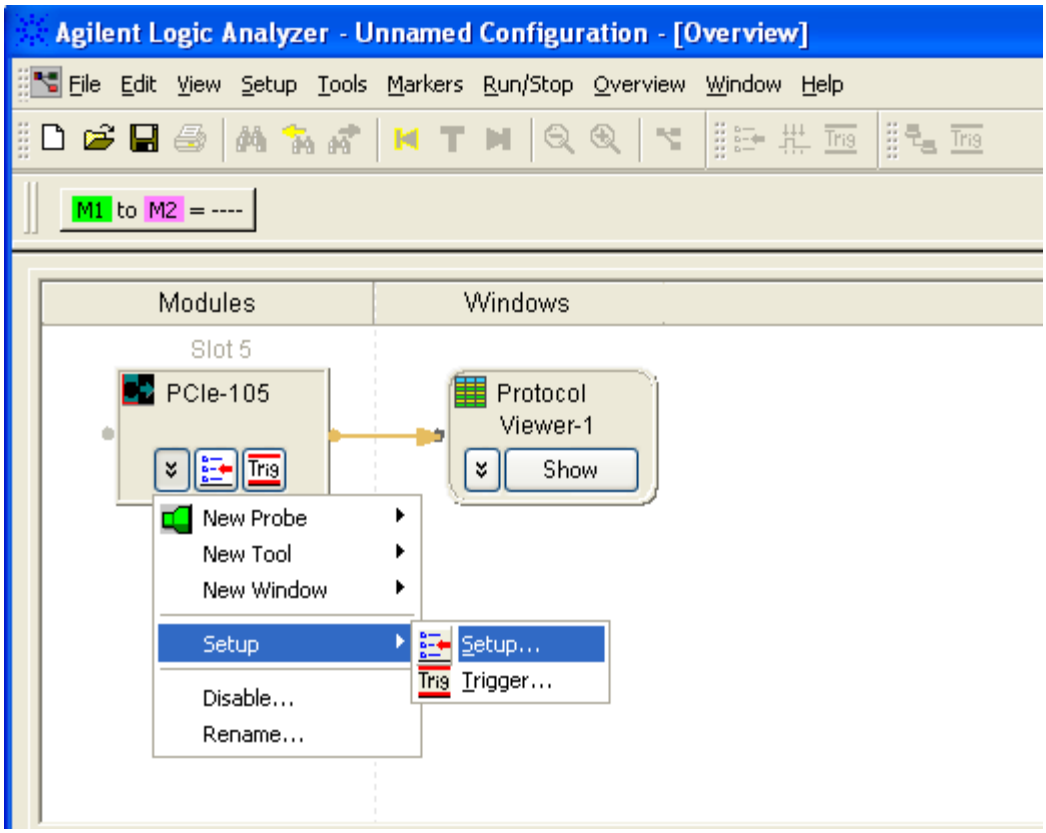
10 The **Lane Ordering** option lets you perform the ordering of the physical lanes of the link with the logical lanes. You can either retain the **Default** lane ordering which means Lane 0 of the link maps to logical Lane 0 and so on. If you want to map Lane 0 of the link to some other Lane, then select **Custom** option from Lane Ordering and click **Specify** to display the **Custom Lane Ordering** dialog box. In this dialog box, select the lane with which you want to map Lane 0. The number of lanes displayed for lane ordering depend on the selected link width. For example, if the link width is selected as x4, then the Lane 0, 1, 2, and 3 are available for lane ordering.


Connection Setup
Capture Setup
Phy Tuning
Module
Link(s)
Footprint
Link Type
Link Width
Help
PCIe-105
U4321A Slot Interposer Both Dir x8
1 Unidirectional up to x16
x4
Connection diagram...
Link Naming and Lane Setup
Name
Clock Source
Master Lane
Lane Reversal
Lane Polarity Inversion
All PCI-Express Links
PCIe-105
PCIe-105
External 2
Custom
Specify...
Rename
Add Folder
Delete Folder
OK
Cancel
Custom Lane Ordering
Lane Reordering Mode
Simple (Recommended)
Advanced
Lane 0 maps to Lane 0
Lane 1 maps to Lane 1
Lane 2 maps to Lane 2
Lane 3 maps to Lane 3
OK
Help

4 Setting the Capture Options

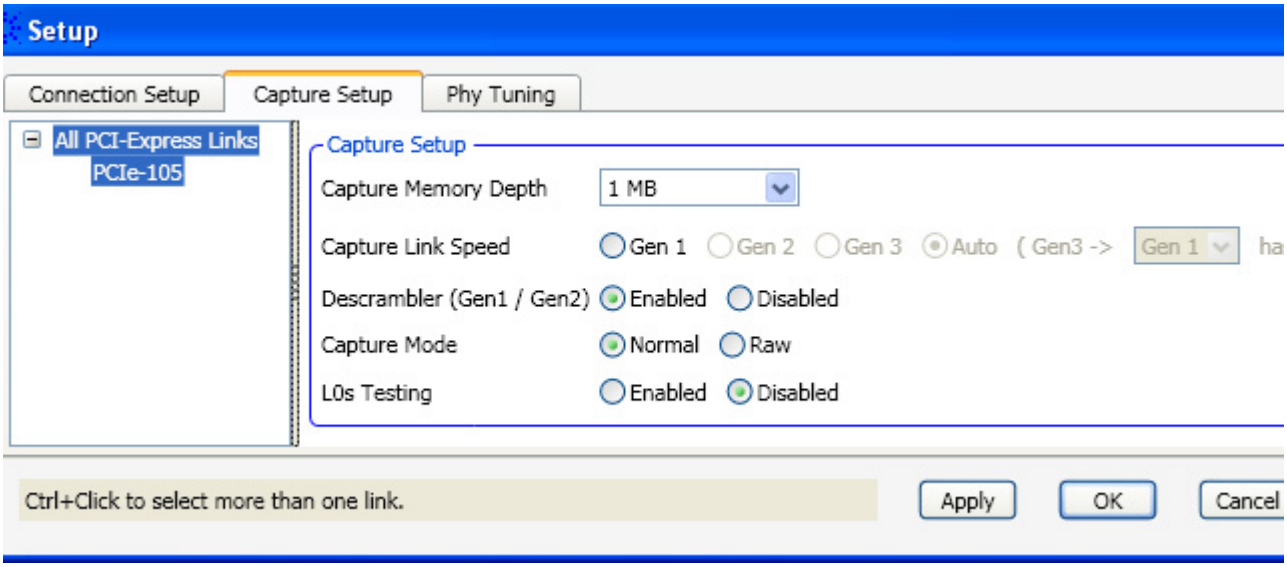
The Capture Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you set basic capture options.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Capture Setup** tab.

3 In the Capture Setup tab, select the appropriate options.



Capture Memory Depth	Lets you select the trace memory depth. Deeper traces capture more activity but take longer to save and process.
Capture Link Speed	Lets you specify the link speed of the data to be captured: • **Gen 1** — select this when capturing data on 2.5 Gbps links. • **Gen 2** — select this when capturing data on 5 Gbps links. • **Gen 3** — select this when capturing data on 8 Gbps links. • **Auto** – select this option when testing link speed switching scenarios. On selecting this option, analyzer automatically detects the link speed change and accordingly starts capturing data based on the changed link speed. The Auto option also has a drop-down listbox displayed with it. From this listbox, you can select either Gen1 or Gen2. If you select **Gen1** from this listbox, then analyzer prioritizes and captures the Gen 1 ordered sets while switching speed from Gen 3. If you select **Gen2** from this listbox, then analyzer prioritizes and captures the Gen 2 ordered sets while switching speed from Gen 3. Based on the selected link speed, the speed LED of the Analyzer pod on which the logical Lane 0 is present will glow. The following color coding is used to interpret the status of the speed LED. • Off - This means that the system is not configured. • Red - This means that the link speed is not detected or not configured. • Yellow - This means that the link speed is 2.5 Gb/s. • Green - This means that the link speed is 5 Gb/s. • Blue - This means that the link speed is 8 Gb/s. If you selected a fixed speed (Gen1, Gen2, or Gen3), then the speed LED will glow according to the selected speed. If you selected the Auto speed option, then the speed LED will glow according to the detected speed.

Descrambler (Gen1 / Gen2)	Tells the analyzer whether the descrambler algorithm is necessary: • **Enabled** — activates the descrambler algorithm. This algorithm generates the descrambled packet stream from an incoming scrambled packet stream. • **Disabled** — deactivates the descrambler algorithm. Select this option when the DUT is transmitting the non-scrambled data. Garbage data is displayed if this is set incorrectly.
Capture Mode	Lets you choose between two capture modes: • **Normal** — captures data only when all the configured lanes are out of the Loss of Sync (LOS) condition, that is, each lane has valid data. In this mode, channel bonding occurs when the analyzer encounters the first SKIP ordered set after exiting from the L0s/L1/L2/recover.speed condition. • **Raw** — captures data by each lane. This means, if only one lane is out of the LOS condition, its data is captured in the trace. In this mode, channel bonding may not exist at all. The Raw mode gives you data visibility even when there are significant PHY layer issues.

L0s Testing	Lets you select whether or not the U4301A module will capture packets in the L0s state.
	• **Enabled** - When you enable the **L0s Testing** option, the U4301A module captures packets in the L0s state and the power management testing capabilities are enabled and enhanced in terms of :
	  • improvement in locking time
	  • faster data capture while coming out of the electrical idle
	• **Disabled** - When you disable the **L0s Testing** option, the power management testing capabilities are available but not enhanced.

NOTE

When testing L0s/L1, ensure that you:

- set manual lane polarity.

- select a fixed capture link speed instead of the Auto speed.

5
Tuning the Analyzer for a Specific DUT

PCIe Gen3 Tuning Overview

What is Tuning

Tuning is the process of adjusting Agilent's probing system to remove the effects of different driving silicon, termination silicon (or other termination schemes), imperfect transmission paths, and the fact that the probes may not be in the "ideal" location for receiving a high-speed signal (that is, at the end of the transmission path).

Furthermore, a PCIe Gen3 system will negotiate its own TX Linear Equalization, and you would like to have the largest eye possible. Tuning does not affect either the transmitter or the receiver; it is used only to increase the eye as seen by the U4301 Analyzer module. This process involves getting the system/device-under-test to a stable PCIe Gen3 transmission state which the analyzer then optimizes its own equalizations settings for.

How Tuning Works

For tuning, you:

- either use a predefined physical layer tuning (.ptu) file with default tuning values appropriate for your probing and connection setup.
- or create a physical layer tuning (.ptu) file..

The .ptu file contains the information necessary to adjust the probing system for a specific device-under-test (DUT). At the 8 Gbps speed, you then need to load this .ptu file into the U4301 Analyzer module's software to have the best possible eye at the Analyzer.

It is recommended that you first use a predefined .ptu file with default tuning values. If the default tuning values do not provide robust and clean tracing results, you should consider creating your own .ptu file.

From this release of the Agilent PCIe Gen3 software, you can create or fine tune a .ptu file using the Agilent Logic and Protocol Analyzer GUI.

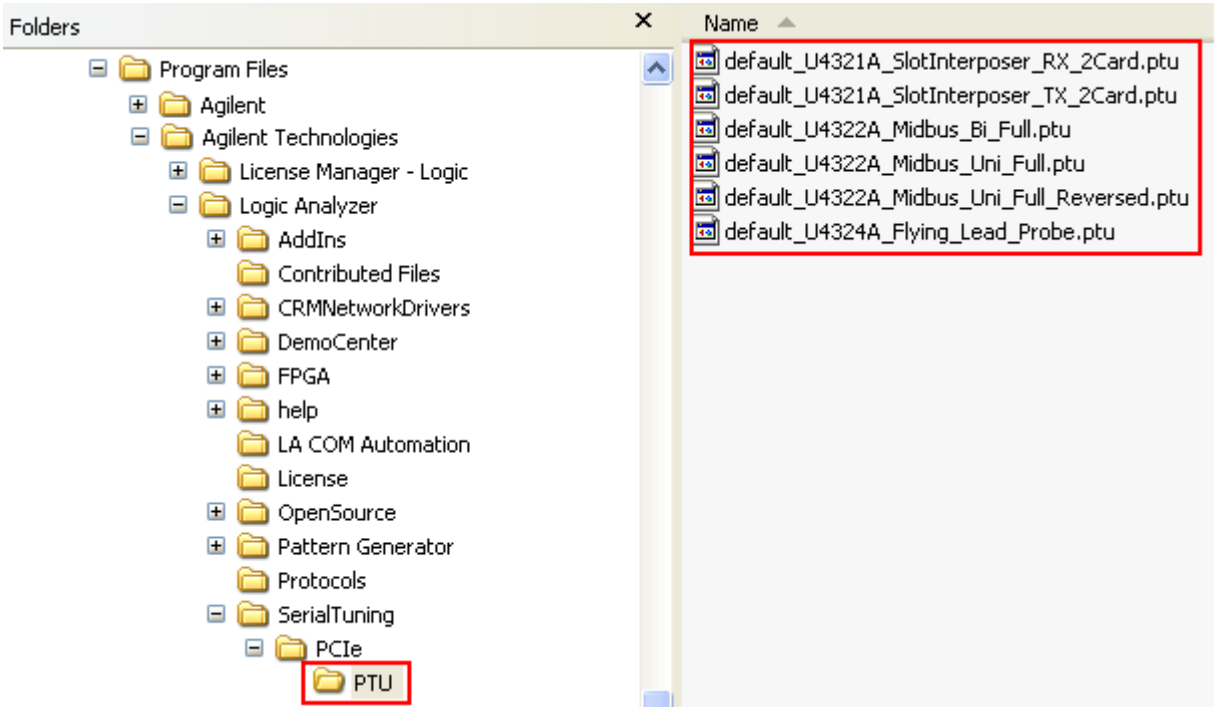
When to Perform Tuning

You should only perform tuning when all of the following conditions are met:

- Poor trace quality which may include red packets, triggers on “Loss of Sync” or “Channel Bonding”.
- No Recovery cycles (that is, cannot Trigger on “Any TS”) on the target.
- When no existing .ptu files are able to provide robust tracing.

Default and User Defined .ptu Files

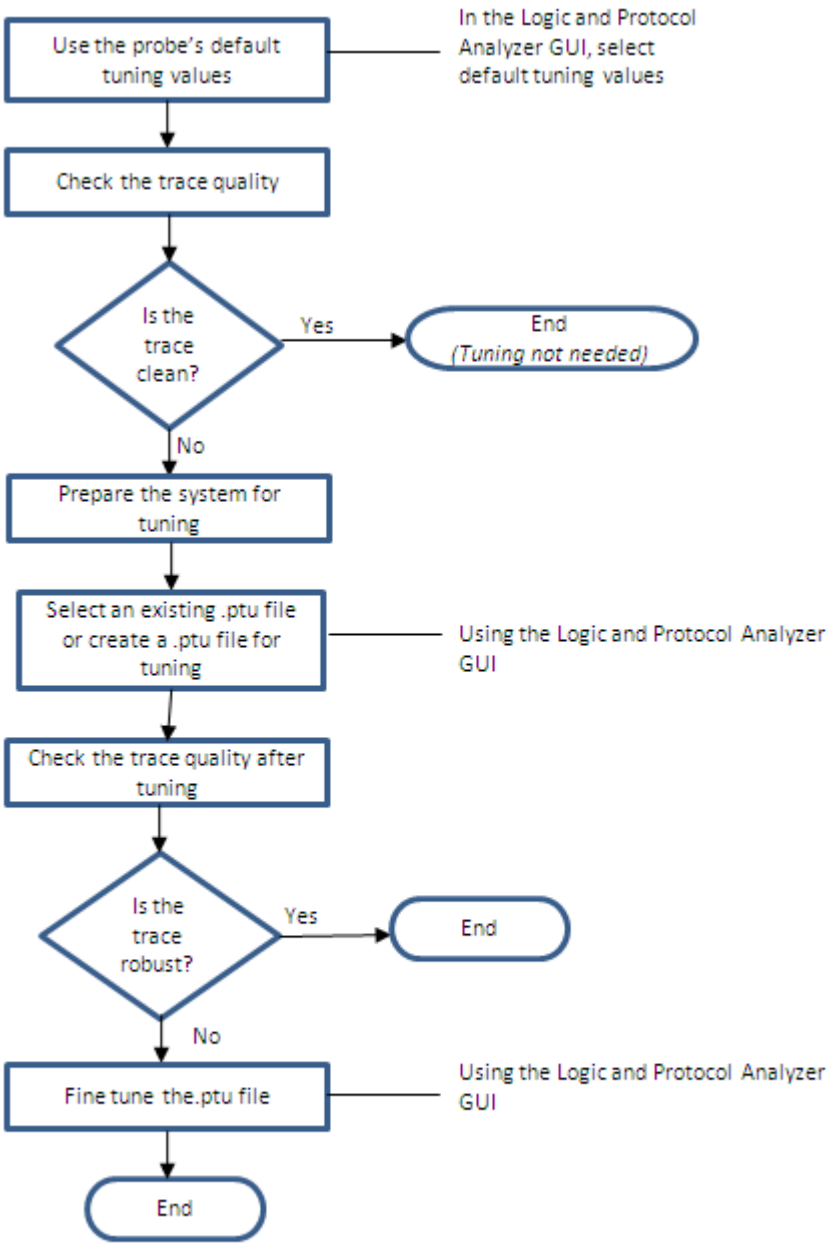
A set of default tuning (.ptu) files are provided with the Agilent Logic and Protocol Analyzer software. These tuning files contain the probe defaults to compensate for the signal impairments associated with the probe. These files are named on the basis of the probe type for which these are created. Based on the probe type you are using, one of these files is used and if the trace quality is clean, you do not need to tune further by creating your own .ptu file. These default .ptu files work fine and support robust tracing in situations where the targets have margin. The following screen displays the location of these default ptu files.



However, if the default .ptu file does not serve the purpose and you find the trace quality to be poor, you can create your own .ptu file with your specific parameters and use it in the Logic and Protocol Analyzer GUI to perform tuning. You can create a .ptu file using the Logic and Protocol Analyzer GUI.

Tuning - Broad steps

The following picture illustrates the broad steps involved in the tuning flow.



All these steps are described in detail in the topics that follow.

Tuning Method

While creating a .ptu file using the Logic and Protocol Analyzer GUI, the **AnalogTune** tuning method is used. This method minimizes the deviations of the observed Vertical Eye characteristics versus the desired Vertical Eye characteristics. From the DUT participation perspective, this method only requires that the DUT must not have transitions to or from Electrical Idle at 8Gbps.

Preparing the U4301A Module and DUT for Tuning

Perform these steps to prepare the setup for tuning:

1 Connect the U4301A Analyzer module to the DUT. Refer to the *PCI Express Gen3 Hardware and Probing Guide* to know how to connect Analyzer to the DUT based on your specific probing situation.

The following Agilent probing options are supported for use with the Analyzer module.

- U4321A solid slot interposer.

  Note that there are four connections on this interposer; the upper two are for the "To Upstream" path (assuming that the card plugged into the top connector of the interposer is the downstream side). The lower two connectors are for the "to Downstream" direction.

- U4322A soft touch midbus 3.0 probe.

  Note that there are several supported footprints that define what lanes are at specific physical connections.

- U4324A PCIe Gen3 flying lead probe.

  Each of these probes provides support for probing one to four channels of a PCIe link making it a total of 16 channels probing support for a set of four probes.

2 If the Resource Bus connector is connecting two Analyzer modules together (the connector at the left of the modules), remove the Resource Bus Connector and do the tuning of one module at a time.

After you have tuned, you can reconnect the Resource Bus Connector without affecting the tuning.

3 Your DUT must enter L0 at Gen3 speed (8 Gbps).

4 The DUT must not transition to or from Electrical Idle at 8Gbps and its TXEQ should have stabilized before tuning. If the DUT is experiencing Recovery cycles, it is likely that it will change its TXEQ to achieve stability.

5 Ensure that the connection settings such as the number of lanes in use and the lanes inverted by the transmitter are correctly set up in the **Connection Setup** tab of the U4301A module's Setup dialog box before starting the tuning. These settings are used in the tuning process and incorrect settings can result in incorrect tuning.

Creating a Physical Layer Tuning File

After you have prepared your system for tuning and configured the connection setup for the U4301A module, you can create a physical layer tuning (.ptu) file. This file stores the information about the test setup (lane inversions, number of lanes, etc) and the tuning parameters that were discovered during tuning. You use this file in the PCIe Analyzer setup in the Logic and Protocol Analyzer GUI to tune the system.

To create a physical layer tuning file

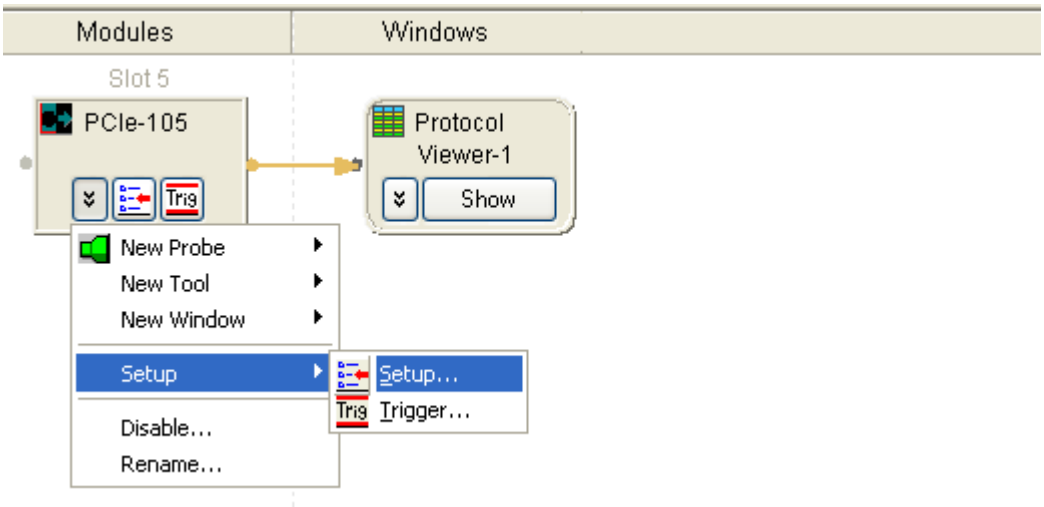
Perform these steps on the host PC that is physically connected to the U4301 Analyzer module.

1 Exit the *Agilent Logic and Protocol Analyzer* application if it is currently active.

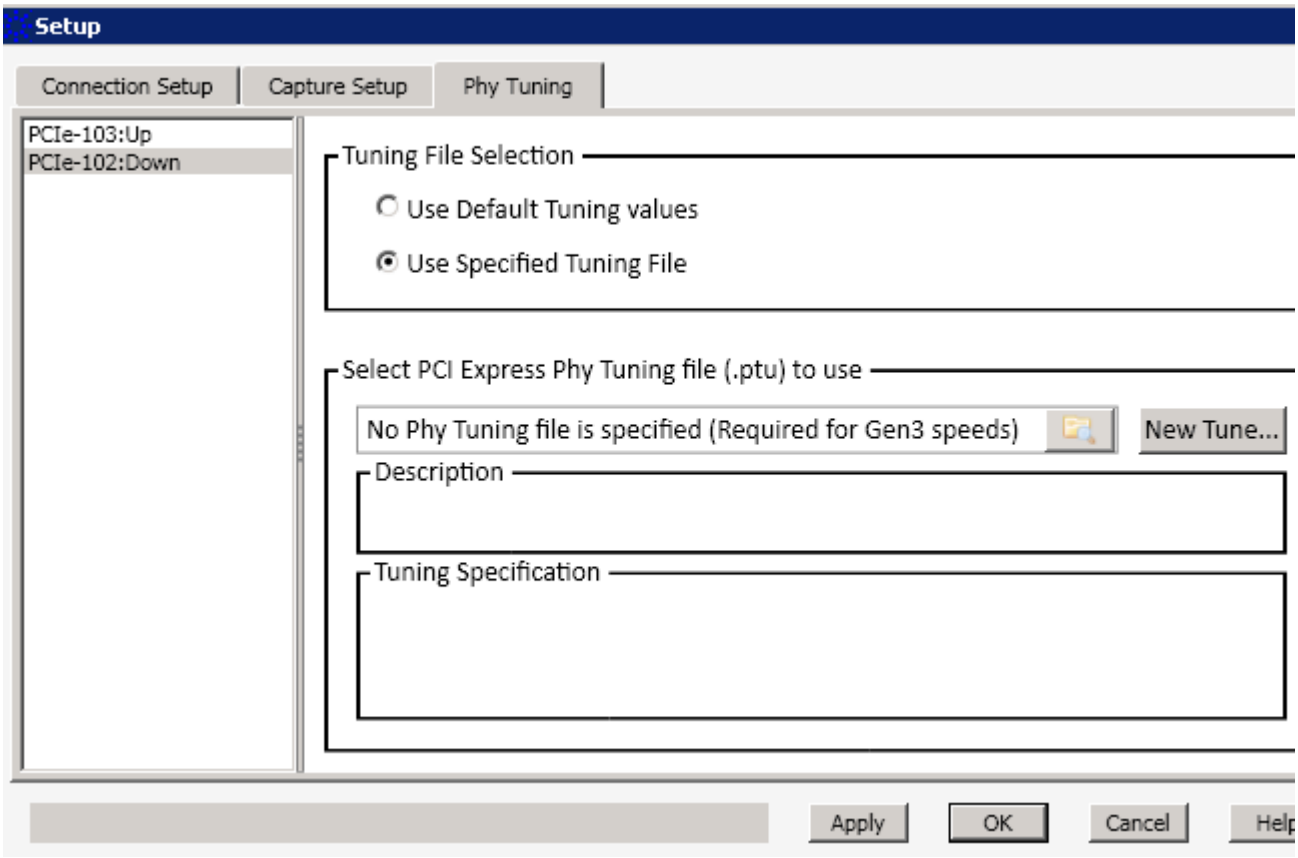
2 Start the *Agilent Logic and Protocol Analyzer* application.

This is done to ensure that all the default settings in the analyzer software are used.

3 In the Logic and Protocol Analyzer GUI's Overview window, select **Setup>Setup...**. from the PCIe analyzer module's drop-down menu to access its Setup dialog box.



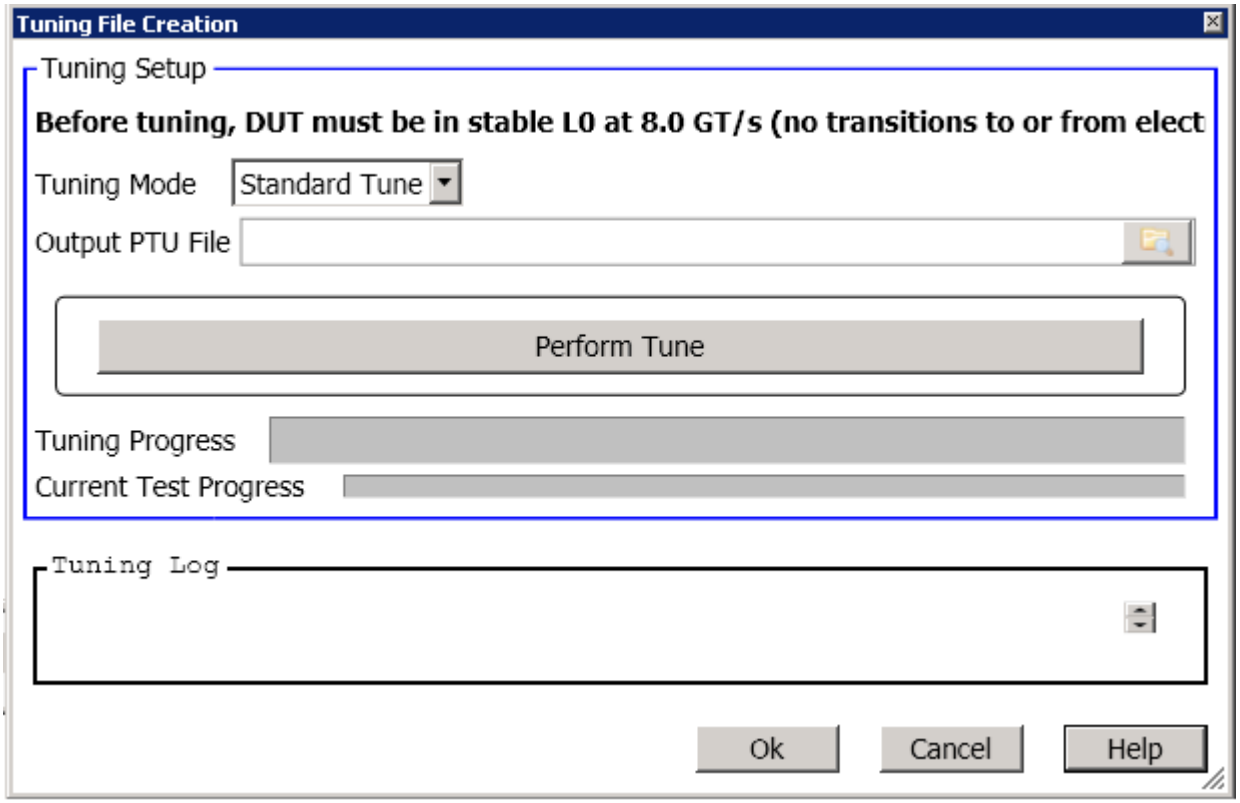
4 Click the **Phy Tuning** tab of the Setup dialog box.



5 The left pane of the Phy Tuning tab displays a list of the currently available PCIe Analyzer modules. From this list, select the module which you want to tune.

6 Select the **Use Specified Tuning File** option from the **Tuning File Selection** section.

7 Click the **New Tune...** button to open the **Tuning File Creation** dialog box.



8 Select one of the following two options from the **Tuning Mode** listbox.

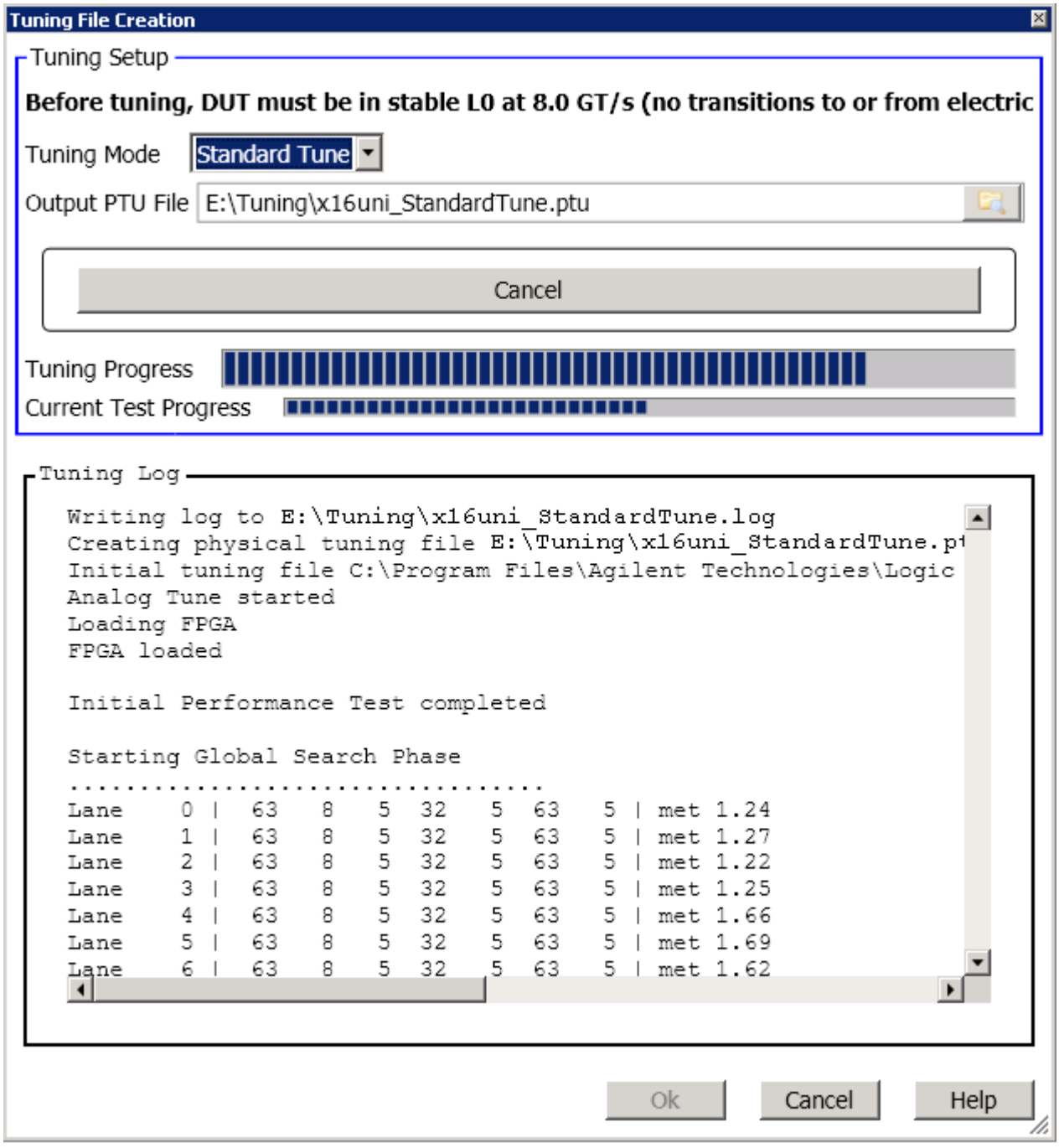
- **Standard Tune** - This option performs an Analog Tune followed by a fine tune. In this option, the number of iterations for a tuning test completion are more than the number of iterations in the Quick Tune option. Standard Tune, therefore takes more time than Quick Tune.
- **Quick Tune** - This option also performs an Analog Tune followed by a fine tune. However, the number of iterations for a test are lesser making this option suitable for performing tuning quickly.

NOTE The third option - **Fine Tune Previous Results** in the Tuning Mode listbox is meant for fine tuning a previously created .ptu file.

9 Click the  icon displayed with the **Output PTU File** field to browse and specify the name and location for the .ptu file.

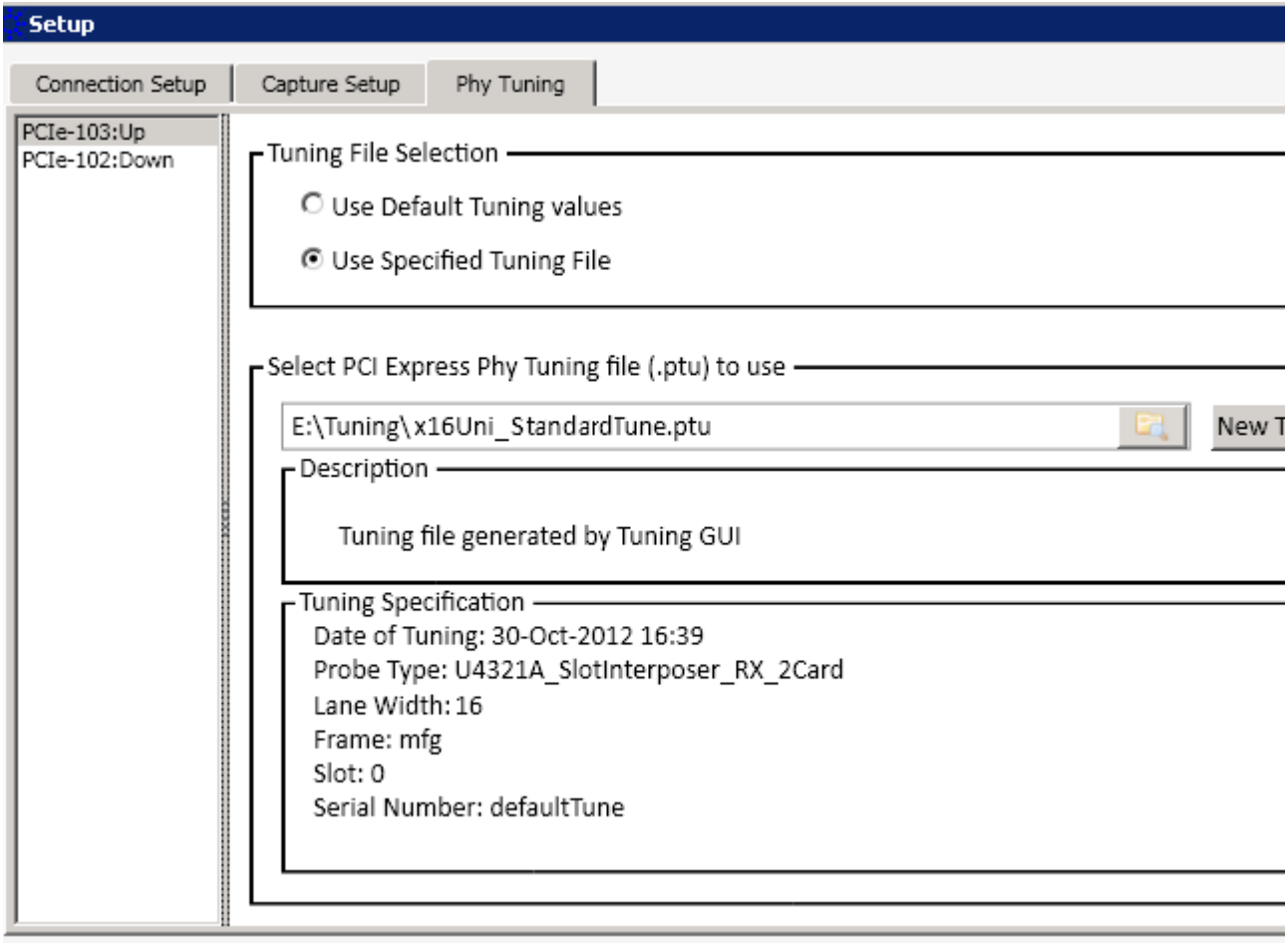
10 Click **Perform Tune**.

The tuning process starts. The **Tuning Log** section displays the results of the tuning process run operation. If the tuning process completes successfully, the specified .ptu file gets created. A tuning log file is also created with the same name and location as the tuning file.



11 Click **OK** to close the Tuning File Creation dialog box.

The newly created tuning file is now loaded for use in the Phy Tuning tab.



LEDs display during BER Based Tuning

The U4301 Analyzer module has 16 channel LEDs and four speed LEDs. The following table lists the interpretation of these LEDs display during BER-based tuning.

Channel LEDs	
Green	Indicates no bit errors on that lane.
Yellow	Indicates loss of sync or "OK"/"ERROR" is toggling quickly. You get "shades of yellow", usually, when there are frequent bit errors.
Red	Indicates bit error on that lane.
Blinking Red / Off	Indicates input FIFO overflow.
Speed LEDs	
Off	Indicates an Idle state.

Channel LEDs	
Blue	Indicates that the data is being taken.

For a general description of the channel and speed LEDs, refer to the *PCI Express Gen3 Hardware and Probing guide*. You can download this guide from www.agilent.com.

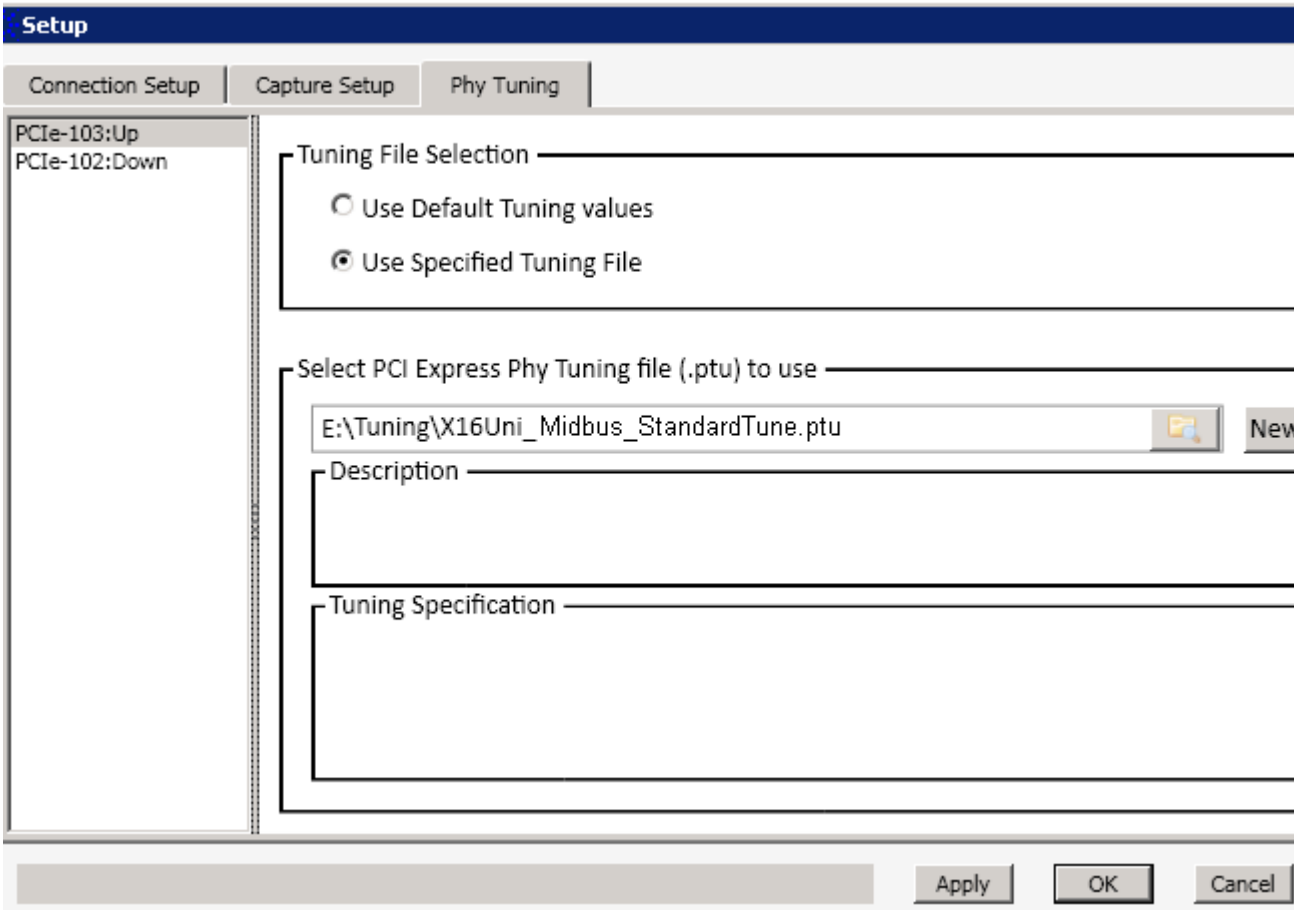
Loading a Tuning File in the Logic and Protocol Analyzer GUI

The Phy Tuning tab lets you load a user-created physical tuning (.ptu) file or the default tuning values from a predefined tuning file.

To load a user-specified tuning file or default tuning values

1. In the *Agilent Logic and Protocol Analyzer* application's Overview window, select **Setup>Setup...** from the PCIe Gen3 analyzer module's drop-down menu.
2. Click the **Phy Tuning** tab.
3. The left pane of the Phy Tuning tab displays a list of the currently available PCIe Analyzer modules. From this list, select the module for which you want to select a tuning file.
4. To load default tuning values:
   a. Select the **Use Default Tuning Values** option from the **Tuning File Selection** section. On selecting this option, the software automatically uses the default tuning values from the predefined .ptu file applicable for your probing and connection setup. This is the default and recommended option for an initial run. If the default tuning values do not produce robust and clean tracing results, you should load a user-specified PTU file for tuning (described in the next step).
5. To load a user-specified tuning file:
   a. Select the **Use Specified Tuning File** option to load a user-specified tuning file.
   b. Click the  icon displayed with the **Select PCI Express PHY Tuning File (.ptu) to use** section to browse and navigate to the tuning file that you want to load.
   c. Select the tuning file and click **Open** in the Open dialog box.

   The tuning file is now loaded for use.



6 Click **Apply** or **OK**.

Tuning a Bidirectional Setup

A single U4301A module can support a x1 to x8 bidirectional configuration. To tune a U4301A module in a x1 to x8 bidirectional configuration, you just need to tune once. A single tuning file is used to perform tuning for both directions.

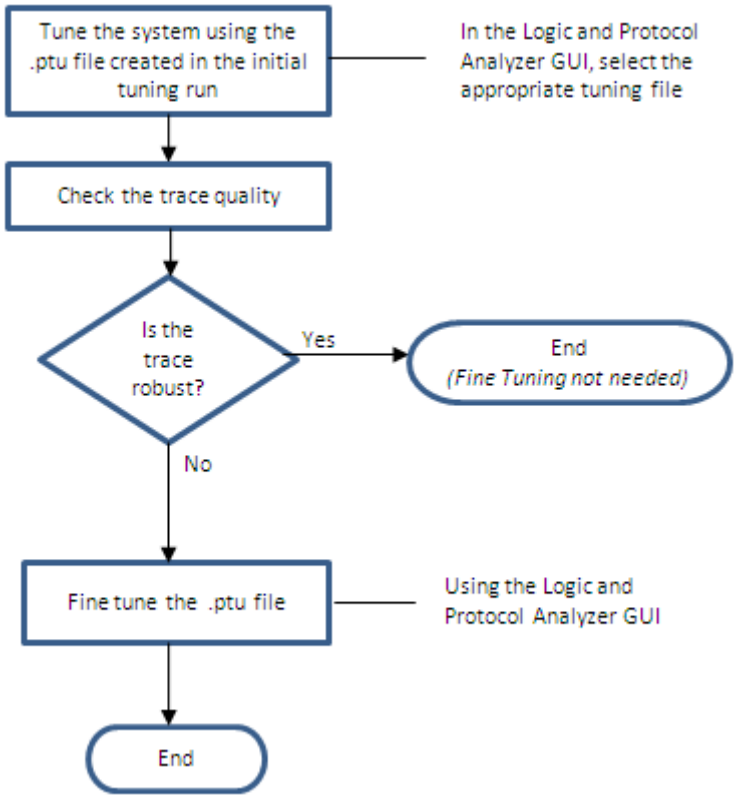
However, for a x16 bidirectional configuration, you need two U4301A modules. Therefore, for such a configuration, you need two separate tuning files, one for each module. Each module is tuned separately using its tuning file.

Fine Tuning a .ptu File

If the .ptu file that you created does not produce robust and clean tracing, then you can fine tune the .ptu file to get the desired results from tuning.

Fine Tuning Flow

The following picture illustrates the fine tuning flow.



To fine tune a .ptu file

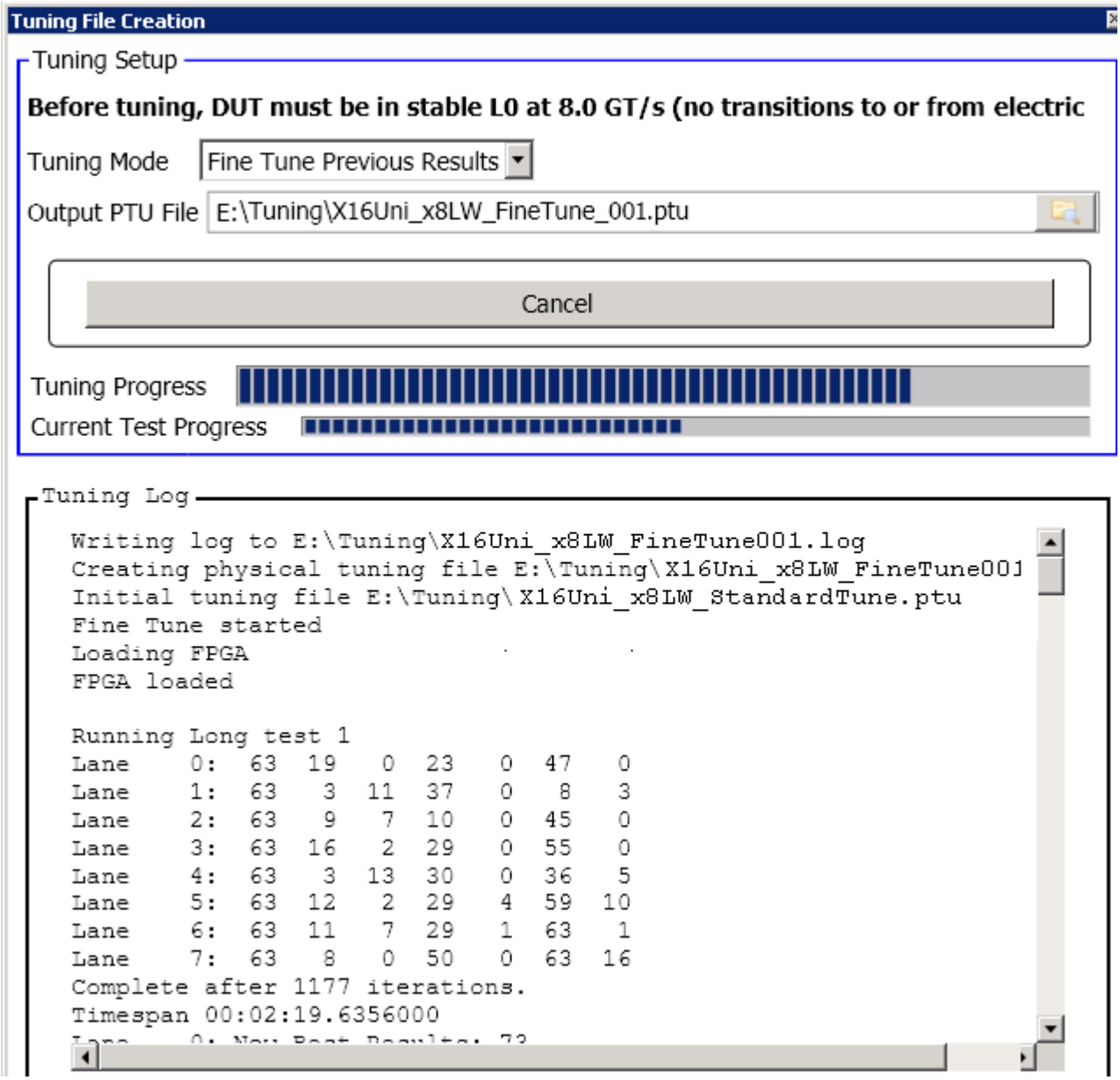
1. In the Setup dialog box of the U4301A Analyzer module, click the **Phy Tuning** tab.
2. Ensure that the **Use Specified Tuning File** option is selected and the .ptu file that you want to fine tune is selected in the **Select PCI Express Phy Tuning File (.ptu) to use** section. If no .ptu file is selected, then the default predefined .ptu file applicable for your probe and connection setup is used for fine tuning.
3. Click **New Tune...**.

4 Select **Fine Tune Previous Results** from the **Tuning Method** listbox in the **Tuning File Creation** dialog box.

5 Click the  icon displayed with the **Output PTU File** field to browse and specify the path and location of the tuning file that will be generated after the fine tuning process.

6 Click **Perform Tune**.

The fine tuning process starts and the fine tuning progress is displayed with a progress bar.



7 When fine tuning completes, click **OK** to close the Tuning File Creation dialog box.

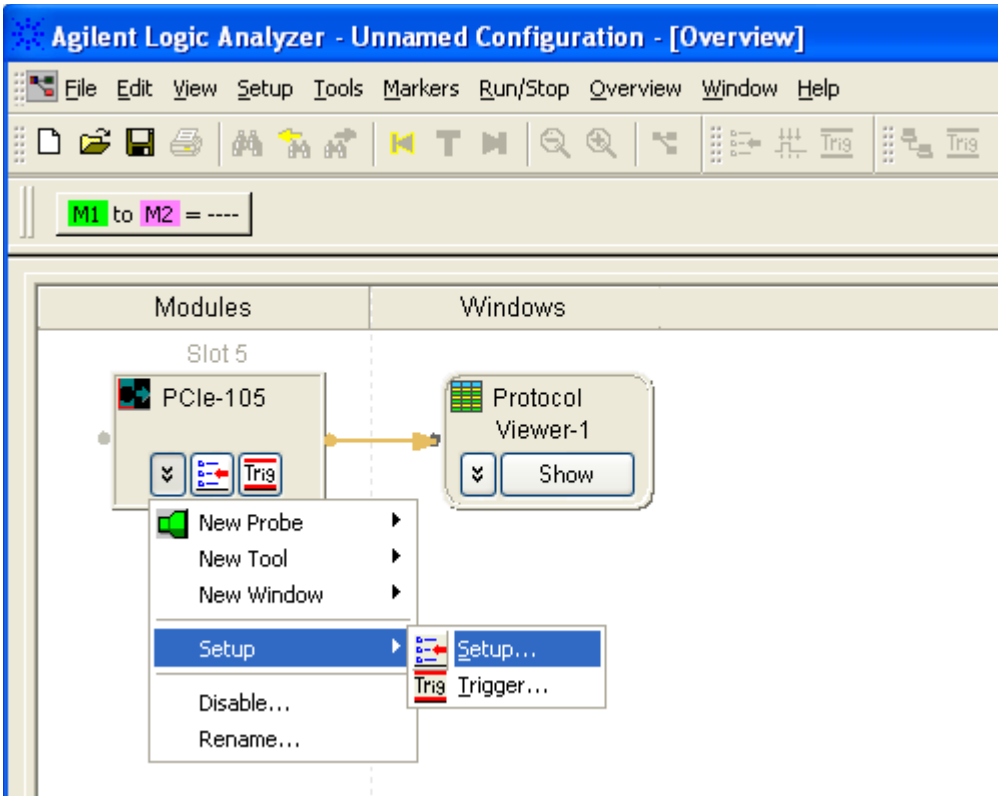
On successful completion, the fine-tuned PTU file is created at the specified location along with a tuning log with the same name as the fine-tuned PTU file.

6 Manually Adjusting the Equalizing Snoop Probe (ESP) Settings

The Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you manually adjust the equalizing snoop probe (ESP) settings.

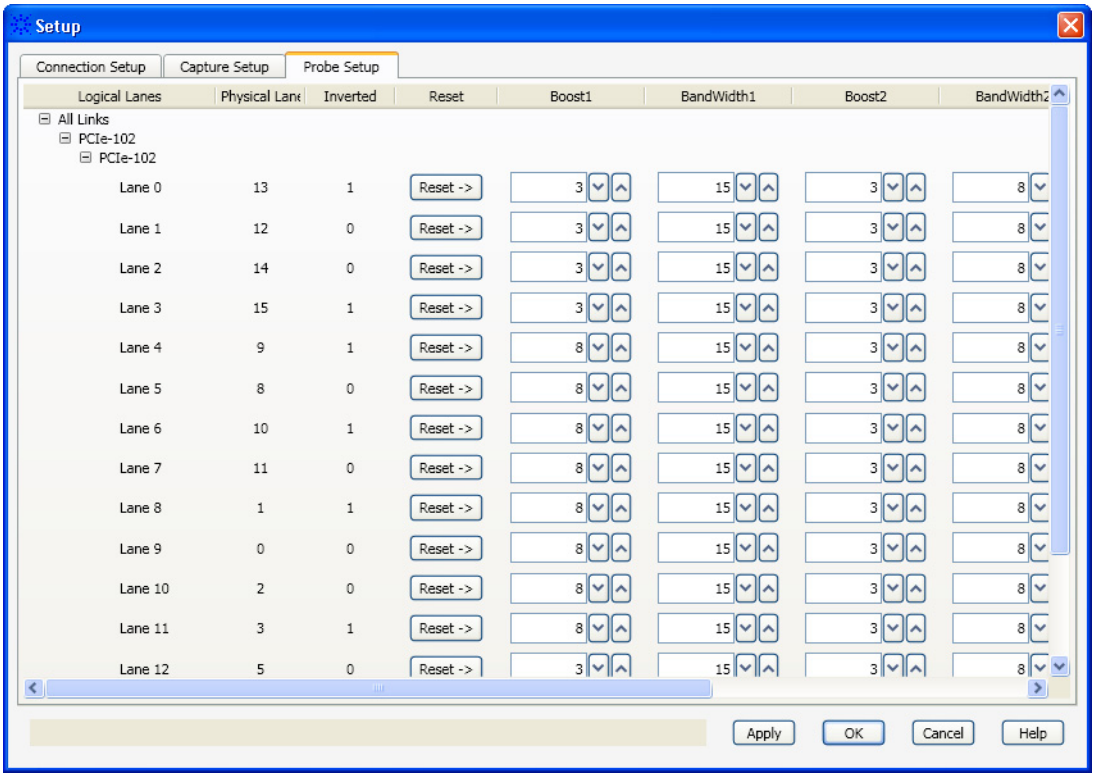
NOTE To enable the Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog, you must check the Enable Advanced Probe Settings (ASP) option in the Options dialog. See "Options Dialog" (in the online help).

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Probe Setup** tab.

3 In the Probe Setup tab, select the appropriate options.



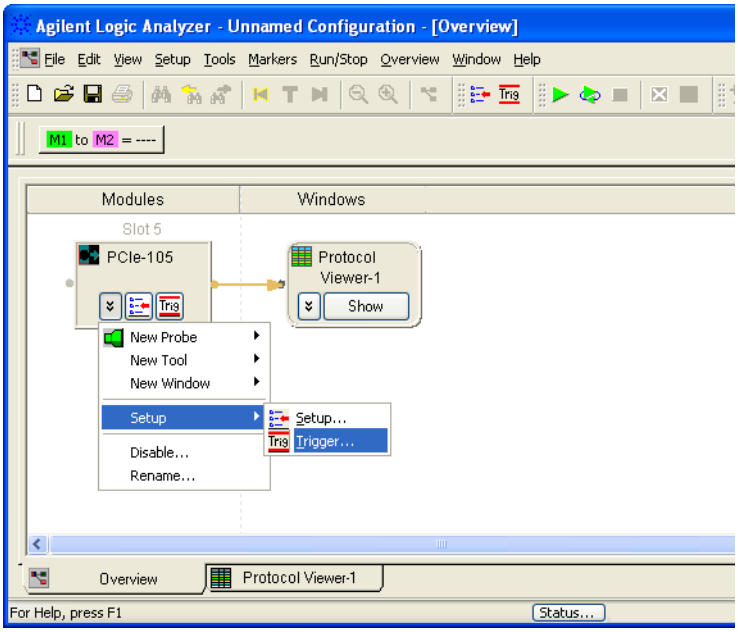
For each lane in the links, you can adjust the boost and bandwith settings. Click **Reset ->** to restore the original settings.

7 Setting Up Triggers

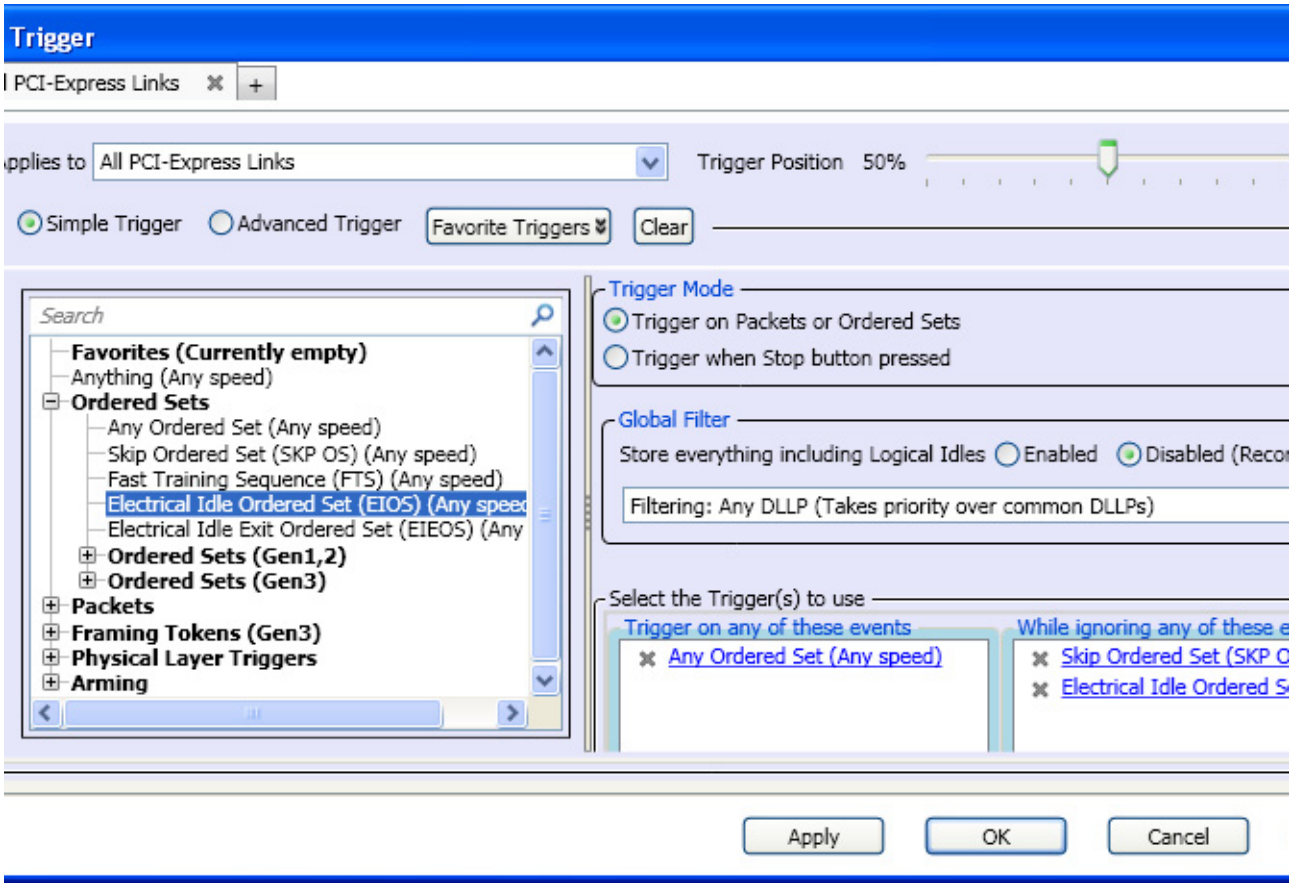
The U4301A PCIe Gen3 analyzer lets you set up triggers (events that specify when to capture a trace) with simple or advanced dialogs.

Setting Up Simple Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Simple Trigger** option.

b Select the **Trigger on Packets or Ordered Sets** Trigger Mode option.

(The **Trigger when Stop button is pressed** Trigger Mode option can be useful, for example, to see the events that lead up to a stop, halt, etc.)

c From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a result, analyzer will keep running and you need to stop it

manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you would like to trigger on from the left-side pane to the **Trigger on any of these events** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed.

To edit events in the trigger box, click the underlined event name.

To remove events from the trigger box, click the "X" to the left of the event name.

d Drag events you'd like to exclude from the trigger to the **While ignoring any of these events** box.

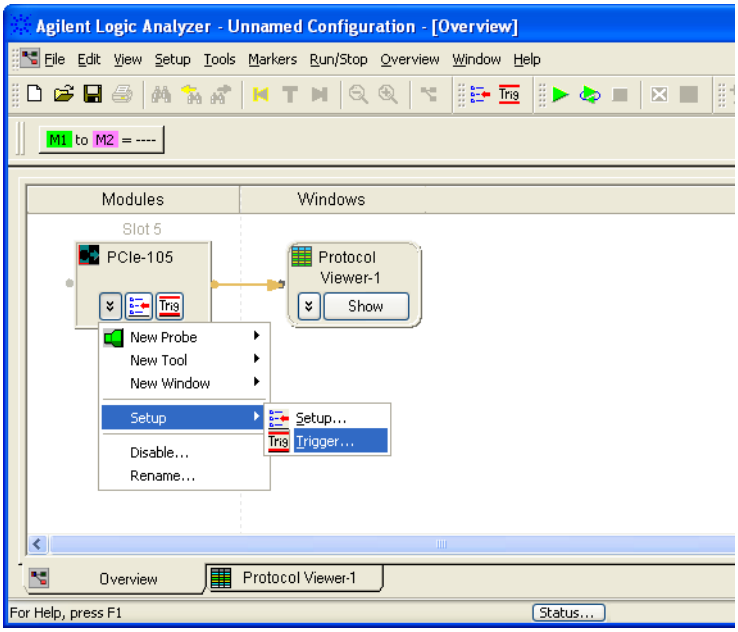
e Click **Apply** or **OK**.

See Also

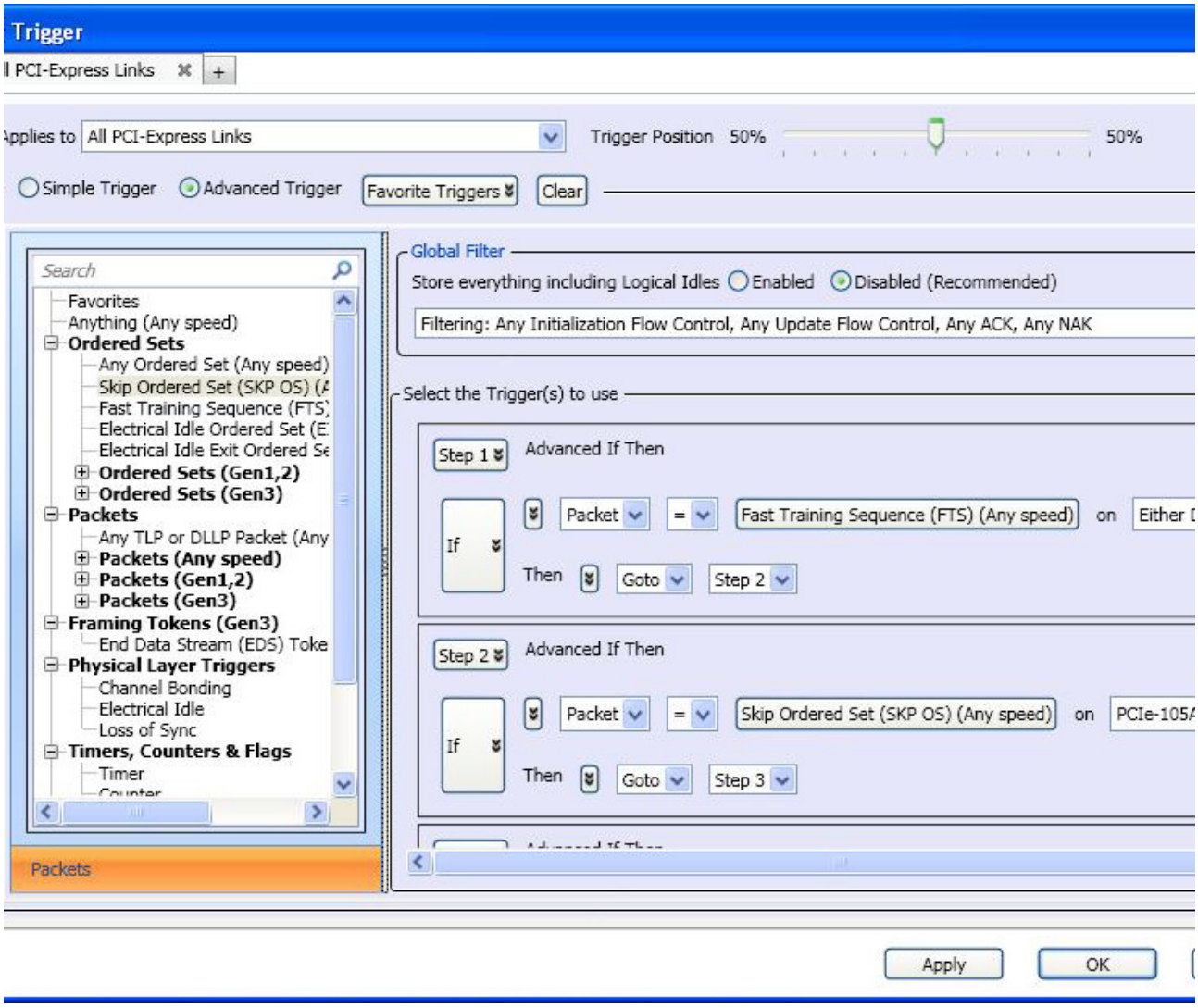
- "To select which links the trigger is for" on page 58
- "To set the trigger position" on page 58
- "To save/recall favorite triggers" on page 59
- "To clear the current trigger" on page 59

Setting Up Advanced Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Advanced Trigger** option.

b From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a

result, analyzer will keep running and you need to stop it manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you'd like to trigger on from the left-side pane to sequence steps in the **Select the Trigger(s) to use** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed. (This is the same event hierarchy displayed in the simple trigger dialog.)

To edit events in the trigger box, click the event button.

To remove events from the trigger box, click the sequence step buttons.

d In the **Select the Trigger(s) to use** box, click buttons, make drop-down selections, and enter values in fields to edit the steps in the trigger sequence:

- The **Step** buttons let you insert or delete steps.
- The **If**/**Else if** buttons let you insert or delete "if" clauses.
- The event chevron buttons let you insert, delete, or logically group (or negate) events.
- The direction drop-down listbox is displayed if you configured the U4301A module's connection setup as a bidirectional setup. It lets you select the direction (upstream or downstream) applicable for the trigger sequence. For a unidirectional data capture setup, this listbox is not displayed.
- The action chevron buttons let you insert or delete actions.
- Use the **Comment** fields to document your advanced triggers.

e Click **Apply** or **OK**.

See Also

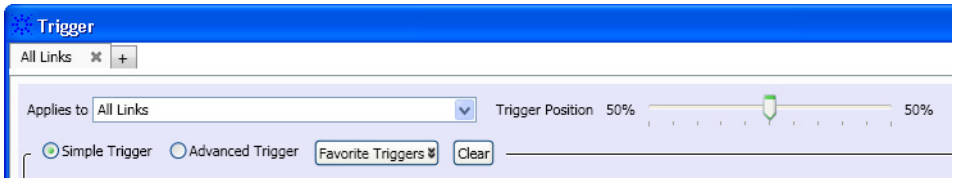
- "To select which links the trigger is for" on page 58
- "To set the trigger position" on page 58
- "To save/recall favorite triggers" on page 59
- "To clear the current trigger" on page 59

Setting General Trigger Options

The top part of the Trigger dialog contains general options that apply to both simple and advanced triggers.

To select which links the trigger is for

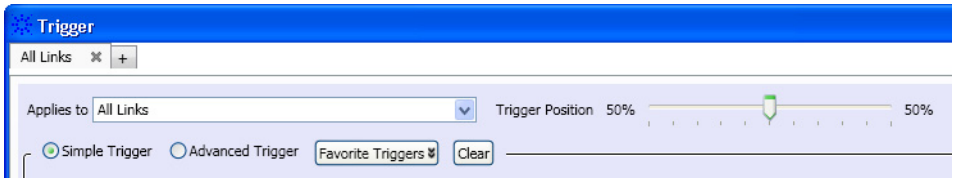
The top of the Trigger dialog has tabs that let you set up separate triggers for different links. You can add tabs for separate triggers and apply them to the links that are set up in the Connection Setup dialog (see Chapter 3, “Specifying the Connection Setup,” starting on page 13).



To set the trigger position

The top of the Trigger dialog has a slider for setting the trigger position within the capture memory.

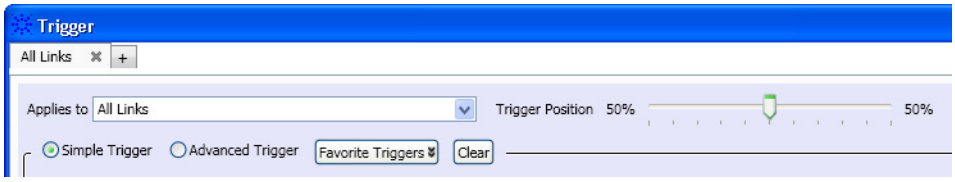
Note that the pre-trigger portion of the capture memory is filled before searching for the trigger.



To save/recall favorite triggers

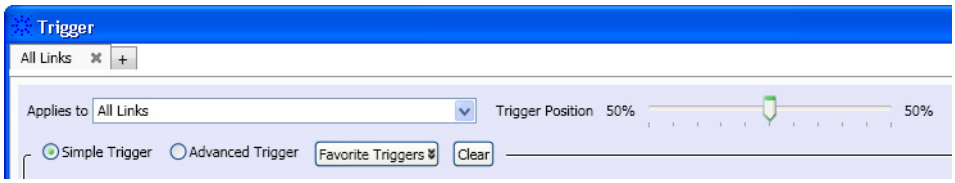
The top of the Trigger dialog has a **Favorite Triggers** drop-down menu for saving trigger setups and recalling previously saved trigger setups.

Do not confuse these "favorite" triggers with the favorites that appear in the left-side pane (which are added using the Event Editor dialog).



To clear the current trigger

The top of the Trigger dialog has a **Clear** button for erasing the current trigger setup and restoring the default trigger setup.

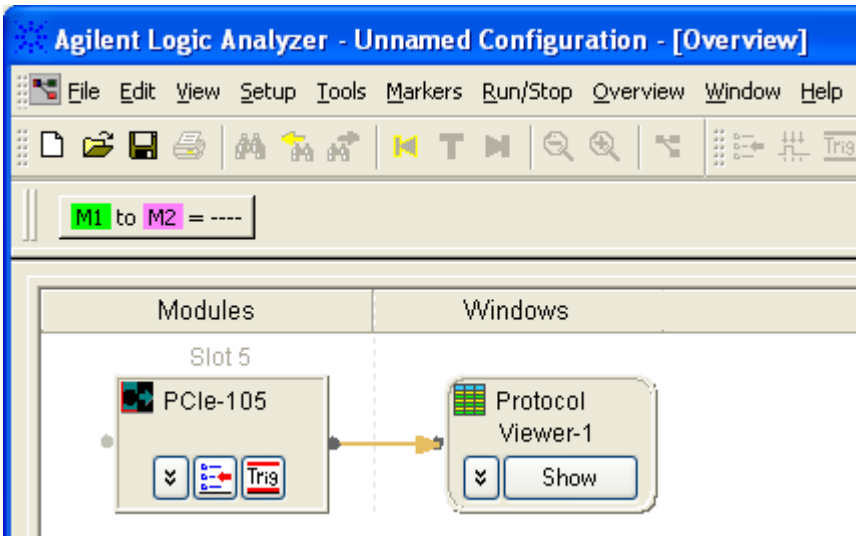


8 Running/Stopping Captures

Running and stopping the U4301A PCIe Gen3 analyzer is just like running and stopping any other analyzer. See "Running/Stopping Measurements" (in the online help).

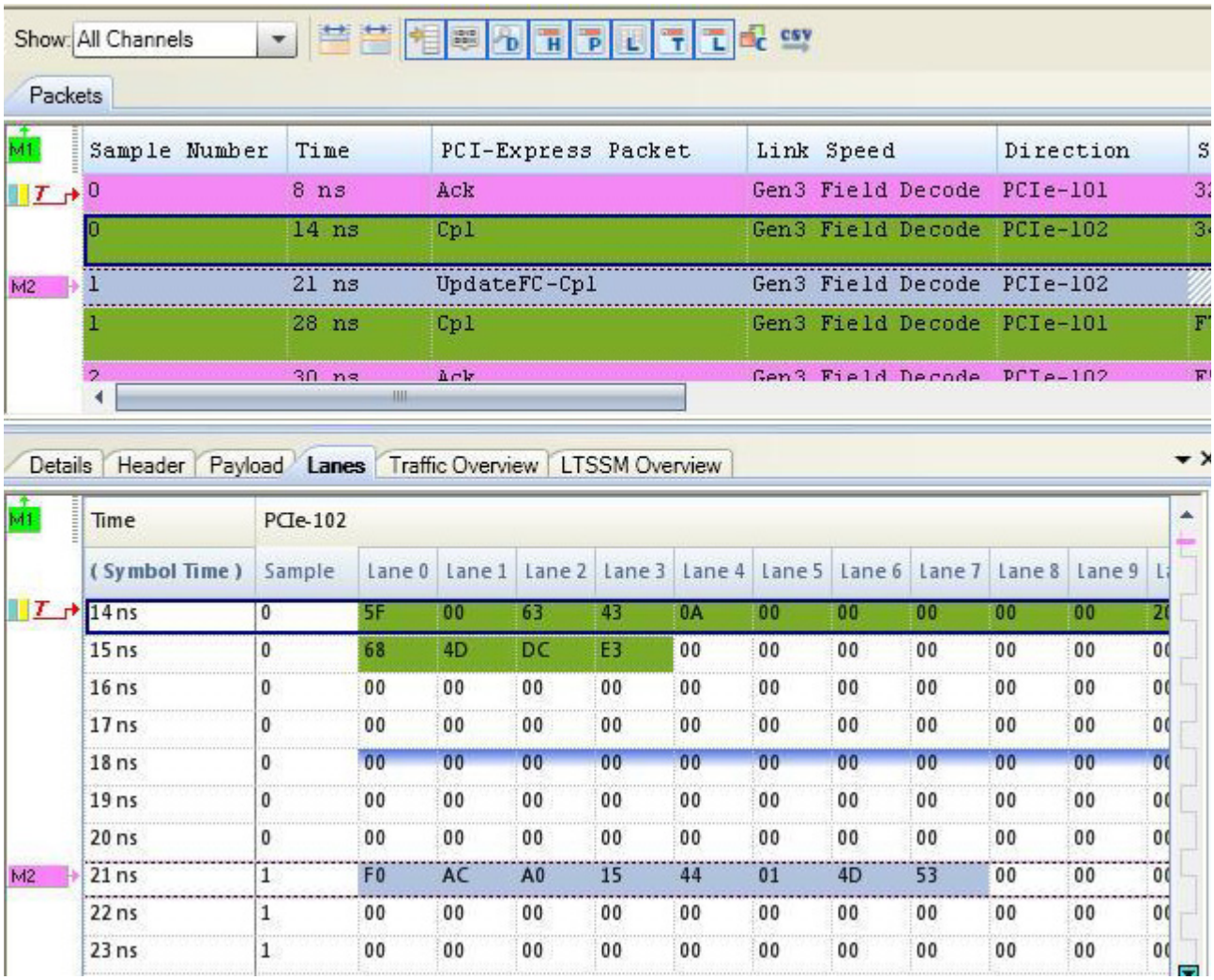
9 Viewing PCIe Gen3 Packets

You can view the data captured by the U4301A PCIe Gen3 analyzer using the Protocol Viewer window. See “Analyzing Packet Data” (in the Agilent Logic Analyzer online help). A Protocol Viewer is automatically added for a U4301A PCIe Gen3 analyzer module in the Logic Analyzer GUI.



The Protocol Viewer window displays the summarized and detailed packet information at the same time within two panes. The upper pane lists the packets. On selecting a packet, the details of that packet are displayed in the lower pane.

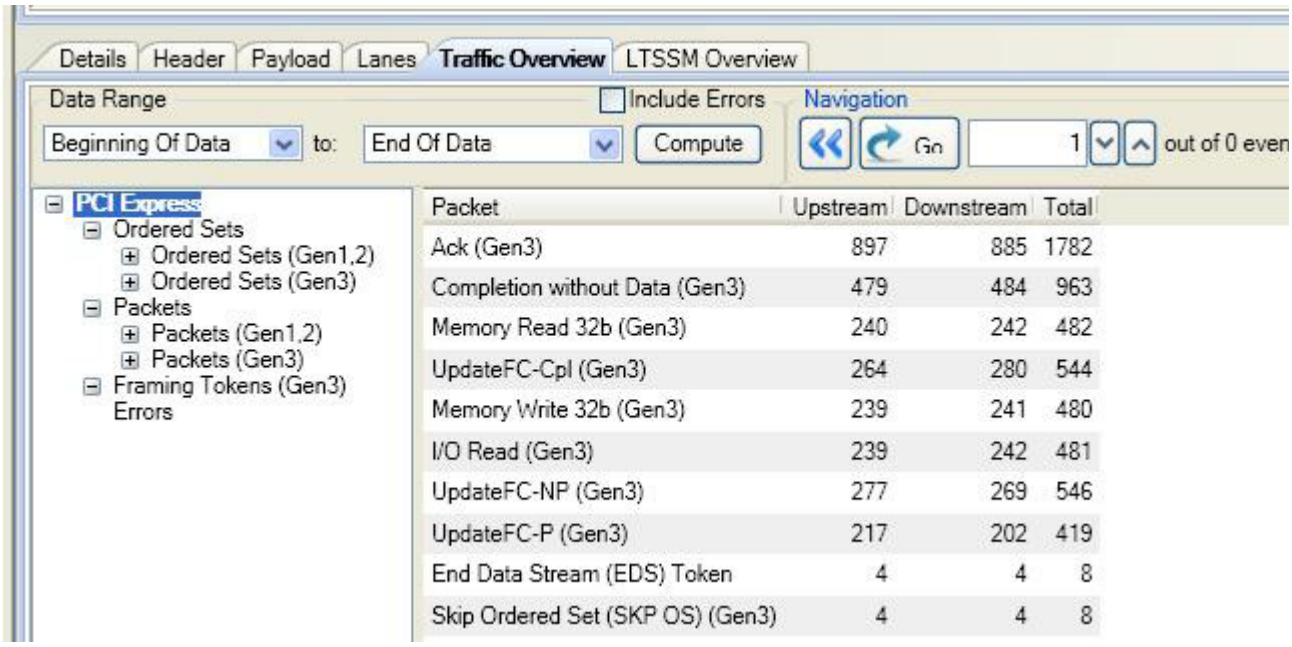
The following screen displays a sample view of the captured PCIe data in the Protocol Viewer window. In this screen, the Lanes tab of the Protocol Viewer window is displayed. The Lanes viewer displays not just the selected packet data across lanes but also the post packet data represented by colors matching the selected packet color in the upper pane.


Show: All Channels
Packets
Sample Number
Time
PCI-Express Packet
Link Speed
Direction
0
8 ns
Ack
Gen3 Field Decode
PCIe-101
0
14 ns
Cpl
Gen3 Field Decode
PCIe-102
1
21 ns
UpdateFC-Cpl
Gen3 Field Decode
PCIe-102
1
28 ns
Cpl
Gen3 Field Decode
PCIe-101
Details
Header
Payload
Lanes
Traffic Overview
LTSSM Overview
Time
PCIe-102
(Symbol Time)
Sample
Lane 0
Lane 1
Lane 2
Lane 3
Lane 4
Lane 5
Lane 6
Lane 7
Lane 8
Lane 9
14 ns 0 5F 00 63 43 0A 00 00 00 00 00
15 ns 0 68 4D DC E3 00 00 00 00 00 00
16 ns 0 00 00 00 00 00 00 00 00 00 00
17 ns 0 00 00 00 00 00 00 00 00 00 00
18 ns 0 00 00 00 00 00 00 00 00 00 00
19 ns 0 00 00 00 00 00 00 00 00 00 00
20 ns 0 00 00 00 00 00 00 00 00 00 00
21 ns 1 F0 AC A0 15 44 01 4D 53 00 00
22 ns 1 00 00 00 00 00 00 00 00 00 00
23 ns 1 00 00 00 00 00 00 00 00 00 00

Viewing the captured PCIe Traffic Statistics

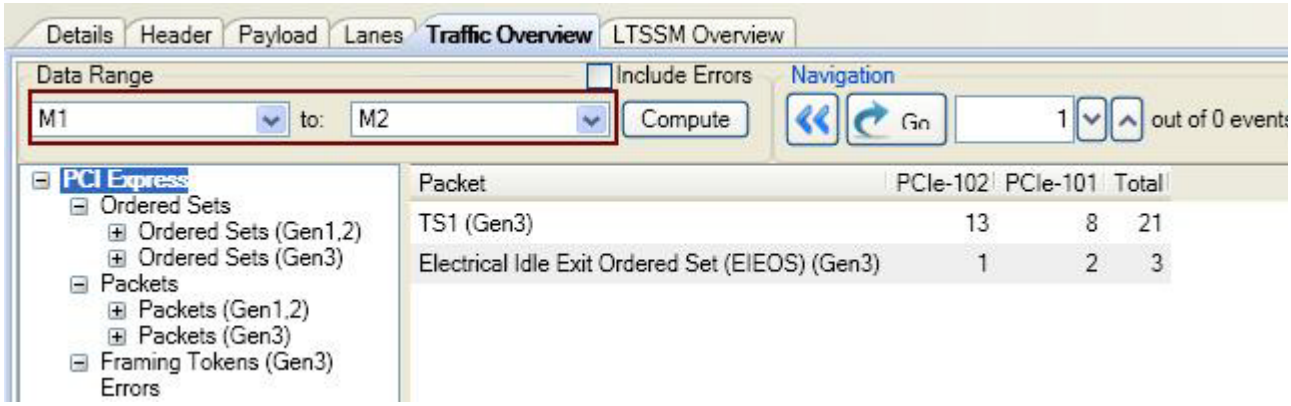
You can use the **Traffic Overview** tab in the lower pane of Protocol Viewer to get an overview of the PCIe traffic that is displayed in the upper pane of Protocol Viewer. This tab provides a count of various PCIe packet types captured and displayed in the upper pane. The count of packets is categorized on the basis of packet types.

For each packet type, the count of packets is further segregated based on the direction (upstream or downstream). The following screen displays the traffic statistics in the lower pane. Notice that for each packet type, the count of packets is displayed for upstream as well as downstream direction along with a sum of packets in both directions.



Packet	Upstream	Downstream	Total
Ack (Gen3)	897	885	1782
Completion without Data (Gen3)	479	484	963
Memory Read 32b (Gen3)	240	242	482
UpdateFC-Cpl (Gen3)	264	280	544
Memory Write 32b (Gen3)	239	241	480
I/O Read (Gen3)	239	242	481
UpdateFC-NP (Gen3)	277	269	546
UpdateFC-P (Gen3)	217	202	419
End Data Stream (EDS) Token	4	4	8
Skip Ordered Set (SKP OS) (Gen3)	4	4	8

You can specify the data range based on which the traffic statistics get computed in the Traffic Overview tab. For instance, you might want to view the traffic statistics only for the PCIe packets between the markers M1 and M2. In such a situation, you can select M1 as the start point and M2 as the end point in the **Data Range** group box and then click **Compute**. Then Protocol Viewer displays the traffic statistics of only the packets that fall in the specified data range and not for all the PCIe packets displayed in the upper pane. The following screen displays the traffic statistics for the data range starting from M1 and ending at M2 markers.

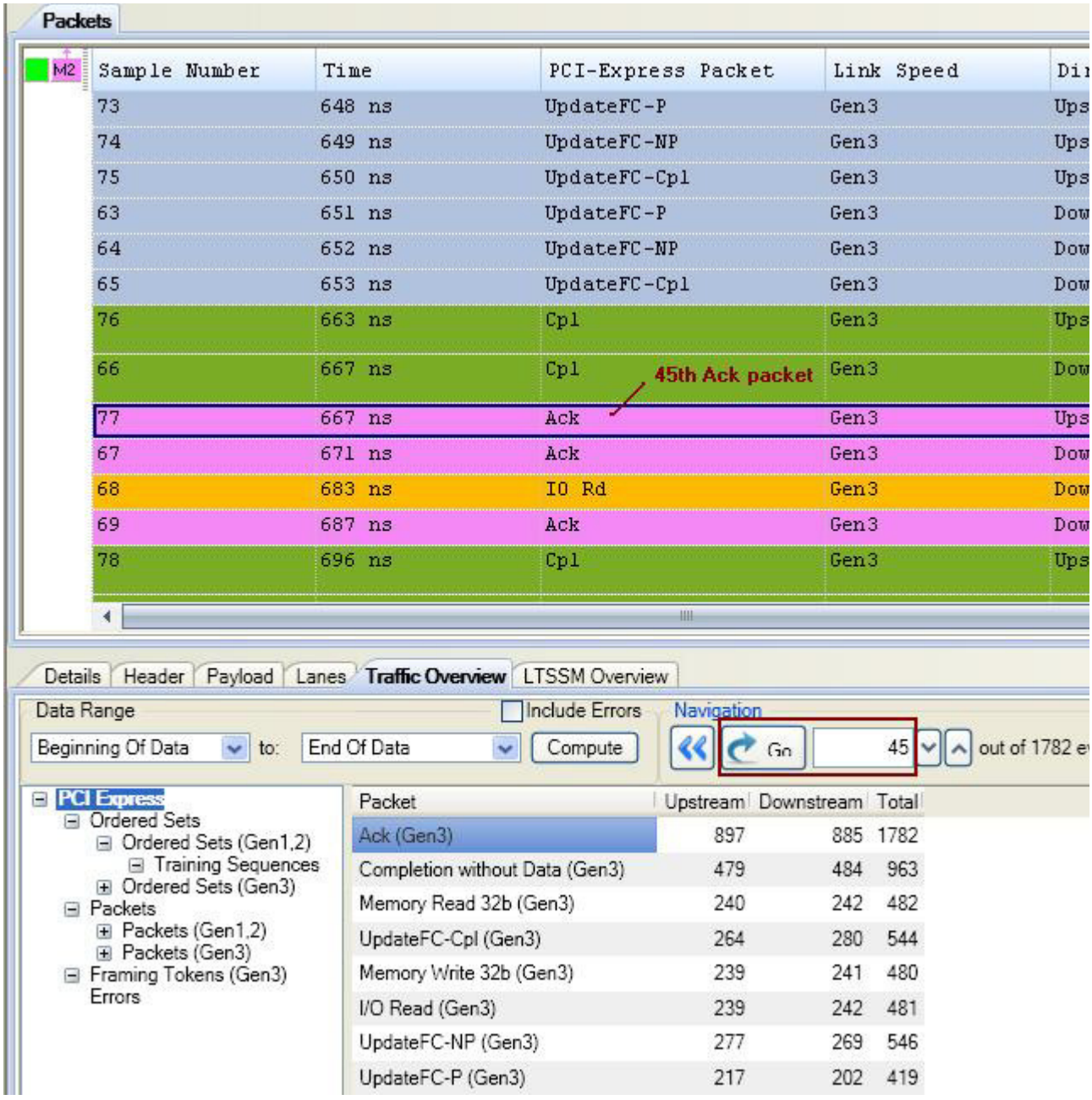


The Compute button is disabled when U4301A PCIe Analyzer module is capturing data. It becomes enabled when the capture has stopped.

Navigating through the captured PCIe packets

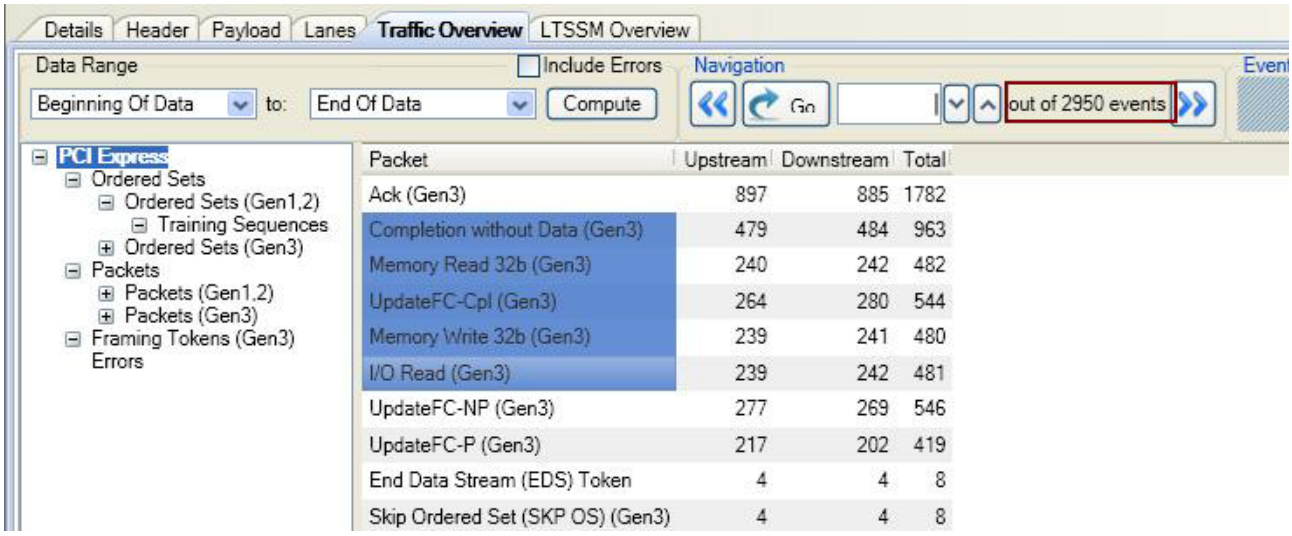
From the displayed traffic overview statistics, you can select a particular packet type and then navigate through the packets displayed in the upper pane for that packet type. For instance, there are total 1782 packets of the type Ack and you want to view the details of the 45th Ack packet out of these 1782 Ack packets. To go directly to the 45th Ack packet out of the total Ack packets, you can select this packet type in the Traffic Overview

results and then type 45 in the Navigation text box and click Go. This takes you directly to the 45th Ack packet in the upper pane of Protocol Viewer.



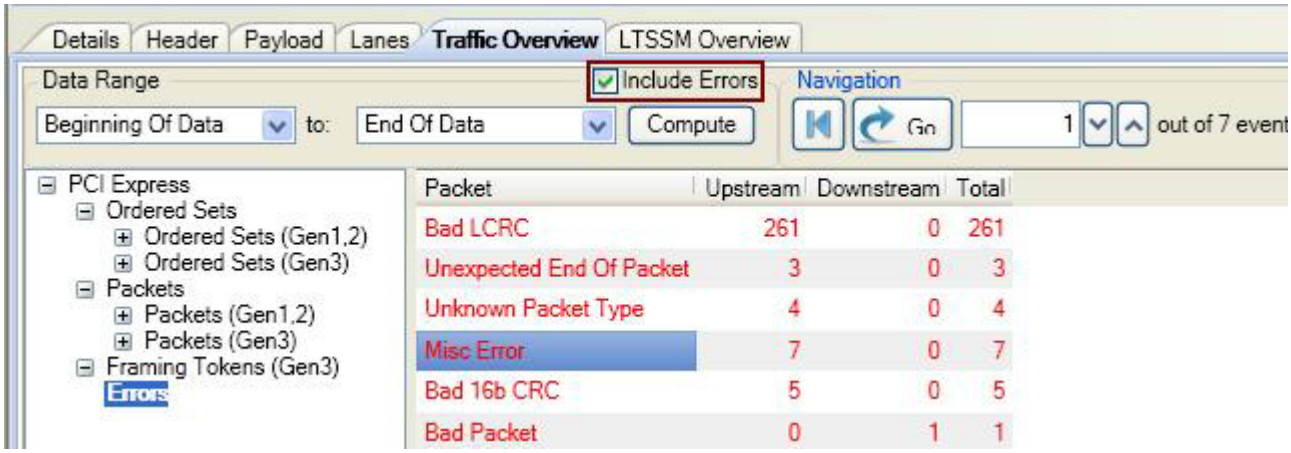
You can also navigate through the PCIe packets of a particular direction (upstream or downstream). To do this, select a particular packet type in the displayed traffic statistics and then select the count column for the required direction. Then specify the packet number in the Navigation text box to reach directly to that packet.

You can also select multiple packet types in the Traffic Overview tab by clicking a packet type and then dragging the mouse over to the other packet types that you want to select. When you select multiple packet types, the Navigation section displays the total packet count for all the selected packet types.



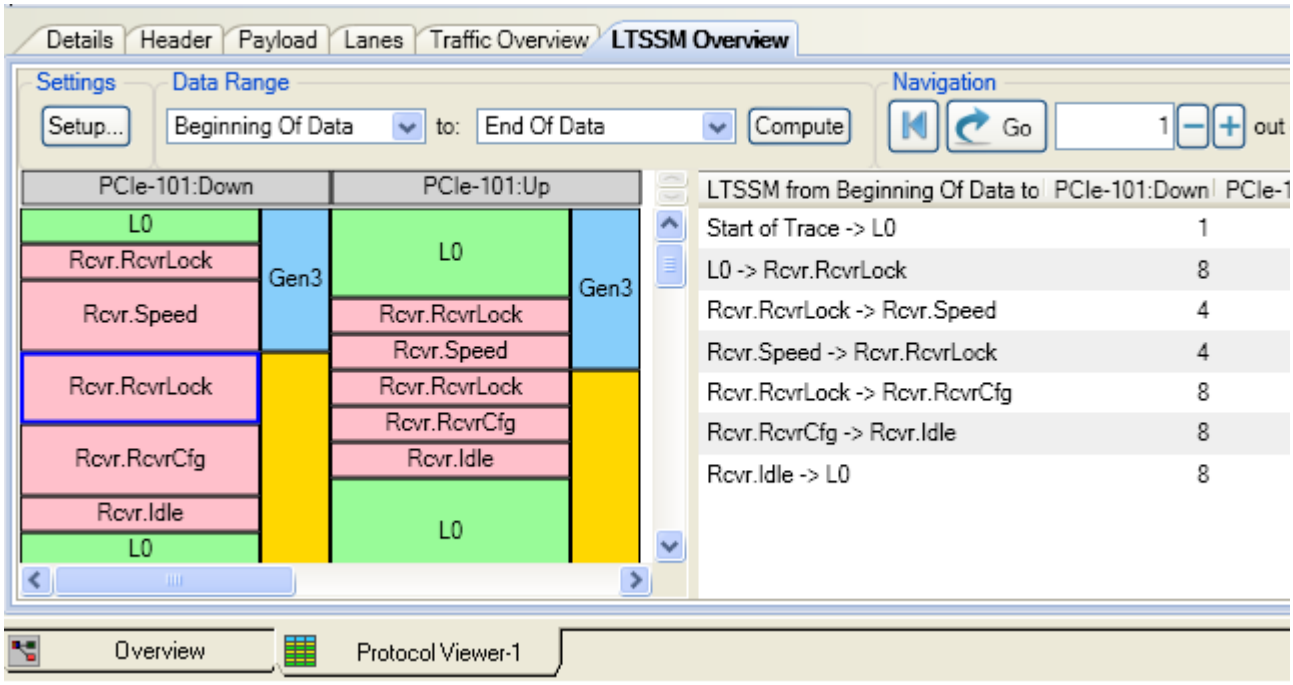
Viewing Errored Packets Statistics

If you want to include the count of errored packets in the traffic overview, then select the **Include Errors** check box. You can then click the Errors option in the left panel of Traffic Overview tab. This displays the count of errored packets categorized based on different error types and direction.



Viewing LTSSM State Transitions

You can use the **LTSSM Overview** tab in the lower pane of Protocol Viewer to get an overview of the LTSSM state transitions that occurred in the PCIe data captured by U4301A module in a trace. This pane provides an overview of the link training process by displaying a sequential list of the LTSSM states and their transitions and the packets exchanged during each state. You can use this information to verify the link training process and find out reasons for any failure in this process.



To get detailed information on how to use Protocol Viewer's LTSSM Overview pane, refer to the chapter "Viewing LTSSM States and State Transitions" on page 71.

Exporting Captured PCIe Data to a .csv File

You can export the captured PCIe packet information from the Protocol Viewer window to a specified .csv file and use it later in other analysis tools. You do this by clicking the  toolbar button in the Protocol Viewer window. On clicking this toolbar button, the **Protocol Export** dialog box is displayed in which you can specify the details of export such as the range of packet data that you want to export and the delimiter that you want to use to delimit the exported data in the specified .csv file.

For details on how to export data to a .csv file, click the Help button in the Protocol Export dialog box.

10 Viewing LTSSM States and State Transitions

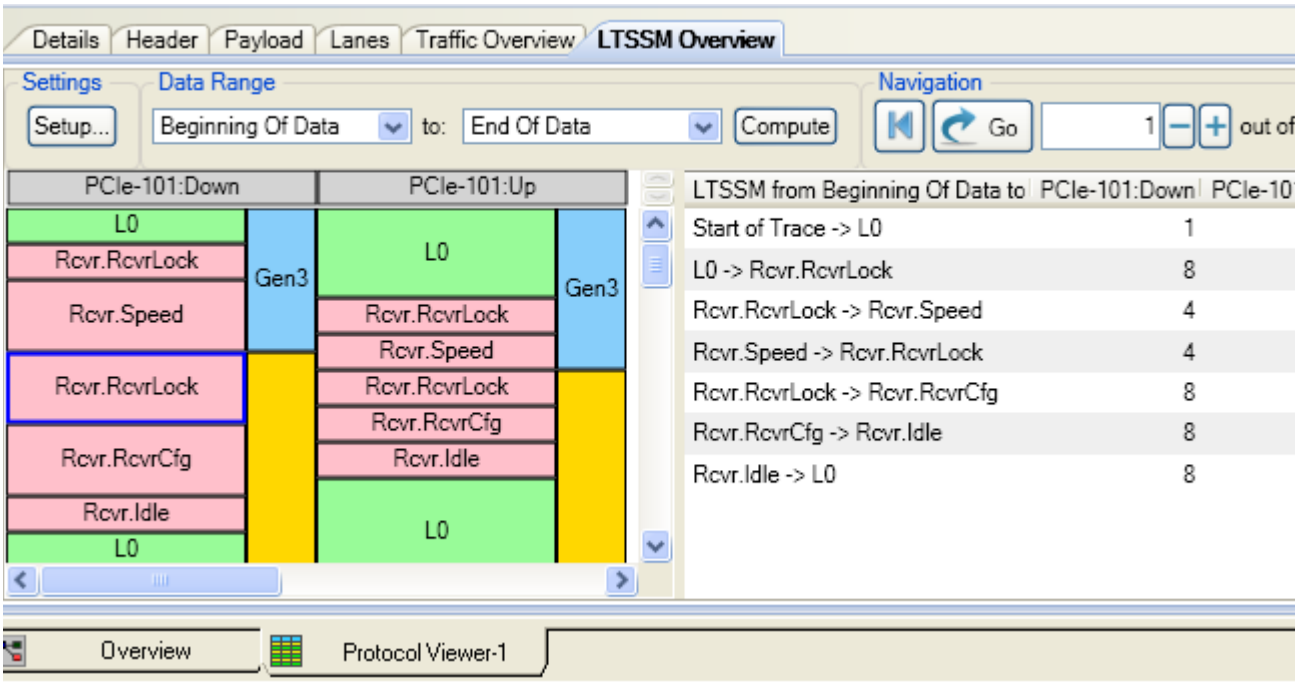
The U4301A PCIe Gen3 analyzer lets you view LTSSM states and their transitions as detected in the data captured in a trace to help you test or debug the DUT's LTSSM functions. This chapter describes how you can view these LTSSM states.

LTSSM Overview

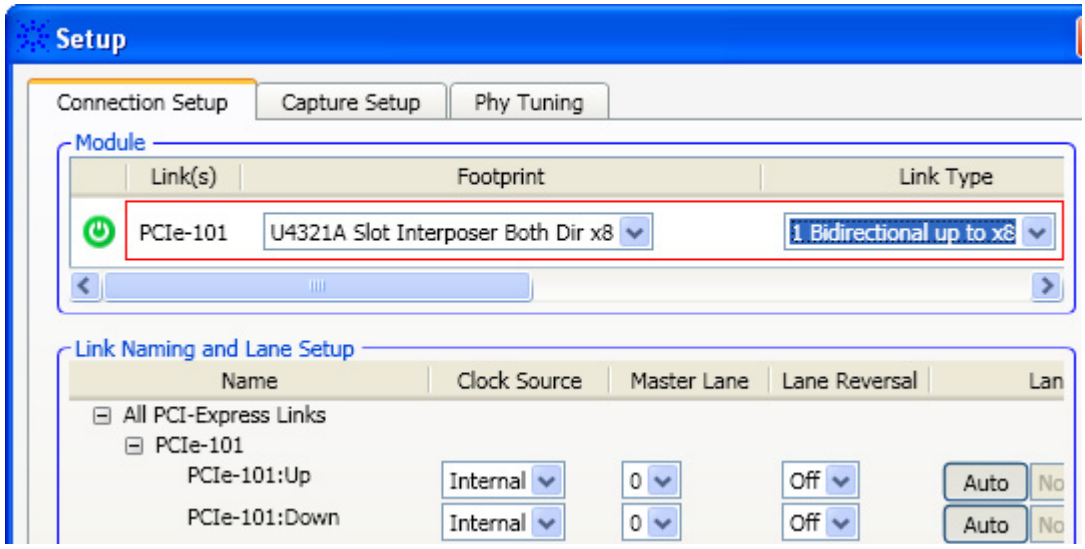
Link Training and Status State Machine (LTSSM) drives and controls the link initialization and training process for a PCIe device to enable the normal data exchange between the two PCIe devices over the link. LTSSM operates at the physical layer level and transits through various states and substates during link initialization, training, and management. During each of these states, appropriate physical layer packets (training sequences) are exchanged between the link partners to initialize, train, and manage the link.

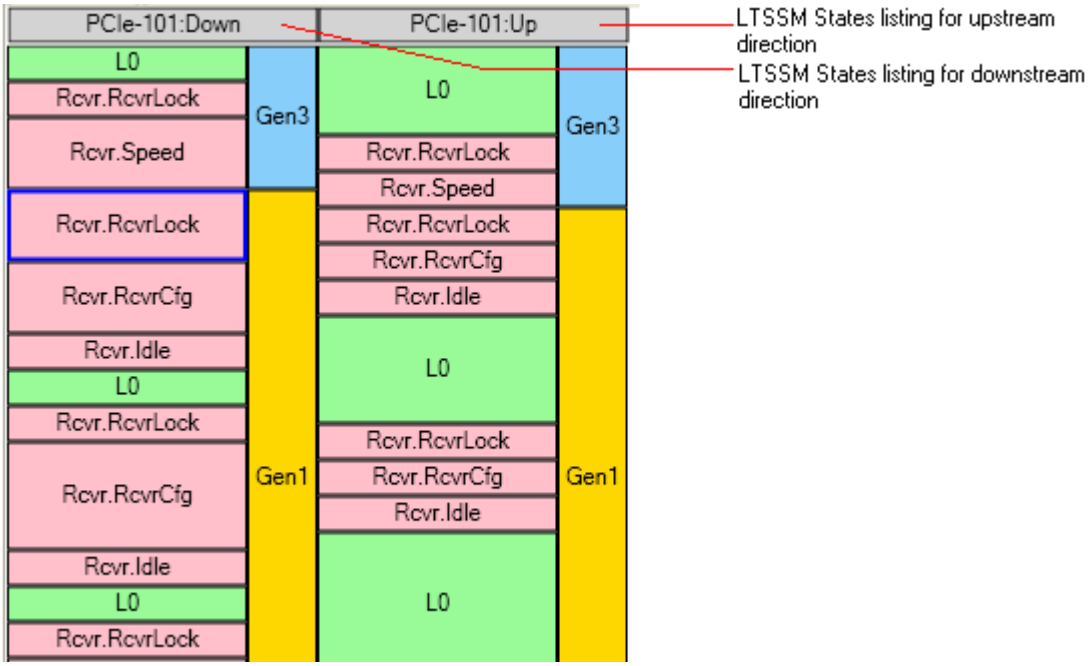
To begin communication with a PCIe device, the link training process must complete successfully. This makes link training one of the most crucial process in testing and validating a DUT. With so many states/substates and training sequences exchange involved in link training, it can be a challenging task to verify and debug this process.

The ***LTSSM Overview*** pane in the Protocol Viewer window of the Logic Analyzer GUI helps you in verifying the link training process and finding out reasons for any failure in this process. This pane provides an overview of the link training process by displaying a sequential list of the LTSSM states and their transitions and the packets exchanged during each state. To display these states and transitions, it analyzes a user-specified data range or the entire data captured in a trace and presents the list of states/transitions from that trace.



The LTSSM Overview pane can display LTSSM states and transitions for both upstream as well as downstream link directions. However, this display depends on how you configured the direction of data capture (upstream, downstream, or bidirectional) in the Connection Setup tab of the Setup dialog box of the U4301A module. For instance, if you configured a bidirectional data capture using U4301A, then LTSSM states are displayed for both directions.





Using the LTSSM Overview pane, you can view the LTSSM states and their transitions during events such as:

- Link initialization and configuration to bring the link to an operational state.
- Link recovery or retraining in situations such as speed changes, power management, or recovering from a link error.
- Downgrading or upgrading the link speed in response to a link speed change request.
- Performing the Equalization procedure before reaching the Gen3 (8.0 GT/s) speed during the link training or retraining.

Prerequisites

Before you can view LTSSM states and transitions, you need to ensure that:

- You have the appropriate node/server software license available and installed for the LTSSM Overview feature.
- You have set up the U4301A analyzer module and captured the PCIe data for the required direction(s).
- You have configured the LTSSM setup to get the data display in the LTSSM overview pane according to your requirements. (Described in the next section)

Configuring and Computing LTSSM States

To view LTSSM states in the LTSSM Overview pane, you need to configure the pane settings and initiate computation of the LTSSM states display based on these settings.

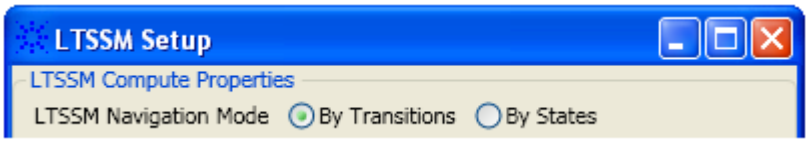
1 Access the captured data along with the U4301A setup details in the Logic Analyzer GUI.

2 Click the **Protocol Viewer** node connected to the U4301A module in the Overview window of the Logic Analyzer GUI.

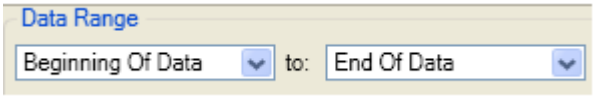
3 Click the **LTSSM Overview** tab in the lower pane of the Protocol Viewer window.

4 Configure the LTSSM setup to get a display of LTSSM states as per your requirements.

   a To configure how the states are displayed in the LTSSM Overview's navigation pane, click **Setup** and then select the appropriate LTSSM navigation mode - **By Transitions** or **By States** from the **LTSSM Setup** dialog box. '*By Transitions*' displays the LTSSM states transitions in the results for navigating through the occurrences of the state transition events in the analyzed data. 'By States' displays the LTSSM states in the results for navigating through the occurrences of the state entry events in the analyzed data.



   b In the **Data Range** groupbox, specify the start and end range for the captured data in the trace for which you want to display the LTSSM states and transitions. Only the specified range of data is analyzed to detect the LTSSM states. The default selections in the Data Range group box ensure that the LTSSM states are displayed for the entire trace. However, you can set markers in the packets listing in the upper pane and then specify the data range using these markers so that LTSSM states are displayed only for that specific range of packets.

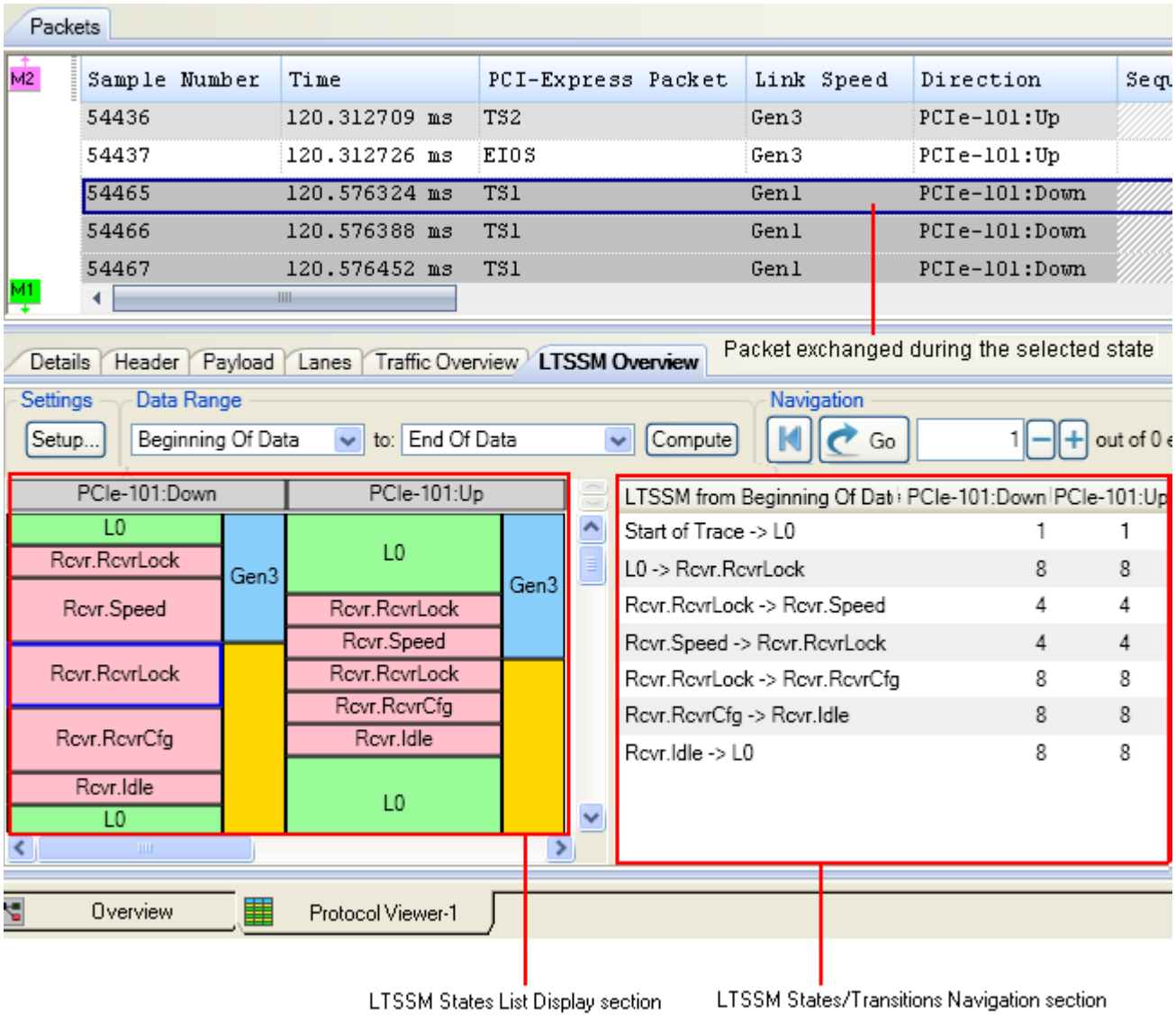


5 Click the **Compute** button displayed with the Data Range fields.

   The LTSSM states are computed and displayed for the specified data range and configured link direction.

Viewing LTSSM States/Transitions

The screen below displays the results of a compute operation for LTSSM states followed by a description of these results.



The LTSSM states results are displayed in the following two sections of the pane as highlighted in the above screen.

LTSSM States List Display section	This section displays a list of the LTSSM states in the sequence in which these occurred in the trace or the specified part of the trace. The states are grouped and listed for a link direction. In the above screen, LTSSM states are displayed for both upstream and downstream directions. For each state in this list, the applicable link speed during the state is also displayed. Clicking a speed in this list highlights the packet representing the transition to that speed in the upper pane of the Protocol Viewer. When you click a state in the list, the packet that is exchanged as the first packet for that state occurrence is highlighted in the upper pane of the Protocol Viewer. This provides you a quick start point for viewing and navigating through the packets exchanged during a particular state. Moving the mouse pointer to a state presents a tool tip with useful information about the state such as the time tag for the state and the packet exchanged at the state change.
LTSSM States/Transitions Navigation section	This section displays a list of the applicable LTSSM states or state transition names. The display of states or transitions in this section depends on whether you selected **By Transitions** or **By States** navigation mode in the LTSSM Setup dialog box. In the above screen, the display in the navigation section is as per the *By transitions* mode. For each of these states/transitions, the section displays the number of events representing the number of occurrences of these states or transitions in the analyzed data. For instance, in the above screen, the transition from Rcvr.Idle to L0 state occurred 8 times in each upstream and downstream direction making the total occurrences of this transition 16. Using this section, you can easily navigate through these occurrences of LTSSM states or transitions and the packets exchanged during these occurrences.

NOTE

You need to recompute the LTSSM states display results if you want to change:

- the data range for which results are to be displayed.
- the LTSSM navigation mode for the navigation pane.
- the link direction for which results are to be displayed.

You can hide or display the LTSSM Overview pane using the  toolbar button in the upper pane of the Protocol Viewer window.

Navigating Through the LTSSM States/Transitions Occurrences

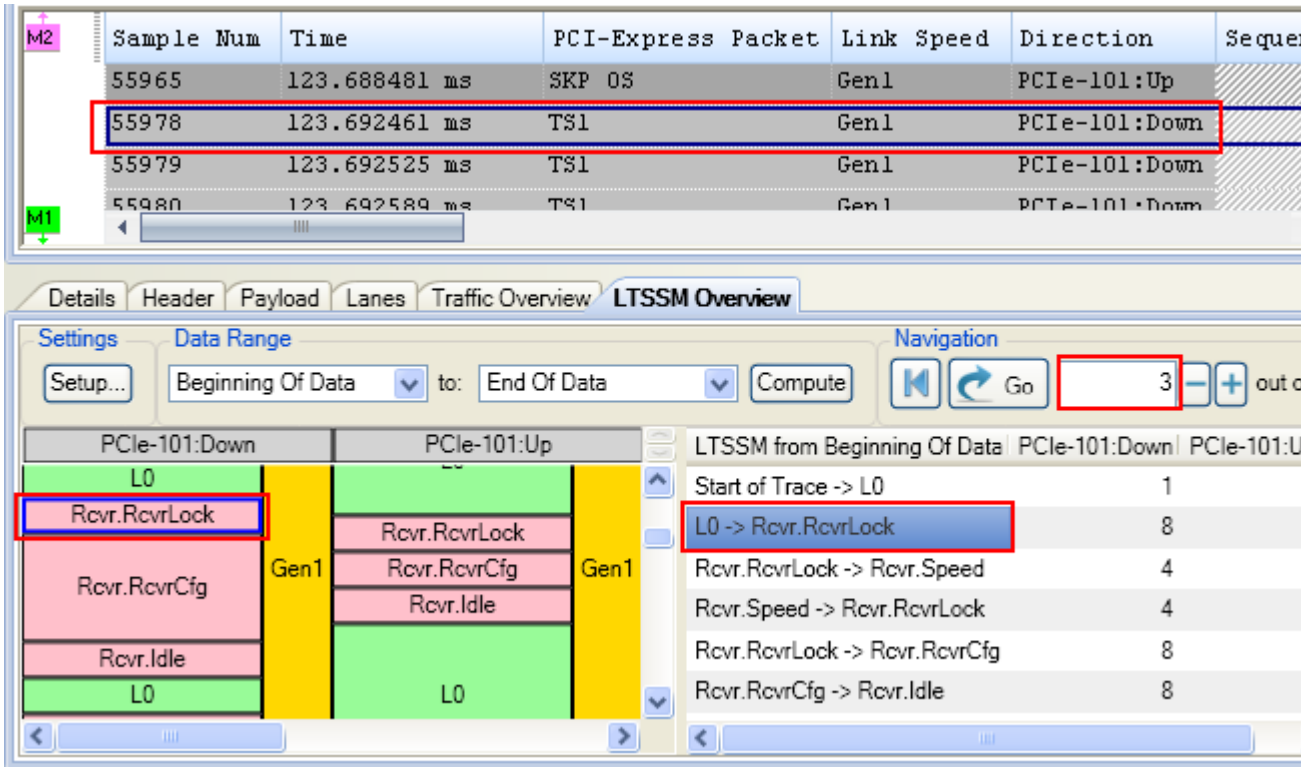
You use the Navigation groupbox in the LTSSM Overview pane to navigate through LTSSM states / transitions occurrences.

1 To navigate through the occurrences of a state for both the directions, select the particular state / transition name in the navigation section. To navigate through the occurrences of a state for a specific direction,

select the number of events displayed for that direction in front of the state / transition name in the navigation section.

2 Either type the number of occurrence to which you want to navigate in the Navigation groupbox and click **Go** or click the + or - buttons in the groupbox to sequentially move to next or previous occurrence of the state/transition.

The specified occurrence of the selected state/transition is highlighted in the state list display and the packet representing the state transition is highlighted in the upper pane of the Protocol Viewer window. For instance, in the following screen, the third occurrence of the transition from L0 to Rcvr.RcvrLock is highlighted in the states list along with the TS1 packet representing the beginning of the third occurrence of Rcvr.RcvrLock state.



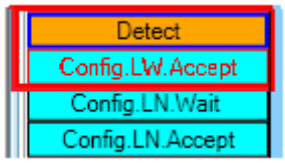
3 Click  toolbar button to navigate to the first packet of the first occurrence of the selected state/transition.

4 Click  toolbar button to navigate to the packet representing the transition to the last occurrence of the selected state/transition.

Interpreting LTSSM Overview Results

Following are some important points about interpreting the states and transitions displayed in the LTSSM Overview pane:

- **Errored LTSSM states** - If an LTSSM state is listed in red colored text, it indicates an erroneous state transition. Following is an example of an erroneous state transition from Detect to Config.LW.Accept. There should have been a transition to the Polling state after Detect.



- The following background color coding is used to represent the three speed in the speed column of the states listing.
  - Yellow - Gen1 (2.5 Gbps)
  - Green - Gen2 (5 Gbps)
  - Blue - Gen3 (8 Gbps)
- The pane displays LTSSM states as detected from the trace. If some events are not represented in the captured data in the trace, then these events will not be part of the LTSSM state transitions list in the LTSSM Overview pane.
- Except for the Configuration and Recovery states, the substates are not displayed for any other state. For instance, the substates of Polling such as Polling.Active, Polling.Compliance and Polling.Configuration are not displayed. Only the Polling state is listed in the pane.

Glossary

D

DUT Device Under Test.

I

interposer Describes a probing method where the probe is located between a slot and the PCI Express device under test.

M

midbus probe Describes a probing method where Soft Touch footprints are designed into a DUT board between the controller and the device under test.

11 Glossary

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