

# Agilent Logic and Protocol Analyzer

**User Guide** 



# Notices

© Agilent Technologies, Inc. 2001-2014

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Agilent Technologies, Inc. as governed by United States and international copyright laws.

#### **Trademarks**

ARM® and Thumb® are registered trademarks and ARM7TDMI(TM) is a trademark of ARM Limited.

Intel® and Pentium® are U.S. registered trademarks of Intel Corporation.

Java(TM) is a U.S. trademark of Sun Microsystems, Inc.

#### **Software Release version**

Version 05.80.0000

#### **Edition**

February 2014

Available in electronic format only

Agilent Technologies, Inc. 1900 Garden of the Gods Road Colorado Springs, CO 80907 USA

#### Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

#### **Technology Licenses**

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

#### **Restricted Rights Legend**

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

#### **Safety Notices**

#### CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

### WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

# Using the Agilent Logic and Protocol Analyzer

The Agilent Logic and Protocol Analyzer application is used with:

- modules in Agilent AXIe chassis (for example the U4154A Logic Analyzer module in M9502A portable 2-slot chassis)
- modules in Agilent Digital Test Console chassis (for example the U4002A portable 2-slot chassis)
- 16900-series logic analysis systems (see page 617), 16800-series logic analyzers (see page 614), and 1680/1690-series logic analyzers (see page 608) and 16850-series logic analyzers.
- It can also be used by itself on a Windows XP/Vista/7/8 computer for *remote access* (see page 85) of logic analysis systems on the network, or for *offline analysis* (see page 233) of captured data (including data captured on 16700-series logic analyzers).

This online help provides the following information.

- What's New (see page 19)
- Getting Started (see page 59)
- Probing the Device Under Test (see page 81)
- Connecting to a Logic Analysis System (see page 85)
- Setting Up the Logic Analyzer (see page 97)
  - Configuring Logic Analyzer Modules (see page 98)
  - "Setting Up Probes" (in the online help)
  - Setting the Logic Analyzer Threshold Voltage (see page 102)
  - Defining Buses and Signals (see page 104)
  - Choosing the Sampling Mode (see page 119)
  - Setting Up Symbols (see page 139)
  - Installing Licensed Hardware Upgrades (see page 147)
- Capturing Data from the Device Under Test (see page 149)
  - Setting Up Quick (Draw Box) Triggers (see page 152)
  - Specifying Simple Triggers (see page 156)
  - Specifying Advanced Triggers (see page 163)
  - Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)
  - Storing and Recalling Triggers (see page 201)
  - Running/Stopping Measurements (see page 203)
  - Saving Captured Data (and Logic Analyzer Setups) (see page 205)
  - Extending Capture Capability with VBA (see page 217)
- Analyzing the Captured Data (see page 219)

- Offline Analysis (see page 233) (after Loading Saved Data and Setups (see page 220))
- Analyzing Waveform Data (see page 239)
- Analyzing Listing Data (see page 259)
- Displaying Names (Symbols) for Bus/Signal Values (see page 269)
- Marking, and Measuring Between, Data Points (see page 271)
- Searching the Captured Data (see page 294)
- Comparing Captured Data to Reference Data (see page 305)
- Viewing Source Code Associated with Captured Data (see page 308)
- Analyzing Packet Data (see page 316)
- Analyzing the Same Data in Different Ways (Using the Window) (see page 345)
- Setting the System Trigger and Skew Between Modules (see page 351)
- Using Display Windows (see page 353)
- Printing Captured Data (see page 354)
- Extending Data Visualization/Analysis with VBA (see page 357)
- "Using Tools" (in the online help)
- "External Oscilloscope Time Correlation and Data Display" (in the online help)
- "Using the Pattern Generator" (in the online help)
- "Using the PCIe Gen3 Analyzer"
- Managing Software Licenses (see page 359)
- Updating Software (see page 367)
- Solving Problems (see page 371)
- Concepts (see page 409)
- **Reference** (see page 451)
- Glossary (see page 787)
- "COM Automation" (in the online help)
- "XML Format" (in the online help)
- See Also > "AXIe Based Logic Analysis and Protocol Test Modules Installation Guide"
  - , "16900-Series Logic Analysis System Installation Guide"
  - Installation/Quick Start Guide
  - "1680-Series Logic Analyzers Quick Start/Installation Guide"
  - Image: "I690-Series Logic Analyzers Quick Start/Installation Guide"
  - > "16850-Series Logic Analyzers Installation/Quick Start Guide"

# Contents

Using the Agilent Logic and Protocol Analyzer 3

#### 1 What's New

| ew                       |    |
|--------------------------|----|
| Version 05.70 What's New | 21 |
| Version 05.60 What's New | 23 |
| Version 05.50 What's New | 25 |
| Version 05.40 What's New | 27 |
| Version 05.30 What's New | 29 |
| Version 05.20 What's New | 31 |
| Version 05.00 What's New | 34 |
| Version 04.00 What's New | 36 |
| Version 03.83 What's New | 37 |
| Version 03.82 What's New | 39 |
| Version 03.80 What's New | 40 |
| Version 03.70 What's New | 41 |
| Version 03.67 What's New | 43 |
| Version 03.65 What's New | 44 |
| Version 03.60 What's New | 45 |
| Version 03.55 What's New | 46 |
| Version 03.50 What's New | 47 |
| Version 03.30 What's New | 49 |
| Version 03.20 What's New | 51 |

- Version 03.00 What's New 52
- Version 02.50 What's New 53
- Version 02.00 What's New 54
- Version 01.40 What's New 55
- Version 01.20 What's New 57
- Version 01.10 What's New 58

#### **2 Getting Started**

| Tutorial - Getting to know your logic analyzer 60  |
|--|
|  |
| Turning on the logic analyzer 61                   |
| Connecting to the device under test 61             |
| Setting up bus/signal names 62                     |
| Setting the acquisition mode 64                    |
| Setting up a simple trigger 64                     |
| Open the tutorial configuration file 65            |
| Using markers 66                                   |
| Zooming in on the data 67                          |
| Loading and saving configuration files 67          |
| Saving and recalling trigger setups 68             |
| Quick marker measurements 69                       |
| Searching data 70                                  |
| Toolbars, tool tips, and mouse shortcuts 71        |
| Measurement Examples 72                            |
| Making a timing analyzer measurement 72            |
| Making a state analyzer measurement 73             |
| To trigger on one of multiple edges or glitches 74 |
| To trigger on ranges 75                            |
|  |
| Demo Center 78                                     |

#### **3** Probing the Device Under Test

To control signals in the device under test 83

#### **4** Connecting to a Logic Analysis System

Connecting to the U4154A Logic Analyzer Module85To add a logic analysis system to the list87To delete a logic analysis system from the list88To refresh the logic analysis system list89To view logic analysis system details90

To enter your "System In Use" comments 91

To select a logic analysis system for auto-connect 92

To chat with another logic analysis system user 93

Setting Up Passwords for Remote Access 94

#### **5** Setting Up the Logic Analyzer

**Configuring Logic Analyzer Modules** 98 To disable and enable modules 98 To unsplit a split analyzer 100 Setting the Logic Analyzer Threshold Voltage 102 **Defining Buses and Signals** 104 To add a new bus or signal 105 To delete a bus or signal 106 To rename a bus or signal 107 To rename the bits of a bus 108 To assign channels in the default bit order 110 To assign channels, selecting the bit order 111 To use clock channels as extra data channels 112 To define buses and signals by importing netlist files 113 To reorder bits by editing the Channels Assigned string 114 To set the default number base 116 To set polarity 117 To add user comments 117 To add a folder 118 To alias a bus/signal name 118 To sort bus/signal names 118 Choosing the Sampling Mode 119 Selecting the Timing Mode (Asynchronous Sampling) 120 Selecting the State Mode (Synchronous Sampling) 122 In Either Timing Mode or State Mode 134 Using Timing Zoom 136 Setting Up Symbols 139 To create user-defined symbols 139 To load symbols from a file 141 To run the symbol reader outside the application 142 To create an ASCII symbol file 143 To change symbol reader options 143 To enter symbolic bus/signal values 146 Installing Licensed Hardware Upgrades 147

#### 6 Capturing Data from the Device Under Test

Setting Up Quick (Draw Box) Triggers 152 To set a Quick Trigger in the Waveform window 152 153 To set a Quick Trigger in the Listing window 154 To set a Quick Trigger in the Source window **Specifying Simple Triggers** 156 To specify bus patterns in a simple trigger 157 158 To specify signal levels in a simple trigger To set a bus/signal edge in a simple trigger 159 Specifying Advanced Triggers 163 **Reading Event and Action Statements** 165 Using Timers 165 Using Counters 166 **Using Flags** 167 To replace or insert trigger functions into trigger sequence steps 169 To specify bus/signal patterns 169 To set a bus/signal edge in an advanced trigger 171 To specify packet events (in "Find a packet" trigger function) 175 To specify a trigger sequence step's goto or trigger action 178 To specify default storage 179 To insert or delete events 180 To negate events 183 To change the evaluation order of AND/OR'ed events 184 To choose between a duration or occurrence count for events (timing mode) 184 To insert or delete actions (in a trigger sequence step) 185 To cut, copy, and paste trigger sequence steps 188 To delete trigger sequence steps 189 To show a trigger sequence step as Advanced If/Then trigger functions 189 To convert a trigger sequence step to Advanced If/Then trigger functions 190 To display or hide "If" clause comments 190 To clear the trigger sequence 192 Triggering From, and Sending Triggers To, Other Modules/Instruments 193 To arm one module with another module's trigger 193 To trigger other instruments - Trigger Out 198 To trigger analyzer from another instrument - Trigger In 199 **Storing and Recalling Triggers** 201 To store a trigger 201 To recall a trigger 202 To set the trigger history depth 202

| Running/Stopping Measurements 203                      |
|--|
| To change the "Go to Trigger on Run" option 204        |
| Saving Captured Data (and Logic Analyzer Setups) 205   |
| To save a configuration file 206                       |
| To export data to standard CSV format files 207        |
| To export data to module CSV format files 210          |
| To export data to module binary (ALB) format files 213 |
| To export data to 16700 ASCII format files 215         |
| Extending Capture Capability with VBA 217              |

7 Analyzing the Captured Data

220 Loading Saved Data and Setups 220 To open a configuration file To recall a recently used configuration file 222 To import 167xx fast binary data 223 To transfer module setups to/from multi-module systems 224 To set up multiple-modules with XML-format configurations 224 Using Data Import Modules 227 **Offline Analysis** 233 Analyzing 16700-Series Logic Analyzer Data 234 Offline Analysis on Logic Analyzers 235 **Offline Analysis on Personal Computers** 236 **Offline File Formats** 237 Analyzing Waveform Data 239 240 To change the display scale (time/division) To go to different locations in the captured data 242 To re-arrange waveforms 243 244 To overlay waveforms To find a bus/signal row 244 To view bus data as a chart 245 To show/hide parts of the waveform display 247 To insert or delete buses/signals 247 248 To group signals into a bus To expand/collapse buses 248 To insert separator rows 248 **Changing Waveform Window Properties** 249 253 Changing Bus/Signal Row Properties **Changing Analog Signal Row Properties** 256

Analyzing Listing Data 259 To go to different locations in the captured data 260 To re-arrange bus/signal columns 261 To find a bus/signal column 261 To show/hide parts of the listing display 262 To insert or delete buses/signals 262 **Changing Listing Window Properties** 263 **Changing Bus/Signal Column Properties** 265 Displaying Names (Symbols) for Bus/Signal Values 269 Marking, and Measuring Between, Data Points 271 To read the markers display and overview bars 272 To create new markers 272 To place markers in data 274 276 To go to a marker To center the display about a marker pair 277 To change a marker's snap to edge setting 277 To delete a marker 278 To create a new time interval measurement 279 To create a new sample interval measurement 280 To create a new value at measurement 282 To rename a marker 282 To send a marker to the back 283 **Changing Marker Properties** 284 Using Voltage Markers for Analog Signals (in the Waveform Display) 286 Searching the Captured Data 294 To quickly find bus/signal patterns 294 To find bus/signal patterns in the captured data 296 298 To find packet patterns in the captured data To find complex patterns in the captured data 302 To store, recall, or delete favorite find patterns 303 To specify "found" marker placement 304 **Comparing Captured Data to Reference Data** 305 To copy data to the reference buffer 305 To find differences in the compared data 306 306 To compare only a range of samples To offset the reference data 306 To run until a number of compare differences 307 To set Compare window properties 307

308 Viewing Source Code Associated with Captured Data To step through captured data by source lines 309 To go to captured data associated with a source line 309 310 To browse source files To search for text in source files 310 To go to the source line associated with the listing center rectangle 311 To edit the source code directory list 311 To select the correlation bus 312 **Changing Source Window Properties** 313 Analyzing Packet Data 316 Viewing the Packet Summary 319 Viewing a Selected Packet 328 **Changing Packet Summary Event Colors** 337 **Changing Protocol Viewer Window Properties** 338 340 **Changing Packet Summary Column Properties** Analyzing the Same Data in Different Ways (Using the Overview Window) 345 To open or display the Overview window 345 To add, duplicate, or delete windows and tools 346 To edit window or tool properties 348 To rename windows, tools, and modules 349 To redraw the Overview window 350 To delete the Overview window 350 Setting the System Trigger and Skew Between Modules 351 **Using Display Windows** 353 To add or delete display windows 353 To turn window tabs on/off 353 354 **Printing Captured Data** To print captured data 354 To copy text to the clip board 355 To copy a screen to the clip board 355 To install a printer 355 355 To connect a LAN Extending Data Visualization/Analysis with VBA 357 8 Managing Software Licenses To view active software license information 360 To activate software licenses 361

To access floating license servers 362

To borrow floating licenses and return them early 364

#### 9 Updating Software

#### **10 Solving Problems**

**Software Installation Problems** 372 Installation Errors on 1680-Series Logic Analyzers 372 If starting in offline mode is unexpected 373 If an ALA format configuration file won't open 374 Interpreting Error Messages 375 **Error Messages** 375 Warning Messages 386 **Informational Messages** 388 Eye Finder Info Messages 388 License Problems 390 390 License Not Available **Floating License Server Communication Timeout** 390 Translating Configuration Files from Other Logic Analyzers 392 To translate 167xG logic analyzer configuration files 392 To translate 16700-series logic analyzer configuration files 393 395 **Running Self Tests** 397 Accessing Japanese Online Help 400 If there are problems writing CDs on a 16900A, 16902A, or 16903A frame **Hibernation Is Not Supported** 401 402 Network Troubleshooting Guide Remote Desktop Set Up 405 For More Information 406 Intrinsic Support 408

#### **11 Concepts**

When should you use an oscilloscope?410When should you use a logic analyzer?411

```
What is a logic analyzer?
                           412
   Sampling clock in the timing analyzer
                                          412
   Sampling in the timing acquisition mode
                                             413
   Triggering the timing analyzer
                                   414
   Sampling clock in the state analyzer
                                        415
   Sampling in the state acquisition mode
                                            415
                                 416
   Triggering the state analyzer
Pod and Channel Naming Conventions
                                        418
Why Are Pods Missing?
                          419
Memory Depth and Channel Count Trade-offs
                                              420
Transitional Timing
                     422
Understanding State Mode Sampling Positions
                                                424
   Eye Scan in Logic Analyzers that Support Differential Signals
                                                                428
Understanding Logic Analyzer Triggering
                                          431
   The Conveyor Belt Analogy
                                431
   Summary of Triggering Capabilities
                                       432
   Sequence Steps
                      433
   Boolean Expressions
                          435
   Branches
               436
   Edges
            436
             437
   Ranges
           437
   Flags
   Occurrence Counters and Global Counters
                                               437
             438
   Timers
   Storage Qualification
                          439
   Strategies for Setting Up Triggers
                                      440
   Conclusions
                  444
ALA vs. XML, When to Use Each Format
                                         445
Multiframe Logic Analysis Systems
                                     446
Agilent Logic Analyzer vs. 16700 Terminology
                                              449
```

#### **12 Reference**

```
Menus
         453
   File Menu
               453
   Edit Menu
               454
   View Menu
                456
   Setup Menu
                 456
   Tools Menu
                458
   Markers Menu
                   460
                     461
   Run/Stop Menu
   Overview Menu
                    462
                  462
   Listing Menu
   Waveform Menu
                     462
   Compare Menu
                    463
   Source Menu
                  464
   Protocol Viewer Menu
                          464
   VbaView Menu
                    465
   Window Menu
                    466
   Help Menu
                467
Toolbars
          469
   Standard Toolbar
                     469
   Pattern Generator Toolbar
                             470
   Analyzer Setup Toolbar
                           471
   External Oscilloscope Setup Toolbar
                                      471
   Data Import Toolbar
                        472
   Probes Toolbar
                   472
   Markers Toolbar
                    472
   Run/Stop Toolbar
                      473
   Visual Basic Toolbar
                        473
   To customize toolbars
                          474
Marker Measurement Display Bar
                                  475
Windows
           476
   Waveform Display Window
                               476
                           482
   Listing Display Window
   Compare Display Window
                             485
   Source Display Window
                            486
   Protocol Viewer Display Window
                                    487
   VbaView Window
                      490
   Overview Window
                       491
```

494 Dialogs Advanced Clocking Setup Dialog 495 Advanced Trigger Dialog 496 Agilent Logic Analyzer Upgrade Dialog 497 Analyzer Setup Dialog 498 **Chat Dialog** 501 Chat Select Destination Dialog 502 **Choose a Protocol Family and Bus Dialog** 502 **Create a New Configuration Dialog** 503 E-mail Dialog 504 **Event Editor Dialog** 505 **Export Dialog** 506 **Export File Selection Dialog** 507 508 External Application Setup Dialog External Trigger Dialog 510 **Find Dialog** 511 Frame/Module Information Dialog 513 Import Dialog 514 Import Setup Dialog 515 Module Mapping Dialog 517 Module Skew and System Trigger Dialog 520 Netlist Import Dialog 520 **Offline Startup Options Dialog** 521 **Options Dialog** 522 Pod Assignment Dialog 524 Printing Data Dialog 525 **Properties Dialog** 526 **Range Properties Dialog** 526 **Recall Trigger Dialog** 527 **Run Properties Dialog** 529 Select Symbol Dialog 530 Select System to Use Dialog 531 Software Licensing Dialog 534 Source Viewer Properties Dialog 538 Specify Mapping Dialog 540 Split Analyzer Setup Dialog 541 Status Dialog 542 Symbols Dialog 545 System Summary Dialog 546 **Target Control Port Dialog** 549 **Thresholds and Sample Positions Dialog** 550

```
TimingZoom Setup Dialog
                              558
Trigger Functions
                   560
   Timing Mode Trigger Functions
                                   560
   State Mode Trigger Functions
                                  573
Data Formats
               588
   ALA Format
                 588
   Standard CSV Format
                          588
   Module CSV Format
                         589
   Module Binary (ALB) Format
                                 598
Object File Formats Supported by the Symbol Reader
                                                    600
General-Purpose ASCII (GPA) Symbol File Format
                                                601
   General-Purpose ASCII (GPA) Record Format Summary
                                                         602
   SECTIONS
                603
   FUNCTIONS
                 604
   USER
           604
   VARIABLES
                 605
   SOURCE LINES
                    606
   START ADDRESS
                      606
   Comments
                606
Product Overviews
                    608
   1680/1690-Series Logic Analyzer Product Overview
                                                      608
   16800-Series Logic Analyzer Product Overview
                                                 614
   16900-Series Logic Analysis System Product Overview
                                                         617
   U4154A Logic Analyzer Product Overview
                                             626
   16850-Series Logic Analyzer Product Overview
                                                 628
   Agilent Logic and Protocol Analyzer Application Product Overview
                                                                   631
Logic Analyzer Notes
                       635
                                           637
   1680/1690-Series Logic Analyzer Notes
   16740/41/42 Logic Analyzer Notes
                                       638
   16750/51/52 Logic Analyzer Notes
                                       640
   16753/54/55/56 Logic Analyzer Notes
                                          643
   16760 Logic Analyzer Notes
                                645
   16800-Series Logic Analyzer Notes
                                      651
                                   654
   16910/11 Logic Analyzer Notes
                                   656
   16950/51 Logic Analyzer Notes
   16960 Logic Analyzer Notes
                                658
   16962 Logic Analyzer Notes
                                668
   U4154A Logic Analyzer Notes
                                  676
   16850-Series Logic Analyzer Notes
                                      711
```

Specifications and Characteristics 714

1680/1690-Series Logic Analyzer Specifications and Characteristics 714 16740/41/42 Logic Analyzer Specifications and Characteristics 717 16750/51/52 Logic Analyzer Specifications and Characteristics 722 16753/54/55/56 Logic Analyzer Specifications and Characteristics 727 16760 Logic Analyzer Specifications and Characteristics 734 16800-Series Logic Analyzer Specifications and Characteristics 742 16910/11 Logic Analyzer Specifications and Characteristics 749 16950/51 Logic Analyzer Specifications and Characteristics 757 764 16960 Logic Analyzer Specifications and Characteristics 16962 Logic Analyzer Specifications and Characteristics 769 16900-Series Logic Analysis System Frame Characteristics 774 U4154A Logic Analyzer Specifications and Characteristics 775 779 16850-Series Logic Analyzer Specifications and Characteristics What is a Specification? 785 What is a Characteristic? 786

#### **13 Glossary**

Index

Agilent Logic and Protocol Analyzer Online Help

# What's New

In this release, version 05.80, of the Agilent Logic and Protocol Analyzer application, the following changes have been made:

- U4431A MIPI M-PHY Analyzer module The Agilent Logic and Protocol Analyzer application now adds support for a new AXIe-based module introduced with this release to capture and decode M-PHY, UniPro, UFS, SSIC, and CSI-3 data. This module is installed in an Agilent AXIe chassis and configured and controlled using the Agilent Logic and Protocol Analyzer application. Refer to the U4431 M-PHY Analyzer Online Help to know how to configure and use with module.
- U4301 PCIe Gen3 analyzer module -
  - You can now decode AHCI transactions as well in addition to NVMe and PCIe transactions from the data captured by the U4301 module. Refer to the topic *Computing and Viewing Decoded Transactions* in the U4301 PCIe Gen3 Analyzer Online Help for more information.
  - A new feature, *Flow Control* is now available in the PCIe Performance Overview tab of the Protocol Viewer. This feature allows you to compute and track the available flow control credits for the data trace that has bidirectional PCIe traffic. Refer to the topic *Viewing Offline Performance Summary* in the U4301 PCIe Gen3 Analyzer Online Help for more information.
- DDR/LPDDR tools enhancements -
  - A new tool named *DDR/LPDDR Custom Configuration Creator* has been added to the *Agilent DDR Setup Assistant and Eyefinder* software package. This tool allows you to define the footprints layout as per your custom probing solution used in the DDR/LPDDR setup and then create an XML configuration file based on this footprint information. Refer to the tool's online help to know more. The online help is accessible from the tool's GUI and also installed at <*logic and protocol analyzer install location*> \*help*\.
  - The *B4623 LPDDR Decoder* now supports decoding and displaying the entry to and exit from Self Refresh and Power Down events. Refer to the topic *Decoding Self Refresh and Power Down Events* in the *LPDDR Bus Decoder Online Help*.



- Five new LPDDR2/3 tests have been added to the DDR Post Process Compliance tool to handle compliance parameters related to power down and self refresh modes. Three of these tests have also been added to the Real Time Compliance tool.
- Support for DDR4 running at > 2.5GHz added.
- **Trigger on edge** For 16850-series and U4154A logic analyzer modules, you can now set a trigger on Rising, Falling, or Either edge in the Timing Asynchronous sampling mode as well as State –Synchronous sampling mode. Refer to the topics *Specifying Simple Triggers* and *Specifying Advanced Triggers* in the *Logic and Protocol Analyzer* online help.

#### See Also • "Version 05.70 What's New" on page 21

- "Version 05.60 What's New" on page 23
  - "Version 05.50 What's New" on page 25
- "Version 05.40 What's New" on page 27
- "Version 05.30 What's New" on page 29
- "Version 05.20 What's New" on page 31
- "Version 05.00 What's New" on page 34
- "Version 04.00 What's New" on page 36
- "Version 03.83 What's New" on page 37
- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.70 What's New

In this release, version 05.70, of the Agilent Logic and Protocol Analyzer application, the following changes have been made:

- **16850 series portable logic analyzers** With this release, the Agilent Logic and Protocol Analyzer application can also be installed and used with the newly introduced 16850 series portable logic analyzers. Refer to the topic *16850-Series Logic Analyzer Notes* to know more about this new series of logic analyzers.
- **Transaction decoding** You can now compute and view decoded transactions from the captured PCIe data using the newly added Transaction Decode tab in the Protocol Viewer. Currently, the support for decoding NVMe transactions is added. The transaction decoding feature is a licensed option. Refer to the help book *Viewing Decoded Transactions* in the U4301 PCIe Gen3 Analyzer online help to know more.
- Offline performance summary computation You can now compute and view offline performance summary from the captured PCIe data using the newly added PCIe Performance Overview tab in the Protocol Viewer. This tab presents statistics for various performance parameters in tabular as well as charts form. The offline performance summary feature is a licensed option. Refer to the help book *Viewing Offline Performance Summary* in the U4301 PCIe Gen3 Analyzer online help to know more.

#### See Also • "Version 05.60 What's New" on page 23

- "Version 05.50 What's New" on page 25
- "Version 05.40 What's New" on page 27
- "Version 05.30 What's New" on page 29
- "Version 05.20 What's New" on page 31
- "Version 05.00 What's New" on page 34
- "Version 04.00 What's New" on page 36
- "Version 03.83 What's New" on page 37
- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47

- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.60 What's New

In this release, version 05.60, of the Agilent Logic and Protocol Analyzer application, the following changes have been made:

- Windows 8 and Windows Server 2008 support added With this release, you can install the Agilent Logic and Protocol Analyzer application on a host with Windows 8 or Windows Server 2008 operating system.
- Enhancements have been made to the Eyescan feature The eyescan feature now supports scaling the voltage axis for an entire bus to a selected value in an eyescan diagram. To know more, refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690.
- **B462X software packages** Both A and B versions of the licenses for B4621/2/3 software packages are now supported in the Logic and Protocol Analyzer application. B version is an upgrade to A version and therefore provides additional capabilities and features. To know more about the feature difference, refer to the *Online help* of these software packages.
- **Repetitive run feature in the DDR Post Process Compliance tool** -You can now run the selected tests in a repetitive mode. To accomplish this, the tool runs the logic analyzer repetitively for data acquisition and then run the tests repetitively on the newly acquired data. To know more, refer to the *DDR Post Process Compliance Tool Online Help*.
- **BMC Firmware Upgrade utility** A new utility named BMC Firmware Upgrade has been provided. This utility upgrades the BMC firmware of a module to the latest version provided with the Logic and Protocol Analyzer software. To know more, refer to the *Agilent AXIe Based Logic Analysis and Protocol Test Module Installation Guide*.
- Support for five independent modules in a chassis You can now install and use five independent modules in an Agilent five-slot AXIe chassis. In earlier releases, a maximum of three module sets were supported. (A module set can be either a single module or a group of modules cabled together to operate as a module.)
- "Or-ing" ARM In support added in triggering You can now set the trigger configurations of an AXIe based module to ARM In from multiple modules in the same chassis or another connected chassis/ logic analysis frame (in a multiframe setup). An AXIe module can now receive ARM IN signals from an "OR'ed" combination of trigger out signals from multiple modules. Refer to the topic "To arm one module with another module's trigger" on page 193 to know more.
- See Also "Version 05.50 What's New" on page 25
  - "Version 05.40 What's New" on page 27

- "Version 05.30 What's New" on page 29
- "Version 05.20 What's New" on page 31
- "Version 05.00 What's New" on page 34
- "Version 04.00 What's New" on page 36
- "Version 03.83 What's New" on page 37
- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.50 What's New

In this release, version 05.50, of the Agilent Logic and Protocol Analyzer application, the following changes have been made:

- U4421A MIPI D-PHY Analyzer and Exerciser module The Agilent Logic and Protocol Analyzer application now adds support for a new module introduced with this release to send D-PHY stimulus and capture and decode D-PHY data. This module is installed in Agilent AXIe chassis and configured and controlled using the Agilent Logic and Protocol Analyzer application. Refer to the U4421 D-PHY Analyzer and Exerciser Online Help to know how to configure and use with module.
- U4301A PCIe Gen3 Analyzer module You can now use the Agilent Logic and Protocol Analyzer application to create a physical layer tuning (.ptu) file for tuning the U4301A analyzer for a DUT. The creation and fine tuning of a ptu file is now GUI based. For more information, refer to the topic *Tuning the Analyzer for a Specific DUT* in the U4301A PCIe Gen3 Analyzer Online Help.
- USB connectivity between AXIe chassis and host computer You can now connect the host computer to the AXIe chassis via PCIe or USB. The USB connectivity support has been added as a licensed option. Refer to the AXIe based Logic Analysis & Protocol Test Modules Installation Guide to know more.
- **B4621B, B4622B, and B4623B software packages** These packages replace the B4621A, B4622A, and B4623A software packages and have the following new additions/updates -
  - B4621B Decoder support for DDR4 added.
  - B4623B Decoder support for LPDDR3 added.
  - B4622B -
    - The three tools contained in this toolset now support DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, and LPDDR3. Several new tests have been added for DDR3/4 and LPDDR2/3.
    - A new tool *Real-Time Compliance Tool* has been added that evaluates DDR/LPDDR data in real- time to detect and report violations to compliance limits specified in DDR/LPDDR specifications. Refer to the *Real-Time Compliance Tool Online Help* to know more.
    - The DDR Validation Tool has been renamed to DDR Post Process Compliance Tool.

• DDR Setup Assistant and DDR Eyescan have been enhanced to include support for LPDDR3 and DDR4. These have also been updated to handle finding the chip select eyes in a separate measurement from the clock. Refer to the DDR Setup Assistant online help and Modifying General or Target-specific Scan Qualifications in this user guide to know more.

#### See Also • "Version 05.40 What's New" on page 27

- "Version 05.30 What's New" on page 29
- "Version 05.20 What's New" on page 31
- "Version 05.00 What's New" on page 34
- "Version 04.00 What's New" on page 36
- "Version 03.83 What's New" on page 37
- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.40 What's New

In this release, version 05.40, of the Agilent Logic and Protocol Analyzer application, the following changes have been made:

- U4301A PCIe Gen3 Analyzer module
  - LTSSM Overview pane added in the Protocol Viewer window You can now view the LTSSM states and their transitions for the PCIe data that you captured using the U4301 module. A new pane called LTSSM Overview has been introduced in the Protocol Viewer window to display these states and transitions. To know about this feature, refer to the topic *Viewing LTSSM States and Transitions* in the U4301 PCIe Gen3 Analyzer Online Help.
- U4154A Logic Analyzer module
  - Eyescan enhancements The eyescan feature of the U4154A module has been enhanced to allow you to modify the general as well as DDR-specific scan qualification. To know about these enhancements, refer to the topic *Modifying General or Target-specific Scan Qualification* in this Online Help.

#### See Also

- "Version 05.30 What's New" on page 29
- "Version 05.20 What's New" on page 31
- "Version 05.00 What's New" on page 34
- "Version 04.00 What's New" on page 36
- "Version 03.83 What's New" on page 37
- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54

- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.30 What's New

In this release, version 05.30, of the Agilent Logic Analyzer application, the following changes have been made:

- U4301A PCIe Gen3 Analyzer module
  - x8 bidirectional configurations supported on a single U4301A module – With this release, a single U4301A module can support a bidirectional (upto x8) configuration. You can use the same U4301A module to probe and capture data in both upstream as well as downstream directions. For detailed information on how to use the U4301A module in bidirectional configurations, refer to the PCI Express Gen3 Hardware and Probing Guide. This guide is available on www.agilent.com and also installed with the Logic Analyzer software at <Logic Analyzer Install location>\help\pdfs.
  - U4324A PCIe Gen3 Flying Lead probe support added Besides the existing probing options, you can now use the new U4324A flying lead probes with the U4301A Analyzer module. For detailed information on this probe and its setup, refer to the PCI Express Gen3 Hardware and Probing Guide. This guide is available on www.agilent.com and also installed with the Logic Analyzer software at <Logic Analyzer Install location>\help\pdfs.
- U4154A Logic Analyzer module
  - A new license option 01G has been introduced for the U4154A module. You now have two license options, 01G and 02G available for the U4154A module. Based on the license option that you purchase, the state speed for the U4154A module is set. A "01G" license sets maximum state speed of U4154A to 1.4Gbs. A "02G option sets it to 2.5Gbs. These license options do not however control and set the timing speed of the module. Besides setting the state speed to 2.5Gbs, the 02G option also provides High Resolution (4.8 ps of time resolution) in eyescans which is not available with the 01G option.
  - **Eyescan enhancements** The eyescan feature of the U4154A module has been enhanced to allow you to modify the unit interval settings, adjusting the sample position markers, enabling/disabling the marker placements to the center of the eye and setting sample positions to their suggested sample positions in a single click. To know about these enhancements, refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690 in this user guide.
- U4998A HDMI Protocol/Audio/Video Analyzer and Generator module
  - **MHL testing support added** Besides supporting HDMI 1.4a and 1.4b, the module now supports the MHL protocol as well. You can now use this module to test MHL source and sink DUTs as well. To know more, refer to the U4998A HDMI and MHL Protocol/Audio/Video Analyzer and Generator Online Help.

- The Protocol Viewer window has replaced the legacy Packet Viewer window. You can now use Protocol Viewer to display the data captured by the U4301A PCIe Gen3 Analyzer module. To know more about Protocol Viewer, refer to the topic Protocol Viewer Window in this user guide.
- See Also "Version 05.20 What's New" on page 31
  - "Version 05.00 What's New" on page 34
  - "Version 04.00 What's New" on page 36
  - "Version 03.83 What's New" on page 37
  - "Version 03.82 What's New" on page 39
  - "Version 03.80 What's New" on page 40
  - "Version 03.70 What's New" on page 41
  - "Version 03.67 What's New" on page 43
  - "Version 03.65 What's New" on page 44
  - "Version 03.60 What's New" on page 45
  - "Version 03.55 What's New" on page 46
  - "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 05.20 What's New

In this release, version 05.20, of the Agilent Logic Analyzer application:

- You can now use the Agilent AXIe M9536A Embedded Controller module as the host computer with the AXIe based instrument modules installed in AXIe chassis. The instrument modules that support this controller module include U4998A HDMI Analyzer, U4301A PCIe Gen3 Analyzer, and U4154A Logic Analyzer modules. The Embedded Controller module is a one-slot module that needs to be installed in slot 1 of the AXIe chassis.
- Windows 7 support has been added for the 16800 and 16900 series of Logic Analyzers with serial number MY51420101 or higher. With the 05.20.0000 release of the Agilent Logic Analyzer application, 16800-series logic analyzers and 16900-series logic analysis systems are shipped from the factory with Windows 7 operating system. Refer to the 16800 and 16900 Install guides to know about the Windows 7 specific procedures, firewall settings and the new recovery procedure of 16800 and 16900 series of Logic Analyzers for Windows 7. These guides are installed with the Logic Analyzer software at <Logic Analyzer Install location>\help\pdfs.
- U4301 PCIe Analyzer module The following changes have been made to the U4301A PCIe Gen3 Analyzer module.
  - The Protocol Viewer window now has an additional tab Traffic Overview" in its lower pane. This tab displays the traffic statistics for the captured PCIe packets displayed in the upper pane of Protocol Viewer. It displays the count of captured packets based on packet types and the link direction (upstream or downstream). Refer to the topic Viewing PCIe Gen3 Packets in the U4301 PCIe Gen3 Analyzer online help to know more.
  - A new feature "CSV Export" has been added to the Protocol Viewer window. This feature allows you to export the displayed PCIe packet data from Protocol Viewer to a specified .csv file. Refer to the topic "Viewing PCIe Gen3 Packets" in the U4301 PCIe Gen3 Analyzer online help to know more.
- U4154A Logic Analyzer module The following changes have been made to the U4154A module features.

- A new license option 01G has been introduced for the U4154A module. You now have two license options, 01G and 02G available for the U4154A module. Based on the license option that you purchase, the state speed for the U4154A module is set. A "01G" license sets maximum state speed of U4154A to 1.4Gbs. A "02G option sets it to 2.5Gbs. These license options do not however control and set the timing speed of the module. Besides setting the state speed to 2.5Gbs, the 02G option also provides High Resolution (4.8 ps of time resolution) in eyescans which is not available with the 01G option.
- The eyescans that you set up and run using the U4154A module now include a scan resolution selection feature. If you have the 02G license of the U4154A module, you can either choose a Normal or a High resolution for eyescans. To know more, refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690 to know more about the eyescan resolutions.
- You can now export eyescan data from the Eye Scan Sample Position and Threshold Settings dialog box to a specified .csv file. To know more, refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690.
- The Transitional / Store Qualified Half Channel 5.0 GHz mode is now available as a Timing mode sampling option for the U4154A module. For details on this mode, refer to "U4154A Logic Analyzer Notes" on page 676.
- See Also "Version 05.00 What's New" on page 34
  - "Version 04.00 What's New" on page 36
  - "Version 03.83 What's New" on page 37
  - "Version 03.82 What's New" on page 39
  - "Version 03.80 What's New" on page 40
  - "Version 03.70 What's New" on page 41
  - "Version 03.67 What's New" on page 43
  - "Version 03.65 What's New" on page 44
  - "Version 03.60 What's New" on page 45
  - "Version 03.55 What's New" on page 46
  - "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54

- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 05.00 What's New

In this release, version 05.00, of the Agilent Logic Analyzer application:

- You can now use the Agilent Logic Analyzer application with the new U4154A Logic Analyzer module hosted in the new Agilent AXIe chassis (for example the M9502A portable 2-slot chassis). U4154A is a 136 channel AXIe based high speed state and timing logic analyzer.
- Trigger capabilities have been enhanced with more levels and deeper bursts (burst levels increased from 4 to 8). New event counter added for specifying the trigger action.
- 12.5 GHz Timing zoom support added for the U4154A Logic Analyzer module. The support has been added for state as well as timing sampling modes.
- The eye scan feature has been added for U4154A to determine optimal threshold voltage and sample position settings for individual channels and automatic adjustment of these settings. Eye scan triggers added to add trigger conditions for the samples that U4154A takes during the eye scan.
- One state clock provided to generate state clock signals for the U4154A logic analyzer module. Four state clock qualifiers have been added to allow you to add conditions to the state clock using qualifiers.
- The Force Prestore option added in the sampling trigger position.
- Advanced probe settings enabled for U4154A and 16962 logic analyzers. You can enable or disable the peaking at the channel/pod/module level for the probing system used for these logic analyzers.
- Two full channel modes (Full channel at 2.5 GHz and Transitional / Store qualified Full channel at 2.5 GHz) and one half channel mode at 5.0 GHz supported for U4154A. Quarter channel timing mode and Transitional / Store qualified Half channel mode not available for the U4154A Logic Analyzer module.
- DDR Setup Assistant tool enhanced to support the set up of the U4154A Logic Analyzer using this tool with automated steps for determining and setting up the sample positions for command, address, and data read and write signals.
- Support for Agilent U4998A HDMI Protocol/Audio/Video capture and generate (PAG) module added. You can now use the Agilent Logic Analyzer application with this module hosted in the Agilent AXIe or AMP chassis.
- Data storage qualifiers, ASPM (power management) support, and lane viewer added in the U4301A PCIe 8 Gbps protocol analyzer.
- See Also "Version 04.00 What's New" on page 36
  - "Version 03.83 What's New" on page 37

- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 04.00 What's New

- The *Agilent Logic Analyzer* application adds support for the new Agilent Digital Test Console chassis (for example the U4002A portable 2-slot chassis) and the U4301 PCIe Gen3 analyzer blade. See "U4301 PCIe Gen3 Analyzer—At a Glance" (in the online help).
- The DDR Setup Assistant has been added. The DDR Setup Assistant helps you properly set up a logic analysis system given the type of logic analyzer, DDR bus, and probing solution. Many of the set up steps are now automated. See "DDR Setup Assistant—At a Glance" (in the online help).
- The "LPDDR Bus Decoder" (in the online help) software is now available; it lets you view transactions, commands, and data captured on LPDDR buses.

#### See Also • "Version 03.83 What's New" on page 37

- "Version 03.82 What's New" on page 39
- "Version 03.80 What's New" on page 40
- "Version 03.70 What's New" on page 41
- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.83 What's New

In version 03.83, of the Agilent Logic Analyzer application:

- Colorized DDR2/DDR3 eye scan measurements, using the 16962A logic analyzer module, were added. These measurements provide new DDR measurement capabilities:
  - Place sample points far more accurately than ever before to get the most reliable data capture.
  - View event qualified eye diagrams to assess both functional and parametric behavior of the device under test. With this new capability, you can rapidly view eye characteristics and identify design defects like inter-symbol interference and driver contention.
  - Gain signal integrity insight and identify problem signals quickly by simultaneously scanning all of the signals in your system.
- The N4851B MIPI D-PHY acquisition probe and N4861B MIPI D-PHY stimulus probe were supported. Also, the capabilities of existing N4851A and N4861A MIPI D-PHY probes are enhanced (as described below with the purchase of the N4851U-004).

MIPI D-PHY analysis additions:

- 3 and 4 lane analysis support at up to 940 Mb/s for the N4851B.
- 3 and 4 lane analysis support at up to 800 Mb/s for the N4851A (requires purchase of the N4851U-004 to access this capability).

Stimulus capabilities:

- 3 lane stimulus support at up to 1 Gb/s for the N4861B.
- 3 lane stimulus support at up to 500 Mb/s for the N4861A (requires purchase of the N4851U-004 to access this capability).

For more information, see "N4851A/B, N4861A/B MIPI D-PHY Acquisition/Stimulus Probes" (in the online help).

- The Add External Oscilloscope wizard was updated to support the latest Agilent oscilloscopes. For the complete list of supported oscilloscopes, see "External Oscilloscope Time Correlation and Data Display" (in the online help).
- The Add or Remove Agilent Logic Analyzer Software tool was updated to let you manage releases, that is, to let you remove old releases and free disk space. See Chapter 9, "Updating Software," starting on page 367.
- See Also "Version 03.82 What's New" on page 39
  - "Version 03.80 What's New" on page 40
  - "Version 03.70 What's New" on page 41

- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.82 What's New

In version 03.82, of the Agilent Logic Analyzer application:

- The new 16962A logic analyzer card was supported in the 16900-series logic analysis system. See "16962 Logic Analyzer Notes" on page 668.
- See Also "Version 03.80 What's New" on page 40
  - "Version 03.70 What's New" on page 41
  - "Version 03.67 What's New" on page 43
  - "Version 03.65 What's New" on page 44
  - "Version 03.60 What's New" on page 45
  - "Version 03.55 What's New" on page 46
  - "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 03.80 What's New

In version 03.80 of the Agilent Logic Analyzer application:

- Timing analysis modes and additional triggering capabilities were added to the 16960A logic analyzer. See "16960 Logic Analyzer Notes" on page 658.
- The *Agilent Logic Analyzer* application supported the Windows<sup>®</sup> Vista operating system in addition to the Windows<sup>®</sup> XP operating system.
- An option in the Filter/Colorize tool to specify how the operation is applied across multiple data sources was added. See "To change the "across all data" option" (in the online help).
- An option to accumulate waveforms in the Waveform window was added. See "To accumulate waveforms" on page 252.
- There were additions to the Signal Extractor tool to allow it to convert timing analysis captures of serial buses into samples that can be decoded and displayed using the Packet Decoder and Packet Viewer. See "What's New in the Signal Extractor Tool" (in the online help).

See Also • "Version 03.70 What's New" on page 41

- "Version 03.67 What's New" on page 43
- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.70 What's New

In version 03.70 of the Agilent Logic Analyzer application:

- Support for the new 16902B logic analysis system was added. See 16900-Series Logic Analysis System Product (see page 617).
- The N4850A DigRF v3 acquisition probe for decoding and displaying DigRF v3 signals and the N4860A DigRF v3 stimulus probe for generating digital signals to emulate baseband IC or RF IC signals was supported. See "N4850/60A DigRF v3 Acquisition/Stimulus Probes" (in the online help).
- The Run Properties dialog that lets you save captured data after each run and stop after a certain number of repetitive runs was added. See Run Properties Dialog (see page 529).
- The Protocol Development Kit (PDK) editor added intelligent context-sensitive popup menus that show valid XML elements and attributes at the cursor location. These popup menus make editing protocol definition files easier. There have also been some minor improvements to the protocol description file XML elements and attributes, the Packet Decoder tool, and the Packet Viewer window. See "Protocol Development Kit (PDK)" (in the online help).
- The COM Connection Tool for testing the COM Automation connection between a controller PC and a logic analysis system was added. See "Test your Distributed COM connection" (in the online help).
- The "Signal Extractor" (in the online help) tool was enhanced with new commands and debugging features to help extract data from one input bus/signal and place it on multiple output buses/signals.
- The *Agilent Logic Analyzer* application required the Windows<sup>®</sup> XP operating system and no longer supported the Windows 2000 operating systems.

**See Also** • "Version 03.67 What's New" on page 43

- "Version 03.65 What's New" on page 44
- "Version 03.60 What's New" on page 45
- "Version 03.55 What's New" on page 46
- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55

- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.67 What's New

In version 03.67 of the Agilent Logic Analyzer application:

- The Add or Remove Agilent Logic Analyzer Software tool was added to help you manage your logic analyzer software and keep it up to date. See Updating Software (see page 367).
- The "FPGA Dynamic Probe for Xilinx FPGAs" (in the online help) supported connecting to JTAG cables on remote PCs or logic analysis systems.
- The pattern generator was enhanced to: let you find instructions or vectors in the sequence, let you use macro, loop, and comment instructions when importing vectors from CSV format files (exporting to CSV format files still gives compiled sequences), and let you change the colors associated with instructions and macros. See "Using the Pattern Generator" (in the online help).
- The Add External Oscilloscope wizard was updated to set up an external oscilloscope module that can import digital channel data from mixed-signal oscilloscopes as well as analog channel data. Also, the update allowed external oscilloscope modules to be correlated with split logic analyzer modules. See " External Oscilloscope Time Correlation and Data Display" (in the online help).
- The external protocol analyzer correlation software supported the N5319A interconnect cable that provides more flexible cross-triggering (via flags). See "External Protocol Analyzer Time Correlation" (in the online help).
- The Status dialog was updated to show more information in the columns of the display and lets you choose which columns are displayed. See Status Dialog (see page 542).
- See Also "Version 03.65 What's New" on page 44
  - "Version 03.60 What's New" on page 45
  - "Version 03.55 What's New" on page 46
  - "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 03.65 What's New

In version 03.65 of the Agilent Logic Analyzer application:

- The new 16951B logic analyzer card was supported in the 16900-series logic analysis system. See 16950/51 Logic Analyzer Notes (see page 656).
- The new "Protocol Development Kit (PDK)" (in the online help) lets you edit and create protocol description files in order to decode, display, and trigger on customized packet data.
- See Also "Version 03.60 What's New" on page 45
  - "Version 03.55 What's New" on page 46
  - "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

### Version 03.60 What's New

In version 03.60 of the Agilent Logic Analyzer application:

- You could control the new 16901A logic analysis system. See 16900-Series Logic Analysis System Product (see page 617).
- The new 16950B logic analyzer card was supported in the 16900-series logic analysis system. See 16950/51 Logic Analyzer Notes (see page 656).
- The "FPGA Dynamic Probe for Altera FPGAs" (in the online help) add-in software was introduced; it lets you probe signals internal to FPGAs.
- You could set up an external protocol analyzer and a logic analyzer to cross-trigger and make time-correlated measurements (using markers). See "External Protocol Analyzer Time Correlation" (in the online help).
- You could open ALA format configuration files "read-only" in any *Agilent Logic Analyzer* application instance (without licenses for tools, windows, etc. that may be in the configuration). See ALA vs. XML, When to Use Each Format (see page 445).

#### See Also • "Version 03.55 What's New" on page 46

- "Version 03.50 What's New" on page 47
- "Version 03.30 What's New" on page 49
- "Version 03.20 What's New" on page 51
- "Version 03.00 What's New" on page 52
- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.55 What's New

In version 03.55 of the Agilent Logic Analyzer application:

- The E9524A MicroBlaze trace toolset updated the "inverse assembler" (in the online help) to support MicroBlaze version 5.
- See Also "Version 03.50 What's New" on page 47
  - "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 03.50 What's New

In version 03.50 of the Agilent Logic Analyzer application:

- You could control the new 16800-series logic analyzers (see page 614).
- You could view decoded packet data in the new Packet Viewer window. See Analyzing Packet Data (see page 316).
- The "Xilinx FPGA Dynamic Probe" (in the online help) added support for MicroBlaze trace cores (MTC) and there was a new E9524A MicroBlaze trace toolset that provides "inverse assembly" (in the online help).
- You could use the new Demo Center (see page 78) application to view logic analysis system feature demonstrations.
- You could use the new "Signal Extractor" (in the online help) tool to extract data from one input bus/signal and place it on multiple output buses/signals. This is useful for extracting I and Q data from simple serial protocols or remultiplexing high-speed digital data that has been demultiplexed onto additional logic analyzer channels.
- You could connect to another logic analysis system without having to go *offline* first. See Connecting to a Logic Analysis System (see page 85).
- There were improvements for multiframe logic analysis systems (see page 446), especially for *performance multiframe configurations*.
- You could rename the bits of a bus and view them when the bus is expanded in the Waveform display window. See To rename the bits of a bus (see page 108).
- You could add separator rows to the Waveform display window. See To insert separator rows (see page 248).
- A graphical trigger was added when viewing module details in the Status dialog (see page 542).
- You could import external data into the logic analysis system from module binary (ALB) format files as well as module CSV format text files. See Using Data Import Modules (see page 227).
- There was a "Force Prestore" option to ensure that the specified percentage of pre-trigger memory is is filled before the logic analyzer begins looking for a trigger. Timing mode used to behave this way while state mode did not. With the "Force Prestore" option, you can choose the desired behavior for both sampling modes. See To specify the trigger position (see page 134).
- You could use the logic analysis system's 10 MHz CLOCK IN input to keep a logic analyzer and an external oscilloscope in sync over long acquisitions. See " Correlation Drift Over Long Acquisitions" (in the online help).

#### 1 What's New

• You could export Listing display window data to 16700 ASCII format files. See To export data to 16700 ASCII format files (see page 215).

See Also

- "Version 03.30 What's New" on page 49
  - "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 03.30 What's New

In version 03.30 of the Agilent Logic Analyzer application:

- You could add an external oscilloscope without the time correlation fixture. Default (typical) deskew values for your logic analyzer and oscilloscope models were used. You could still use the time correlation fixture to get the most accurate deskew values for the actual instruments being used. See " External Oscilloscope Time Correlation and Data Display" (in the online help).
- You could import external oscilloscope data and view it faster with import and waveform drawing performance improvements.
- You could activate software licenses, access floating license servers, and borrow floating licenses much easier using the new license manager interface. See Managing Software Licenses (see page 359).
- You could import external data into the logic analysis system and analyze it just like data acquired by logic analyzer modules. See Using Data Import Modules (see page 227).
- You could use these new VBA (Microsoft Visual Basic for Applications) macros and VbaView windows:
  - SendToExcel VBA macro that sends captured data to Microsoft Excel.
  - *SendToPatternGeneratorModule* VBA macro that sends captured data to a pattern generator module.
  - *Timing Compare* VbaView window that compares timing analyzer data with a specified tolerance (plus or minus a number of samples).

See Tools Menu (see page 458), Windows Menu (see page 466), and the online help included with the macro or VbaView window.

- You could use MatLab in conjunction with the logic analysis system more easily with the new MatLab Connectivity and Analysis package. This licensed package contains these VBA macros and VbaView windows:
  - SendToMatLab VBA macro that sends logic analyzer data to MatLab.
  - *MatLab Analysis* VbaView window that sends logic analyzer data to MatLab for processing and displays the results in an XY scattergram chart.
  - *FFT* VbaView window that performs a Fast Fourier Transform on logic analyzer data and displays the results in a line chart.

See the online help included with the VBA macro and VbaView windows.

• You could use additional remote programming commands with the updated Remote Programming Interface (RPI) compatibility package. See "Using the Remote Programming Interface (RPI)" (in the online help).

- See Also "Version 03.20 What's New" on page 51
  - "Version 03.00 What's New" on page 52
  - "Version 02.50 What's New" on page 53
  - "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 03.20 What's New

In version 03.20 of the Agilent Logic Analyzer application:

- The 16760A logic analyzer card was supported in the 16900-series logic analysis system. See 16760 Logic Analyzer Notes (see page 645).
- You could import data from external oscilloscopes. The Agilent 6000-series oscilloscopes were added to the list of supported oscilloscopes. Also, a new VbaView window let you use the oscilloscope's web interface from within the *Agilent Logic Analyzer* application. See " External Oscilloscope Time Correlation and Data Display" (in the online help).
- The "Serial To Parallel" (in the online help) tool for converting serial data streams into parallel bus data was introduced.
- The "Xilinx FPGA Dynamic Probe" (in the online help) add-in software was updated to support automatic set up features.
- Pattern generator compiled vectors were saved in XML format configuration files as well as ALA format configuration files. See "Using the Pattern Generator" (in the online help).
- Microsoft Visual Basic for Applications (VBA) macros and VbaView windows were saved in XML format configuration files as well as ALA format files. See "Distributing VBA Code" (in the online help).
- You could disable multiple modules at the same time and choose whether or not to remove their connections to tools and display windows. When you leave connections, buses/signals associated with disabled modules remain in display windows, but they have no data. See To disable and enable modules (see page 98).

#### See Also • "Version 03.00 What's New" on page 52

- "Version 02.50 What's New" on page 53
- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 03.00 What's New

In version 03.00 of the Agilent Logic Analyzer application:

- The 16720A pattern generator card was supported in the 16900-series logic analysis system. See "Using the Pattern Generator" (in the online help).
- The *eye finder* feature for automatically adjusting state mode sampling positions was enhanced to automatically determine optimal threshold voltage settings as well. See Understanding State Mode Sampling Positions (see page 424).
- Microsoft Visual Basic for Applications (VBA) was been integrated into the *Agilent Logic Analyzer* application to let you easily automate measurements and add custom control and data visualization tools. See Extending Capture Capability with VBA (see page 217) and Extending Data Visualization/Analysis with VBA (see page 357).

#### See Also • "Version 02.50 What's New" on page 53

- "Version 02.00 What's New" on page 54
- "Version 01.40 What's New" on page 55
- "Version 01.20 What's New" on page 57
- "Version 01.10 What's New" on page 58

# Version 02.50 What's New

In version 02.50 of the Agilent Logic Analyzer application:

- The *eye finder* feature for automatically adjusting sampling positions in state mode was made available for 1680- and 1690-series logic analyzers (this feature was previously only available for logic analyzers in the 16900-series logic analysis system).
- The "Xilinx FPGA Dynamic Probe" (in the online help) add-in software was introduced; it lets you probe signals internal to FPGAs.
- The "General Purpose Probe" (in the online help) add-in software was added; it lets you set up probe definitions in order to:
  - Cause device under test pin/pad numbers to appear in the Buses/Signals setup tab.
  - Document logic analyzer pod connections.
  - Prepare for importing netlist files to automatically define buses/signals.
- The "PCI Express Analysis Probe" (in the online help) add-in software (for the N4220A/B PCI Express analysis probe) was introduced, and the new Packet Decoder tool was used to decode PCI Express bus data.
- In the window, a separate column for probes (general purpose, FPGA dynamic, PCI Express, etc.) was added, and you were able to access probe properties from there.
- See Also "Version 02.00 What's New" on page 54
  - "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 02.00 What's New

In version 02.00 of the Agilent Logic Analyzer application:

- You could control the new 16900-series logic analysis system (see page 617) and access the new features associated with it. The same *Agilent Logic Analyzer* application controls the 1680- and 1690-series logic analyzers and can be used by itself on Windows XP/2000 computers for *remote access* (see page 85) or *offline analysis* (see page 233).
- The ability to split logic analyzer modules was added. This is useful for analyzing buses with different clocks.

With multiple logic analyzer modules, the ability to identify which is the system trigger and specify the skew between the modules was added.

- The *eye finder* feature for automatically adjusting sampling positions in state mode was added for logic analyzers in the 16900-series logic analysis system.
- The ability to load program symbols from compiler-generated output files was added.
- The ability to display the high-level language source code associated with captured data and set up triggers based on source code locations was added in the new Source display window.
- A new dual-sample state sampling clock mode, often used to capture DDR memory bus activity, was added.
- The Netlist Import dialog was reorganized and a separate dialog for defining probes was added.
- New System Summary and Status dialogs for displaying information about the logic analysis system were added.
- Performance improvements were made: waveform drawing became much faster, and the *Agilent Logic Analyzer* application was made into a multi-threaded application.
- See Also "Version 01.40 What's New" on page 55
  - "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 01.40 What's New

Version 01.40 of the Agilent Logic Analyzer application:

- Let you display the same data in multiple windows by using the window (which replaced the previous Tool dialog); for example, you could display the same data filtered in one Listing window and unfiltered in another Listing window.
- In the Buses/Signals dialog, you could reorder bits assigned to a bus/signal name. This is useful in cases where buses in the device under test are not probed by consecutive logic analyzer channels.
- Also in the Buses/Signals dialog, you could import bus/signal names and assignments from a netlist file.
- Let you time-correlate data captured by the logic analyzer to data captured by external Infinitum oscilloscopes using the E5850A time-correlation fixture.
- Let you control logic analyzers with remote programs that communicate with the Instrument COM Automation Server, included with the *Agilent Logic Analyzer* application.
- Let you save more logic analyzer configuration information to generic XML configuration files. You could save trigger specifications in XML format and transfer them between different logic analyzers. Also, you could use portions of generic XML configuration files with several of the COM automation commands.
- Let you show statistics in interval markers and stop a repetitive measurement or send an e-mail message on particular statistic values.
- Let you use the Compare window's properties, and the Difference Properties tab, to specify the run until options. (The Compare window's Run Until button was removed.)
- Let you use the *quick pick* bus/signal name selection feature to quickly select from recently used names. This feature was added to the Filter/Colorize tool properties dialog and to the advanced trigger setup dialog.

| ➤ Bus/Signal    | My Bus 2               |
|-----------------|------------------------|
|                 |                        |
| Select from dia | alog Recent selections |

- When exporting data to comma-separated value (CSV) files, you could choose to export data from selected buses/signals. Also, you could select the number base of the data that is exported.
- In the advanced trigger setup dialog, you could re-group events.

- Let you lock the scrolling on display windows (for example, Waveform, Listing, or Compare) so that when one window is scrolled, all locked windows are scrolled as well. You can find the *Lock* property with other windows property settings.
- Let you set the delay between repetitive measurements so that you could look at the captured data before deciding whether to stop the measurement.
- See Also "Version 01.20 What's New" on page 57
  - "Version 01.10 What's New" on page 58

# Version 01.20 What's New

Version 01.20 of the Agilent Logic Analyzer application:

- Let you, in the timing (asynchronous) sampling mode, trigger on multiple glitches/edges.
- Let you perform a simple compare of captured data sets.
- Added the ability to save/load user-defined symbols to/from XML format logic analyzer configuration files.

This meant you could use text processing tools to re-format symbol information from software development tools, insert them into an XML format configuration file, and load them into the *Agilent Logic Analyzer* application.

- Contained an API and documentation to enable inverse assembler and analysis tool development.
- Extended its offline analysis capability to 16700-series logic analyzers.
- See Also "Version 01.10 What's New" on page 58

# Version 01.10 What's New

Version 01.10 of the Agilent Logic Analyzer application:

• Added a Japanese version of the online help.



- Tutorial Getting to know your logic analyzer (see page 60)
- Measurement Examples (see page 72)
- Demo Center (see page 78)

• 📕 "Quick Start for 16700-Series Users"

Tips for Experienced Users



### 2 Getting Started

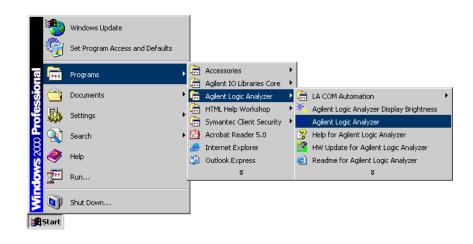
# Tutorial - Getting to know your logic analyzer

|                   | The following tutorial is intended to give you a quick of logic analyzer<br>basics. In addition to learning the concepts of logic analysis, you will see<br>some of the logic analyzer's more common features by going through a<br>measurement . Finally, you are shown some easy time saving tasks that<br>can quickly make you as productive as a more experienced user. |
|-------------------|---|
| Logic analysis    | • When should you use an oscilloscope? (see page 410)   |
| basics            | • When should you use a logic analyzer? (see page 411)  |
|                   | • What is a logic analyzer? (see page 412)  |
|                   | Timing analyzer:  |
|                   | • Sampling clock (see page 412)   |
|                   | • Sampling (see page 413)   |
|                   | • Triggering (see page 414)   |
|                   | State analyzer:   |
|                   | • Sampling clock (see page 415)   |
|                   | • Sampling (see page 415)   |
|                   | • Triggering (see page 416)   |
| Measurement       | The following does not require an active device under test. However, in order to show features that work on data, you are asked to load a configuration file between steps 5 and 6 that contains data to finish the exercise.   |
|                   | • Turning on the logic analyzer (see page 61)   |
|                   | • Connecting to the device under test (see page 61)   |
|                   | • Setting up bus/signal names (see page 62)   |
|                   | • Setting the acquisition mode (see page 64)  |
|                   | • Setting up a simple trigger (see page 64)   |
|                   | • Open the tutorial configuration file (see page 65)  |
|                   | • Using markers (see page 66)   |
|                   | • Zooming in on the data (see page 67)  |
| Time saving tasks | • Loading and saving configuration files (see page 67)  |
|                   | • Saving and recalling trigger setups (see page 68)   |
|                   | • Quick marker measurements (see page 69)   |
|                   | • Searching data (see page 70)  |
|                   | • Toolbars, tool tips, and mouse shortcuts (see page 71)  |
| See Also          | • Product s (see page 608)  |

#### Turning on the logic analyzer

[ Tutorial Home (see page 60) ] [ Next Topic (see page 61) ] [ Previous Topic (see page 416) ]

- 1 Plug in the power cable and press the front-panel On/Off button.
- 2 From the Windows Start bar, click **Start>Programs>Agilent Logic Analyzer>Agilent Logic Analyzer**.



#### NOTE

Toptional: If you have a logic analyzer shortcut icon on screen, double-click the icon.

#### Connecting to the device under test

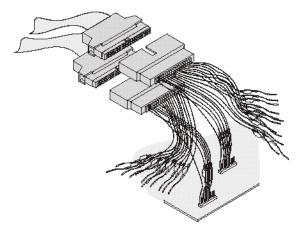
[ Tutorial Home (see page 60) ] [ Next Topic (see page 62) ] [ Previous Topic (see page 61) ]

The first step in using a logic analyzer is to probe signals in the device under test.

#### NOTE

In this tutorial, no probe connections are required. Later on in this tutorial, you are asked to load a configuration file containing data to simulate the results of a probed device under test.

#### 2 Getting Started



For more information about probing options, see Probing the Device Under Test (see page 81).

#### Setting up bus/signal names

[ Tutorial Home (see page 60) ] [ Next Topic (see page 64) ] [ Previous Topic (see page 61) ]

By default, the analyzer has one bus (My Bus 1) set up in the interface. The following exercise cleans up the display defaults and re-configures the bus/signal setup for a new measurement.

Delete bus/signal names 1 In the menu bar click Setup>(Logic Analyzer Module)>Bus/Signal....

2 In the Analyzer Setup dialog that appears, right-click on **My Bus 1**, then select **Delete**. Repeat until all bus signal names are deleted. After the last bus/signal is deleted, "My Bus 1" appears again as a default name.

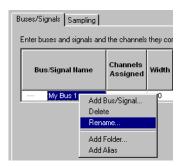
TIP

You can delete all bus/signal configurations at once with the **Delete All** button.

| Bus/Signal Nam  | P | Channels Width Threshold: T    |      |         |    |   |    |   |   |       |                                      |   |   |   |   |   |   |   |   |
|---|---|--------------------------------|------|---------|----|---|----|---|---|-------|--------------------------------------|---|---|---|---|---|---|---|---|
| Duoloighai hain                                       |   | Assigned                       | maan | -<br>15 | 14 |   | 12 |   |   | <br>9 | <b>a b b c b c c c c c c c c c c</b> |   |   |   |   | - | 0 |   |   |
| My Bus 1     My Bus 2     My Signal 1     My Signal 2 | D | dd Bus/Signa<br>elete<br>ename | il   | ~       | ~  | ~ | 1  | 1 | ~ | ~     | 1                                    | 1 | 1 | 1 | 1 | 1 | 1 | 1 | ~ |
|   |   | dd Folder<br>dd Alias          |      | •       |    |   |    |   |   |       |                                      |   |   |   |   |   |   |   | 1 |

Add new1In the Analyzer Setup dialog, right-click on My Bus 1, then selectbus/signal nameRename.

- 2 From the popup keypad that appears, type in the new name "counter".
- 3 Select OK.

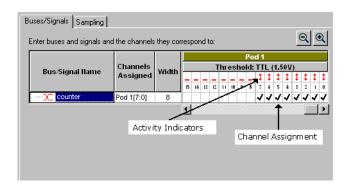


- Map signals into<br/>the analyzerThe logic analyzer must be told which probed signals from the device<br/>under test are to be included in the measurement, and how you want<br/>them grouped. In this exercise, you assign channels 0 7 on Pod 1 under<br/>the name "counter". Notice that when more than one channel is assigned<br/>to "counter" it becomes a bus.
  - 1 Check the activity indicators for verification of proper connection to the device under test. You should see a transition arrow on all 8 channels.

**NOTE** If you have real device under test hardware, you will see activity indicators as shown below. If you are loading the demo configuration file (later in this tutorial) you will not see activity.

**2** Click each **channel assignment box** under channels 0 - 7 on Pod 1. Notice that as you assign channels, the configuration information is updated for the bus/signal.

3 Click OK.



#### Setting the acquisition mode

[ Tutorial Home (see page 60) ] [ Next Topic (see page 64) ] [ Previous Topic (see page 62) ]

Under the Sampling tab of the Analyzer Setup dialog is where you set the analyzer to be either a timing or state analyzer. You also set either the timing options, such as memory depth or sampling period, or the state clocking options.

- 1 From the menu bar, click **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...**, or click the **H** icon in the toolbar.
- 2 Select Timing Asynchronous Sampling.

| Buses/Signals                    | Sampling           |  |  |  |  |  |  |  |  |
|----------------------------------|--------------------|--|--|--|--|--|--|--|--|
| Acquisition-                     |                    |  |  |  |  |  |  |  |  |
| ⊙ Timing - Asynchronous Sampling |                    |  |  |  |  |  |  |  |  |
| O State - S                      | nchronous Sampling |  |  |  |  |  |  |  |  |

3 Click OK.

#### Setting up a simple trigger

[ Tutorial Home (see page 60) ] [ Next Topic (see page 65) ] [ Previous Topic (see page 64) ]

The Simple Trigger is a quick way to configure the analyzer to trigger on either a data pattern on a bus, or an attribute of a single signal such as a rising edge or a low logic level.

- 1 In the Simple Trigger column, click on the **pattern qualifier** and set it to **Equal**.
- 2 Click in the text entry field 5 m and enter the data pattern "E5".

| Bus/Signal   | Simple Trigger | -150 ns -100 ns |
|--------------|----------------|-----------------|
| œ-•∎ counter | =, E5 🛄        |                 |

#### Open the tutorial configuration file

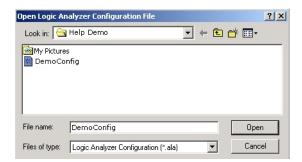
[ Tutorial Home (see page 60) ] [ Next Topic (see page 66) ] [ Previous Topic (see page 64) ]

At this point in a measurement, you would normally run the logic analyzer. However, because you are not connected to a device under test, you cannot capture real data. You will have to load a configuration file that contains this data.

Load the 1

1 Select File>Open.

- configuration file
- 2 From the file manager dialog, select the file named DemoConfig.ala from the following directory: C:\Documents and Settings\All Users\ Documents\Agilent Technologies\Logic Analyzer\Default Configs\ Agilent\Help Demo\
- 3 Select Open.



**View the data** Notice how the logic analyzer triggered on data pattern E5 and placed it in the center of the display. The red line shows that the trigger point is at the start of the data pattern E5.

|             |                | Mi 🗋 W5                         |
|-------------|----------------|---------------------------------|
| Bus/Signal  | Simple Trigger | -100 ns -50 ns 0 s 50 ns 100 ns |
| Sample Nurr |                | 47 47                           |
| Time        |                | -117.5 ns 117.5 ns              |
| ⊞‡ counter  | <b>=,</b> E5 🔳 |                                 |

#### **Using markers**

marker

[ Tutorial Home (see page 60) ] [ Next Topic (see page 67) ] [ Previous Topic (see page 65) ]

Markers are used for creating reference points in data. Once markers are placed in data, you can use them to quickly see what time, sample, or data value the marker is set on.

To create a 1 From the menu bar, click Markers>New.

- **2** From the New Marker dialog that appears, configure the new marker and if desired, specifically a position it in data. When you do not position the marker, by default it is placed at the trigger point.
- 3 Select OK.

| New Marker       |                | ×       |
|------------------|----------------|---------|
| Name M3          |                | ОК      |
| Background Color | <b>•</b>       | Cancel  |
| Foreground Color |                |         |
| Position         | 0 s 📓 - + from | Trigger |
| Comments         |                |         |
|                  |                |         |

- To place a marker<br/>in dataWhen you first create a new marker, you have the option to place it in<br/>data at a specific point in time or a specific sample number. The following<br/>exercise shows you other ways to position markers in data.
  - 1 In the display, click on marker M3 (your new marker) and while holding the mouse button down, drag maker M3 to -100ns before trigger, then release. Notice that the marker position value changes as you move it.
  - 2 From the menu bar, click Markers>Place On Screen, then select M1 and click OK. Notice how M1 is placed at center screen at the red trigger line.
  - **3** Point the mouse cursor at any desired point in data, then right-click and select **Place Marker**. From the Place Marker dialog that appears, choose the M2 marker. Notice that the marker is placed where the mouse was pointing.
- Go To a marker in<br/>dataOnce you have markers set in data, you can quickly find any of them as<br/>follows.
  - 1 From the menu bar, click Markers>GoTo.
  - 2 Select the marker you want to find, and click OK.

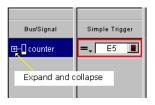
#### Zooming in on the data

[ Tutorial Home (see page 60) ] [ Next Topic (see page 67) ] [ Previous Topic (see page 66) ]

Data from a timing analyzer is displayed (as on an oscilloscope) as waveforms on a horizontal time axis. To zoom in or out on a waveform, change the Scale (time/division) of the time axis of the waveform.

Both state and timing analyzers can have multiple signals grouped together in a bus. To get a view of all signals, you can expand a bus into individual signals.

**Expand a bus** Click the "+" symbol just to the left of the bus named "counter". The collection of signals under "counter" breaks out into individual signals named counter[0] - counter[7].



**Change the scale** Click the zoom out icon to expand the signals to where you want them.

| Scale 5 ns/div |                | Delay   |
|----------------|----------------|---------|
| Bus/Signal     | Simple Trigger | -25     |
| ⊞-‡ My Bus 1   | = * 🗶 🖩        | 5C \ 51 |

#### Loading and saving configuration files

[ Tutorial Home (see page 60) ] [ Next Topic (see page 68) ] [ Previous Topic (see page 67) ]

Many times it is quicker to open an existing configuration file with a similar setup than to create a new configuration from scratch. You simply open a similar file, make the appropriate changes to the setup, then save the file as a new filename.

#### NOTE

When you rename an existing configuration file, you retain the saved trigger setups and "Find" search favorites from the first configuration file.

You already have learned how to open a configuration file. In the following exercise, you will save the "democonfig" file to a new name.

- 1 From the menu bar, click File>Save As....
- 2 From the file manager dialog that appears, type in the new name "myconfig", then click **Save**.

| Eile   |            |
|--|------------|
| New 1  | Ctrl+N     |
| 🚰 Open   | Ctrl+O     |
| ⊆lose  | Ctrl+F4    |
| 📕 <u>S</u> ave   | Ctrl+S     |
| Save <u>A</u> s  |            |
| Import   | Ctrl+I     |
| Export   | Shift+E    |
| 🖨 Print  | Ctrl+P     |
| <recent configurat<="" th=""><th>ion Files&gt;</th></recent> | ion Files> |
| E <u>×</u> it  |            |

### Saving and recalling trigger setups

[ Tutorial Home (see page 60) ] [ Next Topic (see page 69) ] [ Previous Topic (see page 67) ]

Each time you set up a new trigger and run the measurement, the trigger setup is saved in the logic analyzer. It is quicker to recall a trigger setup rather than re-configure the trigger setup each time.

| NOTE                         | The logic analyzer must be run before the trigger setup is stored. Also, trigger setups are stored as part of the configuration file. If you load a new configuration file, the trigger setups will be overwritten by trigger setups stored with the new file. |
|------------------------------|--|
| To recall a trigger<br>setup | <ol> <li>From the menu bar, click Setup&gt;(Logic Analyzer Module)&gt;Recall Trigger</li> <li>From the lower list, select the desired trigger setup, then click OK.</li> </ol>   |
| TIP                          | When the list of most recently used triggers get long, you can store the most often used triggers in the upper favorites list.   |

| 👯 Recall Trigger  | x            |
|---|--------------|
| Stored Favorite Triggers<br>If My Bus 1 = 8F Then Trigger and fill memory | OK<br>Cancel |
|   | Rename       |
|   | Clear        |
| Store Selected Recent Trigger To Favorites List                           | Clear All    |
| Most recently used triggers (added after each run)                        | Details      |
| If Anything Then Trigger and fill memory                                  | Open         |
|   | Help         |
|   |              |

### **Quick marker measurements**

[ Tutorial Home (see page 60) ] [ Next Topic (see page 70) ] [ Previous Topic (see page 68) ]

You can quickly read the time or number of samples between markers.

- 1 Click Markers>New Time Interval Measurement.
- 2 Configure the Interval dialog to display the time from **Beginning of Data** to **Trigger** as shown below.

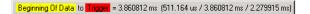
| Time In | terval          |            |    |         |        | × |
|---------|-----------------|------------|----|---------|--------|---|
| From    | Beginning Of Da | ta 💌       | to | Trigger |        | • |
|         |                 | Properties |    | ОК      | Cancel |   |

To show statistics with the time interval measurement (after repetitive runs, click **Properties**; then, in the Interval Properties dialog, check **Show statistics**.

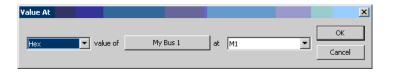
| Interval Properties          | ×            |
|------------------------------|--------------|
| Run Until<br>When interval > | OK<br>Cancel |
| Show statistics              |              |

Click **OK** to close the Interval Properties dialog, and click **OK** to close the Time Interval dialog.

After a repetitive run, the result of the time interval measurement is displayed in the marker measurements display bar.



- 3 Click Markers>New Value At Measurement.
- 4 Configure the Value At dialog to display the Hex value of My Bus 1 at M1 as shown below; then, click OK.



The result of the value at measurement My Bus 10[M1 = 4B] is displayed in the marker measurement display bar.

#### Searching data

[ Tutorial Home (see page 60) ] [ Next Topic (see page 71) ] [ Previous Topic (see page 69) ]

You can search for a data pattern on a bus or a signal. You can also choose when the search begins and ends. Finally, you can save the search criterion in a favorites list.

- 1 From the menu bar, click Edit>Find....
- **2** In the Find dialog, configure the search criterion as shown below to find "AA".
- 3 Select Find.

| M I   |           |         |            |           |           |           |         | Found   |       |      |        |        |     |     |        |       |     |
|-------|-----------|---------|------------|-----------|-----------|-----------|---------|---------|-------|------|--------|--------|-----|-----|--------|-------|-----|
|       | 23.672    |         |            |           | 876 us    |           |         | 23.68 0 |       |      |        | .684 u |     |     |        | 88 us |     |
|       | i i [     | 1.1     | 1 1 1      | 1.1       | 1         | 1         | 1 1     | ۲ i     | 1 1   | 1 1  | 1.1    | 1      | 1.1 | 1   | 1.1    | 1 1   | 1.1 |
| A     | .5        | A6      |            | A7        | X AI      | • X       | A9      |         | AA    | X    | AB     | Х      | AC  | Х   | AD     | X_#   | \E  |
|       |           |         |            |           |           |           |         |         |       |      |        |        |     |     |        |       |     |
|       | Find      |         |            |           |           |           |         |         |       |      |        |        |     |     |        |       | X   |
| Fin   | a         | 1       | <b>-</b>   |           | occurrent | e cearch  | aina    | Forwar  | d 😽   | from | Displa | u Cop  | -or |     |        |       | ~   |
| 1.0.0 | u j       | •       |            | , CO      | occurrent | .e searci | mig     | Forwar  | u 💌   | mon  | Dispia | y Cerr | .cr |     |        |       |     |
| l lr  | ➤ Bus/:   | Signal  | <b>v</b> ( | My Bu     | s 1       | × A       | ll hits | -       |       | ~    | AA     |        | Hex | ភ   |        |       | _   |
|       |           |         |            |           |           |           | i bico  |         |       |      |        |        |     | 9   |        |       |     |
| \     | Vhen En   | tering  |            | ~         | *         |           |         |         |       |      |        |        |     |     |        |       |     |
|       |           |         |            |           |           |           |         |         |       |      |        |        |     |     |        |       |     |
|       |           |         |            |           |           |           |         |         |       |      |        |        |     |     |        |       |     |
|       |           |         |            |           |           |           |         | - —     |       |      |        |        |     |     |        |       | _   |
| 5     | tore Favo | orite 🍣 | Reca       | all Favor | ite 🍣     | Clea      | ar      | Op      | tions |      | Find   |        | C   | ose |        | Help  |     |
|       |           |         | -          |           |           |           |         |         |       |      |        |        |     |     | $\sim$ |       |     |

As you configure the Find dialog, try to think of it as constructing a sentence that reads left-to-right.

"Find the 1st occurrence searching Forward from Display Center, on a bus named My Bus 1, including All bits, a pattern that Equals AA".

#### Toolbars, tool tips, and mouse shortcuts

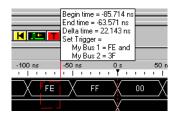
[ Tutorial Home (see page 60) ] [ Previous Topic (see page 70) ]

Throughout this tutorial, the menu bar has been used to access features. There are two other ways to access features as well as other useful tips that can save you time.

**Toolbars** Below the menu bar are groups of icons that represent shortcuts to many dialogs and features. For more information refer to Toolbars (see page 469) in the main help.

D 🛎 🖬 🖨 👬 🕷 🐂 🖬 🛏 T 🍽 Q Q 🛛 📴 봤 🚾 🔰 🏏 🏏 🏏 🗡

- **Mouse Shortcuts** There are many mouse shortcuts available. To access them simply point the mouse over a screen element such as a marker, or screen area, then right-click the mouse. Mouse shortcuts are especially useful within the waveform and listing data display areas.
  - **Tool Tips** Tool tips are small information displays that appear during operations such as moving markers, setting a trigger with the mouse, or hovering the mouse over a bus/signal name. Use them as comments (see page 117), or to monitor your progress or current positions.



| ⊞ 🛾 My Bus 1     | =, 🛛 🖬       |
|------------------|--------------|
| ⊞ My Bus 2 Pod 1 | [7:0]        |
| This i           | s a comment. |

#### 2 Getting Started

# **Measurement Examples**

The following measurement examples show you the typical order of steps to set up and run a measurement. As you go through the examples, you will encounter steps such as probing or triggering where alternative choices are available. In these steps, select the probing or trigger example that best fits your measurement.

- Making a timing analyzer measurement (see page 72)
- Making a state analyzer measurement (see page 73)
- To trigger on one of multiple edges or glitches (see page 74)
- To trigger on ranges (see page 75)

#### **See Also** • Tutorial - Getting to know your logic analyzer (see page 60)

- Timing Mode Trigger Functions (see page 560)
- State Mode Trigger Functions (see page 573)

#### Making a timing analyzer measurement

The following measurement example shows you the steps necessary to configure and run the logic analyzer for a typical timing analyzer measurement. As you go through the example, make the appropriate choices from the selection lists that best match the kind of configuration you need.

| TIP                       | If you are new to logic analysis, refer to "Tutorial - Getting to know your logic analyzer (see page 60)" for a quick tutorial on logic analysis concepts and measurements.  |  |  |  |  |  |  |  |  |
|---------------------------|--|--|--|--|--|--|--|--|--|
|                           | <ol> <li>Connect the probing to the device under test (see Probing the Device<br/>Under Test (see page 81) for more information).</li> <li>Turn on the logic analyzer.</li> </ol>  |  |  |  |  |  |  |  |  |
| Bus and signal<br>setup   | <ol> <li>In the menu bar, select Setup&gt;(Logic Analyzer Module)&gt;Bus/Signal</li> <li>From the Buses/Signals tab, assign bus/signal names to the device under test signals probed. You do this by either renaming (see page 107) existing names, or deleting (see page 106) and creating (see page 105) new names.</li> </ol> |  |  |  |  |  |  |  |  |
|                           | <b>3</b> From the Buses/Signals tab, define buses and signals (see page 104) under the appropriate pods for all probed buses/signals on the device under test.   |  |  |  |  |  |  |  |  |
| Acquisition mode<br>setup | <ol> <li>In the Analyzer Setup dialog, select the Sampling tab.</li> <li>From the Sampling tab, set the acquisition mode to Timing -<br/>Asynchronous Sampling.</li> </ol>   |  |  |  |  |  |  |  |  |

|                     | Buses/Signals       Sampling         Acquisition       O         O       Timing - Asynchronous Sampling         C       State - Synchronous Sampling  |    |
|---------------------|---|----|
|                     | <b>3</b> Set the Sampling Options (see page 120).   |    |
|                     | 4 Set the timing mode Sampling Period (see page 121).   |    |
| Trigger setup       | <b>1</b> The trigger required to capture specific data depends on the measurement. However, the trigger is generally set in two ways.   |    |
|                     | • From within the data display, set up a simple trigger (see page 156)  | ). |
|                     | • From the Advanced Trigger dialog (see page 496), set up a timing mode advanced trigger (see page 560) function.   |    |
| Run the measurement | 1 Run (see page 203) the measurement.   |    |
| See Also            | • To specify the trigger position (see page 134)  |    |
|                     | • To set acquisition memory depth (see page 135)  |    |
| Making a            | a state analyzer measurement  |    |
|                     | The following measurement example shows you the steps necessary to<br>configure and run the logic analyzer for a typical state analyzer<br>measurement. As you go through the example, make the appropriate |    |

|                | you need.  |
|----------------|--|
| TIP            | If you are new to logic analysis, refer to "Tutorial - Getting to know your logic analyzer (see page 60)" for a quick tutorial on logic analysis concepts and measurements.  |
|                | 1 Connect the probing to the device under test (see Probing the Device Under Test (see page 81) for more information).   |
| NOTE           | Be sure that the clock signals of your device under test are connected to clock channels on the pods. Any unused clock channels can be used for additional data channels and will not feed into the state clock setup. |
|                | 2 Turn on the logic analyzer.  |
| Bus and signal | 1 In the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal   |
| setup          | <b>2</b> From the Buses/Signals tab, assign bus/signal names to the device under test signals probed. You do this by either renaming (see  |

choices from the selection lists that best match the kind of configuration

page 107) existing names, or deleting (see page 106) and creating (see page 105) new names.

**3** From the Buses/Signals tab, define buses and signals (see page 104) under the appropriate pods for all probed buses/signals on the device under test.

#### Acquisition mode 1 In the Analyzer Setup dialog, click the Sampling tab.

setup

**2** From the Sampling tab, set the acquisition mode to State - Synchronous Sampling.

| Buses/Signals  | Sampling            |  |
|--|---------------------|--|
| Acquisition-   |                     |  |
| C Timing - Asynchronous Sampling<br>• State - Synchronous Sampling |                     |  |
| State - 5  | ynchionous sampling |  |

- **3** Set the state clock mode (see page 123).
- 4 Set the state sampling clock (see page 128).
- 5 If necessary, set the advanced state clocking (see page 129).
- Trigger setup1The trigger required to capture specific data depends on the<br/>measurement. However, the trigger is generally set in two ways.
  - From within the data display, set up a simple trigger (see page 156).
  - From the Advanced Trigger dialog (see page 496), set up an advanced trigger (see page 573) function.

**Run the** 1 Run (see page 203) the measurement.

#### measurement

- **See Also** To specify the trigger position (see page 134)
  - To set acquisition memory depth (see page 135)

## To trigger on one of multiple edges or glitches

- 1 In the timing sampling mode, set up an Advanced Trigger.
- **2** Select the bus on which you're looking for one of multiple edges or glitches.
- 3 Select All bits in the bus.
- 4 Select Edge.

| Step 1 × Edge  |
|--|
| Find 🞽 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Edge 💽 Edge Spec |
| Then 👻 Trigger and fill memory                             |

- 5 Click Edge Spec....
- 6 In the Set Edge/Glitch dialog, specify edges or glitches you are looking for; use the **Set All** button to make a selection for all signals in the bus.

| Set Edge/Glitch - My Bus 1 |  | × |
|----------------------------|--|---|
|                            | 7 4 3 0  |   |
|                            |  |   |
|                            |  |   |
|                            | Set All 🛛  |   |
|                            | Specifying an edge or glitch on more than one<br>channel logically ORs the edges together. |   |
|                            | Cancel   |   |

- 7 Click OK to close the Set Edge/Glitch dialog.
- 8 Click OK to close the Advanced Trigger dialog.

**NOTE** Glitches are not drawn on the screen. You need an oscilloscope to further troubleshoot glitches and find out when they occur.

#### To trigger on ranges

NOTE

In order to trigger on ranges of bus values, the bus:

- Must not have reordered bits.
- Must not contain clock bits that span pod pairs.
- Must span 2 or fewer pod pairs (up to 64 bits wide).

When setting up simple triggers (see page 156) 1 In the Simple Trigger field for a bus, click the ■ v operator button; then, choose either In Range or Not In Range.

|                   | Waveform Display Window   | Listing/Compare/Source<br>Display Window   |  |
|-------------------|---|--|--|
| Bus Range Trigger | Bus/Signal     Simple Trigger     Pin       □-□     My Bus 1     = *     X     ■       ✓     =     !=        <     >      >       <     >         In Range     Not In Range     Edge       Advanced Trigger | mber     My Bus 1       = ≥     XX       -14     ✓ =       -13     !=       -14     ✓ =       -13     !=       -14     ✓ =       -15        -10     <=       -9     >=       -8     In Range       -7     Not In Range       -6     Edge       -5     -4 |  |
|                   | Bus/Signal     Simple Trigger       ⊡-☐ My Bus 1     R ≥ 80 ■ F0 □  | I<br>mber My Bus 1<br>■ R ¥ 80 ■ F0 ■<br>−14 92  |  |

- 2 Specify the range values, either by entering values in the low range and high range text entry fields or, when the **Symbol** number base is selected, by using the Select Symbol dialog (see page 530).
- 3 From the menu bar, choose **Run/Stop>Run**, or click the ▶ icon from the run/stop toolbar (see page 473).
- 1 Click <sup>™</sup> in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.
- 2 In the Advanced Trigger dialog, select the bus.

| My Bus 1 ¥ All bits = | • | XX 🔳 | Hex 🕹 |
|-----------------------|---|------|-------|
|-----------------------|---|------|-------|

Clicking lets you select from recently used bus/signal names. Clicking elsewhere on a bus/signal name button opens a Select dialog for selecting a different name.

3 Select All bits on the bus.

When setting up advanced triggers (see page 163)

| My Bus 1 🛛 💙 | All bits 💌 😑 💌 00 🔳 Hex 🖇 |
|--------------|---------------------------|
|              | All bits<br>Bit O         |
|              | Bit 1<br>Bit 2            |
|              | Bit 3<br>Bit 4            |
|              | Bit 5<br>Bit 6            |

4 Select either the In Range or Not In Range operator.



5 Select the number base (Binary, Hex, Octal, Decimal, Signed Decimal, also known as two's complement, Ascii, or Symbol).

| My Bus 1 | X All bits 💌 In Range | 💌 80 🔳 to <u>30</u> | Hex 2          |
|----------|-----------------------|---------------------|----------------|
|          |                       |                     | Binary         |
|          |                       |                     | ✓ Hex          |
|          |                       |                     | Octal          |
|          |                       |                     | Decimal        |
|          |                       |                     | Signed Decimal |
|          |                       |                     | Ascii          |
|          |                       |                     | Symbol         |

- 6 Specify the range values, either by entering values in the low range and high range text entry fields or, when the **Symbol** number base is selected, by using the Select Symbol dialog (see page 530).
- 7 From the menu bar, choose **Run/Stop>Run**, or click the ≥ icon from the run/stop toolbar (see page 473).

#### 2 Getting Started

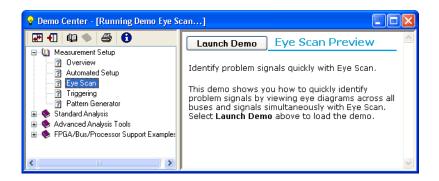
# **Demo Center**

Demo Center is an application that demonstrates logic analysis system features. It loads illustrative configurations into the *Agilent Logic Analyzer* application's *offline-demo* mode and highlights feature capabilities.

#### To launch Demo Center

- From the *Agilent Logic Analyzer* application's main menu, choose **Help>Show Demo...**.
  - From the *Agilent Logic Analyzer* application's Demo Center toolbar, click the 😵 Show Demo icon.
  - From the Windows Start bar, click **Start>All Programs>Agilent Logic Analyzer>Run Logic Analyzer Demo Center**.

The Demo Center application and the *Agilent Logic Analyzer* application are tiled horizontally on the desktop.



The  $\blacksquare$  Float button maximizes the *Agilent Logic Analyzer* application's window lets the Demo Center application window float over it. The  $\blacksquare$  Locate button returns to horizontally tiled windows. The  $\bigcirc$  What is Demo Center button displays more information.

To use Demo1Use the left pane to navigate to the feature demonstration you want to<br/>view.

The  $\square$  Expand and  $\bigotimes$  Collapse buttons affect the feature hierarchy tree.

2 Select the feature you want to learn about by clicking it.

Information about the feature appears in the right pane.

#### 3 Click Launch Demo.

A configuration file that illustrates the feature is loaded into the *Agilent Logic Analyzer* application, and more information about the feature appears in Demo Center's right pane. The B Print button lets you print the information.

4 When you are done exploring the feature, click **Press to Select Another Demo**.

# 2 Getting Started

Agilent Logic and Protocol Analyzer Online Help



# **Probing the Device Under Test**

Before you can make logic analysis measurements on a device under test, you must connect the logic analyzer channels to (in other words, probe) the device under test.

There are several options for probing a device under test:

- Connecting to individual IC pins or test points. This is called *general purpose probing* and is accomplished with flying-lead probe sets.
   Accessories that help with general purpose probing are also available.
- Connecting to all the pins of a specific QFP package. This is called *QFP package probing* and is accomplished with optional elastomeric probe adapter and 1/4 flex adapter products available for several types of QFP packages.
- Designing connectors (or pads and mounting holes for soft-touch connectorless probes and retention modules) into the device under test.
   This is called *target connector probing* or *soft-touch connectorless probing* and is accomplished with optional probes available for various signal and connector types.
- Using processor- or bus-specific probes. These are called *analysis probes* (formerly called *preprocessors*) and are available for many processors and buses. Analysis probes include configuration files for setting up the logic analyzer, and they may include inverse assemblers or other post-processing tools for decoding captured data.
- **See Also** For more information on general-purpose probing, QFP package probing, target connector and connectorless probing, and other probing options, see:
  - "Probing Selection Quick Reference Card"
  - "Probing Solutions for Logic Analyzers" (
     "latest version on web")

For more information on analysis probes and other processor and bus solutions, see:

- "Processor and Bus Support for Logic Analyzers" (
   "latest version
   on web")
- <sup>(a)</sup> "Processor, Bus, and FPGA Support for Logic Analyzers"



For more information on probing signals internal to an FPGA or setting up definitions for the probes used, see:

• "Setting Up Probes" (in the online help)

For more information on controlling signals in the device under test from a logic analysis system, see:

• To control signals in the device under test (see page 83)

## To control signals in the device under test

The 16900A, 16902A, 16902B, and 16903A logic analysis system *frames* (see page 789) have a *target control port*, an 8-bit, 3.3V port that can be used to send signals to a device under test. The target control port does not function like a pattern generator, but more like a remote control for switches in the device under test.

To use the target control port outputs:

1 Connect the target control port cable to the logic analysis system frame.

The target control cable is keyed, so it can be inserted only one way. Plug it into the target control port with the key up and the cable hanging down.

The wires on the target control port cable are color-coded. Bit 0 is brown, bit 1 is red, bit 2 is orange, and so on up to bit 7 (gray). The black and white wires are both ground. Pins 0, 2, 4, and 6 are on the top of the connector and arranged in the same order as the wires.

2 If you plan on using open collector, remember to install pull-up resistors to a maximum 4V. The maximum sink current into the Target Control port is 12 mA and includes a 51 ohm series resistor.

Example:<br/>Resetting YourThis example also applies to other types of signals you may want to send<br/>to your device under test. The reset line in this case is active low.Device Under TestControl of the sector of t

- **1** Attach one of the wires from the target control port cable to the reset line, using proper termination.
- 2 In the Agilent Logic Analyzer application, choose Setup>Target Control Port....
- 3 In the Target Control Port dialog (see page 549), check **Enabled** for the target control port signal you are using.
- 4 Click 1 to output an active high.
- 5 When the device under test needs to be reset, click Pulse.

# Probing the Device Under Test

Agilent Logic and Protocol Analyzer Online Help



# **Connecting to a Logic Analysis System**

If you opened the *Agilent Logic Analyzer* application on a logic analyzer or logic analysis system frame, you are most likely already connected to the local frame. (The right-most part of the status bar shows "Local".)

However, if you are offline (the right-most part of the status bar shows "Offline") and you want to connect to the local frame, or if you want to connect to a different, remote logic analysis system frame, you can do so from the **File** menu.

To connect to the • Choose the File>Go Online To Local Frame menu command.

local frame

remote frame

To connect to a 1 Choose the File>Go Online To... menu command.

2 In the Select System to Use dialog (see page 531), select the system to access; then, click **Connect**.

The logic analysis system can be:

- *Local* connected to the same computer or logic analyzer running the *Agilent Logic Analyzer* application.
- Remote somewhere else on the local area network.
- **3** If you are connecting to a remote logic analysis system that requires a password (see Setting Up Passwords for Remote Access (see page 94)), enter the password in the "Please enter connection password:" dialog, and click **OK**.

When you are connected to a remote logic analysis system frame, the right-most part of the status bar shows "Remote".

## **Connecting to the U4154A Logic Analyzer Module**

Connection to the U4154A Logic Analyzer module is different from connecting to other logic analysis systems and logic analyzers in terms of the hardware setup of the involved components.

The U4154A Logic Analyzer module is installed in a slot of the Agilent AXIe chassis. The Agilent Logic Analyzer application is hosted on a host PC (a laptop or a desktop) or a remote PC connected to the host PC. The U4154A module connects to the host PC through the PCIe interface of the AXIe chassis.



The connection to the U4154A Logic Analyzer module can be:

- Local the Agilent Logic Analyzer application is installed and running on the host PC which is connected to the U4154A module through the PCIe interface of the AXIe chassis.
- Remote the Agilent Logic Analyzer application is installed and running on a computer other than the host PC and is remotely connected to the host PC.

If the PCIe connection between the host PC and AXIe chassis is made, you are most likely already connected to the U4154A Logic Analyzer module installed in the AXIe chassis. (The right-most part of the status bar shows "Local".) However, if you are offline (the right-most part of the status bar shows "Offline") and you want to connect to the U4154A module locally or remotely, you can do so from the **File** menu. The procedures for connection are the same as described above.

#### NOTE

It is recommended that you turn off the standby mode and disable hibernation on the host PC connected to the AXIe chassis via PCIe.

For Windows 7/8, it is also recommended that you disable PCIe power management modes on the host PC.

For more on using the Select System to Use dialog, see:

- To add a logic analysis system to the list (see page 87)
- To delete a logic analysis system from the list (see page 88)
- To refresh the logic analysis system list (see page 89)
- To view logic analysis system details (see page 90)
- To enter your "System In Use" comments (see page 91)
- To select a logic analysis system for auto-connect (see page 92)
- To chat with another logic analysis system user (see page 93)

**See Also** • Offline Analysis (see page 233)

# To add a logic analysis system to the list

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing File>Go Online To...), click Add.
- 2 Enter the logic analysis system frame hostname or IP address in the dialog, and click **OK**.
- See Also Returning to Online Analysis (see page 85)

# To delete a logic analysis system from the list

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), select the logic analysis system you wish to delete.
- 2 Click Delete.
- See Also Returning to Online Analysis (see page 85)

# To refresh the logic analysis system list

1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), click **Refresh**.

The logic analysis system status and detailed information is updated. Status can be:

| Status   | Description   |
|--|---|
| Available  |   |
| Host offline   | The logic analysis system has been powered down or taken off the network. |
| In use   | The "System In Use" comment is displayed in parentheses.                  |
| Incompatible remote<br>service version The version information is displayed in parentheses. The Ag<br>Analyzer application software on the logic analysis system<br>to be updated to match the version of software installed on<br>displaying this dialog. |   |

# To view logic analysis system details

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), select the logic analysis system whose details you wish to view.
- 2 Click **Details...** (you may have to click **More** >> first).

The logic analysis system details are displayed in the Frame/Module Information dialog (see page 513).

# To enter your "System In Use" comments

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), select the logic analysis system whose details you wish to view.
- 2 Click Set My Comments (you may have to click More >> first).
- **3** In the dialog that opens, enter your "system in use" comments.

These comments usually contain your contact information.

# To select a logic analysis system for auto-connect

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), select the logic analysis system that you wish to auto connect to.
- 2 Click Set As Auto-Connect (you may have to click More >> first).
- See Also Returning to Online Analysis (see page 85)

# To chat with another logic analysis system user

- 1 In the Select System to Use dialog (see page 531) (which appears after choosing **File>Go Online To...**), select the logic analysis system to which you want to send a chat message.
- 2 Click Chat (you may have to click More >> first).
- **3** In the Chat Select Destination dialog (see page 502), select whether you want to chat with the person logged into the logic analysis system or the person connected to the frame; then, click **OK**.
- 4 In the Chat dialog (see page 501), enter your message; then, click Send.
- 5 When you are finished with the chat session, click Close.
- **See Also** Returning to Online Analysis (see page 85)

# Setting Up Passwords for Remote Access

The *Agilent Logic Analyzer* application lets you connect to and remotely control logic analysis systems on the network.

If you have a logic analysis system you want to restrict remote frame connections to, you can set up a remote access password. You can password-protect hosted instruments too, by setting a password on the host PC. Because any user on the network with the *Agilent Logic Analyzer* application software installed can force any other user off of a frame, you may wish to protect your local system with a password to prevent this from happening.

#### NOTE

For multiframe logic analysis systems, the remote access password must be the same on every frame. If this is not the case, you will not be able to connect to to the multiframe set. If a password is not set (blank) on one frame, then you will be able to connect to the entire set of frames so long as the remaining frames have identical passwords or a blank password. In other words, a blank password is a don't care condition.

On the logic analysis systems that you want to restrict remote connections to:

1 From the Windows Start menu, choose Start>Programs>Agilent Logic Analyzer>Utilities>Remote Access Password Utility.

(You can also run this utility by clicking **Set Local Password** in the Select System to Use dialog (see page 531).)

2 In the Remote Access Password Utility dialog, if a password is currently set, click **Clear Password**.

| 🔒 Remote Access Password Utility 🛛 🔀   |                     |  |  |  |
|--|---------------------|--|--|--|
| This utility is only available to local system<br>administrators. Here you may either establish a remote<br>access password or clear an existing password. |                     |  |  |  |
| Users of remote machines will not be able to attach to<br>this machine's local hardware without knowing the<br>correct password.                           |                     |  |  |  |
| Enter New Password:  | Enter New Password: |  |  |  |
| Re-Enter New Password:   |                     |  |  |  |
| Clear Password   | Set Password        |  |  |  |

- 3 Enter the new password in the Enter New Password and Re-enter New Password fields; then, click Set Password.
- 4 Click OK to make the password changes and close the dialog.

Password changes take effect immediately; however, they do not affect users currently connected to the local frame.

Clicking Cancel closes the dialog without making any password changes.

- **Notes:** The remote access password is completely separate from Windows user logon passwords. Setting or clearing remote access passwords does not affect Windows user logon passwords.
  - Remote access passwords are encrypted using a one-way encryption algorithm and securely stored.
  - In order to set or clear remote access passwords using this utility, the currently logged-on user must have administrative credentials.
  - Establishing a remote access password does not password-protect access via Windows Remote Desktop.

## 4 Connecting to a Logic Analysis System

Agilent Logic and Protocol Analyzer Online Help

# Ag On 5 S

# **Setting Up the Logic Analyzer**

- Configuring Logic Analyzer Modules (see page 98)
- "Setting Up Probes" (in the online help)
- Setting the Logic Analyzer Threshold Voltage (see page 102)
- Defining Buses and Signals (see page 104)
- Choosing the Sampling Mode (see page 119)
- Setting Up Symbols (see page 139)
- Installing Licensed Hardware Upgrades (see page 147)



# **Configuring Logic Analyzer Modules**

A logic analyzer *module* is a logical collection of channels on a single timebase and trigger. A module can be a single *card* (see page 788) or several cards, and a single card or several card module can be split into two modules. Modules give you the flexibility to:

- Increase logic analyzer channel count by using more than one card.
- Probe buses that have different time domains by splitting a single card into two modules.

Combining cards to increase channel count is done when installing cards into a *frame/chassis* (see page 789 and page 788). Cables are connected between the cards. For more information, see the  $\checkmark$  "16900-Series Logic Analysis System Installation Guide" and the  $\checkmark$  "U4154A Logic Analyzer Module Installation Guide".

**CAUTION** You must power down the AXIe chassis before inserting, replacing, or removing the U4154A Logic Analyzer module. The enclosure surface of the U4154A module may become hot during use. If you need to remove the module, first power down the AXIe chassis, wait for at least five minutes to allow the module to cool, and then pull the module out of the chassis.

Splitting a single card (or cards that were combined during installation) is done from the Setup menu or in the window. To split logic analyzer channels into two modules:

- 1 Choose Setup>(Logic Analyzer Module)>Split Analyzer....
- 2 In the Split Analyzer Setup dialog (see page 541), drag the channel assignment slider to specify the number of channels in each analyzer.

If you'd like to assign particular *pods* (see page 791) or *pod pairs* (see page 791) to a module, check **Advanced Pod Assignment Mode**.

3 Click OK.

**See Also** • To disable and enable modules (see page 98)

- To unsplit a split analyzer (see page 100)
- Memory Depth and Channel Count Trade-offs (see page 420)

#### To disable and enable modules

By default, all modules in a logic analysis system are enabled; however, you can disable modules to stop them from participating in measurements.

# **NOTE** Disabling a module in a split analyzer causes both modules of the split analyzer to be disabled.

To disable 1 In the window, choose Disable... from the module's menu.

Or, choose **Setup>(Logic Analyzer Module)>Disable...** from the main menu.

2 In the Disable dialog:

modules

| Disable   |              |
|---|--------------|
| M 16720A-1<br>M 1674x/5x-1<br>M 16753-56-1<br>M 16760-1<br>M My 16910 - 16911-1 | OK<br>Cancel |
| Delete All Connections  | .::          |

- a Select the modules you want to disable.
- **b** Check **Delete All Connections** if you want to delete module connections to tools and windows. This causes tools and windows connected only to the disabled modules to be deleted as well.

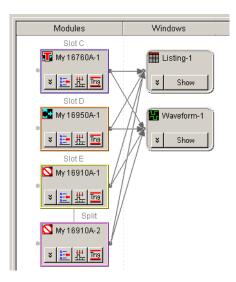
Uncheck **Delete All Connections** if you want to leave module connections to tools and windows. The disabled modules' buses and signals are hidden from tools and windows, but they will reappear when the modules are re-enabled.

c Click OK.

When a module is disabled:

- It no longer runs or sends data to downstream tools or windows, and no data is saved to configuration files.
- The buses and signals defined in the module are hidden from windows and tools.
- You cannot change the setup of the module.

In the widow, disabled modules have the  $\otimes$  icon:



To enable 1 In the window, choose Enable... from the module's menu.

modules

Or, choose Setup>(Logic Analyzer Module)>Enable... from the main menu.

**2** In the Enable dialog:

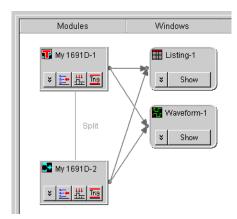
| M 1674x/5x-1<br>M 16753-56-1 | ОК     |
|------------------------------|--------|
| M 16760-1                    | Cancel |
|                              |        |
|                              |        |
|                              |        |
|                              |        |
|                              |        |
|                              |        |
|                              |        |

- **a** Select the modules you want to enable.
- **b** Click **OK**.
- See Also • Configuring Logic Analyzer Modules (see page 98)

# To unsplit a split analyzer

When logic analyzer pods have been split into two modules, you can undo the split and recombine the pods into a single module again.

You can identify a split analyzer in the window by the word "Split" between the modules and an extra line between them.



When looking at the widow, the bottom module shown is the one that will be deleted in an unsplit.

#### CAUTION

When you unsplit an analyzer, all the bus/signal definitions you have set up for the module are deleted throughout the system, including in Windows, triggers, filters, etc. Be sure you are not using the split analyzer before you delete it.

If you are not sure how the unsplit will affect your setup, save your configuration before you unsplit; you cannot "undo" after an unsplit.

To unsplit a split analyzer:

- 1 Choose Setup>(Logic Analyzer Module)>Unsplit Analyzer....
- 2 In the warning dialog that appears, click Yes.
- **See Also** Configuring Logic Analyzer Modules (see page 98)

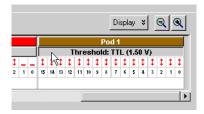
#### **5** Setting Up the Logic Analyzer

# Setting the Logic Analyzer Threshold Voltage

It is very important that you specify a threshold voltage that matches what your device under test is using. Incorrectly specified threshold voltages result in incorrect data.

To learn how to set threshold voltages for 16962 Logic Analyzer or U4154A Logic Analyzer, refer to the topic "Setting Threshold Voltages in the 16962 Logic Analyzer" on page 671.

- 1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**
- 2 In the Buses/Signals Setup dialog, click any **Threshold** button. The Threshold buttons are located under the Pod or Clocks label.



**3** In the Threshold Settings dialog:

| Threshold Settings: Pod 1      | X         |
|--------------------------------|-----------|
| Apply settings to all pods     |           |
| Threshold Settings             |           |
| Probe: General purpose probing | •         |
| ⓒ Standard TTL (1.50 V) ▼      |           |
| C User Defined 0 V ■ - +       |           |
|                                |           |
|                                | OK Cancel |

| Threshold Settings: Slot A Pod 1               | × |
|--|---|
| Apply settings to all pods                     |   |
| Apply settings to clock bits                   |   |
| <ul> <li>Threshold Settings</li> </ul>         | - |
| Probe: E5339A high density/low voltage probing |   |
| • Standard TTL (1.50 V)                        |   |
| OUser Defined 0 V -+                           |   |
| Obifferential                                  |   |
| O External Reference                           |   |
|  |   |
| OK Cancel                                      |   |

Some logic analyzers let you specify threshold voltages for clock channels individually. This may be useful in situations, for example, where the clock channels are probing differential signals while the data channels are probing single-ended signals.

| 👯 Threshold | Settings - Clocks |
|-------------|-------------------|
|             |                   |
| Pod B1      | (                 |
| Pod B2      | No probe attached |
| Pod B3      | No probe attached |
| Pod B4      | No probe attached |
|             |                   |
| 0           | Cancel Help       |

| Threshold Settings: Clock for Pod 1 | ×         |
|-------------------------------------|-----------|
| • Standard TTL (1.50 V)             |           |
| O User Defined 0 ∨ ■ - +            |           |
| C Differential                      |           |
|                                     | OK Cancel |

- **a** Check **Apply settings to all pods** if you want the settings to apply to all pods; otherwise, the settings apply only to the selected pod.
- **b** Check **Apply settings to clock bits** if you want the settings to apply to clock bits; otherwise, the settings apply only to the data channels.
- **c** Select the **Probe** type; this may affect the settings that can be selected.
- d Specify the threshold level. Choices are:
  - Standard you can select from a list of pre-defined threshold levels (which are shown in parentheses).
  - User Defined you can enter a value from -6.00 to 6.00 V.
  - Differential.
  - External Reference some probes have external reference inputs that can define the threshold setting.
- See Also "Setting Threshold Voltages in the 16962 Logic Analyzer" on page 671
  - "Pod and Channel Naming Conventions" on page 418
  - "Pod and Channel Naming Conventions in U4154A Logic Analyzer" on page 680

#### **5** Setting Up the Logic Analyzer

# **Defining Buses and Signals**

Before you can use the logic analyzer, you must define buses and signals by:

- 1 Adding bus/signal names.
- 2 Assigning logic analyzer channels to bus/signal names.

Click in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Bus/Signal...** from the menu bar to open the Buses/Signals setup tab (see page 499).

| Analyzer Setup for My 16910A-     | 1               |          |   |  |
|-----------------------------------|-----------------|----------|---|--|
| Buses/Signals Sampling            |                 |          |   |  |
| Enter buses and signals and the c | channels they c | orrespon | d to:   | Display 2 🔍 🔍  |
| Che                               | annels          | 2000     | Slot A Pod 2 Slot<br>Threshold: TTL (1.50 V) Threshold    |  |
|                                   | signed Widt     | I I I    |   | Polarity   |
| My Bus 1 Pod .                    | A1[7:0] 8       | 1 0      | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 | Comment  |
|                                   |                 | 1        |   | <ul> <li>Threshold</li> <li>Activity</li> <li>Channel Numbers</li> </ul> |
| Add Bus/Signal                    | Delete          | De       | ete All   | System Summary   |
|                                   |                 |          | ОК Са   | ncel Help //   |

The following tasks are performed in the Buses/Signals setup tab:

- To add a new bus or signal (see page 105)
- To delete a bus or signal (see page 106)
- To rename a bus or signal (see page 107)
- To rename the bits of a bus (see page 108)
- To assign channels in the default bit order (see page 110)
- To assign channels, selecting the bit order (see page 111)
- To use clock channels as extra data channels (see page 112)
- To define buses and signals by importing netlist files (see page 113)
- To reorder bits by editing the Channels Assigned string (see page 114)
- To set the default number base (see page 116)

- To set polarity (see page 117)
- To add user comments (see page 117)
- To add a folder (see page 118)
- To alias a bus/signal name (see page 118)
- To sort bus/signal names (see page 118)

Through the **Display** button, you can select what bus/signal setup information is displayed (channels assigned, width, polarity, default base, comment, threshold, activity, or channel numbers).

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

**NOTE** In previous versions of the *Agilent Logic Analyzer* application, the Buses/Signals setup tab had a **Define Probes...** button; now, probes are defined differently (see "To define probes" (in the online help)).

- **See Also** Setting the Logic Analyzer Threshold Voltage (see page 102)
  - Why Are Pods Missing? (see page 419)

#### To add a new bus or signal

The add bus/signal feature allows you to add new buses and signals to the configuration. Once added to the configuration, the new bus/signal is automatically inserted into the data displays and also becomes available in any bus/signal insert function.

- 1 From the menu bar, select **Setup>(Logic Analyzer** Module)>Bus/Signal....
- 2 Select Add Bus/Signal to add a new bus or signal.
- **3** The new bus/signal will appear with a system generated default name. Rename (see page 107) the new bus/signal if desired.

#### NOTE

Before a new bus/signal can be added to the configuration, at least one channel must be assigned to the bus/signal.

#### **5** Setting Up the Logic Analyzer

| Bus/Signal Name Channels<br>Assigned |
|--------------------------------------|
|                                      |
| My Bus 1 Pod 1[7:0]                  |
|                                      |
| My Signal 1 Pod 1[8]                 |
| My Signal 2 Pod 1[9]                 |

- See Also To delete a bus or signal (see page 106)
  - To rename a bus or signal (see page 107)
  - To assign channels in the default bit order (see page 110)
  - To assign channels, selecting the bit order (see page 111)
  - Defining Buses and Signals (see page 104)

## To delete a bus or signal

The delete bus or signal feature allows you to remove buses and signals individually or all at once. The delete bus or signal feature is accessed through the setup menu or the setup toolbar.

- To delete an individual bus or signal (see page 106)
- To delete all buses and signals (see page 107)

To delete an<br/>individual bus or<br/>signal1From the menu bar, select Setup>(Logic Analyzer<br/>Module)>Bus/Signal....2Highlight the bug on signal way want to delete

2 Highlight the bus or signal you want to delete.

#### 3 Click Delete.

| uses/Signals Sampling       |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|-----------------------------|--|--|--|---|---|--|---|--|--|---|---|---|--|---|--|----|----|----|-----|---|--|-----|
| Enter buses and signals and | d the channels                                     | they co  | res  | por   | nd t  | 0:   |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             | channel a  |  |  |   |   |  |   | _  | Pod 2  |   |   |   |  |   |  |    |    |    |     |   |  |     |
| Bus/Signal Name             | Assigned   | Width  | -  |   |   |  |   |  |  |   |   |   |  |   | -  | hr | es | ho | Id: | - |  | 1.8 |
|                             |  |  | 1  | 0   | 15  | 14   | 13  | 12   | 11   | 10  | 9   | 8   | 7  | 6   | 5  |    |    |    |     |   |  |     |
| my Bus 1                    | Pod 1[7:0]   | 8  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
| My Bus 2                    | Pod 1[15:0]  | 16   |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
| My Signal 1                 | Pod 1[8]   | 1  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
| My Signal 2                 | Pod 1[9]   | 1  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  | ٩  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  | _  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
|                             |  |  |  |   |   |  |   |  |  |   |   |   |  |   |  |    |    |    |     |   |  |     |
| 1                           | Add Bus/Sign                                       | al   |  | Del   | ete   |  |   |  |  | D   | ele   | te.   | All  |   |  |    |    |    |     |   |  |     |
|                             | Enter buses and signals and<br>Bus/Signal Hame<br> | There buses and signals and the channels           Bus/Signal Hame         Channels           Assigned         Assigned           Comparison         Pod 1[7:0]           Comparison         Pod 1[15:0]           My Signal 1         Pod 1[8:0]           My Signal 2         Pod 1[9] | There buses and signals and the channels they con Bus/Signal Hame Channels Assigned Width Channels My Bus 1 Pod 1[7:0] 8 Pod 1[15:0] 16 Pod 1[8] 1 | Ther buses and signals and the channels they corres<br>Bus/Signal Hame Channels Assigned Width Channels Channels Width Channels | There buses and signals and the channels they correspondent to the channels they corr | There buses and signals and the channels they correspond to th | There buses and signals and the channels they correspond to:           Bus/Signal Hame         Channels         Width | There buses and signals and the channels they correspond to: | There buses and signals and the channels they correspond to:   Bus:Signal Hame Channels Assigned I I I I I I I I I I I I I I I I I I I | There buses and signals and the channels they correspond to:           Bus/Signal Name         Channels         Width         Thr | Channels         Width         Thres           Bus/Signal Hame         Channels         Width         Image: Channels         Image: Channels           Channels         My Bus         Pod 1[7:0]         8         Image: Channels         Image: Channels           Channels         My Bus 1         Pod 1[7:0]         8         Image: Channels         Image: Channels           Channels         My Bus 2         Pod 1[15:0]         16         Image: Channels         Image: Channels           CMy Bus 2         Pod 1[15:0]         16         Image: Channels         Image: Channels         Image: Channels           CMy Bus 2         Pod 1[15:0]         16         Image: Channels         Image: Channels         Image: Channels           My Signal 1         Pod 1[15:0]         16         Image: Channels         Image: Channels         Image: Channels           My Signal 2         Pod 1[9]         1         Image: Channels         Image: Channels         Image: Channels           My Signal 2         Pod 1[9]         1         Image: Channels         Image: Channels         Image: Channels | Enter buses and signals and the channels they correspond to:           Bus:Signal Hame         Channels<br>Assigned         Width         Thresho | There buses and signals and the channels they correspond to: | Inter buses and signals and the channels they correspond to:         Pod 2         Bus/Signal Hame       Pod 2         Threshold: TT         Assigned       Width       Threshold: TT         0       1       0       1       0 | Enter buses and signals and the channels they correspond to:         Pod 2           Bus:Signal Hame         Channels<br>Assigned         Width         Pod 2         Threshold: TTL (<br>9           CMy Bus 1         Pod 1(7:0)         8         9         9         7         6           CMy Bus 2         Pod 1(15:0)         16         9         9         7         6           CMy Bus 2         Pod 1(15:0)         16         9         9         9         1         9         9         1         9         1         9         1         9         1 |    |    |    |     |   |  |     |

# To delete all1From the menu bar, select Setup>(Logic Analyzerbuses and signalsModule)>Bus/Signal....

2 Click Delete All.

#### NOTE

Some tools "lock" buses and signals because they use the bus or signal to produce their own output. Delete and Delete All will not delete these locked buses and signals. A locked bus or signal has a gray icon to the left of the name instead of a red icon.

**See Also** • Defining Buses and Signals (see page 104)

#### To rename a bus or signal

The rename bus/signal feature allows you to change bus and signal names. All channel, pod, and clock assignments for the renamed bus/signal remain unchanged.

- From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal..., or click the 
  icon in the setup toolbar (see page 471).
- 2 Right-click the bus or signal name and choose Rename...

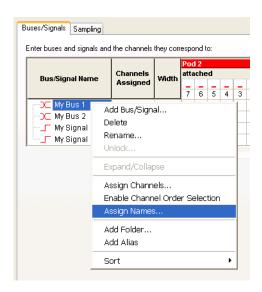
|  |          | the channels                              |         |             |      |      |   | _ |  |  |  |  |  |  |  |
|--|----------|---|---------|-------------|------|------|---|---|--|--|--|--|--|--|--|
|  |          | Channels                                  |         | Poc<br>atta |      |      |   |   |  |  |  |  |  |  |  |
| Bus/Signal Nam   | Assigned | Width                                     | a       |             |      |      |   |   |  |  |  |  |  |  |  |
|  |          |   |         | 7           | 6    | 5    | 4 | 3 |  |  |  |  |  |  |  |
| — <mark>)⊂</mark> My Bus 1<br>— )⊂ My Bus 2<br>— My Signal • |          | dd Bus/Sign<br>elete                      | al      |             |      |      |   | ŀ |  |  |  |  |  |  |  |
| My Signal :  | R        | ename                                     |         |             |      |      |   |   |  |  |  |  |  |  |  |
|  | U        | nlock                                     |         |             |      |      |   |   |  |  |  |  |  |  |  |
|  | E        | (pand/Collap                              | ose     |             |      |      |   |   |  |  |  |  |  |  |  |
|  | Er       | ssign Chann<br>nable Chann<br>ssign Names | el Orde | er Si       | elec | tior | 1 | - |  |  |  |  |  |  |  |
|  |          | dd Folder<br>dd Alias                     |         |             |      |      |   |   |  |  |  |  |  |  |  |
|  | 5        | ort                                       |         |             |      |      |   | 1 |  |  |  |  |  |  |  |

- **3** Enter the new bus or signal name.
- 4 Select OK.
- See Also
  - To add a new bus or signal (see page 105)
    - To delete a bus or signal (see page 106)
    - To rename the bits of a bus (see page 108)
    - Defining Buses and Signals (see page 104)

## To rename the bits of a bus

When a bus is expanded in the Waveform display window, the names of the signals within the bus are like Bus[0], Bus[1], etc., by default. However, you can assign your own names to the bits within a bus.

- From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal..., or click the 
  icon in the setup toolbar (see page 471).
- 2 Right-click the bus name and choose Assign Names....



3 In the Assign Names dialog, enter the new names of bits within the bus.

| Bit Name    | Display Name | OK     |
|-------------|--------------|--------|
| My Bus 1[0] | Ctrl5        |        |
| My Bus 1[1] | Ctrl4        | Cancel |
| My Bus 1[2] | Ctrl3        |        |
| My Bus 1[3] |              |        |
| My Bus 1[4] |              |        |
| My Bus 1[5] |              |        |
| My Bus 1[6] |              |        |
| My Bus 1[7] |              |        |
|             |              |        |

4 Click OK.

Now, you see your names when the bus is expanded in the Waveform window.

| Scale 5 ns/div  |                       | Delay  |
|-----------------|-----------------------|--------|
| Bus/Signal      | Simple Trigger        | -10 ns |
| ⊟⊶∰ My Bus 1    | = × ··· 🔳             | X      |
| [] Ctrl5        | <del>نا</del> ج       | 0      |
| -‡ Ctrl4        | X ×                   | 1      |
| -‡ Ctrl3        | X ×                   | 0      |
| 🕻 My Bus 1 [3]  | X ×                   | 1      |
| (‡ My Bus 1 [4] | X ×                   | 0      |
| 🗐 My Bus 1[5]   | X ×                   | 1      |
| 🕻 My Bus 1[6]   | X ×                   | 0      |
| 🕂 My Bus 1[7]   | X ×                   | 1      |
| <]              | < <u> </u>            |        |
| r               | <br><b>H</b> Waveform | -1     |

- **See Also** To rename a bus or signal (see page 107)
  - To add a new bus or signal (see page 105)
  - Defining Buses and Signals (see page 104)

# To assign channels in the default bit order

To make the logic analyzer display match your system's design, assign the physical channels of the logic analyzer to bus and signal names.

- 1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**
- 2 In the Buses/Signals tab, select squares in the grid to assign channels to bus and signal names. For each signal probed in your device under test, you should have a black check mark mapping the channel to a pod and to a signal name in the interface.

Example: In the picture below, channels 0-7 (pod 1) are mapped to My Bus 1, channels 8-15 (pod 1) are mapped to My Bus 2, and channels 8 and 9 (pod 2) are mapped to My Signal 1 & 2, respectively.

|   | Buses/Signals Sampling     |                |         |      |     |      |     |   |   |   |   |    |    |    |    |    |    |    |     | Die | spla | 211 | - I | 1          | ຈ | 16 | e l |
|---|----------------------------|----------------|---------|------|-----|------|-----|---|---|---|---|----|----|----|----|----|----|----|-----|-----|------|-----|-----|------------|---|----|-----|
|   | Enter buses and signals an | d the channels | they co | rres | ро  | nd I | to: |   |   |   |   |    |    |    |    |    |    |    | _   |     | spie | -1Y |     |            | 4 |    | ~   |
|   |                            |                |         | d 2  |     |      |     |   |   |   |   | L  |    |    |    |    |    | -  | Ро  | _   | _    |     |     |            |   |    |     |
|   | Bus/Signal Name            | Channels       | Width   | П    | L ( | 1.5  | 0 1 | ) | _ | _ |   |    |    |    | T  | hr | es | ho | ld: | TT  | L (  | 1.5 | 0 1 | <i>I</i> ) |   |    |     |
|   |                            | Assigned       |         | -    | -   | -    | -   | - | - | - | - | -  | -  | -  | -  | -  | -  | -  | -   | -   | -    | -   | _   | -          | - | -  | _   |
|   |                            |                |         | 7    | 6   | 5    | 4   | 3 | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8   | 7   | 6    | 5   | 4   | 3          | 2 | 1  | 0   |
|   | My Bus 1                   | Pod 1[7:0]     | 8       |      |     |      |     |   |   |   |   |    |    |    |    |    |    |    |     | 4   | 1    | ~   | ~   | 1          | √ | ~  | 1   |
|   | My Bus 2                   | Pod 1[15:8]    | 8       | Г    |     |      |     |   |   |   |   | 1  | 1  | 4  | 4  | 4  | 4  | 4  | 1   |     |      |     |     |            |   |    |     |
|   | My Signal 1                | Pod 2[0]       | 1       | Γ    |     |      |     |   |   |   | 1 |    |    |    |    |    |    |    |     |     |      |     |     |            |   |    |     |
| ш | My Signal 2                | Pod 2[1]       | 1       | Γ    |     |      |     |   |   | 4 |   |    |    |    |    |    |    |    |     |     |      |     |     |            |   |    |     |
|   |                            |                |         | 4    |     |      |     |   |   |   |   |    |    |    |    |    |    |    |     |     |      |     |     |            |   |    | Þ   |

#### TIP If clock channels are not connected to clock signals, they can be used as extra data channels. Clock channels are grouped together after the last pod in the channel assignment area.

#### **See Also** • To define buses and signals by importing netlist files (see page 113)

- To reorder bits by editing the Channels Assigned string (see page 114)
- Pod and Channel Naming Conventions (see page 418)

# To assign channels, selecting the bit order

In cases where buses in the device under test haven't been probed with consecutive logic analyzer channels, you can assign channels to a bus name in a selected bit order.

- 1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**
- 2 In the Buses/Signals tab, right-click the bus name, and choose **Enable** Channel Order Selection.
- **3** Start selecting squares in the grid to assign channels from the low order bit of the bus to the high order bit.

The bit numbers are displayed as you select squares.

|                      |               |       |   |   |    |    |    |    |    |    |     | Po  | d 2 |     |     |     |    |   |   |   |
|----------------------|---------------|-------|---|---|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|----|---|---|---|
| Bus/Signal Name      | Channels      | Width |   |   |    |    |    | Т  | hr | es | hol | ld: | TΤ  | L ( | 1.5 | 0 ۱ | ŋ. |   |   |   |
| bus/signa hame       | Assigned      | maan  | - | - | -  | _  | _  | _  | -  | -  | -   | _   | _   | _   | _   | -   | _  | - | _ | _ |
|                      |               |       | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8   | 7   | 6   | 5   | 4   | 3  | 2 | 1 | 0 |
| C Default Bit Order  | Pod 2[15:12,  | 8     |   |   | 4  | 1  | ~  | 4  |    |    |     |     | 4   | 1   |     |     | 4  | 4 |   |   |
| C Selected Bit Order | Pod 2[1,5,0,4 | 8     |   |   |    |    |    |    | 0  | 1  | 2   | 3   |     |     | 6   | 4   |    |   | 7 | 5 |

## NOTE

When you select a bit order other than the default, you can only trigger on a sample equal to (=) or not equal (!=) to some value on that bus. You lose the ability to trigger on a sample less than (<), greater than (>), less than or equal to (<=), or greater than or equal to (>=) some value, and you lose the ability to trigger on a sample "in range" or "not in range" of two values.

To reset the default bit order

The default bit order of assigned channels has higher bits on the left and lower on the right (in the Bus/Signal Setup dialog).

|                  |               |       |   |   |    |    |    |    |    |    |     | Po  | d 2 |    |     |     |    |   |   |   |
|------------------|---------------|-------|---|---|----|----|----|----|----|----|-----|-----|-----|----|-----|-----|----|---|---|---|
| Bus/Signal Name  | Channels      | Width |   |   |    |    |    | T  | hr | es | hol | ld: | TT  | L( | 1.5 | 0 V | ŋ. |   |   |   |
| Dus/Jigha Marrie | Assigned      | Maan  | _ | - | -  | _  | _  | _  | -  | _  | _   | _   | _   | _  | _   | _   | -  | _ | _ | _ |
|                  |               |       | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8   | 7   | 6  | 5   | 4   | 3  | 2 | 1 | 0 |
| C Default Order  | Pod 2[15:12,  | 8     |   |   | 7  | 6  | 5  | 4  |    |    |     |     | 3   | 2  |     |     | 1  | 0 |   |   |
| C Reordered Bits | Pod 2[1,5,0,4 | 8     |   |   |    |    |    |    | 0  | 1  | 2   | 3   |     |    | 6   | 4   |    |   | 7 | 5 |

To reset to the default bit order:

- Right-click the bus name, and uncheck **Enable Channel Order Selection**.
- **See Also** To define buses and signals by importing netlist files (see page 113)
  - To reorder bits by editing the Channels Assigned string (see page 114)
  - Pod and Channel Naming Conventions (see page 418)

# To use clock channels as extra data channels

When clock channels are not used for state mode sampling clock inputs, they can be used as extra data channels and assigned to bus/signal names just like ordinary data channels (see To assign channels in the default bit order (see page 110) or To assign channels, selecting the bit order (see page 111)).

When clock channels are used for state mode sampling clock inputs, it is not useful to assign them to bus/signal names.

Each pod in a logic analyzer module has a clock channel. In the Buses/Signals Setup dialog, all the clock channels are grouped together in a virtual **Clocks** pod. (Only ordinary data channels appear under the columns for each pod.)

| Ana | lyzer Setup for My 169      | 1D-1         |           |      |     |       |    |   |    |    |    |    |    |     |     |     |    |     |     |     |      |   |   |   |   |    |    |
|-----|-----------------------------|--------------|-----------|------|-----|-------|----|---|----|----|----|----|----|-----|-----|-----|----|-----|-----|-----|------|---|---|---|---|----|----|
| В   | uses/Signals Sampling       |              |           |      |     |       |    |   |    |    |    |    |    |     |     |     |    |     |     |     |      |   |   |   |   |    |    |
|     | Enter buses and signals and | the channels | they corr | resp | por | nd ti | D: |   |    |    |    |    |    |     |     |     |    |     |     |     |      |   |   |   |   |    |    |
|     |                             |              |           |      | (   | Clo   | ck | s |    |    |    |    |    |     |     |     | Po | d 6 | ;   |     |      |   |   |   |   |    |    |
|     | Bus/Signal Name             | Channels     | Width     |      |     |       |    |   |    |    |    |    | T  | hre | esl | hol | d: | TΤ  | L ( | 1.6 | i0 1 | 0 |   |   |   |    |    |
|     | bus/signal name             | Assigned     | widen     | _    | _   | 1     | \$ | 1 | \$ | _  | _  | _  | _  | _   | _   | _   | _  | _   | _   | _   | _    | _ | _ | _ |   | _  | _  |
|     |                             |              |           | 6    | 5   | 4     | 3  | 2 | 1  | 15 | 14 | 13 | 12 | 11  | 10  | 9   | 8  | 7   | 6   | 5   | 4    | 3 | 2 | 1 | 0 | 15 | 14 |
|     | — 🔀 My Bus 1                | Clks[C4:C1]  | 4         |      |     | 4     | 4  | 4 | ~  |    |    |    |    |     |     |     |    |     |     |     |      |   |   |   |   |    |    |
| 1   |                             |              |           | 4    | Î.  |       |    |   | _  |    |    |    |    |     |     |     |    |     |     |     |      |   |   |   |   |    |    |

#### NOTE

NOTE

There is no separate physical clock pod. Each pod has a single clock channel.

The clock pod can grow to include as many channels as there are pods in the system. In other words, the clock pod can have more than 16 channels if there are more than 16 pods.

In the **Channels Assigned** string, the clock pod name is "Clks" and the channels are named "C1", "C2", etc.

**See Also** • To reorder bits by editing the Channels Assigned string (see page 114)

• Pod and Channel Naming Conventions (see page 418)

## To define buses and signals by importing netlist files

You can create bus/signal names and assign logic analyzer probe channels by importing netlist files. These netlist files come from the Electronic Design Automation (EDA) tools used to design the device under test, and they contain information about the signals on the connectors built into the device under test for the logic analyzer probes.

- 1 If you haven't already defined probes, choose Setup>(Logic Analyzer Module)>New Probe>General Purpose Probe Set and define the probes whose connectors are mapped in the netlist file (see "To define probes" (in the online help)).
- 2 In the Bus/Signal Setup dialog, click Netlist Import....
- 3 Then, enter the netlist file to import bus/signal assignments from, and click OK.

| Netlist Impo  | brt                         | ×      |
|---------------|-----------------------------|--------|
| Netlist File: | C:\My Documents\netlist.txt | Browse |
| OK            | Cancel Trim Buses/Signals   | Help   |

After importing netlist files, connector pin numbers are displayed in the Bus/Signal Setup dialog.

| ises/Signals   Sampling  <br>Inter buses and signals an | d the channels            | they corr | esp | on | d to:   |         |      |    |              |   |          |          |          |      |          |          |     |     |          |   |          |          |   |     |   |   |            | Dis      | pla        |
|---|---------------------------|-----------|-----|----|---------|---------|------|----|--------------|---|----------|----------|----------|------|----------|----------|-----|-----|----------|---|----------|----------|---|-----|---|---|------------|----------|------------|
|   |                           |           |     | -  |         |         |      | ть | res          |   | Po       | _        |          | 1.51 | 0.54     | n.       |     |     |          |   |          |          | т | bra |   | _ | od<br>d: T | _        |            |
| Bus/Signal Name   | Channels<br>Assigned      | Width     | -   | -  | _       | -       | 13 1 |    | 1 10         | _ | _        | -        | -<br>6   | -    | -<br>4   | ,<br>    | - 2 | -   | -        | 1 | _        | -        | - | _   | _ | _ | _          | 1        | 1          |
|   |                           |           | 1   | 0  | 15<br>7 | 14<br>9 | _    | _  | 1 10<br>5 17 |   | <u> </u> | <u> </u> | <u> </u> | -    | <u> </u> | <u> </u> | -   | · · | <u> </u> | _ | 14<br>10 | 13<br>12 | _ | _   | _ | _ | 8<br>22    | _        | 6<br>26    |
| → → → → → → → → → → → → → → → → → → →                   | Pod 1[7:0]                | 8         |     |    |         |         |      |    |              |   |          |          |          |      |          |          |     |     |          |   |          |          |   |     |   |   | ŀ          | <b>/</b> | <b>/</b> . |
|   | Pod 2[5,6,7,8<br>Pod 1[7] | 11<br>1   |     |    | 0       | 1       | 2 3  | 1  | 1 5          | 6 | 7        | 8        | 9        | 10   | _        |          |     |     |          |   |          |          |   |     |   |   | -          | 1        | -          |

Imported bus/signal definitions are placed in the "Netlist Import" folder.

### CAUTION

The "Netlist Import" folder is deleted and re-created on each import. If you want to keep definitions from the "Netlist Import" folder, either rename the folder or move bus/signal definitions out of the folder before the next netlist import.

**Example Line** Netlist files created by Electronic Design Automation (EDA) tools have lines in the following format:

## NET '/Bus1(3)' J1-7

Where:

- **Bus1** = Four bit bus.
- (3) = Bit 3.
- **J1-7** = Connector J1, pin 7.

#### **See Also** • To assign channels in the default bit order (see page 110)

- To assign channels, selecting the bit order (see page 111)
- To reorder bits by editing the Channels Assigned string (see page 114)
- Pod and Channel Naming Conventions (see page 418)

# To reorder bits by editing the Channels Assigned string

You can change the order of the bits in a bus name (assigned in either the default order (see page 110) or a selected order (see page 111)) by editing the **Channels Assigned** text string.

- 1 In the Buses/Signals tab of the Analyzer Setup dialog, click the **Channels Assigned** to the bus name.
- **2** In the Assign Channels dialog, enter the appropriate order of bits in the bus.

| Assign Channels       |                                     |                       | ×      |
|-----------------------|-------------------------------------|-----------------------|--------|
| Bus/Signal: My Bus 1  |                                     |                       | ОК     |
| MSB                   |                                     | LSB                   | Cancel |
| Pod B2[4,5,6,7,3:0]   |                                     | <u></u>               | Help   |
| Default Channel Order | Switch Big Endian <=> Little Endian | Reverse Channel Order |        |

| Example                                  | Description  |
|--|--|
| Pod B1[0]                                | Signal consisting of the first channel in the first pod of slot B.                                     |
| Pod B1[15:0]                             | Bus consisting of all sixteen channels in Pod B1 in default order.                                     |
| Pod B1[7:0], Pod<br>B2[15:8]             | Bus with seven channels from first pod in slot B followed by seven channels from second pod in slot B. |
| Pod B1[7:0,15:8]                         | Big endian, little endian switch on a 16-bit bus.  |
| Pod B1[0,1,2,3]                          | Bus with bits in reverse order.  |
| Clks[C2:C1], Pod<br>B1[0], Pod B2[0]     | Four bit bus including two clock pod channels.   |
| Clks[C2M:C1S], Pod<br>B1M[0], Pod B1S[0] | Four bit bus with demultiplex.   |

See Pod and Channel Naming Conventions (see page 418) to understand naming conventions like "Pod B2".

You can easily **Switch Big Endian** <=> Little Endian or Reverse Channel Order by clicking these buttons.

3 Click OK.

Channel numbers are displayed for reordered bits in the Bus/Signal Setup dialog.

| nter buses and signals ar | nd the channels | they corr | esp | on | id to | D: |    |    |     |    |     |      |      |     |     | D   | ispl | lay | ¥  |    | Q |  | <u></u> |
|---------------------------|-----------------|-----------|-----|----|-------|----|----|----|-----|----|-----|------|------|-----|-----|-----|------|-----|----|----|---|--|---------|
|                           |                 |           |     |    |       |    |    |    |     |    | 5   | Slo  | t B  | Po  | d   | 2   |      |     |    |    |   |  |         |
| Bus/Signal Name           | Channels        | Width     |     |    |       |    |    | Th | пге | sh | olo | 1: O | )iff | еге | ent | ial | (0.  | 00  | V) |    |   |  |         |
| bus/signal name           | Assigned        | 44iutii   | _   | _  | _     | \$ | t  | \$ | \$  | 1  | t   | _    | _    | \$  | \$  | t   | \$   | ŧ   | \$ | \$ | 1 |  |         |
|                           |                 |           | 2   | 1  | 0     | 15 | 14 | 13 | 12  | 11 | 10  | 9    | 8    | 7   | 6   | 5   | 4    | 3   | 2  | 1  | 0 |  |         |
| 🔨 My Bus 1                | Pod B2[4,5,6,   | 8         |     |    |       |    |    |    |     |    |     |      |      | 4   | 5   | 6   | 7    | 3   | 2  | 1  | 0 |  |         |
| 🕂 🔨 My Bus 2              | Pod B2[15:8]    | 8         |     |    |       | 4  | 1  | ~  | 4   | 1  | 1   | 1    | 1    |     |     |     |      |     |    |    |   |  |         |
| My Signal 1               | Pod B3[0]       | 1         |     |    | 4     |    |    |    |     |    |     |      |      |     |     |     |      |     |    |    |   |  |         |
| My Signal 2               | Pod B3[1]       | 1         |     | v  |       |    |    |    |     |    |     |      |      |     |     |     |      |     |    |    |   |  |         |

# NOTE

When bits have been reordered, you can only trigger on a sample equal to (=) or not equal (!=) to some value on that bus. You lose the ability to trigger on a sample less than (<), greater than (>), less than or equal to (<=), or greater than or equal to (>=) some value, and you lose the ability to trigger on a sample "in range" or "not in range" of two values.

To reset the default bit order

the The default bit order of assigned channels has higher bits on the left and lower on the right (in the Bus/Signal Setup dialog).

|                   |               |       |   |   |    |    |    |    |    |    |     | Po  | d 2 |     |     |     |    |   |   |   |
|-------------------|---------------|-------|---|---|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|----|---|---|---|
| Bus/Signal Name   | Channels      | Width |   |   |    |    |    | Т  | hr | es | hol | ld: | TΤ  | L ( | 1.5 | 0 ۱ | ŋ. |   |   |   |
| Duaraignal Marrie | Assigned      | mau   | _ | _ | _  | _  | _  | _  | _  | _  | _   | _   | _   | _   | _   | _   | _  | _ | _ | _ |
|                   |               |       | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8   | 7   | 6   | 5   | 4   | 3  | 2 | 1 | 0 |
| C Default Order   | Pod 2[15:12,  | 8     |   |   | 7  | 6  | 5  | 4  |    |    |     |     | 3   | 2   |     |     | 1  | 0 |   |   |
| C Reordered Bits  | Pod 2[1,5,0,4 | 8     |   |   |    |    |    |    | 0  | 1  | 2   | 3   |     |     | 6   | 4   |    |   | 7 | 5 |

To reset to the default bit order:

- 1 Click the **Channels Assigned** to the bus name.
- 2 In the Assign Channels dialog, click Default Channel Order.
- 3 Click OK.

See Also

- To assign channels in the default bit order (see page 110)
  - To assign channels, selecting the bit order (see page 111)
  - Pod and Channel Naming Conventions (see page 418)

# To set the default number base

You can set the default number base for a bus when you create the bus. The default base is used to display bus and signal values in the listing (see page 267) and waveform (see page 255) views. Default base only affects new buses and signals; if you change default base for an existing bus or signal you will not see a change unless you add a new copy of the bus or signal to a listing or waveform view.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal....
- 2 In the bus/signal setup dialog, select Display.
- **3** Select **Default Base**.

| Bus/Signal Name         Channels<br>Assigned         Writth         1.50 V         Threshold:         Width         Output           2         4         3         2         1         6         4         3         2         1         6   | ter buses and signals ar |             |       | (   |      |    |   |   |   |   | _ | _  |    | _       | _   |       | Por   | _        | hannels Assigned |
|--|--------------------------|-------------|-------|-----|------|----|---|---|---|---|---|----|----|---------|-----|-------|-------|----------|------------------|
| S         4         3         2         1         0         IS         IL         ID         Default Base         Setup/Hold         Default Base         Setup/Hold         Cgmment         Threshold         Default Base         Setup/Hold         Cgmment         Threshold         Thres | Bus/Signal Name          |             | Width | 1.5 | 50 \ | n) |   |   |   |   |   |    | Т  | hr      | esl | hol   | ld: ˈ |          | -                |
| My Bus 2 Pod 1[15:8] 8   |                          | Assigned    |       | - 1 | -    | -  | 2 | - | - |   |   | 13 | 12 | -<br>11 |     | <br>9 |       |          |                  |
| My Signal 1 Pod 2[0] 1 ✓ ✓   | ) My Bus 1               | Pod 1[7:0]  | 8     | 1   | 1    |    |   |   |   |   |   |    |    |         |     |       | Η     | <u>S</u> | etup/Hold        |
|  |                          | Pod 1[15:8] | 8     |     |      |    |   |   |   | 4 | 4 | 1  | ~  | 4       | 1   | 1     | ~     | C,       | omment           |
| My Signal 2 Pog 211 1 √  | My Signal 1              | Pod 2[0]    | 1     |     |      |    |   |   | 4 |   |   |    |    |         |     |       |       | . т      | han a balal      |
|  | My Signal 2              | Pod 2[1]    | 1     |     |      |    |   | 4 |   |   |   |    |    |         |     |       |       | _        |                  |
|  |                          |             |       | 4   | ]    |    |   |   |   |   |   |    |    |         |     |       |       | _        | hannel Numbers   |

**4** To change the default base for a bus or signal, click the default base value.

|                 |             |       |         |            |      |          |    |   |         |    |       | P  |
|-----------------|-------------|-------|---------|------------|------|----------|----|---|---------|----|-------|----|
| Bus/Signal Name | Channels    | Width | Default |            |      |          |    | Т | hre     | es | ho    | ld |
| Sucregation     | Assigned    | man   | Base    | -          | -    |          |    | - | -<br>11 |    | <br>9 | -  |
| m My Bus 1      | Pod 1[7:0]  | 8     | Hex     |            |      |          | 10 | - |         | 10 | ĺ     | F  |
| My Bus 2        | Pod 1[15:8] | 8     | Hex     |            | Bina | <u> </u> |    |   |         |    | ł     | N  |
| My Signal 1     | Pod 2[0]    | 1     | Hex     | <b>~</b> I | lex  | (        |    |   |         |    | Ľ     |    |
|                 | Pod 2[1]    | 1     | Hex     | - (        | Det  | al       |    |   |         |    |       |    |
| └── My Signal 2 | POUZ[1]     |       |         |            |      |          |    |   |         |    |       |    |

- **5** Select a new value.
- 6 Click OK to close the bus/signal dialog.

# To set polarity

You can define buses and signals to display with negative or positive polarity. This affects the display of values and waveforms. When a bus or signal is set to negative polarity, an incoming high voltage will be shown with a low waveform and a logical value of 0. The polarity is reflected in all places that use values, such as trigger and symbols.

The default polarity is positive (high = 1).

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal....
- 2 In the bus/signal setup dialog, select Display.
- 3 Select Polarity.

| Enter buses and signals ar | nd the channels | they co | rres                   | ро | nd I | to:    |        |   |        |   |                |         |         |         |         | ļ  | Di | isplay 🔻 🍳 🍳                    |
|----------------------------|-----------------|---------|------------------------|----|------|--------|--------|---|--------|---|----------------|---------|---------|---------|---------|----|----|---------------------------------|
| Bus/Signal Name            | Channels        | Width   | <mark>1</mark> 2<br>TT |    | 1.5  | 0 \    | n)     |   |        |   |                |         |         | Т       | 'nr     | es | ž  | —                               |
| bus/signal warne           | Assigned        | Wath    | -                      | -  |      | -<br>4 | -<br>3 | 2 | -<br>1 | - | <b>-</b><br>15 | -<br>14 | -<br>13 | -<br>12 | -<br>11 | -  |    | <u>Polarity</u><br>Default Base |
| gen 📜 My Bus 1             | Pod 1[7:0]      | 8       |                        |    |      |        |        |   |        |   |                |         |         |         |         |    |    | <u>S</u> etup/Hold              |
|                            | Pod 1[15:8]     | 8       |                        |    |      |        |        |   |        |   | 1              | √       | √       | √       | 1       | v  |    | Comment                         |
| My Signal 1                | Pod 2[0]        | 1       |                        |    |      |        |        |   |        | ~ |                |         |         |         |         |    |    | Threshold                       |
| i My Signal 2              | Pod 2[1]        | 1       |                        |    |      |        |        |   | 4      |   |                |         |         |         |         |    |    | -                               |
|                            |                 |         | 4                      | J  |      |        |        |   |        |   |                |         |         |         |         |    | ž  | Activity<br>Channel Numbers     |
|                            | Add Bus/Sig     | inal    |                        |    | De   | lete   | •      |   |        |   | D              | ele     | te i    | 4       |         |    |    |                                 |

4 In the polarity column that appears, toggle between + (positive) and – (negative).

# To add user comments



You can attach comments to buses and signals. The comments show up in the tool tip when you hover the mouse over a bus or signal name in both the waveform and listing windows.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal....
- 2 In the Buses/Signals setup tab that appears, select Display.
- **3** Select **Comment**. A new column labeled Comment appears.
- 4 In the Comment column, type your comment for the bus or signal.

5 Click OK to close the Analyzer Setup dialog.

```
NOTE
```

Comments are intended as a descriptor to embellish a bus/signal name and not as a notepad. Comments can be up to 64 character in length.

# To add a folder

The **Add Folder...** feature adds a windows style folder to the bus/signal list. Use folders to help organize bus and signal names when using many bus/signal names with inverse assemblers.

- 1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
- 2 Right-click on a bus/signal name, then select Add Folder.
- **3** The new folder appears directly below the highlighted name. By default, the new folder has a system generated default name. If desired, rename (see page 107) the new folder in the same way you would a bus/signal name.
- **See Also** To alias a bus/signal name (see page 118)

## To alias a bus/signal name

The **Add Alias...** feature adds an exact duplicate bus or signal name (same channel, polarity, etc. assignments). Use alias names along with folders (see page 118) to help organize the many bus and signal names with inverse assembly.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal....
- 2 Right-click on the desired bus/signal name, then select Add Alias.
- **3** The new alias name appears directly below the highlighted name. The new alias name can be renamed (see page 107), however, the new name will also be applied to the original name.

**See Also** • To add a folder (see page 118)

# To sort bus/signal names

You can sort bus/signal names and folder names to help organize them.

- 1 From the menu bar, select **Setup>(Logic Analyzer Module)>Bus/Signal...**.
- 2 Right-click on one of the bus/signal or folder names to be sorted; then, select either **Sort>Ascending** or **Sort>Descending**.
- **See Also** To add a folder (see page 118)

# **Choosing the Sampling Mode**

| Buses/Signals | Sampling   |
|---------------|--|
|               |  |
|               | - Asynchronous Sampling                            |
| C State -     | Synchronous Sampling (400 Mb/s maximum clock rate) |

The Sampling tab is accessed through the menu bar's **Setup>(Logic Analyzer Module)>Timing/State (Sampling)...** item. The Sampling setup tab is used to select and configure the acquisition mode.

In the **Timing - Asynchronous Sampling** acquisition mode, you set the sampling option and the sampling period. The device under test is sampled at regular intervals (the sampling period).

In the **State - Synchronous Sampling** acquisition mode, you set the sampling option, you set up the clocking signal(s) from the device under test that tells the logic analyzer when to sample data, and you adjust sampling positions on each channel relative to the sampling clock to make sure data is sampled when it is valid.

In both state and timing mode, you can set the acquisition (memory) depth and the position of the trigger event within the acquisition memory.

Some logic analyzers have the timing zoom feature which collects additional high-speed timing data around the logic analyzer trigger.

The following tasks are performed in the Sampling setup tab.

- Selecting the Timing Mode (Asynchronous Sampling) (see page 120)
  - To select the timing acquisition mode (see page 120)
  - To select the timing sampling option (see page 120)
  - To set the timing mode sampling period (see page 121)
- Selecting the State Mode (Synchronous Sampling) (see page 122)
  - To select the state acquisition mode (see page 122)
  - To select the state sampling option (see page 122)
  - Selecting the State Sampling Clock Mode (see page 123)
  - To set up the state sampling clock (see page 128)
  - To automatically adjust state sampling positions and threshold voltages (see page 130)
  - To manually adjust state sampling positions (see page 133)
- In Either Timing Mode or State Mode (see page 134)
  - To specify the trigger position (see page 134)

- To set acquisition memory depth (see page 135)
- Using Timing Zoom (see page 136)
  - To turn timing zoom on or off (see page 138)
  - To specify the timing zoom sample period (on some logic analyzers) (see page 138)
  - To specify the timing zoom trigger position (see page 138)
  - To align timing zoom in a split analyzer (see page 138)
- **See Also** Memory Depth and Channel Count Trade-offs (see page 420)

# Selecting the Timing Mode (Asynchronous Sampling)

In *timing mode*, the logic analyzer samples asynchronously, based on an internally-generated sampling clock.

- To select the timing acquisition mode (see page 120)
- To select the timing sampling option (see page 120)
- To set the timing mode sampling period (see page 121)

#### To select the timing acquisition mode

- From the menu bar select Setup>(Logic Analyzer Module)>Timing/State (Sampling)..., or click the ≞ icon from the setup toolbar (see page 471).
- 2 In the Acquisition area of the Sampling setup dialog, select the Timing- Asynchronous Sampling option.

# To select the timing sampling option

| Buses/Signals Sampling   |
|--|
| Acquisition  |
| Timing - Asynchronous Sampling                                 |
| State - Synchronous Sampling                                   |
| Timing Options   |
| Sampling Options: Store transitions only, 136 channels, 200MHz |
| Sampling Period: 136 channels, 400MHz<br>68 channels, 800MHz   |
| Store transitions only, 136 channels, 200MHz                   |

In the timing (asynchronous) sampling mode, you can:

• Trade-off channel width for faster sampling. That is, if you want a smaller sampling period, you can set up the logic analyzer to use half of the maximum channels available.

• Get the most out of acquisition memory and measure an overall greater amount of time by choosing to store only transitions or other store-qualified patterns.

**NOTE** Changing the sampling option will affect the sampling period and may affect bus assignments.

To select the timing mode sampling option:

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>State/Timing (Sampling)....
- 2 Select Timing acquisition mode. Timing Options become selectable.
- **3** Select the sampling option you prefer. Your channel count may be different depending on the logic analyzer model.

| <i>Full Channel Timing Mode</i> (see page 635)                  | Default. All channels are available.  |
|---|---|
| Half Channel Timing<br>Mode (see page 635)                      | Uses one pod from each pod pair.  |
| Transitional / Store<br>Qualified Timing<br>Mode (see page 635) | Provides maximum duration of acquisition because data is only stored<br>when a change from the last value is detected. See transitional timing<br>(see page 422). |

See Also • Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 635)

# To set the timing mode sampling period

In timing mode, a logic analyzer takes a sample of the device under test's activity once per sample period. You can set this sample period in the Sampling Setup tab.

- 1 From the menu bar select Setup>(Logic Analyzer Module)>Timing/State (Sampling)..., or click the ≞ icon from the setup toolbar (see page 471).
- 2 Select Timing Asynchronous Sampling.
- **3** In the Timing Mode area of the Sampling setup dialog, increase or decrease the Sample Period.

### NOTE

To capture signal level changes reliably, the sample period should be less than half of the period of the fastest signal you want to measure. Time interval measurements are made by counting the number of samples in the desired waveform area. These measurements are made to a +/- one sample error, so measurement accuracy is improved if the number of samples is maximized.

#### **5** Setting Up the Logic Analyzer

See Also • Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 635)

# Selecting the State Mode (Synchronous Sampling)

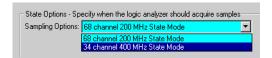
In *state mode*, the logic analyzer samples synchronously, based on a sampling clock signal from the device under test. Typically, the signal used for sampling in state mode is a state machine or microprocessor clock signal.

- To select the state acquisition mode (see page 122)
- To select the state sampling option (see page 122)
- Selecting the State Sampling Clock Mode (see page 123)
- To set up the state sampling clock (see page 128)
- To automatically adjust state sampling positions and threshold voltages (see page 130)
- To manually adjust state sampling positions (see page 133)

## To select the state acquisition mode

- 2 In the Acquisition area of the Sampling setup dialog, select the State Synchronous Sampling option.

### To select the state sampling option



In the state (synchronous) sampling mode, the sampling option specifies the speed up to which the state mode sampling clock will match input clock edges from the device under test. You can trade-off triggering and clocking capability to allow faster state mode sampling speeds.

To select the state mode sampling option:

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>State/Timing (Sampling)....
- 2 Select the **State** acquisition mode. State Sampling Options becomes selectable.
- **3** Select the sampling option you prefer.

| <i>General State Mode</i><br>(see page 636) | Default.   |
|---|--|
| <i>Turbo State Mode</i><br>(see page 636)   | Faster state mode sampling speeds are supported, but triggering and clocking are restricted. |

#### **See Also** • Logic Analyzer Notes, State Mode Sampling Options (see page 636)

### Selecting the State Sampling Clock Mode

The state sampling clock inputs let signals from the device under test specify when data should be captured.

| State Options - | Specify wh | en the logi | c analyzer | should ac | quire samples   |
|-----------------|------------|-------------|------------|-----------|-----------------|
| Clock Mode:     | Master     |             | •          | □ Ad•     | vanced Clocking |
| Pod:            | 4          | 3           | 2          | . 1       |                 |
| Clock:          | Clk4       | Clk3        | Clk2       | Clk1      |                 |
| Activity:       | ŧ          | ŧ           | ŧ          | ŧ         | 1               |
| Master:         | X ×        | X ×         | X ×        | ÷         | Clk1↑           |

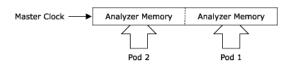
The state sampling clock *mode* specifies how the clock inputs are used for sampling. There are four state sampling clock modes to choose from:

- Master Only (see page 124) all pods sampled on one master clock.
- Master/Slave (see page 124) some pods sampled on master clock; other sampled on slave clock.
- Demultiplex (see page 124) one pod of pair sampled on master and slave clocks.
- Dual Sample (see page 125) one pod of pair sampled on one master clock but with different delays.

For instructions on setting up these state sampling clock modes, see:

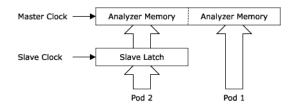
- "To set up the master only sampling clock mode" on page 125
- "To set up the master/slave sampling clock mode" on page 125
- "To set up the demultiplex sampling clock mode" on page 126
- "To set up the dual sample sampling clock mode" on page 127
- See Also "To set up the state sampling clock" on page 128
  - "To set up advanced clocking" on page 129
  - "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674
  - "Pod and Channel Naming Conventions" on page 418

**Master Only Sampling Clock Mode** In the Master only state sampling clock mode, there is one sampling clock signal. When a clock edge occurs, data is captured and saved into one sample of logic analyzer memory.



**See Also** • To set up the master only sampling clock mode (see page 125)

**Master/Slave Sampling Clock Mode** In the Master/Slave state sampling clock mode, you can save data captured on different clock edges into the same sample of logic analyzer memory.

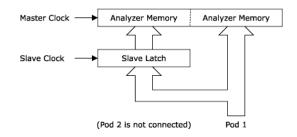


When the slave clock occurs, data captured on the pods that use the slave clock is saved in a slave latch. Then, when the master clock occurs, data captured on the pods that use the master clock, as well as the slave latch data, are saved into logic analyzer memory. If multiple slave clocks occur before the next master clock, only the most recently acquired slave data is saved into logic analyzer memory.

See Also

• To set up the master/slave sampling clock mode (see page 125)

**Demultiplex Sampling Clock Mode** In the Demultiplex state sampling clock mode, you can demultiplex data being probed by one pod into the logic analyzer memory that is normally used for two pods. Demultiplex mode uses the master and slave clocks to demultiplex the data.

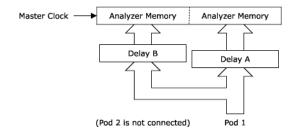


When the slave clock occurs, data captured on the pod is saved into the slave latch for the other pod in the pod pair. Then, when the master clock occurs, data captured on the pod, as well as the slave latch data, are saved in logic analyzer memory. As with master/slave mode, if multiple slave clocks occur before the next master clock, only the most recently acquired slave data is saved into logic analyzer memory.

See Also • To

• To set up the demultiplex sampling clock mode (see page 126)

**Dual Sample Sampling Clock Mode** In the Dual Sample state sampling clock mode, you can save data captured using the master clock at each of two different sample times into the same sample of analyzer memory.



When the master clock occurs, data on the pod is sampled twice using two independent sampling positions. Each of the two sample positions can be set using the Thresholds and Sample Positions dialog (see page 550).

The Dual Sample mode is often used to capture DDR memory bus activity using the common bus clock as the master clock. One sample position is used to capture write data and another is used to capture read data.

- See Also
- "To set up the dual sample sampling clock mode" on page 127
  - "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674

To set up the master only sampling clock mode 1From the menu bar, select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....

- 2 Select State.
- 3 In the State Options, change Clock Mode to Master.
- **4** Set up your master clock (see To set up the state sampling clock (see page 128)).

**See Also** • Master Only Sampling Clock Mode (see page 124)

To set up the master/slave sampling clock mode 1From the menu bar, select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....

- 2 Select State.
- 3 In the State Options, change Clock Mode to Master/Slave/Demux.

NOTE

- 4 Set up your master and slave clocks (see To set up the state sampling clock (see page 128)).
- 5 Select the Buses/Signals tab.
- 6 For each pod, click the clock button under the pod heading and choose either Master Clock or Slave Clock.

|   |   |    |    |    |    |     |    |     | Ро  | d 2 |     |     |      |    |    |   |   |    |    |    |    |     |    |     | Po  | d 1 |     |     |      | 88 |   | 88 | ä |
|---|---|----|----|----|----|-----|----|-----|-----|-----|-----|-----|------|----|----|---|---|----|----|----|----|-----|----|-----|-----|-----|-----|-----|------|----|---|----|---|
|   |   |    |    |    | T  | 'hr | es | ho  | ld: | TT  | L(  | 1.5 | i0 V | ŋ. |    |   |   |    |    |    | T  | 'nr | es | ho  | ld: | TΤ  | L ( | 1.5 | i0 1 | I) |   |    |   |
|   |   |    |    |    |    |     |    | Sla | ve  | Cle | ocł | ¢   |      |    |    |   |   |    |    |    |    |     | N  | las | ste | гC  | loc | :k  |      |    |   |    |   |
| 1 | t | F  | -  | -  | -  | -   | \$ | ‡   | -   | ţ,  | \$  | t   | \$   | _  | \$ | _ | _ | t  | _  | _  | _  | _   | _  | _   | _   | 1   | ‡   | \$  | 1    | 1  | ‡ | 1  | 1 |
| 1 | 0 | 15 | 14 | 13 | 12 | 11  | 10 | 9   | 8   | 7   | 6   | 5   | 4    | 3  | 2  | 1 | 0 | 15 | 14 | 13 | 12 | 11  | 10 | 9   | 8   | 7   | 6   | 5   | 4    | 3  | 2 | 1  | ( |
|   |   |    |    |    |    |     |    |     |     |     |     |     |      |    |    |   |   | 1  | ~  | ~  | 4  | 1   | ~  | 1   | 1   | 1   | 1   | 1   | 4    | 1  | 1 | 4  | ~ |
|   |   | 7  | 1  | 1  | 1  | 4   | 4  | 1   | 1   | 1   | J   | J   | 1    | J  | J  | V | V |    |    |    |    |     |    |     |     |     |     |     |      |    |   |    |   |

**See Also** • Master/Slave Sampling Clock Mode (see page 124)

## To set up the demultiplex sampling clock mode

To capture demultiplexed data, use only one pod of a pod pair.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....
- 2 Select the **State** acquisition mode.
- 3 In the State Options, change Clock Mode to Master/Slave/Demux.
- 4 Set up your master and slave clocks (see To set up the state sampling clock (see page 128)).
- 5 Select the Buses/Signals tab.
- 6 Click the clock button under the pod heading and choose Demultiplex.

| Bu | uses/Signals Sampling       |                      |          |      |     |      |    |    |    |     |    |   |   |              |   |            |    |    |   |   |   |   |   |   |   |    |    |     |     |    |     |     |    |   |            |   |      |
|----|-----------------------------|----------------------|----------|------|-----|------|----|----|----|-----|----|---|---|--------------|---|------------|----|----|---|---|---|---|---|---|---|----|----|-----|-----|----|-----|-----|----|---|------------|---|------|
| E  | inter buses and signals and | I the channels       | they cor | resp | pon | d to | D: |    |    |     |    |   |   |              |   |            |    |    |   |   |   |   |   |   |   |    |    |     |     | Di | spl | ау  | ¥  |   | Q          |   | Ð    |
| Γ  |                             |                      |          |      |     | 88   |    |    | _  | _   | _  | _ | _ | _            | _ | oci        | _  |    | 8 |   |   |   |   |   |   | Pe | od | 1 ( | Sla | we | C   | ocl | Ø. |   |            |   |      |
|    | Bus/Signal Name             | Channels<br>Assigned | Width    | ╞    |     | F    |    |    | Т  | hre | _  | _ | _ | TTL<br>Itipi | _ | .50        | V. | )  |   |   | ┥ |   |   |   |   |    |    |     |     |    |     |     |    |   |            |   |      |
|    |                             | Assigned             |          | ŧ    | \$  | ¢    | -  | -  | -  | -   | -  | - | - | \$           |   | 11         |    |    |   |   |   |   |   | - | - | -  |    |     |     |    |     |     |    |   | 1          |   |      |
|    |                             |                      |          | 1    | 0   | 15   | 14 | 13 | 12 | 11  | 10 | 9 | 8 | 7            | 6 | 5 4        | ٩. | 3  | 2 | 1 |   |   |   |   |   |    |    |     |     |    |     | 5   |    |   | -          | 1 | · ·  |
| L  | C Bus1_Slave                | Pod 1S[15:0]         | 16       |      |     |      |    |    |    |     |    |   |   |              |   |            |    |    |   |   |   | ∢ | ~ | ~ | √ | 1  | ~  | 4   | 4   | <  | ~   | ~   | √  | 1 | <b>v</b> - | √ | </td |
| I  | C Bus1_Master               | Pod 1M[15:0]         | 16       |      |     | 4    | 4  | 4  | ~  | ~   | ~  | 4 | 4 | 4            | 1 | <b>v</b> . | 1  | √. | 1 | 1 | ✓ |   |   |   |   |    |    |     |     |    |     |     |    |   |            |   |      |
| 1  |                             |                      |          | I    | J   |      |    |    |    |     |    |   |   |              |   |            |    |    |   |   |   |   |   |   |   |    |    |     |     |    |     |     |    |   |            |   | Þ    |

The display of the pod and the other pod in the pair changes. For example, if you set Pod 1 to demultiplex, Pod 2 goes away and you see two Pod 1 columns. The first Pod 1 column is labeled Pod 1 (Master Clock), and the second column is Pod 1 (Slave Clock).

Note that you can adjust sampling positions relative to the master clock and to the slave clock by assigning master and slave bus/signal names. (Note the "M" and "S" suffixes on pods in the **Channels Assigned** column to indicate "master clock" and "slave clock".) For more information on adjusting sampling positions, see To automatically adjust state sampling positions and threshold voltages (see page 130) or To manually adjust state sampling positions (see page 133).

**See Also** • Demultiplex Sampling Clock Mode (see page 124)

## To set up the dual sample sampling clock mode

To capture dual sample data, use only one pod of a pod pair.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....
- 2 Select State.
- 3 In the State Options, change Clock Mode to Dual Sample.
- **4** Set up your master clock (see To set up the state sampling clock (see page 128)).
- 5 Select the Buses/Signals tab.
- 6 Click the clock button under the pod heading, and choose Dual Sample.

| Bu | ses/Signals Sampling        |                      |          |         |     |       |    |    |    |    |    |           |   |   |   |   |          |        |    |   |    |    |    |    |    |    |    |    |    |     |      |    |     |   |   |            |   |
|----|-----------------------------|----------------------|----------|---------|-----|-------|----|----|----|----|----|-----------|---|---|---|---|----------|--------|----|---|----|----|----|----|----|----|----|----|----|-----|------|----|-----|---|---|------------|---|
| E  | nter buses and signals and  | the channels         | they cor | res     | pon | id to | D: |    |    |    |    |           |   |   |   |   |          |        |    |   |    |    |    |    |    |    |    |    |    | Dis | spla | ay | ×   |   | Q | 0          | 2 |
| Γ  |                             |                      |          | -       |     |       |    | 88 |    |    |    | (M<br>hol |   |   |   |   |          |        | ** |   | 88 | 8  |    |    | P  | od | 1  | Se | co | nd  | Sa   | m  | ale | 5 |   |            |   |
|    | Bus/Signal Name             | Channels<br>Assigned | Width    | <b></b> | t   | +     | -  |    | _  | _  | _  | )ua       | _ | _ | _ | _ | <b>†</b> | ,<br>† | t  | Ť | 1  | Ŧ  |    |    |    |    |    |    |    | Ť   | Ť    | Ť  | Ť   | Ť | Ť | <b>†</b> 1 | t |
|    |                             |                      |          | ī       | 0   | 15    | 14 | 13 | 12 | 11 | 10 | 9         | 8 | 7 | 6 | 5 | 4        | 3      | 2  | 1 | 0  | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7   | 6    | 5  | 4   | 3 | 2 | 1          | 0 |
|    | C Bus_2ndSamp               | Pod 1S[15:0]         | 16       |         |     |       |    |    |    |    |    |           |   |   |   |   |          |        |    |   |    | 4  | 4  | 4  | 1  | ~  | 4  | 4  | √  | 1   | 1    | 1  | 4   | 1 | 4 | √.         | 1 |
|    | <mark>)⊂</mark> Bus_MasSamp | Pod 1M[15:0]         | 16       |         |     | 4     | 4  | 1  | 4  | 4  | 1  | 4         | 4 | 4 | 1 | 4 | ~        | 4      | 4  | 4 | 4  |    |    |    |    |    |    |    |    |     |      |    |     |   |   |            |   |
|    |                             |                      |          | 4       |     |       |    |    |    |    |    |           |   |   |   |   |          |        |    |   |    |    |    |    |    |    |    |    |    |     |      |    |     |   |   |            | Þ |

The display of the pod and the other pod in the pair changes. For example, if you set Pod 1 to dual sample, Pod 2 goes away and you see two Pod 1 columns. The first Pod 1 column is labeled Pod 1 (Master Sample), and the second column is Pod 1 (Second Sample).

## NOTE

NOTE

Note that timing zoom data is only valid for the selected pod.

7 Assign bus/signal names to the channels in the master sample and to the channels the second sample.

Bus/signal names assigned to the master sample can have different sampling positions than the bus/signal names assigned to the second sample.

8 Adjust the state sampling positions differently for the bus/signals associated with the master sample and the buses/signals associated with the second sample (see To automatically adjust state sampling positions and threshold voltages (see page 130) or To manually adjust state sampling positions (see page 133)).

Note the "M" and "S" suffixes on pods in the **Channels Assigned** column to indicate "master sample" and "second sample".

- See Also "Dual Sample Sampling Clock Mode" on page 125
  - "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674

#### To set up the state sampling clock

The state clock should be set to match the clock signal on your device under test. The logic analyzer can handle clock signals comprised of up to four lines. Clocks can be as simple as a single rising edge, or a complicated combination of edges and highs or lows.

| Pod:      | 4    | 3    |      | 1    |       |
|-----------|------|------|------|------|-------|
| Clock:    | Clk4 | Clk3 | Clk2 | Clk1 |       |
| Activity: |      |      |      |      | 1     |
| Master:   | X    | X    | X    | £    | Clk1↑ |

In the picture above, the clocks refer to the clock signal lines on pods 1 through 4. Depending on model, your logic analyzer may have more pods. However, only the clock lines on the first 4 pods can be used to generate the state clock signal. Clock lines on extra pods can be used like normal data lines.

- 1 Attach logic analyzer pods to your device under test. Clock signals must be connected to the clock lines on pods 1 through 4.
- 2 From the menu bar, select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....
- **3** Select **State Synchronous Sampling**. The State Options area becomes active.
- **4** Select the state clock mode (see page 123). Most measurements use only the master clock.
- **5** Set up a clock description to match the clock(s) in your device under test.

| X          | Don't care. Clock line not used in this clock. |
|------------|--|
| F          | Rising edge.                                   |
| ٦ <u>۲</u> | Falling edge.                                  |
| R I        | Both edges.                                    |
| 1          | Qualifier - high.                              |
| 0          | Qualifier - low.                               |

A clock description must have at least one edge.

See Also

- "Setting up the State Sampling Clock in the 16960 Logic Analyzers" on page 659
- "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674
- "Selecting the State Sampling Clock Mode" on page 123
- "To automatically adjust state sampling positions and threshold voltages" on page 130
- "To manually adjust state sampling positions" on page 133
- "To set up advanced clocking" on page 129

**To set up advanced clocking** If you want to specify more complex clock setups than you can with the normal Master or Slave selections (for example, if you want to use a specific clock channel both as an edge and a qualifier in the same clock description), you need to use advanced clocking.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>State/Timing (Sampling)....
- 2 Select State mode. The state options become selectable.
- **3** Next to the clock mode, select **Advanced Clocking**. The clock controls are replaced by a button.
- 4 Select Master Clock... or Slave Clock... as appropriate.
- **5** In the Advanced Clocking Setup Dialog (see page 495), choose settings as appropriate.

Clock channels can be used both as primary clocks and as clock qualifiers.

6 Click **OK** to close the dialog. The clock description in the Analyzer Setup window updates.

NOTE

If you un-check advanced clocking, all qualifiers are erased.

### **See Also** • Pod and Channel Naming Conventions (see page 418)

#### To automatically adjust state sampling positions and threshold voltages

When adjusting the state mode sampling position with *eye finder* or *eyescan*, the logic analyzer looks at signals from the device under test, figures out the threshold voltage that results in the widest possible data valid window, then figures out the location of the data valid window in relation to the sampling clock, and automatically sets the threshold voltage and sampling position.

Because *eye finder/eyescan* automatically sets the sample position on individual channels, it can correct for the small skew effects caused by probe cables and circuit board traces. This makes the logic analyzer's setup/hold window smaller and lets you accurately capture data at higher clock speeds.

NOTE

You use the *Eye Finder* feature with 16960/62 series of Agilent Logic Analyzers. You use the *Eyescan* feature with the U4154A Logic Analyzer to automatically adjust sample positions on individual channels. Refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690 to know more about the eyescan feature.

#### *Eye finder* requires:

- At least 10 transitions on each signal during its run. (You can use the advanced *eye finder* settings to cause longer or shorter runs.)
- All devices which can drive each signal should contribute to the stimulus.
- All device under test operating modes relevant to the eventual logic analysis measurement should contribute to the stimulus as well.

*Eye finder* measurements and normal logic analyzer measurements cannot run simultaneously.

### **To run eye finder** 1 Probe the device under test by connecting the logic analyzer channels.

- 2 Assign bus/signal names to those logic analyzer channels.
- **3** Make sure that the device under test and the logic analyzer have warmed up to their normal operating temperatures.

NOTE

- **4** Select the state (synchronous sampling) mode (see To select the state acquisition mode (see page 122)).
- 5 In the Sampling Setup dialog, click Thresholds and Sample Positions....
- 6 In the Thresholds and Sample Positions dialog (see page 550), select the buses/signals on which you wish to run *eye finder*.

You may want to run *eye finder* on channel subsets, for example, when certain bus signals transition in one operating mode (of the device under test) and other bus signals transition in a different operating mode.

- 7 Select the type of *eye finder* run you want:
  - Auto Sample Position Setup performs a full time scan at the currently specified threshold voltage to determine the optimal sampling position.
  - Auto Threshold and Sample Position Setup adjusts the threshold voltages while watching activity indicators to find the signal activity envelope and optimal threshold voltage setting; then, performs a full time scan at that threshold, to automatically determine the optimal sampling position.
  - **Eye Scan with Threshold and Sample Position Setup** performs full time scans across the full signal activity envelope to display oscilloscope-like eye diagrams along with optimal threshold voltage and sampling position settings.
  - **Eye Scan with Sample Position Setup Only** performs full time scans across the full signal activity envelope to display oscilloscope-like eye diagrams along with sampling position settings only.
  - Linear Scan Only (no settings changed) without changing the current sample position settings, performs a linear scan (like the Auto Sample Position Setup) and shows you suggested sample positions. Manual adjustments are not allowed.
  - **Eye Scan Only (no settings changed)** without changing the current sample position and threshold settings, performs an Eye Scan and shows you suggested sample positions and thresholds. Manual adjustments are not allowed.
- 8 Click Run.

After checking clock and qualifier inputs for activity and the appropriate thresholds, the *eye finder* measurement runs.

When *eye finder* finds more than one stable region on a channel, it uses the current sampling position as a hint about which stable region it should suggest a position for. If *eye finder* picks the wrong stable region, you can expand the bus/signal and drag the Sampling Position bar or dotted line (blue in stable regions, red in transitioning regions) into the correct stable region. The suggested sampling position for that region will be shown (see How Selected/Suggested Positions Behave (see page 557)).

You can also adjust the threshold voltage setting by dragging the Threshold bar or dotted line. Note that this affects all channels on the same pod (and sometimes the clock input on the pod as well).

**9** If you have moved the sampling position and wish to return to the suggested positions, go to the Thresholds and Sample Positions dialog, right-click on a bus/signal, and choose the **Set Sampling Position to Suggested** command.

If you have moved the threshold voltage setting and wish to return to the suggested positions, go to the Thresholds and Sample Positions dialog, right-click on a bus/signal, and choose the **Set Threshold to Suggested** command.

For more information on the *eye finder* measurement results, right-click on a bus/signal and choose **Properties...** to open the Eye Finder Properties dialog (see page 557). For more information on informational messages in the Thresholds and Sample Positions dialog, see Eye Finder Info Messages (see page 388).

*Eye finder* finds optimal threshold voltages and sample positions for the actual specific conditions -- amplitude, offset, slew rates, and ambient temperature. Therefore, you will get the best results by running *eye finder* under the same conditions that will be present when logic analysis measurements are made.

When running normal logic analyzer measurements, you will be warned if the sampling clock setup, clock thresholds, or sampling clock mode has changed since the last *eye finder* measurement.

To run eye finder repetitively

2 In the Eye Finder Advanced Options dialog (see page 555), select the **Run Mode** tab.

1 In the Thresholds and Sample Positions dialog, click Advanced....

- 3 Check Run Repetitively.
- 4 Click OK.
- 5 In the Thresholds and Sample Positions dialog, click Run.

In the Thresholds and Sample Positions dialog, you can see how the stable and transitioning areas vary over time.

6 To stop the repetitive run, click Stop.

To view eye finder data as a bus composite When you want a compressed, high-level view of the eye finder data:

1 In the Thresholds and Sample Positions dialog, right-click on the sampling position diagram for a bus, and choose the **View Bus As Composite** command.



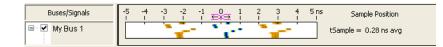
Average sampling positions as well as stable and transitioning areas are displayed for the whole bus. This is the default. Stable areas show positions where every channel in the bus is stable.

To view eye finder data as a stack of channels

data

When you want more resolution in your view of the *eye finder* data:

1 In the Thresholds and Sample Positions dialog, right-click on the sampling position diagram for a bus, and choose the **View Bus As Stack Of Channels** command.



Individual sampling positions and stable and transitioning areas for all the channels in a bus are shown.

To clear eye<br/>finder1In the Thresholds and Sample Positions dialog, right-click on a<br/>bus/signal name, and choose Clear Measurement.measurement

- **See Also** Understanding State Mode Sampling Positions (see page 424)
  - Eye Finder Advanced Options Dialog (see page 555)
  - To manually adjust state sampling positions (see page 133)

### To manually adjust state sampling positions

For 16960/62 series of Logic Analyzers. you use the Thresholds and Sample Positions dialog to manually adjust state sampling positions.

In the Thresholds and Sample Positions dialog, you can manually adjust state mode sampling positions without running *eye finder* (which automatically adjusts state sampling positions).

- 1 Select the state (synchronous sampling) mode (see To select the state acquisition mode (see page 122)).
- 2 In the Sampling Setup dialog, click Thresholds and Sample Positions....

#### **5** Setting Up the Logic Analyzer

3 In the Thresholds and Sample Positions dialog (see page 550), drag the blue sampling position bars to the proper locations.

You can expand or collapse the channels in a bus.

## TIP

To adjust the sample position and/or threshold voltage for multiple buses and signals at the same time, you can group those buses and signals into a folder in the Buses/Signals Setup dialog; then, in the Thresholds and Sample Positions dialog, you can adjust the composite for the folder.

For U4154A Logic Analyzer. you use the Eye Scan - Sample Positions and Thresholds Settings dialog to manually adjust state sampling positions.

In the Eye Scan - Sample Positions and Thresholds Settings dialog, you can manually adjust state mode sampling positions without running eye scan (which automatically adjusts state sampling positions).

- **1** Select the state (synchronous sampling) mode (see To select the state acquisition mode).
- 2 In the Sampling Setup dialog, click **Eye Scan: Sample Positions and Thresholds....** button.
- **3** In the Eye Scan Sample Positions and Thresholds Settings dialog, drag the blue sampling position bars to the proper locations.

You can expand or collapse the channels in a bus.

Sampling positions are saved with the logic analyzer configuration (see To save a configuration file (see page 206)).

- **See Also** Understanding State Mode Sampling Positions (see page 424)
  - To automatically adjust state sampling positions and threshold voltages (see page 130)

# In Either Timing Mode or State Mode

- To specify the trigger position (see page 134)
- To set acquisition memory depth (see page 135)

## To specify the trigger position

The trigger position specifies the amount of trace memory used for samples captured after the trigger. For example, when 10% poststore is selected, 90% of trace memory is used for samples captured before the trigger. When 90% poststore is selected, 10 % of trace memory is used for samples captured before the trigger. When **Force Prestore** is checked, the amount of pre-trigger and post-trigger memory is always what you expect because, after a run, the logic analyzer fills pre-trigger memory before it starts looking for a trigger. If the event you want to trigger on occurs while pre-trigger memory is being filled, the logic analyzer does not trigger.

When **Force Prestore** is unchecked, the trigger position may not end up being where you expect because the logic analyzer starts looking for a trigger immediately after a run (it does not wait for pre-trigger memory to be filled). For example, if you set the trigger position to 50%, but the logic analyzer finds the trigger right away, the amount of pre-trigger memory is less than you expect.

- From the menu bar select Setup>(Logic Analyzer Module)>Timing/State (Sampling)..., or click the ≝ icon from the setup toolbar (see page 471).
- 2 Select the trigger position, and check or uncheck Force Prestore as desired.

| Trigger Posit | ion       |       |
|---------------|-----------|-------|
| 50 🔳          | -+ % Post | store |
|               |           |       |
| M             | ÷         |       |
| V Force P     | restore   |       |
|               |           |       |

- See Also Understanding Logic Analyzer Triggering, The Conveyor Belt Analogy (see page 431)
  - To set the acquisition memory depth (see page 135)

#### To set acquisition memory depth

The acquisition depth control lets you set the amount of memory that is filled with data on an acquisition. The choices available depend on the maximum memory depth available in the analyzer that is being used.

- 1 From the menu bar select Setup>(Logic Analyzer Module)>Timing/State (Sampling)....
- **2** Set the acquisition mode and any state or timing options. These will affect the available memory choices.
- 3 In the Options box to the right, set Acquisition Depth.

| Acquisition Depth:  | 32M 🗸              |
|---------------------|--------------------|
| hresholds and Sampl | 4K<br>8K<br>16K    |
|                     | 32K<br>64K<br>128K |
| Clock Description   | 1M                 |
|                     | 2M<br>4M<br>8M     |
|                     | 16M<br>32M         |

- **See Also** Memory Depth and Channel Count Trade-offs (see page 420)
  - Logic Analyzer Notes, Channels and Memory Depth (see page 635)
  - Understanding Logic Analyzer Triggering, The Conveyor Belt Analogy (see page 431)
  - To specify the trigger position (see page 134)

# **Using Timing Zoom**

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer.

The timing zoom settings are accessed through the TimingZoom box in the Sampling tab.

- To turn timing zoom on or off (see page 138)
- To specify the timing zoom sample period (on some logic analyzers) (see page 138)
- To specify the timing zoom trigger position (see page 138)
- To align timing zoom in a split analyzer (see page 138)
- What is TimingTiming zoom collects a window of additional high-speed timing dataZoom?around the trigger of the logic analyzer.

Because of timing zoom's faster sample rate, you get a higher-resolution view of transitions than with the normal timing mode. Timing zoom data appears in rows with "(TZ)" after bus/signal names.

| M1 to M2 = 250 ps M3 | to M4 = 1.667 ns |                    |                 |
|----------------------|------------------|--------------------|-----------------|
| Scale 500 ps/div 📓   | Delay            | -252.5 ns          | 🖩 阔 <u>Jt</u> T |
| Bus/Signal           | 53.5 ns          | ₩1 ₩2<br>-252.5 ns | -251.5          |
| ⊞∰ My Bus 1          | 9F 🚶             | вэ                 | X A0            |
| 🛱 My Signal 1        | 1                | 0                  |                 |
| ⊞-∰ My Bus 1 (TZ)    | Х в9             |                    | AÖ              |
| 🗍 My Signal 1 (TZ)   | 1                | o                  |                 |
| Time                 | -253.5 ns        | 1                  | -251.5 ns       |
| •                    |                  |                    |                 |
| 🔧 Overview           | Listing-1        | Waveform-1         |                 |

Because of the faster sample rate and the relatively smaller amount of memory for samples, the overall window of time captured by timing zoom is smaller. Timing zoom data is captured around the trigger.

| M1 to M2 = 16.37625 us Beginn | ing Of Data to <mark>End Of D</mark> | <mark>ata</mark> = 436.905 us |         |
|-------------------------------|--------------------------------------|-------------------------------|---------|
| Scale 150 us/div 📓 👥          | tt Delay                             | -252.5 ns 📓 📕                 |         |
| Bus/Signal                    | 300 us -150 us                       | -253 ns 150 us                | 300 u:  |
| ⊞∰ My Bus 1                   |                                      |                               |         |
| 🕻 My Signal 1                 |                                      |                               | 1       |
| ⊞-‡ My Bus 1 (TZ)             |                                      |                               |         |
| 🗄 My Signal 1 (TZ)            |                                      | 249.4                         |         |
| Time                          | -218.453 <mark>33 us</mark>          | 210.4                         | 5167 us |
| <u>د</u>                      |                                      |                               |         |
| Verview                       | Listing-1                            | Waveform-1                    |         |

See Also • Logic Analyzer Notes, Timing Zoom (see page 637)

### To turn timing zoom on or off

If you are not interested in the timing zoom data for a measurement, you can improve logic analyzer performance by turning off timing zoom.

1 In the Sampling tab, check or uncheck **Enable** in the TimingZoom box.

#### To specify the timing zoom sample period (on some logic analyzers)

With some logic analyzers (see Logic Analyzer Notes, Timing Zoom (see page 637)), you can change the sampling period to see more or less sampling resolution around the trigger.

- 1 In the Sampling tab, check **Enable** in the TimingZoom box.
- 2 Click Setup... in the TimingZoom box.
- 3 In the TimingZoom Setup dialog (see page 558), select the Sampling Period.
- **See Also** Logic Analyzer Notes, Timing Zoom (see page 637)

### To specify the timing zoom trigger position

- 1 In the Sampling tab, check **Enable** in the TimingZoom box.
- 2 Click **Setup...** in the TimingZoom box.
- 3 In the TimingZoom Setup dialog (see page 558), drag the **Trigger Position** slider bar to the desired setting.

The trigger position specifies the amount of timing zoom memory used for samples captured after the trigger. For example when "10% poststore" is selected, 90% of timing zoom memory is used for samples captured before the trigger.

**See Also** • Logic Analyzer Notes, Timing Zoom (see page 637)

### To align timing zoom in a split analyzer

On some older logic analyzer modules, if you have split the analyzer, you need to specify which analyzer's trigger timing zoom should be aligned with.

- 1 In the Sampling tab, check **Enable** in the TimingZoom box.
- 2 Click Setup... in the TimingZoom box.
- 3 In the TimingZoom Setup dialog (see page 558), select the logic analyzer to Align Trigger With.

# **Setting Up Symbols**

You can use symbol names in place of bus/signal data values when:

- Setting up triggers.
- Displaying captured data.
- Searching for bus/signal values in the display windows.
- Setting up the Filter/Colorize tool.

Symbol names can be: variable names, procedure names, function names, source file line numbers, etc.

You can enter user-defined symbol names, or you can load symbol name definitions from a program's object file or from a general-purpose ASCII format symbol file.

- To create user-defined symbols (see page 139)
- To load symbols from a file (see page 141)
- To run the symbol reader outside the application (see page 142)
- To create an ASCII symbol file (see page 143)
- To change symbol reader options (see page 143)

Multiple user-defined symbols can have the same name and different values. Symbol value lookups are based on the name and the value.

Multiple symbols with the same name are not allowed when loading symbols from a file. When a symbol file has multiple symbols with the same name, the first is accepted and the rest are ignored.

When two or more symbols have the same value, the first symbol name matching the value is used (even though you may have selected one of the others).

See Also • To enter symbolic bus/signal values (see page 146)

## To create user-defined symbols

You can create and edit user-defined symbols for bus/signal values.

| To add a     | 1 | Select Setup>(Logic Analyzer Module)>Symbols |
|--------------|---|--|
| user-defined |   |  |
| symbol       |   | Setup  |
|              |   |  |

| Decob                    |
|--------------------------|
| 📴 Bus/Signal             |
| ∰ Iming/State (Sampling) |
| Simple Trigger           |
| Tris Advanced Trigger    |
| Store Trigger            |
| <u>R</u> ecall Trigger   |
| Symbols                  |
| Pod Assignment           |
| Split Analyzer           |
| Disable                  |
| <u>R</u> ename           |
| Advanced •               |

2 In the Symbols dialog (see page 545), select the bus or signal for which the new symbol should be displayed.

Each symbol is defined for a particular bus/signal.

- 3 Click Add....
- 4 In the Add Symbol dialog, define a value or range of values.

| 📲 Add Symbol to Bus/Si | gnal: My Bus 1 |              | ×     |
|------------------------|----------------|--------------|-------|
| My Symbol 1            | <b>H</b> =     | ▼ XX H Hex ¥ |       |
|                        |                | OK Apply     | Close |

There are no restrictions on the characters you can use in the name of a symbol.

Many identical symbols for a bus/signal can be entered, all with unique or identical values. During symbol lookup by a window or tool, the first symbol that matches the pattern is used. This is why the Symbol dialog has **Move Up** and **Move Down** buttons for reordering symbols.

5 Click Apply.

To see the symbols in the listing or waveform display, click OK in the Symbols dialog and change the base (see page 267) for the bus/signal to Symbols.

# NOTE

Because XML format logic analyzer configuration files save and load user-defined symbols, you can also add symbols by (1) using text processing tools to re-format symbol information from software development tools, (2) inserting them into an XML format configuration file, and (3) loading the configuration file into the *Agilent Logic Analyzer* application (see "XML Format" (in the online help)).

| To edit a<br>user-defined<br>symbol   | <ol> <li>Select Setup&gt;(Logic Analyzer Module)&gt;Symbols</li> <li>Select the symbol you want to edit.</li> <li>Click Edit.</li> </ol>                               |
|---------------------------------------|--|
| To delete a<br>user-defined<br>symbol | <ol> <li>Select Setup&gt;(Logic Analyzer Module)&gt;Symbols</li> <li>Select the symbol you want to delete.</li> <li>Click Delete.</li> </ol>                           |
| To save symbols                       | Save symbols as part of a configuration file (see page 206). Symbols are saved in the configuration whether or not you select <b>Setup only</b> in the Save As dialog. |
|                                       | You can move user-defined symbols from one bus/signal to another by<br>saving to an XML format configuration file, editing, then reloading the file.                   |
| See Also                              | • Displaying Names (Symbols) for Bus/Signal Values (see page 269)  |

# To load symbols from a file

You can load symbols from object files, which are created by your compiler/linker or other software development tools, or you can load symbols from a general-purpose ASCII (GPA) format symbol files.

- **1** Create the symbol file:
  - Generate an object file with symbolic information using your software development tools (see Object File Formats Supported by the Symbol Reader (see page 600)).
  - Generate an Agilent Symbol Reader ".sym" file by running the symbol reader outside of the *Agilent Logic Analyzer* application (see page 142); loading symbols from ".sym" files is faster than loading them from object files.
  - If your language tools cannot generate object file formats that are supported by the logic analyzer, create an ASCII symbol file (see page 143).
- 2 From the *Agilent Logic Analyzer* application's main menu bar, choose Setup>(Logic Analyzer Module)>Symbols....
- 3 In the Symbols dialog (see page 545), select the bus/signal name you want to load object file symbols for.

In most cases, you will select the bus/signal representing the address bus of the processor you are analyzing.

- 4 Click Load....
- **5** In the Select Symbol File dialog, select the file from which you want to load symbols.
- 6 Click Open.

The name of the symbol file is saved when a configuration file is saved. The symbol file will be reloaded when the configuration is loaded.

| To reload symbols          | 1 Choose Setup>(Logic Analyzer Module)>Symbols   |
|----------------------------|--|
| from a file                | <b>2</b> In the Symbols dialog (see page 545), select the symbol file whose symbols you want to reload.                        |
|                            | 3 Click Load   |
|                            | The values of the symbols being used in the trigger sequence are updated<br>automatically each time a symbol file is reloaded. |
| To delete a<br>symbol file | 1 Choose Setup>(Logic Analyzer Module)>Symbols   |
|                            | <b>2</b> In the Symbols dialog (see page 545), select the symbol file whose symbols you want to delete.                        |
|                            | 3 Click <b>Delete</b> .  |
| See Also                   | • Object File Formats Supported by the Symbol Reader (see page 600)  |
|                            |  |

# To run the symbol reader outside the application

You can run the symbol reader outside the *Agilent Logic Analyzer* application to create an Agilent Symbol Reader ".sym" file that loads faster than the object file.

- 1 Open a Command Prompt window.
- 2 Run the command:

agSymbolBuild.exe [-r <readers.ini>] <object\_file> <dest\_file>.sym

For example:

agSymbolBuild.exe q.elf q.sym

The **agSymbolBuild.exe** symbol reader program is located in the directory:

<Drive letter>:\<Install directory>\SymbolReaders\

For example:

C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\

To change the symbol reader options, copy the readers.ini file from the SymbolReaders directory, edit it, and use the -r <readers.ini> option when running the **agSymbolBuild.exe** program.

For more information on the symbol reader program, see the README.txt file in the SymbolReaders directory.

**See Also** • To load symbols from a file (see page 141)

• To change symbol reader options (see page 143)

## To create an ASCII symbol file

General-purpose ASCII (GPA) symbol files are created by converting object file symbols to a GPA format symbol files and/or by using text editing/processing tools.

To convert object<br/>file symbols to<br/>GPA format<br/>symbol filesWhen you need to apply different offsets to different symbols or sections<br/>of code, you can convert object file symbols to general-purpose ASCII<br/>(GPA) format symbol files. Then, you can use text editing/processing tools<br/>to adjust the symbol or section offset values in the GPA format file before<br/>loading the file into the Agilent Logic Analyzer application.

- 1 Open a Command Prompt window.
- **2** Run the command:

agSymbolQuery.exe -a <object\_file> <dest\_file>.sym > GPA\_file

For example:

agSymbolQuery.exe -a q.elf q.sym > q.gpa

The **agSymbolQuery.exe** program is located in the directory:

<Drive letter>:\<Install directory>\SymbolReaders\

For example:

C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\

For more information on the **agSymbolQuery.exe** program, see the README.txt file in the SymbolReaders directory.

**See Also** • General-Purpose ASCII (GPA) Symbol File Format (see page 601)

# To change symbol reader options

You can change how ELF/Stabs, Ticoff, or Coff/Stabs symbol files are processed by editing the readers.ini file.

1 Make a backup copy of the readers.ini file.

The readers.ini file is located in the directory:

<Drive letter>:\<Install directory>\SymbolReaders\

For example:

C:\Program Files\Agilent Technologies\Logic Analyzer\SymbolReaders\

2 Edit the readers.ini file.

For more information on the symbol reader options, see the comments in the readers.ini file.

# 5 Setting Up the Logic Analyzer

# **Reader Options**

| SectionReloc              | Use the following options to specify the relocation. Replace <sectionname> with the name of your section. Replace <hex_relocation_value> with the hex relocation amount (32-bit max). You can set the relocation for section to an absolute value or you can add a relative relocation amount. The relocation value will be calculated using unsigned 32-bit math.</hex_relocation_value></sectionname> |  |  |  |
|---------------------------|---|--|--|--|
|                           | [SectionReloc]<br>Place this before all relocation options.   |  |  |  |
|                           | AddReloc_AllSections= <hex_relocation_value><br/>Relocates all sections by an amount specified.<br/>If this command is used with subsequent relocation commands<br/>the subsequent commands will override this operation.</hex_relocation_value>  |  |  |  |
|                           | AddReloc_ <sectionname>=<hex_relocation_value><br/>Adds a relative relocation value.</hex_relocation_value></sectionname>   |  |  |  |
|                           | SetReloc_ <sectionname>=<hex_relocation_value><br/>Relocates the section to the absolute address specified.</hex_relocation_value></sectionname>  |  |  |  |
|                           | NonReloc_ <sectionname>=TRUE<br/>Inhibits a section from being relocated.<br/>It is only useful when it follows a AddRloc+AllSections.</sectionname>  |  |  |  |
| C++Demangle               | 1= Turn on C++ Demangling (Default)<br>0= Turn off C++ Demangling   |  |  |  |
| C++DemOptions             | <pre>803= Standard Demangling<br/>203= GNU Demangling (Default Elf/Stabs)<br/>403= Lucid Demangling<br/>800= Standard Demangling without function parameters<br/>200= GNU Demangling without function parameters<br/>400= Lucid Demangling without function parameters</pre>  |  |  |  |
| MaxSymbolWidt<br>h        | 80= Column width max of a function or variable symbol<br>Wider symbols names will be truncated.<br>(Default 80 columns)   |  |  |  |
| OutSectionSymbo<br>IValid | <pre>0= Symbols whose addresses aren't within the<br/>defined sections are invalid (Default)<br/>1= Symbols whose addresses aren't within the<br/>defined sections are valid</pre>  |  |  |  |
|                           | This option must be specified in the Nsr section of the Readers.ini file:   |  |  |  |
|                           | [Nsr]<br>OutSectionSymbolValid=1  |  |  |  |
| ReadElfSection            | 2= Process all globals from ELF section (Default)<br>Get size information of local variables 1= Get size information of global and local variables<br>Symbols for functions will not be read, and<br>only supplemental information for those symbols in<br>the Dwarf or stabs section will be read. 0= Do not read the Elf Section  |  |  |  |
|                           |   |  |  |  |

If a file only has an ELF section this will have no effect and the ELF section will be read completely. This can occur if the file was created without a "generate debugger information" flag (usually -g). Using the -g will create a Dwarf or Stabs debug section in addition to the ELF section.

ReadOnlyTicoffPaReadOnlyTicoffPage tells the ticoff reader to read only the symbolsgeassociated with the specified page (as an example 'ReadOnlyTicoffPage=0'<br/>reads only page 0 symbols). A value of -1 tells the ticoff readers to read<br/>symbols associated with all pages.

ReadOnlyTicoffPage=-1 Read all symbols associated will all ticoff pages (Default) ReadOnlyTicoffPage=p Read only symbols associated with page 'p' (where p is any integer between 0 and n the last page of the object file).

AppendTicoffPag
AppendTicoffPage tells the ticoff reader to append the page number to the symbol value. This assumes that the symbol value is 16-bits wide and that that page number is a low positive number which can be ORed into the upper 16 bits of an address to create a new 32-bit symbol address. For example, if the page is 10 decimal and the symbol address is 0xF100 then the new symbol address will be 0xAF100.

AppendTicoffPage=1 Append the ticoff page to the symbol address AppendTicoffPage=0 Do not append the ticoff page to the symbol address (Default)

#### **Examples**

| Example for<br>Elf/Stabs                           | [ReadersElf]<br>C++Demangle=0<br>C++DemOptions=203<br>MaxSymbolWidth=60                   |
|--|---|
|  | StabsType=2   |
| Example for<br>Coff/Stabs (using<br>Ticoff reader) | [ReadersTicoff]<br>C++Demangle=0<br>C++DemOptions=203<br>MaxSymbolWidth=60<br>StabsType=2 |
| Example for Ticoff                                 | [ReadersTicoff]<br>C++Demangle=0  |

```
C++DemOptions=203
MaxSymbolWidth=60
ReadOnlyTicoffPage=4
AppendTicoffPage=1
```

#### To enter symbolic bus/signal values

When entering bus/signal values while setting up triggers, searching display windows, or setting up the Filter/Colorize tool:

- 1 Select the desired operator for the bus/signal value.
- 2 Select the Symbol number base.
- **3** Click the value button.
- **4** In the Select Symbol dialog (see page 530), select the symbol you want to use.

All of the symbols for the current bus/signal, regardless of type, are available in the dialog.

- 5 Click OK.
- **See Also** Select Symbol Dialog (see page 530)

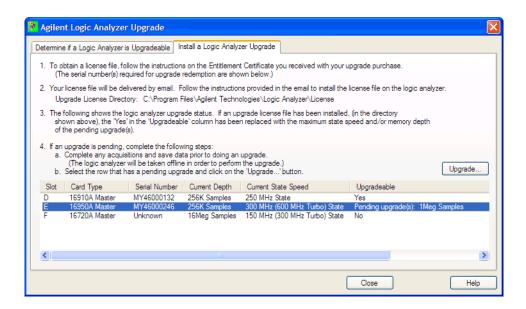
#### **Installing Licensed Hardware Upgrades**

Some of the newer logic analysis system cards (like the 16910/11A or 16950 logic analyzers or 16850-series logic analyzers) have hardware features (like state speed and memory depth) that can be upgraded by purchasing a license.

| NOTE | When installing licensed hardware upgrades, you must run the <i>Hardware Update Utility</i> program on the frame that contains the cards you want to upgrade. In other words:  |  |  |  |
|------|--|--|--|--|
|      | <ul> <li>In a multiframe logic analysis system, you must run the <i>Hardware Update Utility</i> program on each frame that has cards to be upgraded.</li> <li>You cannot install module upgrades over a remote connection (including remote connections via Remote Desktop, NetOp, or RealVNC).</li> </ul> |  |  |  |
|      | To install a licensed hardware upgrade:  |  |  |  |
|      | 1 After you have ordered the hardware upgrade product/option and have received your license file, copy the license file to the directory:  |  |  |  |
|      | C:\Program Files\Agilent Technologies\Logic Analyzer\License\  |  |  |  |
|      | If you have installed the <i>Agilent Logic Analyzer</i> application in a different directory, copy the license file to the directory:  |  |  |  |
|      | <drive letter="">:\<install directory="">\License\</install></drive>   |  |  |  |
|      | If upgrade options were ordered for several cards at the same time,<br>there will be one license file for all submitted serial numbers.  |  |  |  |
|      | License file names must have the ".lic" extension in order to work.  |  |  |  |
|      | 2 In the <i>Agilent Logic Analyzer</i> application, choose <b>Help&gt;Logic Analyzer Upgrade</b> .   |  |  |  |
|      | Or, from the Windows Start bar, click <b>Start&gt;All Programs&gt;Agilent</b><br>Logic Analyzer>Utilities>Hardware Update Utility.   |  |  |  |
| NOTE | The Agilent Logic Analyzer Upgrade dialog will read "No Hardware Found" for 1680/1690-series logic analyzers because they do not contain upgradeable modules. This is  |  |  |  |

not an indication of a problem with your hardware.

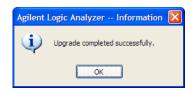
**3** In the Agilent Logic Analyzer Upgrade dialog's "Install a Logic Analyzer Upgrade" tab, select the card that has an upgrade pending.



#### CAUTION

The *Agilent Logic Analyzer* application will be taken offline in order to perform the upgrade. Therefore, complete any acquisitions and save data before performing the upgrade.

- 4 Click Upgrade....
- 5 When the upgrade completed information dialog appears, click OK.



The Agilent Logic Analyzer Upgrade dialog shows the upgraded hardware.

6 Click Close to close the Agilent Logic Analyzer Upgrade dialog.

Once you complete the hardware upgrade, the hardware will retain its new settings and can be moved to any 16900-series logic analysis system frame.

Agilent Logic and Protocol Analyzer Online Help

## Ag On On Of C

### Capturing Data from the Device Under Test

After you have probed the device under test (see page 81) and set up the logic analyzer (see page 97) (by defining buses and signals (see page 104) and choosing the sampling mode (see page 119)), you are ready to tell the logic analyzer when to capture/acquire data (in other words, set up a trigger) and run the measurement.

You can set up:

- *Quick Triggers* by drawing a box in a display window around the data to trigger on,
- *Simple Triggers* in a display window by specifying bus/signal values to trigger on, or
- Advanced Triggers by opening a dialog box and choosing from collections of predefined trigger functions (see page 560).

Advanced triggers let you trigger the logic analyzer after a sequence of events occur in the device under test.

Once you have set up a trigger, you can run the measurement. When the measurement completes, you can view the captured data (see page 219) and save it (along with the logic analyzer setup).

- Setting Up Quick (Draw Box) Triggers (see page 152)
  - To set a Quick Trigger in the Waveform window (see page 152)
  - To set a Quick Trigger in the Listing window (see page 153)
  - To set a Quick Trigger in the Source window (see page 154)
- Specifying Simple Triggers (see page 156)
  - To specify bus patterns in a simple trigger (see page 157)
  - To specify signal levels in a simple trigger (see page 158)
  - To set a bus/signal edge in a simple trigger (see page 159)
- Specifying Advanced Triggers (see page 163)
  - To replace or insert trigger functions into trigger sequence steps (see page 169)
  - To specify bus/signal patterns (see page 169)



- To set a bus/signal edge in an advanced trigger (see page 171)
- To specify packet events (in "Find a packet" trigger function) (see page 175)
- To specify a trigger sequence step's goto or trigger action (see page 178)
- To specify default storage (see page 179)
- To insert or delete events (see page 180)
- To negate events (see page 183)
- To change the evaluation order of AND/OR'ed events (see page 184)
- To choose between a duration or occurrence count for events (timing mode) (see page 184)
- To insert or delete actions (in a trigger sequence step) (see page 185)
- To cut, copy, and paste trigger sequence steps (see page 188)
- To delete trigger sequence steps (see page 189)
- To show a trigger sequence step as Advanced If/Then trigger functions (see page 189)
- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)
- To display or hide "If" clause comments (see page 190)
- To clear the trigger sequence (see page 192)
- Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)
- Storing and Recalling Triggers (see page 201)
  - To store a trigger (see page 201)
  - To recall a trigger (see page 202)
  - To set the trigger history depth (see page 202)
- Running/Stopping Measurements (see page 203)
- Saving Captured Data (and Logic Analyzer Setups) (see page 205)
  - To save a configuration file (see page 206)
  - To export data to standard CSV format files (see page 207)
  - To export data to module CSV format files (see page 210)
  - To export data to module binary (ALB) format files (see page 213)
  - To export data to 16700 ASCII format files (see page 215)
- Extending Capture Capability with VBA (see page 217)
- **See Also** Probing the Device Under Test (see page 81)

- Setting Up the Logic Analyzer (see page 97)
- Defining Buses and Signals (see page 104)
- Choosing the Sampling Mode (see page 119)
- Analyzing the Captured Data (see page 219)

#### Setting Up Quick (Draw Box) Triggers

Within the Waveform, Listing, and Source windows, you can quickly set up a simple trigger by drawing a rectangle with the mouse or right-clicking on a source line.

After the simple trigger has been defined, and the analyzer is run, the trigger saved in the most recently used triggers list and can be recalled (see page 202) at any time.

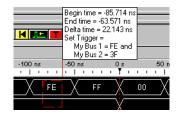
- To set a Quick Trigger in the Waveform window (see page 152)
- To set a Quick Trigger in the Listing window (see page 153)
- To set a Quick Trigger in the Source window (see page 154)

#### To set a Quick Trigger in the Waveform window

In the Waveform window, you can quickly set up a simple trigger by drawing a rectangle with the mouse.

- 1 Make sure the Waveform window's Fast Zoom In (see page 252) option is not selected.
- **2** Using the mouse, point to the upper-left corner of your desired trigger rectangle.
- **3** While holding down the mouse button, drag the mouse pointer to the lower-right corner of your desired rectangle, then release the mouse button.

As you draw the rectangle, you can monitor the trigger as it is set with the tool tip readout that appears.



As you move the mouse left-to-right and top-to-bottom, the signal edge/level or bus value in contact with the **left of the rectangle** becomes the trigger.

Only one edge can be set.

If a bus is expanded into its separate signals, three conditions apply:

- **a** If drawing starts on a bus, none of its expanded signals can be included.
- **b** If drawing starts on a signal, the bus cannot be included.
- **c** Edges and levels are mutually exclusive. That is, either one edge can be set, or all levels can be set, but not both at the same time.

#### NOTE

In the Waveform display window, it may be necessary to redraw the rectangle if you do not get your desired trigger points dictated by the left-side line of the rectangle. You could also try drawing the rectangle backwards leaving the left-side rectangle line set last.

#### 4 Select Set Quick Trigger.



**General** • Any bus/signals with overlapping bits are not included within the trigger specification.

**Example:** Bus\_1 has channels 0 through 7 of pod 1 assigned and Bus\_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus\_1 and Bus\_2. Now you draw the rectangle over both bus\_1 and bus\_2. Since Bus\_1 channels 3 through 6 are repeated (overlapped) on Bus\_2, they will not be included in the trigger specification.

- Only a single sequence step can be defined by a drawn rectangle.
- As you draw the rectangle, a tool tip is displayed showing the current trigger specification that would be set.

#### To set a Quick Trigger in the Listing window

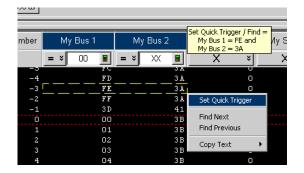
In the Listing window, you can quickly set up a simple trigger by drawing a rectangle with the mouse.

- 1 Using the mouse, point to the sample that you want to use as the quick trigger.
- 2 While holding down the mouse button, drag the mouse pointer horizontally to draw a rectangle around the buses/signals you want to include in the trigger; then, release the mouse button.

As you draw the rectangle, a tool tip shows the trigger that will be set.

Dragging the mouse pointer vertically does not affect the sample used for the quick trigger; the sample used is always the one from which the drawn rectangle originates.

3 Select Set Quick Trigger.



## **General** • Any bus/signals with overlapping bits are not included within the trigger specification.

**Example:** Bus\_1 has channels 0 through 7 of pod 1 assigned and Bus\_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus\_1 and Bus\_2. Now you draw the rectangle over both bus\_1 and bus\_2. Since Bus\_1 channels 3 through 6 are repeated (overlapped) on Bus\_2, they will not be included in the trigger specification.

- Only a single sequence step can be defined by a drawn rectangle.
- As you draw the rectangle, a tool tip is displayed showing the current trigger specification that would be set.

#### To set a Quick Trigger in the Source window

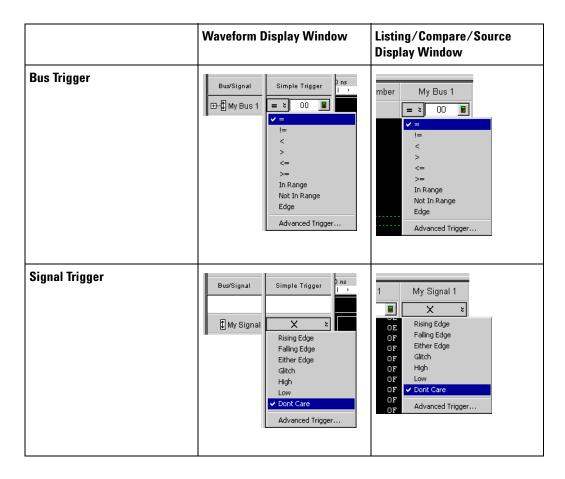
1 In the Source window's source pane, right-click the source line you want to set a Quick Trigger on, and choose **Set Quick Trigger**.

| Displa            | yed File C:\My Documents\source\ecs2.c          | Browse   | ⇒{ <b>↑</b> { <b>↓</b> { | 1 <sub>64</sub> 5 <sub>64</sub> |
|-------------------|---|--|--------------------------|---------------------------------|
| 145<br>146<br>147 | <pre>proc_spec_init(); for (;;)</pre>           |  |                          | <u>^</u>                        |
| 148               | (   |  |                          |                                 |
| 149<br>150        | update system(num checks);<br>num checks++;     | Set Quick Trigger  |                          |                                 |
| 151<br>152        | update_display(num_checks);<br>proc specific(); | Find in Source<br>Find Next Selected Source Line<br>Find Prey Selected Source Line |                          | •<br>  •                        |
|                   |   | Symbols  |                          |                                 |
|                   |   | Properties   |                          |                                 |

- **See Also** To change the "Set Quick Trigger" alignment (see page 315)
  - Running/Stopping Measurements (see page 203)
  - Viewing Source Code Associated with Captured Data (see page 308)

#### **Specifying Simple Triggers**

Simple triggers let you quickly set up triggers on edges and bus/signal patterns from within display windows.

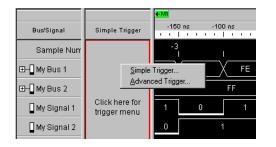


Buses are compared to entered pattern values using a relational operator (=, !=, <, >, <=, >=, In Range, Not In Range) or to one of multiple edges.

Signals are compared to edges (**Rising Edge**, **Falling Edge**, **Either Edge**, or a logic level pattern (**High**, **Low**). Edge options are available in timing mode only. For 16850 series and U4154A Logic Analyzer modules, edge options are also available in the state mode.

You can specify multiple bus/signal pattern values and one edge, all of which must evaluate to true for a sample to trigger the logic analyzer. (If you try to specify multiple edges, the last edge specified has priority, and the previously specified edge is changed to don't care.) When buses/signals overlap (that is, the same logic analyzer channels are assigned to multiple buses/signals), the last change has highest priority. For example, if you specify a pattern on Bus A and then specify a rising edge on Signal B, which is bit 0 on Bus A, the previously specified pattern is erased.

When the desired trigger condition requires more than a simple AND expression (for example, one pattern OR another pattern on a bus, patterns in a sequence of samples, testing timer or counter values, etc.), you can choose **Advanced Trigger...** to specify an advanced trigger (see page 163). When an advanced trigger surpasses the functional limits of a simple trigger, the simple trigger fields go away; to restore them, you must either change the advanced trigger so that it doesn't surpass the limits of a simple trigger, or click **Click here for trigger menu** and choose **Simple Trigger...** to reset the trigger.



- To specify bus patterns in a simple trigger (see page 157)
- To specify signal levels in a simple trigger (see page 158)
- To set a bus/signal edge in a simple trigger (see page 159)
- **See Also** Setting Up Quick Triggers (see page 152)
  - Specifying Advanced Triggers (see page 163)
  - To store a trigger (see page 201)
  - To recall a trigger (see page 527)

#### To specify bus patterns in a simple trigger

When specifying simple triggers (see page 156), you can specify bus patterns to trigger on.

|             | Waveform Display Window   | Listing/Compare/Source<br>Display Window   |  |
|-------------|---|--|--|
| Bus Trigger | Bus/Signal       Simple Trigger       Ins         Im-Im My Bus 1       Image       Image         Im-Im My Bus 1       Image       Image         Image       Image       Image         Image | mber My Bus 1<br>= z 00 II<br>!=<br><<br>><br>In Range<br>Not In Range<br>Edge<br>Advanced Trigger |  |

To specify a bus<br/>pattern1In the Simple Trigger field for a bus, click theImage: specify a bus<br/>operator button;then, choose from one of the following operators:

- = (Equal To)
- != (Not Equal To)
- < (Less Than)</li>
- > (Greater Than)
- <= (Less Than Or Equal To)
- >= (Greater Than Or Equal To)
- In Range
- Not In Range

# **NOTE** The <, >, <=, >=, **In Range**, and **Not In Range** operators are not available when a bus with reordered bits has been selected. Also, these operators cannot be used when the selected bus contains clock bits that span pod pairs. The **In Range** and **Not In Range** operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

2 In the text entry field  $\square \times \square$ , enter the bus pattern value to compare.

#### To specify signal levels in a simple trigger

When specifying simple triggers (see page 156), you can specify signal levels to trigger on.

|                | Waveform Display Window   | Listing/Compare/Source<br>Display Window   |
|----------------|---|--|
| Signal Trigger | Bus/Signal       Simple Trigger       Instruction         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigger         Image: Simple Trigger       Image: Simple Trigger       Image: Simple Trigg | 1     My Signal 1       ■     ×       0F     Rising Edge       0F     Falling Edge       0F     Either Edge       0F     Either Edge       0F     High       0F     Low       0F     Dont Care       0F     Advanced Trigger |

- To specify a<br/>signal level1In the Simple Trigger field for a signal, click theX\*edge/levelbutton; then, choose from:
  - High
  - Low
  - **See Also** To specify bus patterns in a simple trigger (see page 157)

#### To set a bus/signal edge in a simple trigger

You can set a trigger on Rising, Falling, or Either Edge when the logic analyzer is configured in the Timing - Asynchronous sampling mode.

NOTE For 16850-series and U4154A logic analyzer modules, you can set a trigger on edge in the Timing - Asynchronous sampling mode as well as State –Synchronous sampling mode.

Trigger on edge options are available in a simple trigger, an advanced trigger, and an eyescan trigger.

**NOTE** The trigger event occurs between the previous state clock and the state clock at which the trigger point is marked.

If there is a rising edge and a falling edge on the same signal between the previous state clock and the state clock at which the trigger point is marked, such that the actual state of the signal is the same at both the previous state clock and the state clock at which the trigger point is marked, then the trigger will not occur.

You can configure trigger on edge in a simple trigger from the Waveform or Listing display window. The trigger settings that you configure in one of these windows is reflected automatically in the other window.

From WaveformFor a simple trigger created from Waveform Viewer, you can set a triggerVieweron edge at an individual bit/signal level or at bus level.

At the bus level, you can set trigger on edge on one or more signals within the bus. If you set trigger on edge on multiple signals within a bus, then trigger on edge for these signals is ORed.

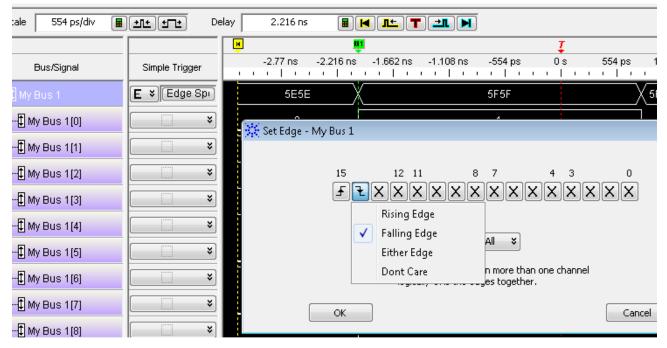


Figure - Trigger on edge set from Waveform viewer for a bus

At the individual signal level, you can set trigger on edge for one signal at a time. If you try to specify multiple edges, the last edge specified has priority, and the previously specified edge is changed to "Don't Care".

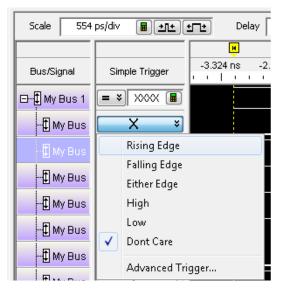


Figure - Trigger on edge set from Waveform viewer for a signal

**From Listing** For a simple trigger created from Listing Viewer, you can set a trigger on edge on one or more signals within a single bus. For multiple signals, trigger on edge is ORed.

|               | Sample Number | 1   | My Bus 1      | My Bus 2 | My Bus 3     |
|---------------|---------------|-----|---------------|----------|--------------|
|               |               | = * | 🔳             | = * 🕅    | = * 🗶        |
|               |               | ✓   | =             |          |              |
|               |               |     | !=            |          |              |
|               |               |     | <             |          |              |
|               |               |     | >             |          |              |
|               |               |     | <=            |          |              |
|               |               |     | >=            |          |              |
|               |               |     | In Range      |          |              |
| ≖→            | -8            |     | Not In Range  |          | 5E5E         |
|               | -7            |     | Edge          |          | SESE         |
|               | -6<br>-5      |     |               |          | 5E5F<br>5F5F |
| <u>, 11</u> + | -5            |     | Advanced Trig | 3ger     | 5F5F         |

Figure - Trigger on edge set from Listing viewer for a bus

To specify edges<br/>on a bus1In the Simple Trigger field for a bus, click the ■operator button;then, choose Edge.

2 Click Edge Spec....

E ¥ Edge Spec...

3 In the Set Edge dialog, specify edges you are looking for; use the **Set All** button to make a selection for all signals in the bus.

| Set Edge/Glitch - My Bus 1 |  | ×      |
|----------------------------|--|--------|
|                            | 7 4 3 0<br>1 1 1 1 1 1 1 1   |        |
|                            | Set All  |        |
|                            | pecifying an edge or glitch on more than one namel logically ORs the edges together. |        |
| []                         |  | Cancel |

4 Click OK to close the Set Edge dialog.

#### To specify a

signal edge 1 In the Simple Trigger field for a signal, click the <u>×</u> edge/level button; then, choose from:

- Rising Edge
- Falling Edge
- Either Edge

#### **See Also** • To specify signal levels in a simple trigger (see page 158)

• Understanding Logic Analyzer Triggering, Edges (see page 431)

#### **Specifying Advanced Triggers**

When you need to set up triggers that are more complex than just finding particular bus/signal values (for example, when you need to trigger on a sequence of events in the device under test), you set up advanced triggers.

To open the Advanced Trigger dialog, click in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.

| ta an    | lvanced Trigger               |                                       |                           |    |            |      |
|----------|-------------------------------|---------------------------------------|---------------------------|----|------------|------|
| т        | rigger Functions              | Trigger Sequence                      |                           |    |            |      |
| Patterns | Pattern n<br>times            | Default Storage (overridden by sequer | nce level store actions): |    |            |      |
| other    |                               | Step 1 ¥ Pattern n times              |                           |    |            |      |
| ŝ        |                               | Find 1 📕 - +                          | occurrence of             |    |            |      |
| l ee     | N consecutive<br>samples with | 🗧 📕 Bus/Signal 💌 My                   | Bus 1 🛛 🛛 🗙 🖌 All bits 💌  | -  | XX 🖩 Hex 🛛 | ]    |
| Advanced | Pattern1                      | Then 🗧 Trigger and fill memo          | ry                        |    |            |      |
|          |                               | × with × Default St                   | orage 💌                   |    |            |      |
|          | Pattern1 💌                    |                                       |                           |    |            |      |
|          |                               | Simple Trigger Store                  | Recall Clear              | ОК | Cancel     | Help |

Advanced triggers are specified by dragging-and-dropping predefined *trigger functions (see page 560)* into trigger sequence steps. If the trigger function you need doesn't exist, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

Each step in the trigger sequence looks for *events (see page 165)* in data samples captured from the device under test (or in logic analyzer timers, counters, or flags), and when those events are found, takes some *action (see page 165)* (like triggering or going to another step in the sequence). You can also insert actions for timers, counters, or flags.

*Default storage* lets you ignore the question, in individual trigger sequence steps, of which captured samples should be stored in logic analyzer memory. However, you can insert *storage control* actions in individual trigger sequence steps to specify whether samples should be stored or to specify whether default storage should be turned on or off. Sequence step storage control actions override the default storage specification.

- To replace or insert trigger functions into trigger sequence steps (see page 169)
- To specify bus/signal patterns (see page 169)
- To set a bus/signal edge in an advanced trigger (see page 171)

- To specify packet events (in "Find a packet" trigger function) (see page 175)
- To specify a trigger sequence step's goto or trigger action (see page 178)
- To specify default storage (see page 179)
- To insert or delete events (see page 180)
  - To insert a timer event (see page 181) (see also Using Timers (see page 165))
  - To insert a counter event (see page 181) (see also Using Counters (see page 166))
  - To insert a flag event (see page 182) (see also Using Flags (see page 167))
  - To insert an "Arm in from" event (see page 182)
- To negate events (see page 183)
- To change the evaluation order of AND/OR'ed events (see page 184)
- To choose between a duration or occurrence count for events (timing mode) (see page 184)
- To insert or delete actions (in a trigger sequence step) (see page 185)
  - To insert a timer action (see page 185) (see also Using Timers (see page 165))
  - To insert a counter action (see page 186) (see also Using Counters (see page 166))
  - To insert a reset occurrence counter action (see page 186)
  - To insert a flag action (see page 187) (see also Using Flags (see page 167))
  - To insert a storage control action (see page 188)
- To cut, copy, and paste trigger sequence steps (see page 188)
- To delete trigger sequence steps (see page 189)
- To show a trigger sequence step as Advanced If/Then trigger functions (see page 189)
- To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)
- To display or hide "If" clause comments (see page 190)
- To clear the trigger sequence (see page 192)
- **See Also** Specifying Advanced Triggers in the 16960 Logic Analyzer (see page 660)
  - Understanding Logic Analyzer Triggering (see page 431)
  - State Mode Trigger Functions (see page 573)
  - Timing Mode Trigger Functions (see page 560)

• Specifying Simple Triggers (see page 156)

#### **Reading Event and Action Statements**

Event and action statements in trigger sequence steps read from left-to-right like:

Find an event in the device under test; when the event is found, take some action.

Or:

If an event is found in the device under test; then, take an action.

For example, suppose you want to see what happens after a read from the address 406F6H. To do this, set up the trigger to look for a rising edge on the RD (memory read) signal and an address bus pattern of 406F6H (hexadecimal):

| Step 1 × Edge and Pattern      |   |
|--------------------------------|---|
| Find 🛛 Bus/Signal 💌 RD         | × Rising Edge   |
| And 🔀 Bus/Signal 💌 ADDR        | ▼         All bits         ▼         4 06F6         Hex ¥ |
| Then 🗙 Trigger and fill memory | <b>_</b>  |

As you set up the trigger, think of it as constructing a sentence that reads left-to-right. For example:

Find a Signal named RD with a Rising Edge And a Bus named ADDR with All bits= (equal) to the pattern 406F6 Hex. When found, then Trigger and fill memory.

- **See Also** Specifying Advanced Triggers (see page 163)
  - Understanding Logic Analyzer Triggering, Sequence Steps (see page 433)

#### **Using Timers**

Timers are like stopwatches. Use timers to create either a user-defined delay or a time standard which valid data duration is evaluated against. The timer can **Start** from reset, **Stop** and reset, **Pause**, or **Resume**.

Timer considerations:

- It takes a certain amount of time for timers to reset; this is called the *timer reset latency*. To find the timer reset latency for your logic analyzer, see the description of its characteristics (see page 714).
- The number of timers available in a module depends on the selected acquisition mode and sampling option:

#### **6** Capturing Data from the Device Under Test

| Acquisition Mode                    | Sampling Option    | # Timers Available                               |
|-------------------------------------|--------------------|--|
| State mode (synchronous sampling)   | General State Mode | # pod pairs not reserved for<br>time tag storage |
|                                     | Turbo State Mode   | 0  |
| Timing mode (asynchronous sampling) | all                | # pod pairs not reserved for<br>time tag storage |

Refer to your logic analyzer characteristics (see page 714) for the actual number of timers available. For information on when pod pairs are reserved for time tag storage, see Why Are Pods Missing? (see page 419).

- Timers are checked in event statements, and started in action statements.
- Timers must be started before they can be checked. This is done by either including the timer start action with the timer check event within the same trigger step or starting the timer in a preceding trigger step.

The following example shows the timer start action and check event within the same trigger step.

|                  | Step 1 × User defined                                 |
|------------------|---|
| Timer<br>Checked | Find 🛛 Timer  |
| Спескеа          | 🛎 Bus/Signal 🔹 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌 |
| Timer            | Then 🗵 Timer 🔽 1 🔽 Start from reset 💌                 |
| Started          | Soto Next V   |

- Once a timer event is configured, you can reuse the timer by selecting its identification number. The same timer must always be checked against the same value. To check for different durations, use different timers.
- **See Also** To insert a timer action (see page 185)
  - To insert a timer event (see page 181)
  - Understanding Logic Analyzer Triggering, Timers (see page 438)

#### **Using Counters**

Counters are available in both Event and Action statements, and like other events, they evaluate to either true or false. Use counters to create a user-defined delay, or to create a standard against which valid data duration is evaluated. Once configured, a counter persists throughout all the steps of the trigger sequence. Counter considerations:

- Maximum counters available is 2.
- When using counters in the transitional timing mode, one counter is used internally so only one counter is available in a sequence step.
- Once a counter is configured, you can reuse the counter by selecting its identification number. Each use of the counter must check it for the same value.

# **NOTE** The logic analyzer also has occurrence counters, and a **reset occurrence counter** action. Occurrence counters only exist within steps that contain the "occurs" phrase and are not affected by the other counter actions described on this page.

- **See Also** To insert a counter action (see page 186)
  - To insert a counter event (see page 181)
  - Understanding Logic Analyzer Triggering, Counters (see page 437)

#### **Using Flags**

Flags can be used to signal between modules in the logic analysis system including a multiframe logic analysis system as well as between modules installed in an Agilent AMP/AXIe chassis. Using flags, logic analyzer modules can communicate back and forth with each other multiple times during a data acquisition, both before and after their trigger events occur. (By comparison, a module can arm another module one time when its trigger occurs.)

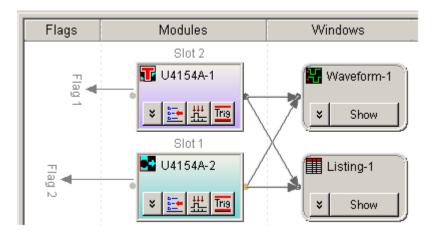
#### NOTE

Flags are not available in 1680/1690-series logic analyzers.

There are 4 flags that are shared across all connected logic analysis/AMP/AXIe system frames. By default, flags are cleared. In the Advanced Trigger dialog of the module, you can insert actions to set, clear, pulse set, or pulse clear a flag. You can also insert flag events in the Advanced Trigger dialog of different modules to test whether a particular flag is set or clear.

#### Setting a Flag

In legacy logic analysis systems, a particular flag may be driven (set) or received by multiple modules. However, in newer AMP/AXIe based instrument modules, only one module can set a particular flag. Multiple modules cannot set the same flag. But multiple modules can insert flag events for the same flag to test whether the flag is set or clear.



#### **Clearing a Flag**

A flag that is set by a module remains set until that module clears it. In legacy logic analysis systems, if multiple modules set the same flag, then all those modules must clear the flag before it becomes clear. In newer AMP/AXIe based instrument modules, multiple modules cannot set the same flag and therefore, the module that sets the flag can only clear it.

Flag actions are not available in *Turbo State Mode*; however, you can still check flags with flag events.

Flags can also be used to drive the logic analysis system's Port Out signal.

See Also

NOTE

- To insert a flag action (see page 187)
- To insert a flag event (see page 182)
- Understanding Logic Analyzer Triggering, Flags (see page 437)

#### To replace or insert trigger functions into trigger sequence steps

Multiple steps in the trigger sequence are necessary when you want to trigger on a sequence of events in the device under test. When you want to trigger on one event in (that is, a single sample from) the device under test, a single step in the trigger sequence is all you need.

1 In the Advanced Trigger dialog, **drag- and- drop** the desired Trigger Function (see page 560) into the Trigger Sequence display area.

| Trigger F                | Functions   | Trigger Sequence  |
|--------------------------|---|---|
|                          | attern n<br>times   | Drag and Drop   |
| eed Other bed Other Ball | attern n times<br>lelease mouse<br>utton to replace<br>tep 1 with new<br>function | Step 1 *       Pattern n times         Find       1       -+         occurrence of       *         Bus/Signal       •       My Bus 1         Then       *       Trigger and fill memory         *       with       *         Bus/Signal       •       My Bus 1         *       With       *         *       With       *         *       With       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       *         *       *       * |

To replace an existing step:

• Drag-and-drop the trigger function on top of an existing step in the trigger sequence. A red box around the old function indicates the replace operation.

To insert a trigger function as a new step:

- Drag-and-drop the trigger function above or below an existing step in the trigger sequence. When the mouse is positioned above or below an existing step, a red insert bar appears to indicate the relative insert location of the trigger function.
- See Also Understanding Logic Analyzer Triggering, Sequence Steps (see page 433)
  - To delete trigger sequence steps (see page 189)
  - State Mode Trigger Functions (see page 573)
  - Timing Mode Trigger Functions (see page 560)

#### To specify bus/signal patterns

1 In the Advanced Trigger dialog, select the bus or signal.

| My Bus 1 🛛 🛛 🕷 | All bits 💌 = | 🔻 🛛 XX 📓 Hex 🔾 |
|----------------|--------------|----------------|
|----------------|--------------|----------------|

Clicking lets you select from recently used bus/signal names. Clicking elsewhere on a bus/signal name button opens a Select dialog for selecting a different name. 2 If a bus has been selected, either select **All bits** on the bus or select an individual bit.

| My Bus 1 🛛 🕹 🛠 | All bits 🔻 = 💌 00 🖩 Hex 🐳 |
|----------------|---------------------------|
|                | All bits<br>Bit O         |
|                | Bit 1<br>Bit 2            |
|                | Bit 3<br>Bit 4            |
|                | Bit 5                     |
|                | Bit 7                     |

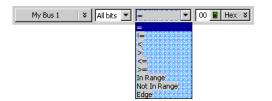
**3** Specify the bus/signal value:

If a signal or one bit of a bus has been selected, select the signal pattern value (**High**, **Low**, or **Dont Care**).

| My Bus 1[0] | ¥ Bit 0 | • | Dont Care 💌                 |
|-------------|---------|---|-----------------------------|
|             |         |   | Rising Edge<br>Falling Edge |
|             |         |   | Either Edge<br>Glitch       |
|             |         |   | High<br>Low                 |
|             |         |   | Dont Care                   |

If all bits of a bus have been selected:

a Select one of the operators: = (equal to), != (not equal to), < (less than), > (greater than), <= (less than or equal to), >= (greater than or equal to), In Range, Not In Range, or Edge.



#### NOTE

The <, >, <=, >=, **In Range**, and **Not In Range** operators are not available when a bus with reordered bits has been selected. Also, these operators cannot be used when the selected bus contains clock bits that span pod pairs. The **In Range** and **Not In Range** operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

b Select the number base (Binary, Hex, Octal, Decimal,
 Signed Decimal, also known as two's complement, Ascii, or Symbol).

| My Bus 1 🛛 😽 All E | its 💌 😑 | ▼ <u>00</u> ■ H | lex 2          |
|--------------------|---------|-----------------|----------------|
|                    |         |                 | Binary         |
|                    |         |                 | • Hex          |
|                    |         |                 | Octal          |
|                    |         |                 | Decimal        |
|                    |         |                 | Signed Decimal |
|                    |         |                 | Ascii          |
|                    |         |                 | Symbol         |

**c** Enter the pattern value(s).

When the **Symbol** number base is selected, you use the Select Symbol dialog (see page 530) to specify the pattern values.

- **See Also** To specify default storage (see page 179)
  - To insert or delete events (see page 180)
  - Understanding Logic Analyzer Triggering, Ranges (see page 437)

#### To set a bus/signal edge in an advanced trigger

You can set a trigger on Rising, Falling, or Either Edge when the logic analyzer is configured in the Timing - Asynchronous sampling mode.

NOTE

For 16850-series and U4154A logic analyzer modules, you can set a trigger on edge in the Timing - Asynchronous sampling mode as well as State –Synchronous sampling mode.

Trigger on edge options are available in a simple trigger, an advanced trigger, and an eyescan trigger.

#### NOTE

The trigger event occurs between the previous state clock and the state clock at which the trigger point is marked.

If there is a rising edge and a falling edge on the same signal between the previous state clock and the state clock at which the trigger point is marked, such that the actual state of the signal is the same at both the previous state clock and the state clock at which the trigger point is marked, then the trigger will not occur.

In an advanced trigger step, you can set a trigger on edge on an individual bit/signal or multiple signals of a bus (edges are ORed in this case). The following screen displays an example of the Edge options available in an advanced trigger in timing mode.

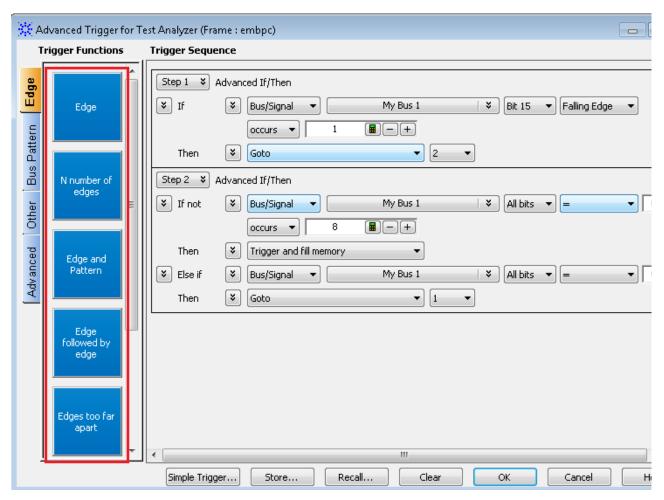


Figure - Trigger on edge options for the timing mode

To specify trigger on edge on a signal in an advanced trigger 1 In the Advanced Trigger dialog, select the bus and then its signal on which you want to set trigger on edge.

| Step 2 💙 Edge       |          |         |               |
|---------------------|----------|---------|---------------|
| Find 😻 Bus/Signal 🔻 | My Bus 1 | Bit 1 🔻 | Dont Care 🛛 🔻 |
| Then<br>Goto        | ▼ Next ▼ |         | •             |

2 Select the edge value (**Rising Edge**, **Falling Edge**, or **Either Edge**) for the signal.

| Step 2 🛛 Edge       |          |         |                |
|---------------------|----------|---------|----------------|
| Find 🛛 Bus/Signal 🔻 | My Bus 1 | Bit 1 🔻 | Falling Edge 🔻 |
| Then 💙 Goto         | ▼ Next ▼ |         |                |

To specify 1 bus/signal edges in advanced trigger

**1** In the Advanced Trigger dialog, select the bus on which you want to set trigger on edge.

| Step 2 ¥ Edge       |          |         |             |
|---------------------|----------|---------|-------------|
| Find 🛛 Bus/Signal 🔻 | My Bus 1 | Bit 0 🔻 | Dont Care 🔹 |
| Then 💙 Goto         | ▼ Next ▼ | -       |             |

2 Select the All bits option for the bus.

| Step 2 ¥ Edge        |          |                |             |
|----------------------|----------|----------------|-------------|
| Find<br>Bus/Signal 🔻 | My Bus 1 | Bit 0 🔫        | Dont Care 🔻 |
| Then 😽 Goto          | ▼ Next ▼ | All bits       |             |
|                      | NEXT -   | Bit 0<br>Bit 1 |             |
|                      |          | Bit 2          |             |
|                      |          | Bit 3          |             |
|                      |          | Bit 4          |             |
|                      |          | Bit 5          |             |
|                      |          | Bit 6<br>Bit 7 |             |
|                      |          | DIL /          |             |

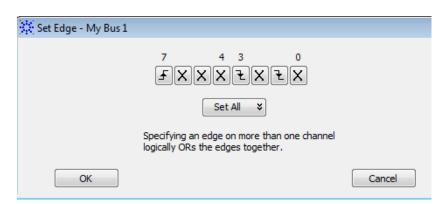
**3** Select the **Edge** option.

| Step 2 🔾 User defined                   |                          |        |
|---|--------------------------|--------|
| Find 🔾 Bus/Signal 🔻 My Bus 1 All bits 🔻 | = •                      | 00 🔳 🛛 |
| Then 🕏 Goto 🔹 Next 💌                    | =<br>!=                  |        |
|   | <<br>>                   |        |
|   | <=<br>>=                 |        |
|   | In Range<br>Not In Range |        |
|   | Edge                     |        |

When the Edge operator is selected, the Edge Spec... button is displayed.

| Step 2 🛛 Edge       |          |            |        |           |
|---------------------|----------|------------|--------|-----------|
| Find 🛛 Bus/Signal 🔻 | My Bus 1 | All bits 🔻 | Edge 🔻 | Edge Spec |
| Then 💙 Goto         | ▼ Next ▼ |            |        |           |

4 Click the **Edge Spec...** button to open the **Set Edge** dialog for specifying multiple edges on a bus. In the Set Edge dialog, specify edges you are looking for; use the **Set All** button to make a selection for all signals in the bus.



5 Click **OK** to close the Set Edge dialog.

Trigger on edge in<br/>an eyescan<br/>triggerYou can also set a trigger on edge when configuring an eyescan trigger.<br/>This trigger allows you to control when logic analyzer should take samples<br/>to be used in the eyescan for determining the optimal threshold and<br/>sample positions.

To know more about eyescan triggers and how to configure these, refer to the topic Modifying General or Target-specific Scan Qualification.

| Trigger Functions  | Trigger Sequence   |  |
|--|--|--|
| Patterns   | Default Storage<br>Overridden by store actions in individual trigger steps:<br>Store Anything        |  |
| Adv anced Other Edges<br>Edge and<br>Edge and<br>Battern | Step 1 * Edge       Find * Bus/Signal • My Bus 3 * Bit 2 • Falling Edge •       Then * Goto • Next • |  |
| Edge and<br>Pattern                                      |  |  |
|  | Store Recall Clear OK Cancel Help  |  |

Figure - Trigger on edge in an eyescan trigger

See Also

- To specify default storage (see page 179)
- To insert or delete events (see page 180)
- Understanding Logic Analyzer Triggering, Edges (see page 436)

#### To specify packet events (in "Find a packet" trigger function)

- 1 In the Advanced Trigger dialog, replace or insert the Find a packet (see page 580) trigger function into the trigger sequence (see To replace or insert trigger functions into trigger sequence steps (see page 169)).
- 2 In the "Find a packet" trigger sequence step, click Select a bus.
- **3** In the Choose a Protocol Family and Bus dialog (see page 502), select the protocol family and the type of bus being probed; then, click **OK**.
- 4 In the "Find a packet" trigger sequence step, click Select a packet.
- **5** In the Event Editor Dialog (see page 505), select the type of packet event and enter packet field values to trigger on; then, click **OK**.

#### **See Also** • Using the Packet Event Editor (see page 175)

#### **Using the Packet Event Editor**

The packet event editor lets you specify packet events in the "Find a packet" trigger function.

| 🔆 Event Editor   |             |                                      |   |                  |
|--|-------------|--------------------------------------|---|------------------|
| Events   | Name        | 4DW Msg - Ro                         | uted by ID                                | Add to Favorites |
| <ul> <li>□ PCI Express</li> <li>□ Favorites</li> <li>□ Ordered Sets</li> <li>□ Packets</li> </ul>  |             | <b>kpress : Physical</b><br>Symbol   | STP                                       |                  |
| Any Packet     DLLP Packets  | PCIE        | xpress : Data Link                   |   | =====            |
| TLP Packets     Any TLP Packet   | Reser       | ved                                  | X Hex X                                   |                  |
| Gradient Stresservice     Gradient Str |             | ence Number                          | XXX 🔳 Hex 🕉 🔀                             |                  |
| 4DW Memory Read Request<br>4DW Memory Request-Locked<br>4DW Msg - Routed to Root Cor   | PCI E       | <pre>kpress : Transaction ved1</pre> | X 📕 Bin 🔻 🔀                               |                  |
| - 4DW Msg - Routed by Address<br>4DW Msg - Routed by ID  | Fmt<br>Type |                                      | 4DW header, no data<br>Msg - Routed by ID |                  |
| 4DW Msg - Broadcast from Roc<br>4DW Msg - Local - Terminate al<br>   | Reser       | ved2                                 |   |                  |
|  | тс          |                                      | Don't Care VX                             | ~                |
| Organize Favorites   | < l         | 10<br>                               |   | >                |
|  | Cle         | ear View as Bits                     | OK Cancel                                 | Help             |

To use the packet event editor:

- 1 Select the event type from the left side of the dialog.
- 2 Enter or select field values on the right side of the dialog.

To clear a field value, click  $\boxtimes$ .

- 3 If desired, you can enter or modify the Name of the event.
- 4 When you are done editing the packet event, click **OK**.

The packet event editor also allows you:

- To view a packet event as bits (see page 176)
- To save favorite packet events (see page 176)
- To organize favorite packet events (see page 177)
- **See Also** Find a packet (see page 580) trigger function
  - **To view a packet event as bits** 1While specifying packet events using the Event Editor Dialog (see page 505), click **View as Bits...**

The packet event is displayed in format similar to packet descriptions in specification documents.

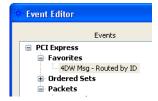
| 🔆 View as Bits [4DW Msg - Routed by ID] |         |                    |   |    |       |      |      | ×         |    |    |      |      |              |     |        |   |     |                 |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
|---|---------|--------------------|---|----|-------|------|------|-----------|----|----|------|------|--------------|-----|--------|---|-----|-----------------|---|---|------|---|---|---|---|---|---|------|------|-------|------|------|-----|----|
| Base: Binary                            |         |                    |   |    |       |      |      |           |    |    |      |      |              |     |        |   |     |                 |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
|   | +0      |                    |   |    | +1    |      |      |           |    | +2 |      |      |              | +3  |        |   |     |                 | _ |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
|   |         | 7                  | 6 | 5  |       | 3    |      | 1         | 0  | 7  | 6    | 5    | 4            | 3   | 2      | 1 | 0   | 7               | 6 | 5 | 4    | 3 | 2 | 1 | 0 | 7 | 6 |      | 4    | 3     | 2    | 1    | 0   |    |
| Byte C                                  | ı I     |                    |   | St | art S | 6 yn | nbol |           |    | F  | lese | erve | d            |     |        |   |     |                 |   |   | lum  |   |   |   |   | R | F | mt   |      | 1     | Гуре | з    |     |    |
| byte e                                  | ,       | 1                  | 1 | 1  | 1     | 1    | 0    | 1         | 1  |    | Х    |      |              |     |        | Х | Х   | Х               |   |   |      |   | Х | Х | X | Х |   |      | 1    | 0     | 0    | 1    | 0   |    |
| Byte 4                                  | L       | R                  |   | TC |       | F    |      | erve      |    |    | ΕP   |      |              |     | R      |   |     |                 |   |   | ngth |   |   |   |   |   |   | Nun  |      | (R)   | equ  | esti | er) |    |
| - J.C.                                  |         | Х                  |   | X  |       | X    |      | X         |    | Х  | Х    | Х    |              |     | Х      | Х | Х   | Х               |   |   |      |   |   |   | X | 0 |   | 0    |      |       | 0    |      | 0   |    |
| Byte 8                                  | 1       | Dev # (Req) F# (R) |   |    |       |      |      |           | ag |    |      |      | Message Code |     |        |   |     | Reserved[63:56] |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
| 5,000                                   | Dyte o  | 0                  | 0 | 0  | 0     | 0    | 0    | 0         | 0  | 0  | 0    | 0    | 0            | 0   |        | 0 | 1   | 0               |   | 1 | 1    | 0 | 0 | 0 | 1 | Х | Х | Х    | Х    | Х     | Х    | Х    | Х   |    |
| Byte 12 Reserved[55:24]                 |         |                    |   |    |       |      |      |           |    |    |      |      |              |     |        |   |     |                 |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
| ,                                       | byte 12 | Х                  | Х | Х  | X     | X    | X    | X         | Х  | Х  |      |      |              |     |        |   | Х   | Х               | Х | X | Х    | Х | Х | Х | X | Х | X | X    | Х    | Х     | Х    | Х    | Х   |    |
| Byte 1                                  | 6       |                    |   |    |       |      |      |           |    |    |      |      |              |     | 23:0   |   |     |                 |   |   |      |   |   |   |   |   |   | LP I | Dige | est[( | 31:2 | 24]  |     |    |
| Dyter                                   | 0       | Х                  | Х | Х  | X     | X    | X    | X         | Х  | Х  |      |      |              |     |        |   | Х   | Х               | Х | Х | X    | Х | Х | Х | X | Х | X |      |      |       |      |      | Х   |    |
| TLP Digest[23:0] L(                     |         |                    |   |    |       |      |      | RC[31:24] |    |    |      |      |              |     |        |   |     |                 |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
| Dyle 2                                  | .0      | Х                  | Х | Х  | X     | X    | X    | X         | Х  | Х  | Х    |      |              |     |        | Х | Х   | Х               | Х | Х | Х    | Х | Х | Х | X | Х | Х |      | Х    | Х     | Х    | Х    | Х   |    |
| Byte 2                                  | м       |                    |   |    |       |      |      |           |    |    |      | LC   | RC           | [23 | 8:0]   |   |     |                 |   |   |      |   |   |   |   |   |   | Er   | nd S | ym    | bol  |      |     |    |
| Dyle 2                                  |         | Х                  | Х | Х  | X     | X    | X    | X         | Х  | Х  | Х    | Х    | Х            | Х   | Х      | Х | Х   | Х               | Х | Х | Х    | Х | Х | Х | X | Х | Х | X    | Х    | Х     | Х    | Х    | Х   |    |
|   |         |                    |   |    |       |      |      |           |    |    |      |      |              |     |        |   |     |                 |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
|   |         |                    |   |    |       |      |      |           |    |    |      |      |              |     | (***** |   |     |                 | - |   |      |   |   |   |   |   |   |      |      |       |      |      |     |    |
|   |         |                    |   |    |       |      |      |           |    |    |      |      |              |     | L      | C | ose | ;               |   |   |      |   |   |   |   |   |   |      |      |       |      |      |     | .: |

- 2 If desired, you can select a different number Base.
- 3 When you are finished viewing the packet event as bits, click Close.
- See Also
- To specify packet events (in "Find a packet" trigger function) (see page 175)

**To save favorite packet events** While specifying packet events using the Event Editor Dialog (see page 505), you can save the event as a favorite.

- 1 If desired, enter or modify the Name of the event.
- 2 Click Add to Favorites.

The packet event appears in the event list tree on the left side of the dialog.



- **See Also** To organize favorite packet events (see page 177)
  - To specify packet events (in "Find a packet" trigger function) (see page 175)

**To organize favorite packet events** While specifying packet events using the Event Editor Dialog (see page 505), you can organize saved packet event favorites.

- 1 Click Organize Favorites....
- 2 In the Organize Favorites dialog, you can:

| * Orangize Favorites [PCI Express]  |                        |  |  |  |  |  |  |
|---|------------------------|--|--|--|--|--|--|
| To create a new folder, click on the Create<br>Folder buttton. To rename or delete an<br>item, select the item and click Rename or<br>Delete. | 4DW Msg - Routed by ID |  |  |  |  |  |  |
| Create Folder Rename  |                        |  |  |  |  |  |  |
| Move to Folder Delete   |                        |  |  |  |  |  |  |
|   |                        |  |  |  |  |  |  |
|   |                        |  |  |  |  |  |  |
| Load from File Save to File Close   |                        |  |  |  |  |  |  |

- Create folders, move selected events to folders, and rename or delete selected events.
- Save favorites to a file, or load saved favorites from a file.
- 3 When you are done organizing packet event favorites, click Close.

See Also

- To save favorite packet events (see page 176)
- To specify packet events (in "Find a packet" trigger function) (see page 175)

#### To specify a trigger sequence step's goto or trigger action

**1** In the Advanced Trigger dialog, within a sequence step, select the desired trigger action:

| Then ¥ | Trigger and fill memory                     |
|--------|---|
| _      | Goto  |
|        | Trigger and fill memory<br>Trigger and goto |
|        | Trigger, send e-mail, and fill memory       |

You can select:

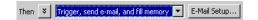
• Goto-To go to another trigger sequence step.



- **Trigger and fill memory**—To trigger the logic analyzer and fill memory, without going to any other steps in the trigger sequence.
- **Trigger and goto**—To trigger the logic analyzer and go to another trigger sequence step. (This can be useful when you use trigger sequence steps to specify what samples get stored.)

| Then | <ul> <li>Trigger and goto</li> </ul> | ▼ Next ▼ |
|------|--------------------------------------|----------|
|      |                                      | 1<br>2   |

• **Trigger, send e-mail, and fill memory**—To trigger the logic analyzer, send e-mail, and fill memory, without going to any other trigger sequence steps. Clicking **E-Mail Setup...** opens the E-mail dialog (see page 504) for entering the e-mail address, subject, and message.



2 If you selected one of the actions that specify **fill memory** and you are in the state mode or in the store qualified timing mode with custom storage selected, enter the storage qualifier used to fill memory.

| Then | <ul> <li>Trigger and fill memory</li> </ul> | • |
|------|---|---|
|      | Vith Default Storage Constraints            |   |

**See Also** • To insert or delete events (see page 180)

- To specify default storage (see page 179)
- To insert or delete actions (in a trigger sequence step) (see page 185)

#### To specify default storage

Storage qualifiers are used to specify which samples (captured from the device under test) are stored in logic analyzer memory. By storing only the samples you are interested in, you can make better use of the available memory and capture activity for a greater amount of time.

*Default Storage* means "unless *storage control* actions or *fill memory* storage qualifiers in trigger sequence steps specify otherwise, this is what should be stored". Storage qualifiers in trigger sequence steps always override default storage.

The default storage qualifier is available in state sampling mode and in the store qualified (transitional) timing mode.

In Transitional / Store Qualified Timing Mode

- 1 Select the type of storage qualification: either Transitional or Custom.
  - When **Transitional** is selected, samples that have transitions from the previous sample are stored.

| Trigger Sequence  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|
| Default Storage (overridden by sequence level store actions): |  |  |  |  |  |  |  |  |
| Transitional 💌 Exclude buses/signals                          |  |  |  |  |  |  |  |  |

If you want to exclude certain bus/signal transitions from being stored, click **Exclude buses/signals...**, and specify which buses/signals should be excluded.

• When **Custom** is selected, edit or insert events that should be stored (or not stored) in logic analyzer memory.

| Trigger Sequence  |
|---|
| Default Storage (overridden by sequence level store actions): |
| Custom  |
| Store X Anything  |

In State Mode 1 Edit or insert events that should be stored (or not stored) in logic analyzer memory.

| Trigger Sequence  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|
| Default Storage (overridden by sequence level store actions): |  |  |  |  |  |  |  |  |
| Store Anything  |  |  |  |  |  |  |  |  |

- See Also To insert or delete events (see page 180)
  - To negate events (see page 183)
  - To change the evaluation order of AND/OR'ed events (see page 184)
  - To insert a storage control action (see page 188) (in a trigger sequence step)
  - To specify a trigger sequence step's goto or trigger action (see page 178)
  - Understanding Logic Analyzer Triggering, Storage Qualification (see page 439)

#### To insert or delete events

1 In the Advanced Trigger dialog, in a trigger sequence step, click the button associated with an event (after Find or If in trigger sequence step conditions, or after Store or with in storage qualifiers), and choose Insert Event After (AND/OR), Insert Event Before (AND/OR), or Delete Event.

| Find 🐮 Bus/Signal 💌 My Bus 1 | All bits 💌 = | ▼ XX 🖩 Hex ¥ And ▼ |
|------------------------------|--------------|--------------------|
| Insert Event After (AND/OR)  |              |                    |
| Insert Event Before (AND/OR) |              |                    |
| Delete Event                 |              |                    |

2 If inserting an event, select the type of event.

| Find<br>Bus/Signal 💌                    | My Bus 1 | × All bits 💌 = | ▼ XX Hex ¥ And ▼ |
|---|----------|----------------|------------------|
| Bus/Signal                              |          |                |                  |
| Anything                                |          |                |                  |
| Nething                                 |          |                |                  |
| Anything<br>Timer<br>Nothing<br>Counter |          |                |                  |
| Flag                                    |          |                |                  |
| Flag<br>Arm in from                     |          |                |                  |

Depending on where you are inserting the event, the following event types may be available:

- **Bus/Signal**-Bus/signal value, To specify bus/signal patterns or edges (see page 169).
- **Anything**—Any sample.
- Nothing–No sample.
- **Timer**–A timer value, see To insert a timer event (see page 181).
- **Counter**–A counter value, see To insert a counter event (see page 181).
- Flag–A flag value, see To insert a flag event (see page 182).
- Arm in from—An arming signal from another logic analyzer module or an external instrument, see To insert an "Arm in from" event (see page 182).

**3** If inserting an event, specify whether the event should be **And**'ed or **Or**'ed with the other events.



**See Also** • To negate events (see page 183)

- To change the evaluation order of AND/OR'ed events (see page 184)
- Understanding Logic Analyzer Triggering, Boolean Expressions (see page 435)

#### To insert a timer event

1 Select the timer that you want to check.

| Find | ¥ Timer | • | 1 🔻    | >= 💌 | 80 ns | <b>-</b> + | And 💌 |
|------|---------|---|--------|------|-------|------------|-------|
|      |         |   | 1<br>2 |      |       |            |       |

**2** Select the timer compare operator.



3 Enter the timer value to compare against.

**NOTE** The **Start from reset** timer action can be placed in either the same sequence step as the timer check event, or it can be placed in a preceding trigger step. Checking a timer without starting it will generate an error.

For more information on timers, see Using Timers (see page 165).

**See Also** • To insert or delete events (see page 180)

#### To insert a counter event

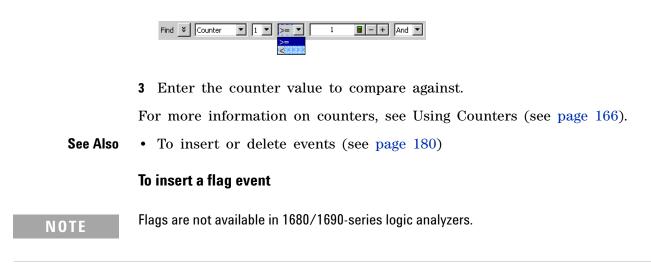
A counter must be started with a counter action before it can be evaluated with a counter event.

**1** Select the counter that you want to check.



2 Select the counter compare operator.

#### **6** Capturing Data from the Device Under Test



1 Select the flag that you want to check.



2 Enter the flag value to compare against.



There is approximately 100 ns of delay before a flag action can be seen by a flag event.

Multiple modules can insert flag events for the same flag to test whether the flag is set or clear.

For more information on flags, see Using Flags (see page 167).

**See Also** • To insert or delete events (see page 180)

## To insert an "Arm in from" event

1 Specify the source of the arming signal by selecting another module or **External trigger**.



For more information on triggering on signals from other logic analyzer modules or external instruments, see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193).

**See Also** • To insert or delete events (see page 180)

## To negate events

Everywhere in the Advanced Trigger dialog where you can edit or insert events, you can also negate the events.

1 Click the **s** button associated with the events, and choose **Negate**.

| Default Storage (overridden by seq |  |  |  |  |  |
|------------------------------------|--|--|--|--|--|
| 🐮 Store 👻 Anything 💌               |  |  |  |  |  |
| Negate                             |  |  |  |  |  |
| Group Events [f/Then               |  |  |  |  |  |

| ≥ If Sus/Signa          | al 🔻       |         | My Bus 1 | All bits 💌 = | ▼ XX 🖩 Hex ¥ |
|-------------------------|------------|---------|----------|--------------|--------------|
| Insert If Clause After  | h 🗖        | 1       | ■ - +    |              |              |
| Insert If Clause Before |            |         |          |              |              |
|                         | nd fill me | mory    | •        |              |              |
| Negate If Clause        | Defaul     | : Stora | ge 💌     |              |              |
| - Group Events          |            |         |          |              |              |

| Then | × Trigger and fill men | nory 💌    |
|------|------------------------|-----------|
|      | 🗧 with 🔰 Default       | Storage 💌 |
|      | Negate                 |           |
|      | Group Events           |           |

Text in the dialog changes to indicate that events are negated.

| Default Storage (overridden by sequence level store actions):         Store everything except         Anything |  |  |  |  |  |
|--|--|--|--|--|--|
| Step 1 💙 Advanced If/Then  |  |  |  |  |  |
| 🗴 If not 🛛 🗴 Bus/Signal 💌 My Bus 1 All bits 💌 = 🔍 XX 📱 Hex 🍣   |  |  |  |  |  |
| occurs 🔽 1 🔳 – +   |  |  |  |  |  |
| Then Trigger and fill memory   |  |  |  |  |  |
| with everything except V Default Storage V   |  |  |  |  |  |

#### NOTE

Negate is not available for storage qualifier events in the Turbo State Mode (see page 122).

**See Also** • To insert or delete events (see page 180)

#### To change the evaluation order of AND/OR'ed events

When specifying advanced triggers (or after converting trigger functions to advanced *if/then* steps) and there are multiple events in an event list, you can specify their evaluation order by grouping the events.

1 In the Trigger tab's Trigger Sequence area, select the *If*, *If not*, *Else if*, or *Else if not* button; then, choose **Group Events...**.

| Trigger Sequence  |
|---|
| Step 1 ¥ Advanced If/Then   |
| Insert If Clause After<br>Insert If Clause Before                         |
| Delete If Clause     Signal 3     High       Negate If Clause     1     + |
| Group Events  |

2 In the Parenthesis dialog, either select Add Parens button to group events or select **Remove Parens** to ungroup events.

| arenthesis                    |                       |    |        | × |
|-------------------------------|-----------------------|----|--------|---|
| (Bus/Signal And Bus/Signal) ( | )r Bus/Signal         |    |        |   |
| Add Parens Remove Par         | ens Remove All Parens | OK | Cancel |   |

- 3 When you have finished grouping events, click OK.
- **See Also** To insert or delete events (see page 180)

#### To choose between a duration or occurrence count for events (timing mode)

When specifying advanced triggers in the timing mode, you can choose between specifying an occurrence count for events or a time that the events must be present for.

1 In the trigger sequence step, select either **occurs** or **present for >** to change the setting.

| Step 1 🛛 🕹 | Advanced If/Then   |                       |              |
|------------|--|-----------------------|--------------|
| ¥ IF       | ¥ Bus/Signal ▼   | My Bus 1 All bits 💌 = | ▼ XX 🖩 Hex ¥ |
|            | occurs 💌   | 1 📕 - +               |              |
| Then       | occurs<br>present for > present for presen | <b>•</b>              |              |

**See Also** • To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)

#### To insert or delete actions (in a trigger sequence step)

1 In the Advanced Trigger dialog, in a trigger sequence step, click the subutton associated with an action (after Then), and choose Insert Action After, Insert Action Before, or Delete Action.



2 If inserting an action, select the type of action.



The following action types are available:

- **Timer**—For starting, stopping, pausing, or resuming a timer, see To insert a timer action (see page 185).
- **Counter**–For incrementing or resetting a counter, see To insert a counter action (see page 186).
- **Reset occurrence counter**—For resetting the occurrence counter, see To insert a reset occurrence counter action (see page 186).
- **Flag**—For setting or clearing a flag, see To insert a flag action (see page 187).
- **Storage control**—For storing samples or not or for turning on/off default storage, see To insert a storage control action (see page 188).
- **See Also** To insert or delete events (see page 180)

#### To insert a timer action

1 Select the timer that you want to specify an action for.



2 Specify the timer action by selecting either Start from reset, Stop and reset, Pause, or Resume.

| Then<br>Timer | ▼ 1 ▼ Start from reset ▼ |
|---------------|--------------------------|
|               | Start from reset         |
|               | Stop and reset           |
|               | Pause                    |
|               | Resume                   |

NOTE

The **Start from reset** timer action can be placed in either the same sequence step as the timer check event, or it can be placed in a preceding trigger step. Checking a timer without starting it will generate an error.

For more information on timers, see Using Timers (see page 165).

**See Also** • To insert or delete actions (in a trigger sequence step) (see page 185)

#### To insert a counter action

1 Select the counter that you want to specify an action for.



2 Specify the counter action by selecting either Increment or Reset.

| Then 🛛 Counter | ▼ 1 ▼ Increment ▼  |
|----------------|--------------------|
|                | Increment<br>Reset |

For more information on counters, see Using Counters (see page 166).

See Also • To insert or delete actions (in a trigger sequence step) (see page 185)

#### To insert a reset occurrence counter action

The trigger sequence step below shows how the **Reset occurrence counter** action is used.

| Step 1 🛛 🕹 | Step 1 🛛 Advanced If/Then                                 |  |  |  |  |  |
|------------|---|--|--|--|--|--|
| ¥ IF       | 🔻 Bus/Signal 💌 My Bus 1 All bits 💌 = 💌 FF 📓 Hex 💐         |  |  |  |  |  |
|            | occurs 💌 100 📓 – + eventually 💌                           |  |  |  |  |  |
| Then       | Trigger and fill memory                                   |  |  |  |  |  |
|            | Vith Vite Contract Vite Vite Vite Vite Vite Vite Vite Vit |  |  |  |  |  |
| × Else if  | 🔻 Bus/Signal 💌 My Bus 1 All bits 💌 = 💌 00 🗮 Hex 💐         |  |  |  |  |  |
| Then       | Reset occurrence counter                                  |  |  |  |  |  |
|            | Soto  |  |  |  |  |  |

While searching for a number of occurrences of one event, if some other event is found, you can reset the occurrence counter and restart the search.

See Also

- To insert or delete actions (in a trigger sequence step) (see page 185)
  - Understanding Logic Analyzer Triggering, Occurrence Counters (see page 437)

#### To insert a flag action

# NOTE Flags are not available in 1680/1690-series logic analyzers.

1 Select the flag that you want to specify an action for.



2 Specify the flag action by selecting either Set, Clear, Pulse set, or Pulse clear.



Flags in pulse mode sit in the opposite state when not being pulsed. If you insert a **Pulse set** action for a flag in one module, you cannot insert a **Pulse clear** action for the same flag in a different module.

NOTE

Within a module, the same flag cannot be used in both pulse and level (Set/Clear) modes. If a flag action is inserted or modified with a different mode than other actions for the same flag, all actions for that flag will change to match the new mode.

In case of multiple modules, legacy logic analysis systems allow a particular flag to be set by multiple modules. However, in newer AMP/AXIe based instrument modules, only one module can set a particular flag. Multiple modules cannot set the same flag.

A flag that is set by a module remains set until that module clears it. In legacy logic analysis systems, if multiple modules set the same flag, then all those modules must clear the flag before it becomes clear. In newer AMP/AXIe based instrument modules, multiple modules cannot set the same flag and therefore, the module that sets the flag can only clear it.

3 If you selected **Pulse set** or **Pulse clear**, enter the pulse width.

# **NOTE** Within a module, a flag's pulse width must be the same in every action for that flag. Whenever the pulse width is changed in a flag action, it changes in all other actions for that flag.

For more information on flags, see Using Flags (see page 167).

**See Also** • To insert or delete actions (in a trigger sequence step) (see page 185)

#### To insert a storage control action

1 Specify the storage control action by selecting either Store sample, Don't store sample, Turn on default storage, or Turn off default storage.

| Then | Storage control | Store         | e sample 💌  |
|------|-----------------|---------------|---|
|      |                 | Don't<br>Turn | e sample<br>: store sample<br>on default storage<br>off default storage |

For more information on sequence step storage and storage control actions, see Understanding Logic Analyzer Triggering, Storage Qualification (see page 439).

**See Also** • To insert or delete actions (in a trigger sequence step) (see page 185)

## To cut, copy, and paste trigger sequence steps

1 In a trigger sequence step, click **Step N** and choose **Cut**, **Copy**, **Paste Before**, or **Paste After**.

| Trigger Sequence  |                            |
|---|----------------------------|
| Step 1     Pattern       Find     V     Bus/Signal       Then     Trigger and fill memory | All bits V = V XX () Hex V |
| Step 2 ¥ Edge and Pattern   | Bit 0 V Dont Care V        |
| Cut<br>Copy<br>Paste Before   | All bits V = VX Hex 3      |
| Paste After If Clause Comments  | •                          |
| Show trigger step as if/then (read-only)<br>Convert step to if/then (can't undo)          |                            |

There must be at least one step in the trigger sequence.

**See Also** • To delete trigger sequence steps (see page 189)

## To delete trigger sequence steps

1 In a trigger sequence step, click Step N and choose Delete.

| Step 2 8 Pattern   |                               |
|--|-------------------------------|
| Delete   | s 1 All bits ▼ = ▼ XX 🖩 Hex ¥ |
| Show trigger step as if/then (read-only)<br>Convert step to if/then (can't undo) | Vext V                        |

There must be at least one trigger sequence step.

## To show a trigger sequence step as Advanced If/Then trigger functions

NOTE

The Advanced (If/Then or N-Way Branch) trigger functions do not allow alternative display types. By default, they are in the expanded graphical form that cannot be changed.

1 In a trigger sequence step, click **Step N** and choose **Show trigger step** as if/then (read-only).

|    | Step 1 🎽 Pattern                         |                               |
|----|--|-------------------------------|
|    |  | s 1 All bits 💌 = 💌 XX 🖩 Hex 🐳 |
| IF | Show trigger step as if/then (read-only) |                               |
| L  | Convert step to if/then (can't undo)     |                               |

The trigger sequence step will be shown as the equivalent Advanced If/Then trigger functions in read-only form.

| Ste | p1 ¥ P | attern                               |
|-----|--------|--------------------------------------|
| 1.1 | If     | Bus/Signal My Bus 1 = XX<br>occurs 1 |
|     | Then   | Trigger and fill memory              |

 To undo a trigger sequence step, click Step N and choose the checked Show trigger step as if/then (read-only) item to return to the normal view of the trigger function.

 Advanced

 If/Then trigger functions

| Step 1 2 Pattern   |          |  |
|--|----------|--|
| Delete   |          |  |
| <ul> <li>Show trigger step as if/then (read-only)</li> </ul> |          |  |
| L Convert step to if/then (can't undo)                       | <u> </u> |  |

**See Also** • To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)

#### To convert a trigger sequence step to Advanced If/Then trigger functions

If the trigger function you need doesn't exist, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

**NOTE** The Advanced (If/Then or N-Way Branch) trigger functions do not allow alternative display types. By default, they are in the expanded graphical form that cannot be changed.

1 In a trigger sequence step, click **Step N** and choose **Convert trigger step to if/then (can't undo)**.

| Step 1 २ Pattern                         |                                |
|--|--------------------------------|
|  | 51 All bits ▼ = ▼ XX III Hex ¥ |
| Show trigger step as if/then (read-only) |                                |
| Convert step to if/then (can't undo)     |                                |

The trigger sequence step will be converted to the equivalent Advanced If/Then trigger functions.

| Step 1 🛛 😽 | Advanced If/Then          |                       |              |
|------------|---------------------------|-----------------------|--------------|
| ¥ If       | ➤ Bus/Signal ▼            | My Bus 1 All bits 💌 😑 | ▼ XX 🖬 Hex ¥ |
|            | occurs                    | 1 📓 - +               |              |
| Then       | × Trigger and fill memory | V                     |              |

- See Also To show a trigger sequence step as Advanced If/Then trigger functions (see page 189)
  - Understanding Logic Analyzer Triggering, Branches (see page 436)

## To display or hide "If" clause comments

When using Advanced If/Then trigger functions, you can include comments with the "If" clauses in a trigger sequence step. It is useful to have descriptions in complex trigger functions.

To show all "If"1In a trigger sequence step, click Step N and choose If Clauseclause commentsComments>Show All.

| a an        | Advanced Trigger for My 16950A-1 |   |                                      |  |  |
|-------------|----------------------------------|---|--------------------------------------|--|--|
| т           | rigger Functions                 | Trigger Sequence  |                                      |  |  |
| Edge        | Advanced<br>If/Then              | Step 1 📚 Advanced If/Then   |                                      |  |  |
| Bus Pattern | Advanced<br>2-Way<br>Branch      |   | All bits V =                         |  |  |
| ced Other   | Advanced<br>3-Way<br>Branch      | If Clause Comments  Show trigger step as if/then (read-only) Convert step to if/then (can't undo) | Show All<br>Hide Empty =<br>Hide All |  |  |
| Advanced    | Advanced                         |   |                                      |  |  |

All "If" clause comments are show, including empty comments.

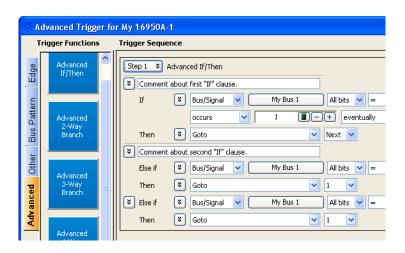
| a a               | Advanced Trigger for My 16950A-1 |  |  |  |
|-------------------|----------------------------------|--|--|--|
| т                 | rigger Functions                 | Trigger Sequence   |  |  |
| Edge              | Advanced<br>If/Then              | Step 1 * Advanced If/Then Comment about first "If" clause. |  |  |
| attern            | Advanced                         | If V Bus/Signal V My Bus 1 All bits V =                    |  |  |
| Other Bus Pattern | 2-Way<br>Branch                  | Then V Goto  |  |  |
| Ŀ.                |                                  | Comment about second "If" clause.                          |  |  |
| 듕                 | Advanced                         | Else if 🛛 Bus/Signal 🔽 My Bus 1 All bits 💟 =               |  |  |
| ced               | 3-Way<br>Branch                  | Then 😻 Goto 💌 1 💌  |  |  |
| Advanced          |                                  |  |  |  |
| P                 |                                  | Else if 🛛 Bus/Signal 👻 My Bus 1 All bits 👽 =               |  |  |
|                   | Advanced<br>4-Way                | Then 💐 Goto 💌 1 💌  |  |  |
|                   | Branch                           |  |  |  |

To hide empty "If" clause comments

1 In a trigger sequence step, click **Step N** and choose **If Clause Comments>Hide Empty**.

Empty "If" clause comments are hidden.

#### **6** Capturing Data from the Device Under Test



To hide all "If" clause comments

#### 1 In a trigger sequence step, click **Step N** and choose **If Clause Comments>Hide All**.

All "If" clause comments are hidden.

| a all     | Advanced Trigger for My 16950A-1 |   |              |                  |                       |
|-----------|----------------------------------|---|--------------|------------------|-----------------------|
| т         | rigger Functions                 |   | Trigger Sequ | ence             |                       |
| Edge      | Advanced<br>If/Then              | ^ | Step 1 💙     | Advanced If/Then |                       |
| -         |                                  |   | 💙 If         | 🗧 😽 Bus/Signal 🔽 | My Bus 1 All bits 💙 = |
| tern      |                                  |   |              | occurs 💌         | 1 III eventually      |
| s Pattern | Advanced<br>2-Way                |   | Then         | Soto             | Next 💌                |
| Bus       | Branch                           |   | Else if      | 🗧 🛛 😸 😸 😸        | My Bus 1 All bits 💙 = |
| Other     |                                  |   | Then         | 🗧 Goto           | ✓ 1 ✓                 |
| ą         | Advanced                         |   | Else if      | 🗧 🗧 Bus/Signal 🔽 | My Bus 1 All bits 💌 = |
| anced     | 3-Way<br>Branch                  | ∃ | Then         | Soto             | ▼ 1 ▼                 |
| a         |                                  |   |              |                  |                       |

**See Also** • To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)

## To clear the trigger sequence

1 In the Advanced Trigger dialog, click Clear at the bottom of the dialog.

# **Triggering From, and Sending Triggers To, Other Modules/Instruments**

#### **ARM In from modules**

You can cause the trigger from one module to arm another module installed in the same chassis or in a chassis/logic analysis system (interconnected via multiframe cables in a multiframe setup). Refer to the topic "To arm one module with another module's trigger" on page 193 to know about ARM In feature in detail.

#### **External triggering**

You can also send a module's trigger signal to an external instrument, or you can allow a signal from an external instrument to arm a module.

There are Trigger In and Trigger Out BNC connectors located on the logic analyzer (rear panel of 1680-series and 16900-series, front panel of 1690-series, and front panel of AXIe chassis for the U4154A module). Use these connectors to connect the analyzer to an external instrument and either send or receive a trigger signal. To know more about external triggering, refer to the topics "To trigger other instruments - Trigger Out" on page 198 and "To trigger analyzer from another instrument - Trigger In" on page 199.

#### To arm one module with another module's trigger

A module can receive ARM In from a single or multiple modules installed in the same chassis or in an interconnected chassis of a multiframe setup. To use this ARM In feature, you use the *Wait for arm from another module* trigger function in the Advanced Trigger dialog. This topic describes various ARM In scenarios.

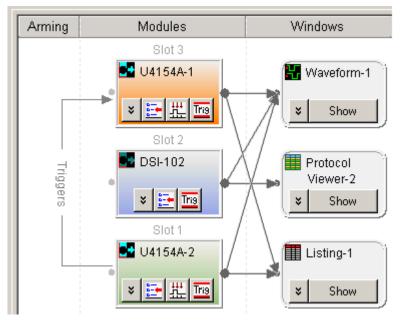
#### ARM In from a module to another module in the same/different chassis

- 1 Click in the analyzer setup toolbar, or choose **Setup>(Logic Analyzer Module)>Advanced Trigger...** from the menu bar.
- 2 In the Advanced Trigger dialog (see page 496), select the Other trigger functions tab; then, drag-and-drop the Wait for arm from another module trigger function into the trigger sequence area.

| Step 2 💙 | Wait for arm from another module            |  |  |
|----------|---|--|--|
| × A      | rm in from 💌 U4154A-2 💌                     |  |  |
| Then     | <ul> <li>Trigger and fill memory</li> </ul> |  |  |

- **3** From the module name drop-down, select the module whose trigger will arm this module (and satisfy the event condition in the trigger sequence step).
- 4 Click OK in the Advanced Trigger dialog.

The arming setup in the Overview window looks like:

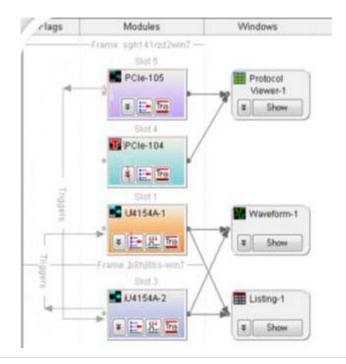


**5** Run the measurement (see Running/Stopping Measurements (see page 203)).

When the arm from another module (U4154A-2 in this case) is received, the module (U4154A-1 in this case) takes the action(s) described in its trigger sequence step.

#### NOTE

You can create an ARM In trigger in the same manner (as described above) between modules installed in different chassis of a multiframe setup. In a multiframe setup, flags are consumed for each ARM IN trigger configuration that you create. There are 4 flags available. If all these flags are unused, then you can create a maximum of four ARM In configurations across the connected chassis of the multiframe chain. An example of two ARM In configurations in a multiframe setup is displayed below.



## And vice-versa

You may have a situation where you have two modules looking for trigger events, and when either module finds its trigger event, the other should be armed. To do this:

1 Set up the first module's trigger (for example, for My 16742A-1):

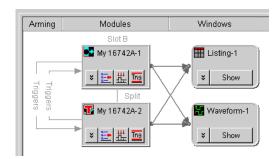
| Step 1 🛛 Wait for arm from another module |                              |
|---|------------------------------|
| Bus/Signal      My Bus 1                  | All bits V = V FF Hex V Or V |
| × Arm in from  My 16742A-2                |                              |
| Then 🛛 Trigger and fill memory            | <b>•</b>                     |
| 🗧 with 🔰 Default Storage 💌                |                              |

2 Set up the second module's trigger (for example, for My 16742A-2):

#### **6** Capturing Data from the Device Under Test

| Step 1 🛛 Wait for arm from another module |                                |
|---|--------------------------------|
| V Bus/Signal V My Bus 2                   | All bits 💌 = 🔍 00 📓 Hex 🐳 Or 💌 |
| × Arm in from  My 16742A-1                |                                |
| Then 🗧 Trigger and fill memory            | •                              |
| 💙 with 💙 Default Storage 💌                |                                |

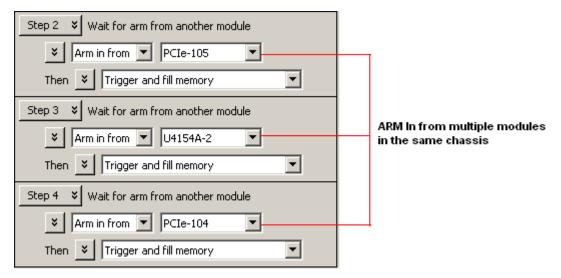
The arming setup in the Overview window looks like:

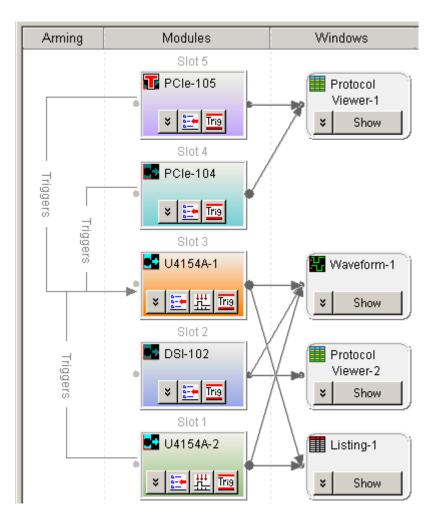


**3** Run the measurement.

#### ORed ARM In from multiple modules to a module in the same chassis

You can set the trigger configurations of a module to receive ARM In from multiple modules in the same chassis. On doing so, the trigger configuration acts as an ORed combination of ARM In from multiple modules. Any of the selected modules can send ARM In to trigger the module. In such a scenario, the trigger configuration of the module receiving the ARM In consists of multiple *Wait for arm from another module* trigger sequence steps as displayed below.



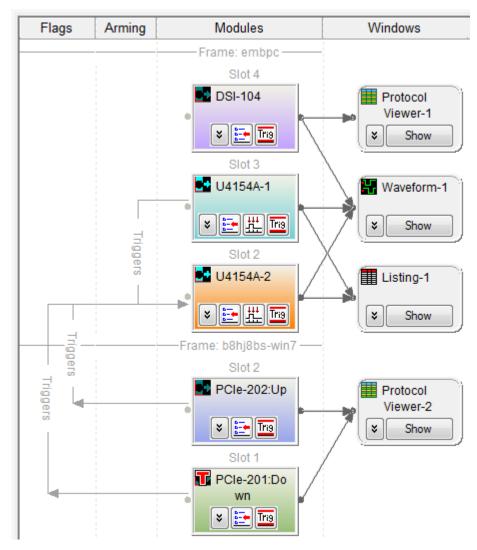


The arming setup in the Overview window looks like:

As displayed in the above figure, an ORed ARM In trigger is represented by multiple unidirectional lines merging together before pointing to the destination module receiving the ARM In.

#### ORed ARM In from multiple modules to a module in a multiframe setup

You can also set the ORed ARM In for a module from multiple modules in other connected chassis of a multiframe setup. To create an ORed ARM In in a multiframe scenario, you need to create multiple **Wait for arm from another module** trigger sequence steps for the receiving module. The following screen displays the ORed ARM In trigger for the U4154A-2 modules from three modules in a multiframe setup.



- See Also
- Wait for arm from another module (state) (see page 582)
- Wait for arm from another module (timing) (see page 570)

## To trigger other instruments - Trigger Out

- 1 Connect a BNC cable from the **Trigger Out** BNC to the external instrument you want to trigger.
- 2 Choose Setup>External Trigger....

- **3** In the External Trigger dialog (see page 510):
  - **a** If you are using a 1680/1690-series logic analyzer, specify whether the trigger will appear as a rising or falling edge on the **Trigger Out** BNC.

If you are using a 16800-series logic analyzer or a 16900-series logic analysis system:

- Enable the output.
- Select the polarity (active high or active low).
- Select the output mode (use feedthrough to see flag settings on the output).
- Select the trigger and flag events that cause Trigger Out.
- **b** Click **OK**.
- **4** Configure the logic analyzer as you would normally for any other measurement.
- 5 When the analyzer's trigger sequence becomes true and the analyzer triggers, a trigger signal is sent out through the **Trigger Out** BNC to the external instrument.
- **See Also** External Trigger Dialog (see page 510)

## To trigger analyzer from another instrument - Trigger In

- 1 Connect a BNC cable from the **Trigger In** BNC to the external instrument that will send the trigger signal.
- 2 Choose Setup>External Trigger....
- **3** In the External Trigger dialog (see page 510), specify whether a rising or falling edge on the **Trigger In** BNC will indicate a trigger; then, click OK.
- 4 Click in the analyzer setup toolbar, or choose Setup>(Logic Analyzer Module)>Advanced Trigger... from the menu bar.
- **5** In the Advanced Trigger dialog (see page 496), select the **Other** trigger functions tab; then, drag-and-drop the **Wait for external arm** trigger function into the trigger sequence area.

| Step 1 🕹              | Wait for external arm |  |
|-----------------------|-----------------------|--|
| Wait for external arm |                       |  |

- 6 Click OK in the Advanced Trigger dialog, and run the measurement (see Running/Stopping Measurements (see page 203)).
- 7 Run the measurement on the external instrument.

When the arm from the external instrument is received, the logic analyzer takes the actions described in the trigger sequence step.

See Also

- Wait for external arm (state) (see page 582)
  - Wait for external arm (timing) (see page 569)
  - External Trigger Dialog (see page 510)

# **Storing and Recalling Triggers**

Triggers are stored in three ways:

- Automatically, after measurements are run, to the recently-used list.
- By storing them (see page 201) to the favorites list.
- By storing them (see page 201) to XML format trigger specification files.

You can recall triggers (see page 202) from the recently-used list, the favorites list, or from XML-format trigger specification files.

You can move recently-used triggers to the favorites list (see page 202).

You can control the length of the recently-used and favorites list by setting the trigger history depth (see page 202).

#### NOTE

The current trigger setup (and the favorites list) are stored as part of the logic analyzer configuration. If you load a new configuration file, the trigger setup (and the favorites list) will be overwritten.

## To store a trigger

- 1 Choose the **Setup>(Logic Analyzer Module)>Store Trigger...** command, or in the Advanced Trigger dialog, click **Store...**.
- 2 In the Store Trigger dialog:

| ×                 |
|-------------------|
| Store as favorite |
| Save to file      |
| Cancel            |
|                   |

To store the trigger in the favorites list:

- **a** Enter the name of the trigger.
- **b** Click **Store as favorite**.

To store the trigger in an XML format file:

- a Click Save to file....
- **b** In the Save As dialog, enter the name of the file, and click **Save**.

**See Also** • To recall a trigger (see page 202)

• To set the trigger history depth (see page 202)

## To recall a trigger

| 1 | Choose Setup>(Logic Analyzer Module)>Recall Trigger   | from | the |
|---|---|------|-----|
|   | menu, or in the Advanced Trigger dialog, click Recall |      |     |

- 2 In the Recall Trigger dialog (see page 527):
  - Select the desired trigger from the favorites or recently-used list; then, click **OK**.
  - Or, to recall a trigger from a previously saved XML format trigger specification file, click **Open...** and select the file.

To move a<br/>recently-used<br/>trigger to the<br/>favorites list1Choose Setup>(Logic Analyzer Module)>Recall Trigger... from the<br/>menu.2In the Recall Trigger dialog (see page 527), select the trigger from the<br/>recently-used list.3Click Store Selected Recent Trigger To Favorites List.

**See Also** • To store a trigger (see page 201)

## To set the trigger history depth

- 1 Choose the Edit>Options... command.
- 2 In the Options dialog, enter the Trigger History Depth.

The number you enter is used for both the recently-used trigger list and the favorites list.

**See Also** • To store a trigger (see page 201)

• To recall a trigger (see page 202)

# **Running/Stopping Measurements**

| To run the<br>analyzer in single<br>run mode        | <ul> <li>The single run measurement captures data and fills trace memory one time. The amount of data stored during a single run is equal to the amount of trace memory allotted. For example, if trace memory is equal to 2M, the amount of data stored after one run is equal to 2M.</li> <li>From the menu bar, choose <b>Run/Stop&gt;Run</b>, or click the ▶ icon from the run/stop toolbar (see page 473).</li> </ul> |
|---|--|
|   |  |
|   | See also To save captured data after each run (see page 203) below.  |
| To run the<br>analyzer in<br>repetitive run<br>mode | The run repetitive measurement captures data and fills trace memory<br>repetitively. The amount of data stored in a repetitive run is the same as<br>a single run. During a repetitive run, once the trace memory is full, the<br>system clears the trace memory and begins to refill with new data. This<br>cycle continues until the run is stopped.   |
|   | • From the menu bar, choose <b>Run/Stop&gt;Run Repetitive</b> , or click the local icon from the run/stop toolbar (see page 473).  |
| NOTE  | If you are repeatedly making measurements and looking at data some fixed time after the trigger (for example), you can change the "go to trigger on run" behavior (see page 204) so that the location being displayed doesn't change after each measurement.   |
|   | See also To save captured data after each run (see page 203) and To stop repetitive runs after a certain number of acquisitions (see page 204) below.  |
| To view analyzer<br>run status                      | • From the menu bar, choose <b>Run/Stop&gt;Status</b> , or click <b>Status</b> in the status bar.  |
|   | The run status is displayed in the System Status tab of the Status dialog (see page 542).  |
| To stop the<br>analyzer                             | When a measurement is stopped, the amount of data gathered is equal to<br>the amount of trace memory used up until the stop occurred. For example,<br>if trace memory is equal to 2M and the measurement is stopped exactly<br>half way through the run, the amount of data in trace memory would<br>equal 1M.   |
|   | • From the menu bar, choose <b>Run/Stop&gt;Stop</b> , or click the <b>I</b> icon from the run/stop toolbar (see page 473).   |
|   | See also: "Stop Behavior in the 16960/16962 Logic Analyzers" on page 676   |
| To save captured                                    | 1 From the menu bar, choose Run/Stop>Run Properties  |
| data after each<br>run                              | 2 In the Run Properties dialog (see page 529), check <b>Save after every acquisition</b> and set the additional options for saving data after each run; then, click <b>OK</b> .  |

|   | 3 | Run the analyzer in either single run mode or repetitive run mode.   |
|---|---|--|
| To stop repetitive                                | 1 | From the menu bar, choose Run/Stop>Run Properties  |
| runs after a<br>certain number of<br>acquisitions | 2 | In the Run Properties dialog (see page 529), check <b>Stop running after</b> and enter the number of acquisitions; then, click <b>OK</b> . |
| acquisitions                                      | 3 | Run the analyzer in repetitive run mode.   |
| See Also  | • | To change the "Go to Trigger on Run" option (see page 204)   |

• Run Properties Dialog (see page 529)

## To change the "Go to Trigger on Run" option

After a measurement is run and it completes, the default behavior of the *Agilent Logic Analyzer* application is to display the data captured around the system trigger.

If you are repeatedly making measurements and looking at data some fixed time after the trigger (for example), you can change the "go to trigger on run" behavior so that the location being displayed doesn't change after each measurement.

- 1 Choose Edit>Options....
- 2 In the Options dialog (see page 522), check or uncheck the Go to Trigger on Run box.

Option settings are saved in the registry; this means your changes will be present the next time you start the *Agilent Logic Analyzer* application.

# Saving Captured Data (and Logic Analyzer Setups)

You can save logic analyzer setups and captured data to configuration files. Later, the configuration files can be opened to set up the logic analyzer and re-load the data. When saving configuration files, you can choose to save only the logic analyzer setup (that is, without the data).

You can also save captured data to comma-separated value (CSV) files. CSV files can be imported into spreadsheet, database, or other data analysis programs.

- To save a configuration file (see page 206)
- To export data to standard CSV format files (see page 207)
- To export data to module CSV format files (see page 210)
- To export data to module binary (ALB) format files (see page 213)
- To export data to 16700 ASCII format files (see page 215)

## To save a configuration file

The save feature allows you to save a configuration file for later use. The first time a file is saved the logic analyzer configuration file dialog box will appear. The **Save As...** feature allows an existing configuration file to be saved under a different name.

1 From the menu bar, select File>Save or select the ■ icon in the standard toolbar (see page 469).

| Save As          |                             |            |           | ?        | × |
|------------------|-----------------------------|------------|-----------|----------|---|
| Save in: 🔁       | Config Files                | •          | 🦛 🗈 (     | * 💷 *    |   |
| 🙁 config.ala     |                             |            |           |          |   |
|                  |                             |            |           |          |   |
|                  |                             |            |           |          |   |
|                  |                             |            |           |          |   |
|                  |                             |            |           |          |   |
| File name:       | E.                          |            |           | Save     |   |
|                  |                             |            |           | Cancel   |   |
| Save as type:    | Standard Configuration (*.a | alaj       | <b>_</b>  | Lancel   |   |
| Source:          | All                         |            | Ψ.        |          |   |
|                  |                             |            |           |          |   |
| – File Header Ir | formation                   |            |           |          |   |
| Owner:           |                             | Project:   |           | <b>_</b> |   |
| Owner:           | <u> </u>                    | Project: j |           |          |   |
| Description:     |                             |            |           |          |   |
| File Options -   |                             |            |           |          | ] |
|                  | nd Setup ု 🔘 Setup Only     | C Range    | Propertie | 35       |   |
|                  |                             |            |           | Help     |   |

2 Enter the File name.

### CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

3 Select the Save as type.

For information on when to use the ALA (\*.ala) format and when to use the XML (\*.xml) format, see ALA vs. XML, When to Use Each Format (see page 445).

4 If you are saving as an XML format file, select the Source.

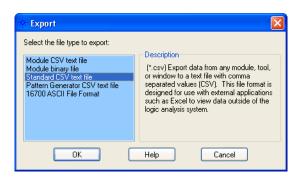
You can save configuration information and data from all modules or individual modules.

|           | <b>5</b> If desired, fill-in the <b>Owner</b> , <b>Project</b> , and <b>Description</b> fields under the file header information. These fields help identify the configuration file when it is reopened. |
|-----------|--|
|           | <b>6</b> Select the file options:  |
|           | <ul> <li>All Data and Setup — if you wish to save captured data and<br/>instrument settings.</li> </ul>  |
|           | • <b>Setup Only</b> – if you wish to save only the instrument settings and not the captured data.  |
|           | <ul> <li>Range – if you wish to save instrument settings and a range of<br/>captured data. Click Properties; in the Range Properties dialog,<br/>specify the range.</li> </ul>                           |
| NOTE      | Configuration files that include data are much larger than files that do not contain data.   |
|           | 7 Click Save.  |
| NOTE      | If you are using the logic analyzer without a keyboard, you can access an on-screen<br>keyboard by selecting <b>Start&gt;Programs&gt;Accessories&gt;Accessibility&gt;On-Screen</b><br><b>Keyboard</b> .  |
| See Also  | • To open a configuration file (see page 220)  |
|           | Offline Analysis (see page 233)  |
|           | • ALA vs. XML, When to Use Each Format (see page 445)  |
|           | • ALA Format (see page 588)  |
|           | • "XML Format" (in the online help)  |
| To export | a data to standard CSV format files  |

You can export captured data to standard comma-separated value (CSV) files. Standard CSV files can be imported into spreadsheet, database, or other data analysis programs.

- 1 From the menu bar, select File>Export....
- 2 In the Export dialog, select Standard CSV text file; then, click OK.

#### **6** Capturing Data from the Device Under Test



**3** In the following Export dialog:

| Export                |                                     | ? 🔀     |
|-----------------------|-------------------------------------|---------|
| Savejn: 🗁             | Export Files 💽 📀 🏂                  | ⊳ 🖽     |
| 🕖 module.csv          |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
| File <u>n</u> ame:    | module.csv                          | Save    |
| Save as <u>t</u> ype: | Comma Separated Value Files (*.csv) | Cancel  |
| Source:               | My 16950A-1                         | Options |
| File Options          |                                     |         |
| All Data              | Data Range Bus Signal Selection     |         |
|                       |                                     | Help    |

a Enter the CSV file name.

#### CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

- **b** Select the **Source** module, tool, or display window from which to export data.
- **c** If you want to use a delimiter other than a comma, or if you want to specify that line numbers be written, click **Options...** In the File Export Options dialog, make your selections; then, click **OK**.

| File Export Options      |             | X      |
|--------------------------|-------------|--------|
| Separation Character(s): | ,           |        |
| Vrite line number column | Line Number |        |
|                          | ОК          | Cancel |

- d If you want to export a range of data and/or selected bus/signal data, uncheck All Data.
- e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.

| Range Prope      | erties               |     |              |
|------------------|----------------------|-----|--------------|
| Data Range       | Bus/Signal Selection |     |              |
| <u>∩ A</u> ll    |                      |     |              |
| <u>◯ T</u> ime   | from: -873.81333 us  | to: | 1.2233387 ms |
| ⊙ <u>M</u> arker | from: M1             | yo: | M2 🗸         |
|                  |                      |     |              |
|                  |                      |     |              |
|                  |                      |     |              |
|                  |                      |     |              |
|                  | 0                    | K C | Cancel Help  |

f To select certain bus/signal data to export, click **Bus Signal Selection...** In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.

| Range Properties                |                           |
|---------------------------------|---------------------------|
| Data Range Bus/Signal Selection |                           |
| P -                             | Select All<br>Select None |
| DK Cano                         | el Help                   |

## NOTE

You can only choose particular buses/signals when a module or tool is selected as the **Source** of the data export. When a display window is selected as the **Source**, all buses/signals are exported. (You can, however, delete unwanted buses/signals from a display window before exporting its data.)

- 4 Click Save.
- **See Also** Standard CSV Format (see page 588)

## To export data to module CSV format files

You can export captured data to module comma-separated value (CSV) files. Module CSV files can be post-processed and re-imported into the logic analysis system using a *data import module*.

## CAUTION

Do not modify module CSV files with Microsoft Excel. When it saves the file, Excel will change the CSV format so that the data cannot be re-imported into the logic analysis system without a lot of manual text editing.

- 1 From the menu bar, select File>Export....
- 2 In the Export dialog, select Module CSV text file; then, click OK.

| 🔆 Export  | X  |
|---|--|
| Select the file type to export:<br>Module CSV text file<br>Module binary file<br>Standard CSV text file<br>Pattern Generator CSV text file<br>16700 ASCII File Format | Description<br>(".csv) Export analyzer data to a text file<br>with comma separated values (CSV). This<br>simple file format is designed for<br>processing data by external applications.<br>This file format can be imported back into<br>the logic analysis system (See<br>File->Import). |
| ОК  | Help Cancel  |

**3** In the following Export dialog:

| Export                |                                     | ?       |
|-----------------------|-------------------------------------|---------|
| Save jn: 🚞            | Export Files 💽 🕑 🥬                  | ⊳ 🖽     |
| 🖲 module.csv          |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
|                       |                                     |         |
| File <u>n</u> ame:    | module.csv                          | Save    |
|                       | 0                                   |         |
| Save as <u>t</u> ype: | Comma Separated Value Files (*.csv) | Cancel  |
| Source:               | My 16950A-1                         | Options |
| File Options          |                                     |         |
| 🔄 <u>A</u> ll Data    | Data Range Bus Signal Selection     |         |
|                       |                                     | Help    |
|                       |                                     |         |

a Enter the CSV file name.

CAUTION When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

**b** Select the **Source** module from which to export data.

You can export data to module CSV format files from logic analyzer and import modules only. You can export timing zoom data from a logic analyzer module, but it must be exported separately from the module's main data.

**c** If you want to use a delimiter other than a comma, if you want to specify that line numbers be written, or if you want to exclude the header information, click **Options...** In the File Export Options dialog, make your selections; then, click **OK**.

| K File Export Options                                    |             |         |
|--|-------------|---------|
| Separation Character(s):                                 | ,           |         |
| Vrite line number column                                 | Line Number |         |
| ✓ Include Header. Required t<br>system (See File->Import |             | nalysis |
|  | ОК С        | ancel   |

Header information must be included in order to re-import the data into the logic analysis system; however, header-less files may be easier for external tools to use.

- d If you want to export a range of data and/or selected bus/signal data, uncheck All Data.
- e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.

| Range Prope      | rties 🛛 🔀                                |
|------------------|--|
| Data Range       | Bus/Signal Selection                     |
| <u>⊖ A</u> ll    |  |
| ◯ <u>I</u> ime   | from: -873.81333 us 🔳 to: 1.2233387 ms 🔳 |
| ⊙ <u>M</u> arker | from: M1 💌 to: M2                        |
|                  |  |
|                  |  |
|                  |  |
|                  |  |
|                  | OK Cancel Help                           |

f To select certain bus/signal data to export, click **Bus Signal Selection...** In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.

| Range Properties                |          |                           |
|---------------------------------|----------|---------------------------|
| Data Range Bus/Signal Selection |          |                           |
| G - G My 16950A-1               |          | Select All<br>Select None |
|                                 | OK Cance | Help                      |

4 Click Save.

See Also

- To create a data import module (see page 227)
- Module CSV Format (see page 589)

## To export data to module binary (ALB) format files

You can export captured data to module binary files. Future releases of the *Agilent Logic Analyzer* application will be able to import module binary files into the logic analysis system using a *data import module*.

- 1 From the menu bar, select File>Export....
- 2 In the Export dialog, select Module binary file; then, click OK.

| 🔆 Export  | $\mathbf{X}$  |
|---|---|
| Select the file type to export:<br>Module CSV text file<br>Module binary file<br>Standard CSV text file<br>Pattern Generator CSV text file<br>16700 ASCII File Format | Description<br>(*.alb) Export analyzer data to a binary file.<br>This simple file format is designed for<br>processing data by external applications.<br>This file format can be imported back into<br>the logic analysis system (See<br>File->Import). |
| ОК  | Help Cancel   |

**3** In the following Export dialog:

| Export                |                                 | ?  |
|-----------------------|---------------------------------|----|
| Savejn: 🚞             | Export Files 🕑 🕝 🏂 📂 🖽 🗸        |    |
| 🔤 module.alb          |                                 |    |
|                       |                                 |    |
|                       |                                 |    |
|                       |                                 |    |
|                       |                                 |    |
|                       |                                 |    |
| File <u>n</u> ame:    | module.alb                      | •  |
| Save as <u>t</u> ype: | Module Binary Files (*.alb)     | el |
| Source:               | My 16950A-1 Option:             |    |
| File Options          |                                 |    |
| 🗌 <u>A</u> ll Data    | Data Range Bus Signal Selection |    |
|                       | He                              | P  |
|                       |                                 |    |

**a** Enter the ALB file name.

CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

**b** Select the **Source** module from which to export data.

You can export data to module binary format files from logic analyzer modules only. You can export timing zoom data from a logic analyzer module, but it must be exported separately from the module's main data.

**c** If you want to exclude the header information, click **Options...** In the File Export Options dialog, make your selections; then, click **OK**.

| 🔆 File Export Options 🛛 🛛 🔀   |
|---|
| <ul> <li>Include Header. Required to import back into the logic analysis<br/>system (See File-&gt;Import).</li> </ul> |
| OK Cancel   |

Header information must be included in order to re-import the data into the logic analysis system; however, header-less files may be easier for external tools to use.

- d If you want to export a range of data and/or selected bus/signal data, uncheck All Data.
- e To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.

| Range Prope      | erties               |       |              |
|------------------|----------------------|-------|--------------|
| Data Range       | Bus/Signal Selection |       |              |
| O <u>A</u> II    |                      |       |              |
| <u>◯ T</u> ime   | from: -873.81333 us  | to:   | 1.2233387 ms |
| ⊙ <u>M</u> arker | from: M1             | v to: | M2 🔽         |
|                  |                      |       |              |
|                  |                      |       |              |
|                  |                      |       |              |
|                  |                      |       |              |
|                  |                      | ОК    | Cancel Help  |

**f** To select certain bus/signal data to export, click **Bus Signal Selection...** In the Bus/Signal Selection tab of the Range Properties dialog, select the buses/signals whose data you want to export; then, click **OK**.

| Range Properties   |          | ×                         |
|--|----------|---------------------------|
| Data Range Bus/Signal Selection  My 16950A-1  # Sample Number My Bus 1  © Time |          | Select All<br>Select None |
|  | OK Cance | I Help                    |

- 4 Click Save.
- See Also Module Binary (ALB) Format (see page 598)

## To export data to 16700 ASCII format files

You can export captured data to a text file that matches the output of the 16700 logic analysis system's "Print to File" format.

- 1 From the menu bar, select File>Export....
- 2 In the Export dialog, select 16700 ASCII File Format; then, click OK.

| 🔆 Export  | N 1997   |
|---|--|
| Select the file type to export:<br>Module CSV text file<br>Module binary file<br>Standard CSV text file<br>Pattern Generator CSV text file<br>15700 ASCII File Format | Description<br>(".txt) Export listing data to a text file that<br>matches the output of the 16700 Print to<br>File format. |
| ОК  | Help Cancel  |

**3** In the following Export dialog:

#### **6** Capturing Data from the Device Under Test

| Export                |                                 | ? 🛛          |
|-----------------------|---------------------------------|--------------|
| Savejn: 🚞             | Export Files 💽 🕝 🦻              | ⊳ 🖽          |
| 🗐 16700_asci          | i.txt                           |              |
|                       |                                 |              |
|                       |                                 |              |
|                       |                                 |              |
|                       |                                 |              |
|                       |                                 |              |
| File <u>n</u> ame:    | 16700_ascii.txt 💌 🔳             | <u>S</u> ave |
| Save as <u>t</u> ype: | Text files (*.txt)              | Cancel       |
| Source:               | Listing-1                       |              |
| File Options          |                                 |              |
| All Data              | Data Range Bus Signal Selection |              |
|                       |                                 | Help         |
|                       |                                 |              |

a Enter the 16700 ASCII text file name.

CAUTION When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

- **b** Select the **Source** Listing display window from which to export data.
- c If you want to export a range of data, uncheck All Data.
- **d** To specify a range of data to export, click **Data Range...**. In the Data Range tab of the Range Properties dialog, select the range by time or by markers; then, click **OK**.

| Range Properties |                      |    |     |              |
|------------------|----------------------|----|-----|--------------|
| Data Range       | Bus/Signal Selection |    |     |              |
| O <u>A</u> II    |                      |    |     |              |
| <u>◯ T</u> ime   | from: -873.81333 us  |    | to: | 1.2233387 ms |
| ⊙ <u>M</u> arker | from: M1             | *  | ţo: | M2           |
|                  |                      |    |     |              |
|                  |                      |    |     |              |
|                  |                      |    |     |              |
|                  |                      |    |     |              |
|                  |                      | OK |     | Cancel Help  |

4 Click Save.

# **Extending Capture Capability with VBA**

With the integrated Microsoft Visual Basic for Applications (VBA), you can extend the data capture capabilities of the logic analyzer. For example:

- In the case that the logic analyzer isn't able to trigger on the event of interest, VBA can be used to do a run, analyze the captured data looking for the event and if not found, run again. For events that are relatively frequent, this allows the logic analyzer to find events that are too complex to be able to define a trigger.
- In situations where you need a lot of data to find an elusive fault, you can set up the logic analyzer to repetitively run and save data.
- You can create dynamic triggers between repetitive runs by performing a run, modifying the trigger based on analysis of the captured data, and then running again.

These are all things you could previously do with the logic analyzer's COM automation capabilities; however, it's easier and more convenient now that VBA is integrated with the *Agilent Logic Analyzer* application.

**See Also** • "Using the Advanced Customization Environment (ACE)" (in the online help)

# Capturing Data from the Device Under Test

Agilent Logic and Protocol Analyzer Online Help

# Analyzing the Captured Data

- Offline Analysis (see page 233) (after Loading Saved Data and Setups (see page 220))
- Analyzing Waveform Data (see page 239)
- Analyzing Listing Data (see page 259)
- Displaying Names (Symbols) for Bus/Signal Values (see page 269)
- Marking, and Measuring Between, Data Points (see page 271)
- Searching the Captured Data (see page 294)
- Comparing Captured Data to Reference Data (see page 305)
- Viewing Source Code Associated with Captured Data (see page 308)
- Analyzing Packet Data (see page 316)
- Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)
- Setting the System Trigger and Skew Between Modules (see page 351)
- Using Display Windows (see page 353)
- Printing Captured Data (see page 354)
- Extending Data Visualization/Analysis with VBA (see page 357)



# **Loading Saved Data and Setups**

You can set up the logic analyzer and load data by opening previously saved configuration files. This lets you return to the stopping point of a previous logic analysis session, load previously saved data for *offline analysis*, or just load saved logic analyzer setups. When opening configuration files that contain data, you can choose to load only the logic analyzer setup (that is, without the data).

You can import 167xx fast binary data for *offline analysis* of data captured on 16700-series logic analyzers.

- To open a configuration file (see page 220)
- To recall a recently used configuration file (see page 222)
- To import 167xx fast binary data (see page 223)
- To transfer module setups to/from multi-module systems (see page 224)
- To set up multiple-modules with XML-format configurations (see page 224)
- Using Data Import Modules (see page 227)
  - To create a data import module (see page 227)
  - To edit data import module bus/signal definitions (see page 229)
  - To view data import module file information (see page 231)
  - To re-read data import module files (see page 232)
- **See Also** Offline Analysis (see page 233)

#### To open a configuration file

You can open configuration files to return to a previous logic analysis session, to load previously saved data for *offline analysis*, or to load saved logic analyzer setups.

NOTE

To avoid *pod truncation* (see page 791) when opening configuration files for offline analysis, open the configuration file in a second instance of the *Agilent Logic Analyzer* application (which runs in *Offline* mode).

A quick way to start the *Agilent Logic Analyzer* application and open a configuration file is by double-clicking an ALA format configuration file in Windows Explorer. (An association for the .ala file extension was set up when the application was installed.) When you do this, however, there are no options for partial loading (setup only, modules only, etc.).

To open a configuration file from within the *Agilent Logic Analyzer* application:

1 From the menu bar, select File>Open... or select the icon in the standard toolbar (see page 453).

| pen  |                           |                |  | ?            |
|--|---------------------------|----------------|--|--------------|
| Look in: 🔁   | My Documents              | •              | + 🗈  | -111 *       |
| Motorola F<br>Config.ala<br>data.ala<br>default.ala<br>ModifiedCo<br>mpc860syn | onfig.ala                 | ault Configs   | ⊯ <mark>mpc860:</mark><br>■ project1<br>■ screens.<br>■ test.ala |              |
| •  |                           |                |  | Þ            |
| File name:   | mpc860sym_trig.ala        |                |  | Open         |
| Files of type:   | Logic Analyzer Configurat | ion (*.ala)    | •  | Cancel       |
| -File Header I   | nformation                |                |  |              |
| Content:   | Logic Analyzer Configurat | ion (With Data | )  |              |
| Date:  | Jun 13, 2003 15:13:18     | Version:       | 02.00.038  | 8-f_mtxdev_m |
| Owner:   |                           | Project:       |  |              |
| Description:   |                           |                |  | *<br>*       |
| -File Options -  |                           |                |  |              |
| Setup/Data   |                           | Тос            | ls/Viewers   |              |
| 🔿 All Data   | and Setup                 | ۲              | Include To   | ols/Viewers  |
| Setup Or   | nly                       | C              | Modules O  | nly          |
|  |                           |                |  |              |

The file browser portion of the Open dialog behaves the same as other standard Windows file browser dialogs (that is, you can rename files, use right-mouse operations, etc.).

2 Select the type of configuration file you wish to open (either \*.ala or \*.xml).

For information on when ALA (\*.ala) and XML (\*.xml) formats are used, see ALA vs. XML, When to Use Each Format (see page 445).

3 Select the name of the configuration file you wish to open.

The **Content**, **Date**, **Version**, **Owner**, **Project**, and **Description** fields show information about the selected configuration file. The file was created with the *Agilent Logic Analyzer* version shown in the **Version** field. The **Date** field displays the date the configuration file was created.

- 4 Select the appropriate Setup/Data option.
  - Select All Data and Setup to load the logic analyzer setup and data.
  - Select Setup Only to load only the logic analyzer setup.

- **5** Select the appropriate Tools/Viewers option.
  - Select **Include Tools/Viewers** to load tools and viewers, as well as modules, from the configuration file.
  - Select **Modules Only** to load only the module information from the configuration file.
- 6 Select Open.

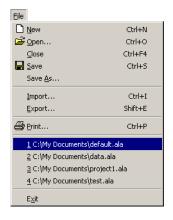
# **NOTE** If you are using the logic analyzer without a keyboard, you can access an on-screen keyboard by selecting **Start>Programs>Accessories>Accessibility>On-Screen Keyboard**.

| See Also | ٠ | То | recall | a | recently | used | configuration | file | (see | page | 222 | ) |
|----------|---|----|--------|---|----------|------|---------------|------|------|------|-----|---|
|----------|---|----|--------|---|----------|------|---------------|------|------|------|-----|---|

- To save a configuration file (see page 206)
- To transfer module setups to/from multi-module systems (see page 224)
- Offline Analysis (see page 233)
- ALA vs. XML, When to Use Each Format (see page 445)
- ALA Format (see page 588)
- "XML Format" (in the online help)

### To recall a recently used configuration file

- 1 From the menu bar, select File.
- 2 Select the configuration file you wish to open from the list provided.



# To import 167xx fast binary data

#### NOTE

Copy 167xx Fast Binary Files to the local hard disk before importing them. Performance of the *Agilent Logic Analyzer* application is much better when fast binary data files are on the local hard disk than when they are on the network.

- 1 From the menu bar, select File>Import....
- 2 In the Import dialog, select 16700 Fast Binary Data, and click OK.

| Select the file type to import<br>Select the file type to import:<br>Module DSV text file<br>Module binary file<br>Pattern Generator CSV text file<br>Pattern Generator Binary file<br>16700 Fast Binary Data<br>Licensed Pattern Generator file | Description<br>Fast Binary Data from 167xx Logic<br>Analysis System. The application<br>will be taken offline before import<br>proceeds. |
|--|--|
| ОК Н   | elp Cancel   |

**3** In the next Import dialog, select or enter the **File name** of the 167xx fast binary data file you wish to import.

| Import   |   |  | ? ×    |
|--|---|--|--------|
| Look in: 🔁                                       | Config Files  | 💌 🖛 🔁  | -* 🎟 - |
| B4655A_de<br>expanded_<br>DtoA_Shor<br>860demo.f | pg_q.csv~<br>tDemo.data<br><mark>bo</mark>  | xml_with_data01o   | v      |
| config_mtx                                       | data01of01.mfb<br>33_data01of02.mfb<br>33_data02of02.mfb<br>tDemoD_data01of01.mfb | ) 1_pod_8M.pgb<br>6_pods_1M.pgb<br>6_pods_4K.pgb<br>alabel_example_2.p | gb     |
| •  |   |  | Þ      |
| File name:                                       | 860demo.fbo   | ▼ ■  | Open   |
| Files of type:                                   | 167xx Fast Binary Files (*.*)   | <b>•</b>   | Cancel |
| Destination:                                     |   | -  |        |

4 Click Open.

Bus/signal names from a 16700-series logic analyzer fast binary data file are organized into a hierarchy of folders based on the module, analyzer, and bus/signal names.

See Also

- Analyzing 16700-Series Logic Analyzer Data (see page 234)
- 16700 Pod and Bit Association in Offline Analysis (see page 235)
- Offline Analysis (see page 233)

## To transfer module setups to/from multi-module systems

You can move logic analyzer setups from one logic analysis system to another by saving/opening setups to/from configuration files. When systems have multiple modules, you must map which module setup from the configuration file gets loaded into which module in the logic analysis system.

- **1** Make sure the setup (configuration file) you want to load is in the proper format:
  - If the modules are compatible (for example, in the same or similar logic analyzer families like the 16740/41/42A and 16750/51/52A/B), you can use ALA format configuration files to move a setup from one module to another.
  - If the modules are not compatible, you must use XML format configuration files to move a setup from one module to another.
- **2** Open the configuration file (see To open a configuration file (see page 220)).
- 3 Answer the question about clearing all modules before loading.
- 4 In the Module Mapping dialog (see page 517), select Manually specify module mapping; then, click Specify Mapping....
- **5** In the Specify Mapping dialog (see page 540), for the module you want load the setup into, select the module setup from the configuration file to load.
- 6 Click OK to close the Specify Mapping dialog.
- 7 Click OK to close the Module Mapping dialog and load the setup.

When loading module setups from XML format configuration files, an information dialog describes any parsing errors or warnings.

- **See Also** To save a configuration file (see page 206)
  - To open a configuration file (see page 220)
  - ALA vs. XML, When to Use Each Format (see page 445)

#### To set up multiple-modules with XML-format configurations

Included with the *Agilent Logic Analyzer* application is the Large System Setup utility program which makes it easy to set up large, multiple-module logic analysis systems using XML-format configuration files. For example, if your logic analysis system has several logic analyzer modules, each probing the same kind of bus, you can use the Large System Setup utility to set up each module with the same XML-format configuration file. (Doing the same thing in the main application requires many time-consuming steps.) The Large System Setup utility program can also be used in *offline* mode. In this case, you can add as many logic analyzer modules as desired and specify XML-format configurations for each.

To use the Large System Setup utility program:

- 1 If the *Agilent Logic Analyzer* application hasn't already been started, start it, and connect to the logic analysis system you want to set up, or go offline if you want to set up in *offline* mode.
- 2 From the Windows Start menu, choose Start>All Programs>Agilent Logic Analyzer>Utilities>Large System Setup.

| 🛃 Large System Setup    |           |               |           |           |        | ×           |
|-------------------------|-----------|---------------|-----------|-----------|--------|-------------|
| Module Type             | Num Slots | Module Name   | Load File | File Name |        | File Module |
| 1674x/5x Logic Analyzer | 1         | My 1674x/5x-1 |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
|                         |           |               |           |           |        |             |
| •                       |           |               |           |           |        |             |
| Offline Module Setup    |           |               |           | ОК        | Cancel | Help        |

**3** If you have connected to the logic analysis system you want to set up, go to step 5; otherwise, in offline mode, click **Offline Module Setup...** in the Large System Setup dialog.

| 0 | ffline Module Setup                    |            |                   |    | ×      |
|---|--|------------|-------------------|----|--------|
|   | Module Type<br>1674x/5x Logic Analyzer | Slots<br>1 |                   |    |        |
|   |  |            |                   |    |        |
|   |  |            |                   |    |        |
|   |  |            |                   |    |        |
|   |  |            |                   |    |        |
|   |  |            |                   |    |        |
|   | Add Module Delete Selected             | Module De  | elete All Modules | OK | Cancel |

- **4** In the Offline Module Setup dialog, for each module that you want to add:
  - a Click Add Module....
  - **b** In the Add Module dialog, choose the type of card the module is made up of and the number of cards in the module.

| Add Module       | 2                       | × |
|------------------|-------------------------|---|
| Type of Card:    | 1674x/5x Logic Analyzer |   |
| Number of Cards: | 1 Card                  |   |
| OK               | Cancel                  |   |

c Click OK.

You can delete all or selected modules by clicking **Delete All Modules** or **Delete Selected Module**.

When you are finished adding modules, click **OK** to close the Offline Module Setup dialog.

5 In the Large System Setup dialog, enter the **Module Name** for each module.

(The module name from the XML-format configuration file is not used because the same XML file can be used to set up multiple modules.)

- 6 For each module that you want to configure with an XML-format configuration file, make sure the Load File box is checked, and click **Browse...** to select the configuration file name.
- 7 If the XML-format configuration files contain setups for multiple logic analyzer modules, select the file's module setup you want to use.

|           |                                 | ×                 |
|-----------|---------------------------------|-------------------|
| Load File | File Name                       | File Module       |
| N         | C:\Documents and Setting        | My 16740A-1       |
| N         | C:\Documents and Setting        | My 16750B-1       |
| N         | C:\Documents and Setting        | MPC860 Demo Board |
| N         | C:\Documents and Setting        | My 16950A-1       |
|           | C:\Documents and Setting Browse | My 16950A-1       |

8 Click **OK** to close the Large System Setup dialog and set up the logic analysis system as specified.

#### **Using Data Import Modules**

Data import modules read data from module CSV or module binary (ALB) files and make it available to tools and display windows. Module CSV or module binary (ALB) files can be created by external tools or saved from any module using the main menu's **File>Export...** command.

**NOTE** Data import modules are a licensed feature. You can use data import modules without a license, but the amount of data that can be imported is limited to 16 rows.

- To create a data import module (see page 227)
- To edit data import module bus/signal definitions (see page 229)
- To view data import module file information (see page 231)
- To re-read data import module files (see page 232)

Data import modules (and import file names) are saved with logic analyzer configurations (both ALA and XML format). If a configuration is saved "with data" and then opened again, the import module's data is present, and is not re-read from the import file. If a configuration is saved "without data" (setup only) and opened again, you must re-read the data import module file (see To re-read data import module files (see page 232)).

#### **See Also** • To export data to module CSV format files (see page 210)

- Module CSV Format (see page 589)
- To export data to module binary (ALB) format files (see page 213)
- Module Binary (ALB) Format (see page 598)

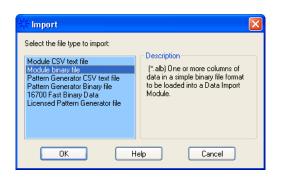
#### To create a data import module

#### NOTE

Copy module CSV or module binary (ALB) files to the local hard disk before importing them. Performance of the *Agilent Logic Analyzer* application is much better when importing files from the local hard disk than when importing them from a network drive.

- 1 From the menu bar, select File>Import....
- 2 In the Import dialog, select Module CSV text file or Module binary file, and click OK.

#### 7 Analyzing the Captured Data

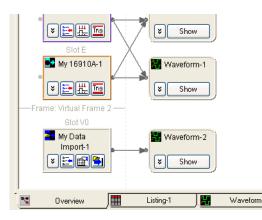


**3** In the following Import dialog:

| Import                 |   |   |     |   |              | ?× |
|------------------------|---|---|-----|---|--------------|----|
| Look jn: 🙋             | Config Files                              | • | 3 🦻 | ø | •            |    |
| isource<br>module.alb  | Default Configs                           |   |     |   |              |    |
| File <u>n</u> ame:     | module.alb                                | • | -   | C | <u>O</u> pen |    |
| Files of <u>t</u> ype: | Module Binary Files (*.alb)               |   | ~   |   | Cance        |    |
| Destination:           | <new data="" import="" module=""> 👻</new> |   |     |   |              |    |

- a Select or enter the File name of the data file you wish to import.
- b Select the Destination of the data file you wish to import. You can choose an existing data import module or "<New Data Import Module>".
- c Click Open.

Data import modules appear in the Overview window like other logic analyzer modules. Because the data does not come from acquisition hardware in a logic analysis system frame, a *virtual* frame is created for data import modules. You can add tools and display windows to data import modules just like you add them to logic analyzer modules.



#### See Also

- To edit data import module bus/signal definitions (see page 229)
- To view data import module file information (see page 231)
- To re-read data import module files (see page 232)
- Module CSV Format (see page 589)
- To export data to module CSV format files (see page 210)
- Module Binary (ALB) Format (see page 598)
- To export data to module binary (ALB) format files (see page 213)

#### To edit data import module bus/signal definitions

- 1 Click in the data import toolbar, or choose **Setup>(Data Import Module)>Bus/Signals...** from the menu bar.
- 2 In the Import Setup dialog's Buses/Signals tab (see page 516):

#### 7 Analyzing the Captured Data

| D               | Channels      |       |    |    |    |    | M  | /ly B | us 3 |      |      |          |    |   |   |   |   |   |   |    |     |     | М | Μ |
|-----------------|---------------|-------|----|----|----|----|----|-------|------|------|------|----------|----|---|---|---|---|---|---|----|-----|-----|---|---|
| Bus/Signal Name | Assigned      | Width | 21 | 20 | 19 | 18 | 17 | 16    | 15   | 14 1 | 3 12 | 11       | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3  | 2 . | 1 0 | 0 | 0 |
| C My Bus 1      | My Bus 1[7:0  | 8     |    |    |    |    |    |       |      |      |      | <u> </u> |    | - | - |   | - | - | - | -  | -   |     | 1 | F |
| 🔿 My Bus 2      | My Bus 2[15:  | 16    |    |    |    |    |    |       |      |      |      |          |    |   |   |   |   |   |   |    |     |     |   | F |
| 🔿 My Bus 3      | My Bus 3[31:  | 32    | 1  | 1  | 1  | 1  | 1  | 1     | 1    | < .  | ' 🗸  | 1        | 1  | 1 | 1 | 1 | ~ | 1 | 1 | √. | 1.  | / / |   | Г |
| Mu Oissen 1.4   | My Signal 1[0 | 1     |    |    |    |    |    |       |      |      |      |          |    |   |   |   |   |   |   |    |     |     | 1 | Г |
| My Signal 1     | My Signar (0  |       |    |    |    |    |    |       |      |      |      |          |    |   |   |   |   |   |   |    |     |     |   |   |
| My Signal 2     | My Signal 2[0 |       | <  |    |    |    |    |       |      |      |      |          |    |   |   |   |   |   |   |    |     |     |   | 1 |

Notice that *pods* are created for data value columns in the imported data file. These are like pods in logic analyzer modules except they can be any bit width.

When editing bus/signal definitions in an import module, you can:

- Add a new bus or signal.
- Delete a bus or signal.
- Rename a bus or signal.
- Assign channels in the default bit order.
- Assign channels, selecting the bit order.
- Reorder bits by editing the Channels Assigned string.
- Set the default number base.
- Set the polarity.
- Add comments.
- Add a folder.
- Alias a bus/signal name.
- Sort bus/signal names.

These operations are just like defining buses and signals in logic analyzer modules (see Defining Buses and Signals (see page 104)).

Through the **Display** button, you can select what bus/signal setup information is displayed (channels assigned, width, polarity, default base, comment, or channel numbers).

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

- **See Also** To view data import module file information (see page 231)
  - To re-read data import module files (see page 232)
  - Module CSV Format (see page 589)

#### To view data import module file information

- 1 Click ☐ in the data import toolbar, or choose Setup>(Data Import Module)>File Info... from the menu bar.
- 2 In the Import Setup dialog's File Information tab (see page 517):

| Buses/Signals     File Information       File name:     C:\Documents and Settings\pw       File     Description = Text (.csv)       Time file was imported = 12/05/2005 03:       Yalue separator = "","       Fill in value = Zeros       Number of rows = 1048576 read       My Bus 1     8       My Bus 2     16       My Bus 3     32       My Bus 1     1                                       | 39:52 PM<br>42:00 PM                                   | Hex<br>Hex  |
|--|--|---|
| Column Name         Width           Column Name         Width           Sample Number         8           My Bus 1         8           My Bus 2         16           My Bus 3         32   | 39:52 PM<br>42:00 PM<br>Type<br>Sample Number<br>Value | Time/Trigger         Sampling period = 2 ns         Trigger row = 524288         Trigger correlation offset = 0 s         Format         r         Signed Decimal         Hex         Hex |
| Column Name         Width           Column Name         Width           Sample Number         8           My Bus 1         8           My Bus 2         16           My Bus 3         32   | 39:52 PM<br>42:00 PM<br>Type<br>Sample Number<br>Value | Time/Trigger         Sampling period = 2 ns         Trigger row = 524288         Trigger correlation offset = 0 s         Format         r         Signed Decimal         Hex         Hex |
| Description = Text (.csv)           Time file was modified = 12/05/2005 03:           Time file was imported = 12/05/2005 03:           Value separator = ";"           Fill in value = Zeros           Number of rows = 1048576 read           Column Name         Width           Sample Number         8           My Bus 1         8           My Bus 2         16           My Bus 3         32 | 42:00 PM<br>Type<br>Sample Number<br>Value             | Sampling period = 2 ns<br>Trigger row = 524288<br>Trigger correlation offset = 0 s<br>Format<br>I Signed Decimal<br>Hex<br>Hex  |
| Time file was modified = 12/05/2005 03:           Time file was imported = 12/05/2005 03:           Value separator = ","           Fill in value = Zeros           Number of rows = 1048576 read           Column Name         Width           Sample Number           My Bus 1         8           My Bus 2         16           My Bus 3         32   | 42:00 PM<br>Type<br>Sample Number<br>Value             | Trigger row = 524288         Trigger correlation offset = 0 s         Format         r         Signed Decimal         Hex         Hex   |
| Sample Number<br>My Bus 1 8<br>My Bus 2 16<br>My Bus 3 32  | Sample Number<br>Value                                 | Signed Decimal<br>Hex<br>Hex  |
| My Bus 1         8           My Bus 2         16           My Bus 3         32   | Value  | Hex<br>Hex  |
| My Bus 2 16<br>My Bus 3 32   |  | Hex   |
| My Bus 3 32  | Value  |   |
|  |  |   |
| MySignal 1 1   | Value  | Hex   |
|  | Value  | Hex   |
| My Signal 2 1  | Value  | Hex   |
| Time   | Time Absolute  | Float Exponent=-12 Scale Factor=1.000000e+000   |
|  |  |   |
|  |  |   |
|  |  |   |
|  |  |   |
|  |  |   |

- The file name and other file information is displayed.
- The time column and trigger row are displayed. The trigger correlation offset is displayed.
- The module data import file's column name, width, type, and format are displayed.
- **See Also** To edit data import module bus/signal definitions (see page 229)
  - To re-read data import module files (see page 232)

|                               | • Module CSV Format (see page 589)  |
|-------------------------------|---|
|                               | To re-read data import module files   |
|                               | When you create a data import module, data is read from the imported<br>file. You can also cause the data import file to be re-read without going<br>through the file selection dialog again. |
| To re-read the                | Do one of the following:  |
| data import file              | • From the menu bar, choose Run/Stop>(Data Import Module)>Read.   |
|                               | • Click the 🔊 icon from the data import toolbar (see page 472) or from the data import module in the Overview window.   |
| To view data<br>import module | • From the menu bar, choose <b>Run/Stop&gt;Status</b> , or click <b>Status</b> in the status bar.   |
| read status                   | The read status is displayed in the System Status tab of the Status dialog (see page 542).  |
| See Also                      | • To view data import module file information (see page 231)  |

# **Offline Analysis**

Offline analysis lets you analyze captured data while the logic analyzer's data acquisition hardware is used for making other measurements.

You can use the *Agilent Logic Analyzer* application on stand-alone personal computers, 16800-series or 1680/1690-series logic analyzers, or 16900-series logic analysis systems to perform offline analysis.

By placing configuration/data files on shared file systems, offline analysis can be performed from remote locations on the network.

**Example:** A typical scenario is to capture data in a 16700-series logic analysis system, load the data file into the *Agilent Logic Analyzer* application for offline analysis, and then continue using the 16700-series logic analysis system to look for the next elusive defect or crash. By analyzing the data offline, you can keep your logic analyzer hardware busy making new measurements while you analyze the last one.

**Example:** Another scenario is to use the *Agilent Logic Analyzer* application to configure and exchange logic analyzer configuration files containing trigger setups with a team of colleagues located on-site or in remote locations.

General offline analysis considerations

- To analyze data from 16700-series logic analyzers, the data must be saved in the fast binary data format. This is done using the File Out Tool (see Analyzing 16700-Series Logic Analyzer Data (see page 234)).
  - When analyzing data offline, there is no data acquisition hardware, so functions such as triggering, hardware assist, and run functions are not available.
  - Multiple instances of the *Agilent Logic Analyzer* application can be displayed side-by-side on a logic analyzer or a personal computer, but their data cannot be time-correlated.
  - You can install the *Agilent Logic Analyzer* on any computer meeting the minimum PC requirements (see page 237); however, licensed tools require a license for each computer they run on.

For more specific information about offline analysis, see:

- Analyzing 16700-Series Logic Analyzer Data (see page 234)
- Offline Analysis on Logic Analyzers (see page 235)
- Offline Analysis on Personal Computers (see page 236)

To return to online analysis, see:

• Connecting to a Logic Analysis System (see page 85)

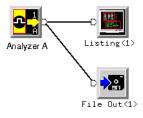
**See Also** • Offline File Formats (see page 237)

# **Analyzing 16700-Series Logic Analyzer Data**

Before you can analyze 16700-series logic analyzer data with the *Agilent Logic Analyzer* application, you must save the measurement data in fast binary out format using the File Out Tool.

The following example shows the general process to use. Refer to the 16700-series logic analysis system online help for any specific information.

- 1 Configure the 16700-series logic analyzer to capture the desired data.
- **2** Connect a File Out Tool.



Data loaded for offline analysis must appear as one data set. Data from a two-machine measurement (as with Pentium 4 processor solution data, for example) must be merged before saving as fast binary output data; in other words, both machines must feed into the same File Out tool.

**3** Configure the File Out tool to save the measurement data in fast binary out format.

For better search performance, limit the size of fast binary data files by using the partial fast binary out option.

**NOTE** If you want the File Out Tool to save the fast binary out file directly to a shared drive, be sure to configure all LAN connections (see page 355) to enable file sharing.

- 4 Run the 16700-series logic analyzer to capture the data.
- **5** Copy the fast binary data file to the local hard disk of the personal computer or logic analyzer on which the *Agilent Logic Analyzer* application runs.

Performance of the *Agilent Logic Analyzer* application is much better when fast binary data files are on the local hard disk than when they are on the network.

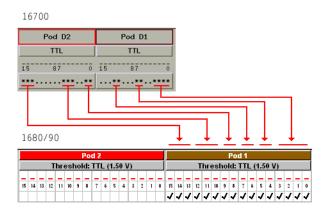
6 In the Agilent Logic Analyzer application, use the File>Import... command to import from the fast binary data (see page 223) file.

More 16700 • Only bus/signal names and measurement data are saved in the fast binary out format.

- The 16700 pod and bit association is collapsed (see page 235) when viewed in the *Agilent Logic Analyzer* application.
- After importing fast binary data files, you cannot use the Bus/Signal Setup dialog to add new bus/signal names or change the channel assignments of the imported bus/signal names. You can, however, change bus/signal polarity, rename or delete buses/signals, and add comments.
- Because 16700-series logic analyzer sampling mode options cannot be used to set up a 1680/1690-, 16800-, or 16900-series logic analyzer, the Timing/State Sampling Mode Setup dialog is not available.
- See Also 16700 Pod/Bit Association in Offline Analysis (see page 235)

#### 16700 Pod and Bit Association in Offline Analysis

The offline analysis application will display the 16700 pod and bit association differently. For any given bus/signal, all assigned bits across all pods in the 16700 interface is converted to sequentially ordered bits under sequentially ordered pods, starting with pod 1.



#### Offline Analysis on Logic Analyzers

You can perform offline analysis with 16800-series, 16850-series, or 1680/1690-series logic analyzers or 16900-series logic analysis systems, in general, by running a second instance of the *Agilent Logic and Protocol Analyzer* application and loading previously saved data into that instance. With two instances of the application running, one in online (either *Local* or *Remote*) mode and one in *Offline* mode, you can continue making measurements in one instance while you perform offline analysis in the other.

You can perform offline analysis on fast binary data files saved from 16700-series logic analyzers as well as configuration files (.ala format) from any 16800-series, 16850-series, or 1680/1690-series logic analyzer or 16900-series logic analysis system.

Keep these things in mind when performing offline analysis with a logic analyzer or logic analysis system:

• You can start multiple instances of the *Agilent Logic Analyzer* application.

If logic analyzer acquisition hardware is present, the first instance opens in online (either *Local* or *Remote*) mode. If acquisition hardware is not present, the first instance opens in *Offline* mode.

- Logic analyzer run functions do not work in Offline mode.
- In the *Offline* mode, you can continue to create triggers and save them in configuration files that can be opened by other instances of the *Agilent Logic Analyzer* application.
- If you import 167xx fast binary data into an online (either *Local* or *Remote*) instance of the *Agilent Logic Analyzer* application, the application automatically switches to *Offline* mode, and all hardware functions are automatically turned off.
- If you open a logic analyzer configuration (.ala) file for offline analysis in an online (either *Local* or *Remote*) instance of the *Agilent Logic Analyzer* application, run functions will overwrite the data that has been loaded.
- **NOTE** To open, copy, or save files directly from shared disk drives, make sure to configure all LAN connections (see page 355) to enable file sharing.
  - **See Also** To open a configuration file (see page 220)
    - To import 167xx fast binary data (see page 223)
    - To save a configuration file (see page 206)

#### **Offline Analysis on Personal Computers**

A personal computer (PC) with the *Agilent Logic Analyzer* application installed can perform offline analysis on fast binary data files saved from a 16700-series logic analyzer as well as configuration files (.ala format) from any 16800-series or 1680/1690-series logic analyzer or 16900-series logic analysis system.

When using the *Agilent Logic Analyzer* application by itself on a PC for offline analysis:

- The logic analyzer run functions are not available (because there is no acquisition hardware).
- You can save logic analyzer setups (including trigger sequences) to .ala format configuration files, and you can pass these files between personal computers (running the *Agilent Logic Analyzer* application) and other 16800-series or 1680/1690-series logic analyzers or 16900-series logic analysis systems.
- You can have more than one instance of the *Agilent Logic Analyzer* application running.
- Licensed tools require a license for each computer they run on.

**NOTE** To open, copy, or save files directly from shared disk drives, make sure to configure all LAN connections (see page 355) to enable file sharing.

- **See Also** To open a configuration file (see page 220)
  - To import 167xx fast binary data (see page 223)
  - To save a configuration file (see page 206)
  - Minimum PC Requirements (see page 237)

#### **Minimum PC Requirements**

Minimum PC requirements for offline analysis:

- Processor and Memory: 1 GHz processor, 512 M RAM.
- Operating System:
  - Windows XP Service Pack 2 and 3.
  - Windows 7 (32/64 bit)
  - Windows 8 (64 bit)
  - Windows Server 2008 (64bit)

#### **Offline File Formats**

**.ala Format** You can open logic analyzer configuration files (.ala (see page 588) extension) for offline analysis. These files are saved by the *Agilent Logic Analyzer* application.

The logic analyzer configuration (.ala) file format is an internal format used by the *Agilent Logic Analyzer* application for saving and re-opening setups and data. ALA format configuration files contain everything that is needed to restore a session (in other words, the information necessary to reconstruct the display appearance, instrument settings, and optionally, captured data).

#### 7 Analyzing the Captured Data

**.xml Format** Generic configuration files (".xml" (in the online help) extension) can be used when setting up the logic analysis system configuration when importing fast binary data format files for offline analysis. XML format configuration files are saved by the *Agilent Logic Analyzer* application.

The generic configuration (.xml) file format is an eXtensible Markup Language format that can be edited (using an ASCII text editor) and post-processed by scripts (or other tools) and re-opened by the *Agilent Logic Analyzer* application. These files contain buses/signals, channels assigned to buses/signals, and user-defined symbols.

- Fast Binary DataYou can import Fast Binary Data Format files (no common file extension)FormatFormatfor offline analysis. These files are created on a 16700-series logic analysissystem using the *File Out* tool. These files contain buses/signals and datafrom the 16700-series logic analyzer.
  - **CSV Format** You can export captured data to CSV (Comma-Separated Values) Format (see page 588) files (.csv extension) for offline analysis in other applications like Excel. These files contain buses/signals and data.

# **Analyzing Waveform Data**

The Waveform window displays captured data as a digital waveform. You can configure the window to display selected buses and signals with time or pattern markers in the data. You can also set up bus pattern triggers and signal trigger options.

| Scale 5 ns/div    |                | Delay 5 ns 📓 📕 🕂 🕇 🍽                  |
|-------------------|----------------|---------------------------------------|
|                   |                | -5 ns 0 s 5 ns 10 ns 15 ns            |
| Bus/Signal        | Simple Trigger |                                       |
| ⊞‡ My Bus 1       | = × XX 🔳       | <u>B2X B3 X B4 X B5 X B6 X B7 X X</u> |
| 🗘 My Signal 1     | X ×            | 1 0 1 0 1 0 1 0 1 0 1 0               |
| ⊞-∯ My Bus 1 (TZ) |                | Х вз ЖХ в4 Х в5 ХХ в6 Х в7 ХХХ        |
| 🗓 My Signal 1 (T. |                |                                       |
| Time              |                | -8.75 ns<br>18.75 ns                  |
|                   |                | -                                     |
|                   | <b>۱</b>       |                                       |
| J                 | J              |                                       |

The Waveform window is accessed through the menu bar's **Window>Waveform** command. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

- To change the display scale (time/division) (see page 240)
- To go to different locations in the captured data (see page 242)
- To re-arrange waveforms (see page 243)
- To overlay waveforms (see page 244)
- To find a bus/signal row (see page 244)
- To view bus data as a chart (see page 245)
- To show/hide parts of the waveform display (see page 247)
- To insert or delete buses/signals (see page 247)
- To group signals into a bus (see page 248)
- To expand/collapse buses (see page 248)
- To insert separator rows (see page 248)
- Changing Waveform Window Properties (see page 249)
  - To change the waveform background color (see page 250)
  - To change the overlaid waveform color (see page 250)
  - To change the filtered data color (see page 250)
  - To change the timing zoom background color (see page 251)
  - To change the waveform font size (see page 251)

- To change the Fast Zoom In option (see page 252)
- To lock scrolling with other display windows (see page 251)
- To change the waveform tool tip display (see page 253)
- Changing Bus/Signal Row Properties (see page 253)
  - To change a waveform's color (see page 254)
  - To change a waveform's height (see page 255)
  - To change a bus/signal's number base (see page 255)
  - To show/hide a bus/signal's numeric data values (see page 255)
- Changing Analog Signal Row Properties (see page 256)
  - To change the analog properties (see page 257)

**See Also** • Defining Buses and Signals (see page 104)

- Setting Up Quick (Draw Box) Triggers (see page 152)
- Specifying Simple Triggers (see page 156)
- Marking, and Measuring Between, Data Points (see page 271)
- Setting Up Symbols (see page 139)
- Displaying Names (Symbols) for Bus/Signal Values (see page 269)
- Searching the Captured Data (see page 294)

### To change the display scale (time/division)

The Waveform window displays data similarly to an oscilloscope, that is, waveforms on a horizontal time axis. Therefore, to zoom in or out on a waveform, you simply change the Scale (time/division) of the time axis that the waveform is viewed with.

To change the scale by clicking the zoom out/in buttons 1 Click the zoom out/in buttons to raise/lower the time/division scale.

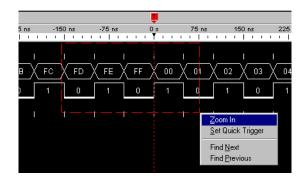
| Scale 5 ns/div |                | Delay  |
|----------------|----------------|--------|
| Bus/Signal     | Simple Trigger | -25    |
| ⊞∰ My Bus 1    | = * 🗙 🖩        | 5CX 51 |

The scale ranges from 1 ps/div to 1 ks/div.

You can also change the time/division by entering a numeric value in the **Scale** field.

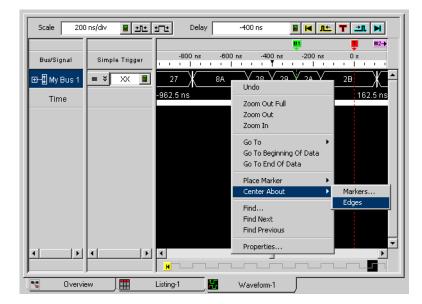
To zoom in by drawing a rectangle in the data

- 1 Point the mouse to the upper-left corner of the desired view area; then, click and hold while moving the mouse to the lower-right corner; then, release the mouse button.
  - 2 If the Fast Zoom In (see page 252) option is not selected, choose Zoom In from the popup menu.



The new display scale is adjusted to the width of the box drawn.

- To center about<br/>edges1Position the mouse cursor over a waveform, between the edges you<br/>want to center the display about.
  - 2 Right-click and choose Center About>Edges.



The new display scale is adjusted to the width of the waveform edges.

#### 7 Analyzing the Captured Data

| Scale 54.5  | 5 ns/div 📕 <b>±∩±</b> | t⊓t  | Delay   | Γ   | -651    | 1.25 | 5 ns    |   | M    | ٦£ | Т  | ' <b>  ⊒</b> | L   I     | H    |
|-------------|-----------------------|------|---------|-----|---------|------|---------|---|------|----|----|--------------|-----------|------|
|             |                       |      |         |     |         |      |         |   |      |    |    |              | ļ         | U2-> |
| Bus/Signal  | Simple Trigger        |      | -760 ns |     | 706 ns  |      | -651 ns |   | -597 | ns | -4 | 542 n:       | 5         |      |
| Busyorginar | Simple Engger         | 1.1  | 1.1.1   | 1.1 | -   - E | 1    | , T i   | 1 | 1.1  | 1  |    |              | 1 1       | - 1  |
| ⊞‡ My Bus 1 | = * XX 🔳              |      |         |     |         |      | 8A      |   |      |    |    |              | $\supset$ | Ľ    |
| Time        |                       | -802 | 5 ns    |     |         |      |         |   |      |    |    | -            | 500       | Ins  |
|             |                       |      |         |     |         |      |         |   |      |    |    |              |           |      |
|             |                       |      |         |     |         |      |         |   |      |    |    |              |           |      |
|             |                       |      |         |     |         |      |         |   |      |    |    |              |           |      |

# To go to different locations in the captured data

Delay |

In the Waveform display window, you can go to different locations in the captured data by using the horizontal scroll bars, by using the Delay field and buttons, or by choosing Go To commands from popup menus.

To go to different locations by changing the delay 1 Click one of the buttons in the Delay field or enter a delay value.

15 ns 📓 🖊 🅂 🕇 斗 🕨

The delay adjusts the display window relative to the waveform data. The display window's relative position in time is dependent on the trigger point, and the beginning and end of data. Use the following delay controls to position the display window over the desired data.

|    | Use the keypad to enter a numeric value. If the value you enter is greater than or less than the time of the data range, the window will be moved to the beginning or end limit. |
|----|--|
| M  | Moves the window over the beginning of data.   |
| ۸t | Scrolls the window towards the beginning of data.  |
| т  | Moves the window over the trigger point.   |
| ±∎ | Scrolls the window towards the end of data.  |
| M  | Moves the window over the end of data.   |

To go to different locations using popup menus 1 Right-click in the waveform display area, and choose one of the **Go To** commands.



Or, click in the marker overview bar, and choose one of the Go To commands.



You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

## To re-arrange waveforms

- 1 Position the mouse pointer over the bus/signal name associated with the waveform you want to move.
- 2 Click and hold the mouse button.
- **3** Drag-and-drop the bus/signal to its new position.

The name is placed above the red position indicator that appears.

- **See Also** To overlay waveforms (see page 244)
  - To expand/collapse buses (see page 248)

NOTE

# To overlay waveforms

Use the Overlay feature to place multiple bus or signals into one row of displayed data. When multiple signals are overlaid, you can see the relationships visually between all signals. The overlaid bus or signal is drawn first, then the main bus/signal is drawn last as to overwrite the overlaid bus/signals for clarity.

| ⊞ <mark>1</mark> My Bus 1                | =, 🛛 🔳 | A RD | FE | RF ) | 00 | an | 012 |
|--|--------|------|----|------|----|----|-----|
| ⊞ <mark>_</mark> My E <mark>u</mark> s 2 | =, 🛛 🔳 |      | 7F |      |    | 00 |     |
| My Signal 1                              | X •    | 1 0  | 1  | 0    | 1  | 0  | 1   |

- 1 Right-click on the bus or signal you want to overlay another bus or signal onto, then select **Overlay...** .
- **2** From the Overlay selection dialog that appears, select the bus or signal you want to overlay onto the highlighted bus or signal.

You can overlay analog signals (from an " external oscilloscope module" (in the online help)) with digital signals or with other analog signals.

The scaling for an original analog signal is used for *all* signals overlaid onto its row; therefore, if user-defined scaling and offset values are used, it is possible that overlaid signals may not be visible. When automatic scaling is used, it will take into account the minimum and maximum voltages of *all* overlaid signals, and all signals will be visible.

3 If you want to change the color of the overlaid bus or digital signal, see To change the overlaid waveform color (see page 250).

When analog signals are overlaid onto other signals, the overlay signal color comes from the external oscilloscope module's setup options (which you can access by right-clicking the analog signal name, choosing **Assign Channels...**, and selecting the " Options tab" (in the online help)) instead of the Waveform window's overlay color setting.

# To find a bus/signal row

When there are many bus/signal rows in the Waveform display window, you can search for a particular bus/signal row instead of scrolling through all the rows.

- 1 In the Waveform display window, right-click in the Bus/Signal column, and choose **Find Bus/Signal...**.
- 2 In the Find Bus/Signal dialog, enter the name (or part of the name) of the bus/signal you wish to find.



- 3 Then, click:
  - Prev to search for the string backward in the bus/signal rows.
  - Next to search for the string forward in the bus/signal rows.
  - Close to close the Find Bus/Signal dialog.

# To view bus data as a chart

Œ

You can view bus data values as a chart instead of the conventional bus shape.

1 In the Waveform display window, right-click on a bus name, and choose View As Chart....

Or, in the Waveform Properties dialog's Row Properties tab, for the **Bus** property, click **View As...** 

| Bus/Signal   |   |  |  |  |  |
|--------------|---|--|--|--|--|
| 🕂 🕻 My Bus 1 | Undo  |  |  |  |  |
|              | Insert Row Before<br>Insert Row After<br>Delete |  |  |  |  |
|              | Expand  |  |  |  |  |
|              | Assign Channels<br>Rename<br>Group into Bus     |  |  |  |  |
|              | Overlay<br>Overlay Remove                       |  |  |  |  |
|              | Symbols   |  |  |  |  |
|              | Find<br>Find Bus/Signal                         |  |  |  |  |
|              | View As Chart                                   |  |  |  |  |
|              | Display<br>Properties                           |  |  |  |  |

2 In the View As dialog, set the following options:

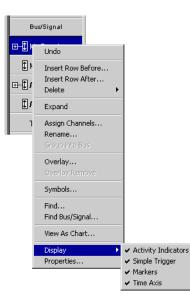
| Yiew As X  |
|--|
| Bus     M58 Ordering     Expand into signals   |
| <ul> <li>Chart</li> <li>✓ Show Axis</li> <li>✓ Connect samples</li> <li>Limits</li> <li>Lock to Setup</li> </ul> |
| Max FF I   |
| Show Clipped   |
| OK Cancel  |

- Show Axis causes a small axis, which represents the center of the range of values being displayed, to be drawn in the center of the waveform. When checked, you can also change the axis color.
- Connect Samples causes lines to be drawn between samples.
- Lock to Setup sets the range limits based on the width of the bus. For example, an 8-bit bus is set to a range of 0-255.
- Max/Min sets the range limits of the displayed axis.
- **Show Clipped** enables out-of-range data values to be displayed in a user-defined color.

| NOTE                         | Because there is no hardware to accelerate chart drawing, Waveform windows that have charts draw slowly. You may want to place buses viewed as charts in a separate Waveform window.  |
|------------------------------|---|
| To view bus data<br>as a bus | <ul><li>You can return the bus waveform appearance to a conventional bus shape.</li><li>1 In the Waveform display window, right-click on a bus name, and choose View As Bus</li></ul> |
|                              | Or, in the Waveform Properties dialog's Row Properties tab, for the <b>Bus</b> property, click <b>View As</b> .   |
|                              | <b>2</b> In the View As dialog, check or uncheck the following options as desired:  |
|                              | • <b>MSB Ordering</b> – the ordering of the signals in the bus are changed from least significant bit first to most significant bit first.  |
|                              | • <b>Expand into signals</b> – expands the bus into individual signals (as if you selected the Expand (+) field to the left of the bus name).   |
| See Also                     | Changing Bus/Signal Row Properties (see page 253)   |

# To show/hide parts of the waveform display

1 Right-click in the Bus/Signal column of the Waveform display, and choose **Display>**.



Then, check or uncheck one of the following to show or hide that part of the Waveform display window:

- Activity Indicators either a low bar (low level), high bar (high level), or a transition arrow (transitioning signal) displayed to the left of bus/signal names.
- Simple Trigger the Simple Trigger column.
- Markers the markers display bar (see page 480).
- **Time Axis** the time axis (and column headings).

You can also make these selections in the **Display Options** area of the Waveform Properties dialog's Window Properties tab.

**See Also** • Changing Waveform Window Properties (see page 249)

#### To insert or delete buses/signals

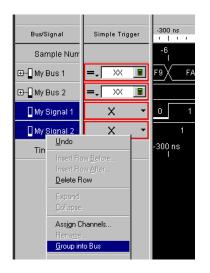
| To insert<br>buses/signals          | 1 | In the Waveform display window, right-click in the Bus/Signal column; then, choose <b>Insert Row</b> .   |
|-------------------------------------|---|--|
|                                     | 2 | In the Insert dialog, select the buses/signals you want to insert; then, click <b>OK</b> .   |
| To delete selected<br>buses/signals | 1 | In the Bus/Signal column, highlight the buses/signals you want to delete (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names). |
|                                     | 2 | Right-click in the Bus/Signal column; then, choose <b>Delete&gt;Row</b> .  |

#### 7 Analyzing the Captured Data

**See Also** • Defining Buses and Signals (see page 104)

#### To group signals into a bus

- 1 While holding the shift key down, click on all desired signals.
- 2 With the mouse pointer over any one of the highlighted signals, right-click and select **Group into Bus**.



#### To expand/collapse buses

In the Waveform display window's Bus/Signal column:

- Click the "+" or "-" symbol associated with a bus.
- Right-click the bus, and choose Expand or Collapse.

**See Also** • Defining Buses and Signals (see page 104)

# To insert separator rows

To add distance between waveforms, you can add separator rows to the Waveform display window.

1 In the Waveform display window, right-click in the Bus/Signal column; then, choose **Insert Separator**.

Separator rows can be sized, colored, re-arranged, and deleted just like bus/signal waveform rows.

# **Changing Waveform Window Properties**

You can change properties that affect the entire Waveform display window.

1 Right-click in a blank area of the waveform display, and choose **Properties...**.

Or, with no bus/signal names selected, choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Window Properties tab:

| Waveform Properties   |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|
| Window Properties Row Properties Column Properties Marker Properties  |  |  |  |  |  |  |  |  |  |
| Color Background V Display Options<br>Font Size 9 • • • Display Activity Indicators<br>V Display Simple Trigger<br>V Display Markers<br>V Display Markers<br>V Display Time Axis<br>Accumulate<br>Fast Zoom In<br>V Show Tooltip Values<br>V Transition Width |  |  |  |  |  |  |  |  |  |
| OK Cancel Apply Help  |  |  |  |  |  |  |  |  |  |

You can:

- Change the waveform background color (see page 250)
- Change the overlaid waveform color (see page 250)
- Change the filtered data color (see page 250)
- Change the timing zoom background color (see page 251)
- Change the waveform font size (see page 251)
- Lock scrolling with other display windows (see page 251)
- Show/hide parts of the waveform display (see page 247)
- Change the accumulate waveforms option (see page 252)
- Change the Fast Zoom In option (see page 252)
- Change the waveform tool tip display (see page 253)
- **3** Click **OK** to apply the changes and close the Waveform Properties dialog.
- See Also Changing Bus/Signal Row Properties (see page 253)

#### To change the waveform background color

1 In the Waveform Properties dialog's Window Properties tab, select the **Background** color, click the selection button, and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### To change the overlaid waveform color

When buses/signals are overlaid (see To overlay waveforms (see page 244)), the overlay property specifies the color used for the overlaid waveforms.

1 In the Waveform Properties dialog's Window Properties tab, select the **Overlay** color, click the selection button, and select the desired overlaid waveform color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### To change the filtered data color

When a filter tool is used to hide data from the Waveform display window, cross-hatching appears at locations where data is hidden; the filter property specifies the color used for the cross-hatched areas.

1 In the Waveform Properties dialog's Window Properties tab, select the **Filter** color, click the selection button, and select the desired filter color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### To change the timing zoom background color

You can give waveforms from the timing zoom feature a different background color than other waveforms.

1 In the Waveform Properties dialog's Window Properties tab, select the **TimingZoom** color, click the selection button, and select the desired timing zoom background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### To change the waveform font size

The font size property adjusts the data display, bus/signal, and simple trigger text size.

1 In the Waveform Properties dialog's Window Properties tab, enter the desired **Font Size**.

Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

As the font size is changed, the row height may be automatically increased to fit the new text size.

#### To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

- 1 In the Waveform Properties dialog's Window Properties tab, click Lockstep Windows....
- **2** In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.

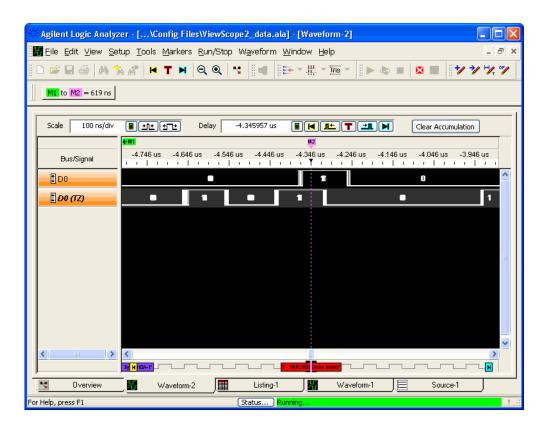
| Lockstep Windows |          |               |     |       |                   | ×            |
|------------------|----------|---------------|-----|-------|-------------------|--------------|
| Lockstep window  | ig - 1 💌 | and offset by | 0 s | ■ - + | from Waveform - 1 | OK<br>Cancel |

- 3 Click OK to close the Lockstep Windows dialog.
- 4 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### To accumulate waveforms

- 1 In the Waveform Properties dialog's Window Properties tab's Display Options area, check or uncheck **Accumulate** to specify whether waveforms are accumulated on the display.
- 2 Click **OK** to apply the changes and close the Waveform Properties dialog.

When the accumulate option is enabled and you run repetitively, waveforms overlay previously captured waveforms.



To clear accumulated waveforms, click **Clear Accumulation** at the top of the Waveform window.

#### To change the Fast Zoom In option

When the Fast Zoom In option is selected, you can drag the mouse cursor over the area you want to zoom in on, and when you release the mouse button, the zoom happens immediately, without having to select **Zoom In** from a popup menu.

- 1 In the Waveform Properties dialog's Window Properties tab, select or deselect the **Fast Zoom In** option.
- 2 Click **OK** to apply the changes and close the Waveform Properties dialog.

#### **See Also** • To change the display scale (time/division) (see page 240)

- To set a Quick Trigger in the Waveform window (see page 152)
- To quickly find bus signal patterns (see page 294)

#### To change the waveform tool tip display

A *tool tip* (that is, a small box with text) can appear when the mouse pointer is over a waveform and held motionless for a second.

1 In the Waveform Properties dialog's Window Properties tab's Display Options area, check or uncheck **Show Tooltip Values** to specify whether bus/signal values are shown as tool tips.

If **Show Tooltip Values** is checked, check or uncheck **Transition Width** to specify whether transition (or pulse) width values are included in the tool tips.

2 Click **OK** to apply the changes and close the Waveform Properties dialog.

# **Changing Bus/Signal Row Properties**

In the Waveform display window, you can change the color or size of a waveform, and you can choose whether numeric values are displayed with the waveform.

# NOTE

Property changes to a bus affect all signals within the bus. For example, if you change the color of a bus and then expand the bus, you will see that the color is changed for all signals in the bus.

To change the properties of a waveform in the Waveform window:

1 Right-click on a bus/signal name or on a waveform, and choose **Properties...**.

Or, highlight the buses/signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Row Properties tab:

| Waveform Properti | es X   |
|-------------------|--|
| Window Properties | Row Properties Column Properties Marker Properties |
| Bus/Signal        | My Bus 1   |
| Color             | •  |
| Height            | 30 🔳 - +   |
| Base              | Hex  |
| 🔽 Show Values     |  |
| Bus               | View As  |
|                   | OK Cancel Apply Help                               |

You can:

- Select the **Bus/Signal** to which the property changes apply. You can select:
  - Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 104)
  - ).
  - **<all>** buses/signals.
  - **<selected>** buses/signals if more than one is highlighted in the Bus/Signal column.
- Change a waveform's color (see page 254)
- Change a waveform's height (see page 255)
- Change a bus/signal's number base (see page 255)
- Show/hide a bus/signal's numeric data values (see page 255)
- View bus data as a chart or a bus (see page 245)
- **3** Click **OK** to apply the changes and close the Waveform Properties dialog.
- **See Also** Changing Waveform Window Properties (see page 249)

#### To change a waveform's color

1 In the Waveform Properties dialog's Row Properties tab, click the **Color** selection button and select the desired waveform color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

- 2 Click **OK** to apply the changes and close the Waveform Properties dialog.
- **See Also** Changing Analog Signal Row Properties (see page 256)

# To change a waveform's height

1 In the Bus/Signal column of the Waveform display window, position the mouse pointer over a row separator line; when the cursor changes to a resizing cursor, drag the row border.

Or:

1 In the Waveform Properties dialog's Row Properties tab, enter the **Height** value in pixels.

The minimum row height is set by the font size (see To change the waveform font size (see page 251)). The maximum height is 1000 pixels.

- 2 Click **OK** to apply the changes and close the Waveform Properties dialog.
- **See Also** Changing Analog Signal Row Properties (see page 256)

#### To change a bus/signal's number base

When a bus/signal's numeric data values are displayed (see To show/hide a bus/signal's numeric data values (see page 255)), the base property specifies the number base to use.

- 1 In the Waveform Properties dialog's Row Properties tab, select the desired number **Base** from:
  - Binary
  - Hex
  - Octal
  - Decimal
  - Signed Decimal (two's complement)
  - Ascii
  - Symbol (see Displaying Names (Symbols) for Bus/Signal Values (see page 269))
- **2** Click **OK** to apply the changes and close the Waveform Properties dialog.

# To show/hide a bus/signal's numeric data values

You can display (and specify the color of) numeric data values with a waveform.

# NOTE

If the waveform time scale is small, "..." may appear in the data value to indicate that more text will be displayed if you expand the scale.

1 In the Waveform Properties dialog's Row Properties tab, check or uncheck **Show Values** to show or hide numeric data values with the waveform.

If **Show Values** is checked, click the color selection button and select the desired data value color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

- 2 Click **OK** to apply the changes and close the Waveform Properties dialog.
- **See Also** Changing Analog Signal Row Properties (see page 256)

# **Changing Analog Signal Row Properties**

In the Waveform display window, you can change the color or size of an analog signal waveform, and you can choose whether voltage and volts/division values are displayed with the waveform. Analog signals come from an external oscilloscope module (see " External Oscilloscope Time Correlation and Data Display" (in the online help)).

To change the properties of an analog signal waveform in the Waveform window:

1 Right-click on an analog signal name or on a waveform, and choose **Properties...**.

Or, highlight the analog signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the analog signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Waveform Properties dialog's Row Properties tab:

| Wavef    | orm Proper   | ties          |                    |                  | ×            |
|----------|--------------|---------------|--------------------|------------------|--------------|
|          | Time Mark    | er Properties | Γ V                | oltage Marker Pr | operties     |
| <u>ا</u> | Window Prope | rties         | Row Properties     | Colum            | n Properties |
| Bu       | s/Signal     | My So         | cope C1            | •                |              |
| Col      | lor          |               | <b> </b> *         |                  |              |
| He       | ight         | 150           | ■ - +              |                  |              |
| ~        | Show Values  |               | <b></b>   <b>*</b> |                  |              |
| Ba       | se           |               | Y                  |                  |              |
| An       | alog         | Pr            | operties           |                  |              |
|          |              |               |                    |                  |              |
|          |              | OK            | Cancel             | Apply            | Help         |

You can:

- Select the **Bus/Signal** to which the property changes apply. You can select:
  - Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 104)).
  - **<all>** buses/signals.
  - **<selected>** buses/signals if more than one is highlighted in the Bus/Signal column.
- Change a waveform's color (see page 254)
- Change a waveform's height (see page 255)
- Show/hide a signal's numeric data values (see page 255)
- Change the analog properties (see page 257)
- **3** Click **OK** to apply the changes and close the Waveform Properties dialog.
- See Also Changing Waveform Window Properties (see page 249)

### To change the analog properties

You can change the properties of an analog signal in the Waveform display window.

- **1** In the Waveform Properties dialog's Row Properties tab, for the **Analog** property, click **Properties...**.
- 2 In the Analog Properties dialog, set the following options:

| Analog Properties      | ×      |  |  |  |  |
|------------------------|--------|--|--|--|--|
| Scaling                | ОК     |  |  |  |  |
| Automatic              | Cancel |  |  |  |  |
| C User Defined         |        |  |  |  |  |
| Scale 602 mV/div 🔳 – + |        |  |  |  |  |
| Offset 2.672 V 🔳 – +   |        |  |  |  |  |
| Grid Style Axis        |        |  |  |  |  |
| Connect Samples        |        |  |  |  |  |
| Show Clipped           |        |  |  |  |  |

- **Scaling** you can select **Automatic** (to have the voltage scale and offset automatically set) or **User Defined** (to be able to set your own voltage scale and offset values). Be careful not to enter scale and offset values that will move the waveform out of the display area.
- Grid Style/Color you can select None, Axis (to have axis lines drawn through the center of the waveform display area), or Grid (to have grid lines drawn for voltage and time divisions). If you choose axis or grid, you can specify its color.

# 7 Analyzing the Captured Data

- **Connect Samples** specifies whether lines are drawn between waveform data sample points.
- **Show Clipped** enables out-of-range data values to be displayed in a user-defined color.

# **Analyzing Listing Data**

The Listing window displays your captured data as a state listing. You configure the window to display selected buses and signals in columns. Within the listed data, you can insert time or pattern markers. You can also configure the bus pattern triggers and signal trigger options.

|      | Sample Number | Bus 1  | Bus 2     | Signal 1 | Signal 2 | Time         |
|------|---------------|--------|-----------|----------|----------|--------------|
|      |               | =, 🛛 🏢 | =, XXXX 🏢 | ⊠ -      |          |              |
|      | -7            | ŁА     | 3889      | 1        | 1        | -350 🔺 🔔     |
|      | -6            | FA     | 3FFA      | 1        | 1        | -300 🗖 🖪     |
| M1   | -5            | FB     | 3FFB      | 1        | 1        | -2.50        |
|      | -4            | FC     | 3FFC      | 1        | 1        | -200         |
|      | -3            | FD     | 3FFD      | 1        | 1        | -150         |
|      | -2            | FE     | 3FFE      | 1        | 1        | -100         |
|      | -1            | FF     | 3 F F F   | 1        | 1        | -50          |
| ∎→   | 0             | 00     | 0000      | 0        | 0        | 0 — I MI     |
|      | 1             | 01     | 0001      | 0        | 0        | 50           |
|      | 2             | 02     | 0002      | 0        | 0        | 100          |
|      | 3             | 03     | 0003      | 0        | 0        | 150          |
|      | 4             | 04     | 0004      | 0        | 0        | 200          |
| M2 - | 5             | 05     | 0005      |          | 0        | 250 4        |
|      | 6             | 06     | 0006      | 0        | 0        | 300 <b>E</b> |
|      | 7             | 07     | 0007      | <u> </u> | <u> </u> | 3.50         |
|      | 4             |        |           |          |          |              |

The Listing window is accessed through the menu bar's **Window>Listing**. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

- To go to different locations in the captured data (see page 260)
- To re-arrange bus/signal columns (see page 261)
- To find a bus/signal column (see page 261)
- To show/hide parts of the listing display (see page 262)
- To insert or delete buses/signals (see page 262)
- Changing Listing Window Properties (see page 263)
  - To change the listing background color (see page 263)
  - To change the timing zoom background color (see page 264)
  - To change the listing font size (see page 264)
  - To lock scrolling with other display windows (see page 264)
  - To show/hide the center rectangle (see page 265)
- Changing Bus/Signal Column Properties (see page 265)
  - To change a bus/signal's data color (see page 266)
  - To change the width of a bus/signal column (see page 266)
  - To change the alignment of a bus/signal column (see page 267)
  - To change a bus/signal's number base (see page 267)
  - To select the marker for marker-relative times (see page 268)

- To select fixed time units (see page 268)
- **See Also** Defining Buses and Signals (see page 104)
  - Setting Up Quick (Draw Box) Triggers (see page 152)
  - Specifying Simple Triggers (see page 156)
  - Marking, and Measuring Between, Data Points (see page 271)
  - Setting Up Symbols (see page 139)

D 🖻 🖬 🎒 🖓 🚀 🖬 🔍 🔍 🤫

- Displaying Names (Symbols) for Bus/Signal Values (see page 269)
- Searching the Captured Data (see page 294)

# To go to different locations in the captured data

In the Listing display window, you can go to different locations in the captured data by using the vertical scroll bars, by using the Go To buttons on the standard toolbar, or by choosing Go To commands from popup menus.

To go to different locations using toolbar buttons **1** Click one of the Go To buttons in the standard toolbar.

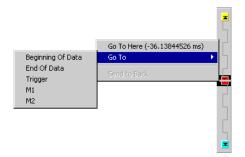
| K  | Go to Beginning — centers the beginning of the acquisition data. |
|--|--|
| <b>T</b> Go to Trigger — centers the trigger point of the acquisition. |  |
| Go to End — centers the end of the acquisition data.                   |  |

To go to different locations using popup menus

**1** Right-click in the waveform display area, and choose one of the **Go To** commands.

| B8                      | 0       |
|-------------------------|---------|
| . 80                    | 0       |
| Undo                    | 1       |
| Go To 🔶 🕨               | Time    |
| Go To Beginning Of Data | Sample  |
| Go To End Of Data       | Trigger |
| Place Marker 🔹 🕨        | M1      |
| Find                    | M2      |
| Find Next               | More    |
| Find Previous           | 1       |
| Properties              | 0       |
| roporcostri             | 0       |

Or, click in the marker overview bar, and choose one of the Go To commands.



You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

# To re-arrange bus/signal columns

- 1 Position the mouse pointer over the bus/signal name associated with the column you want to move.
- 2 Click and hold the mouse button.
- **3** Drag-and-drop the bus/signal to its new position.

The name is placed to the left of the red position indicator that appears.

# To find a bus/signal column

When there are many bus/signal columns in the Listing display window, you can search for a particular bus/signal column instead of scrolling through all the columns.

- 1 In the Listing display window, right-click in any Bus/Signal column heading, and choose **Find Bus/Signal...**.
- 2 In the Find Bus/Signal dialog, enter the name (or part of the name) of the bus/signal you wish to find.

| Find Bus/Signal |      | X     |
|-----------------|------|-------|
| TSIZ            |      |       |
| Prev            | Next | Close |

- 3 Then, click:
  - Prev to search for the string backward in the bus/signal columns.
  - Next to search for the string forward in the bus/signal columns.
  - Close to close the Find Bus/Signal dialog.

# To show/hide parts of the listing display

1 Right-click in the Bus/Signal column heading of the Listing display, and choose **Display>**.

|      | Undo            |                             |
|------|-----------------|-----------------------------|
| 13   | Insert Column   |                             |
| .s   | Delete          |                             |
| s    | Assign Channels |                             |
| IS   |                 | -                           |
| s    |                 |                             |
| IS   |                 | -                           |
| s    | Find            |                             |
| s    | Find Bus/Signal |                             |
| IS   | Display         | Activity Indicators         |
| ıs   | Properties      | Column Base                 |
| IS I |                 | ✓ Simple Trigger            |
| IS   |                 | <ul> <li>Markers</li> </ul> |

Then, check or uncheck one of the following to show or hide that part of the Listing display window:

- Activity Indicators either a low bar (low level), high bar (high level), or a transition arrow (transitioning signal) displayed to the left of bus/signal names.
- Column Base the number base row in the column headings.
- **Simple Trigger** the Simple Trigger row in the column headings (see Specifying Simple Triggers (see page 156)).
- Markers the markers display bar (see page 480).

You can also make these selections in the **Display Options** area of the Listing Properties dialog's Window Properties tab.

See Also • Changing Listing Window Properties (see page 263)

# To insert or delete buses/signals

| To insert<br>buses/signals          | <b>1</b> In the Listing display window, right-click in the Bus/Signal column headings; then, choose <b>Insert Column</b> . |   |
|-------------------------------------|--|---|
|                                     | 2  | In the Insert dialog, select the buses/signals you want to insert; then, click <b>OK</b> .  |
| To delete selected<br>buses/signals | 1  | Highlight the headings of the bus/signal columns you want to delete (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names). |
|                                     | 2  | Right-click in an empty area of the column headings row; then, choose <b>Delete&gt;Column</b> .   |
| To delete all<br>buses/signals      | 1  | Right-click anywhere in the column headings row; then, choose <b>Delete&gt;All Columns</b> .  |
| See Also                            | •  | Defining Buses and Signals (see page 104)   |

# **Changing Listing Window Properties**

You can change properties that affect the entire Listing display window.

1 Right-click in a blank area of the listing display, and choose **Properties...**.

Or, with no bus/signal names selected, choose **Edit>Window Properties...** from the main menu.

2 In the Listing Properties dialog's Window Properties tab:

| l | Listing Properties   |
|---|--|
|   | Window Properties Column Properties Time Marker Properties   |
|   | Background   |
|   | TimingZoom   |
|   | Font Size 10 🗮 - + Display Options   |
|   | Lockstep Windows Display Activity Indicators<br>Display Column Base<br>Display Simple Trigger<br>Display Markers |
|   | OK Cancel Apply Help   |

You can:

- Change the listing background color (see page 263)
- Change the timing zoom background color (see page 264)
- Change the listing font size (see page 264)
- Lock scrolling with other display windows (see page 264)
- Show/hide the center rectangle (see page 265)
- Show/hide parts of the listing display (see page 262)
- 3 Click OK to apply the changes and close the Listing Properties dialog.
- See Also Changing Bus/Signal Column Properties (see page 265)

### To change the listing background color

1 In the Listing Properties dialog's Window Properties tab, click the **Background** color selection button and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Listing Properties dialog.

# To change the timing zoom background color

In the Listing display window, you can give columns from the timing zoom feature a different background color than other bus/signal data columns.

1 In the Listing Properties dialog's Window Properties tab, click the **TimingZoom** color selection button and select the desired timing zoom background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click OK to apply the changes and close the Listing Properties dialog.

## To change the listing font size

The font size property adjusts the data display, bus/signal, and simple trigger text size.

1 In the Listing Properties dialog's Window Properties tab, enter the desired **Font Size**.

Fonts can range from size 6 through 72 points.

2 Click OK to apply the changes and close the Listing Properties dialog.

As the font size is changed, the column width may be automatically increased to fit the new text size.

# To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

- 1 In the Listing Properties dialog's Window Properties tab, click Lockstep Windows....
- **2** In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.

| Lockstep Windows X           |  |          |  |
|------------------------------|--|----------|--|
| Lockstep window Waveform - 1 |  | ting - 1 |  |

- 3 Click OK to close the Lockstep Windows dialog.
- 4 Click OK to apply the changes and close the Listing Properties dialog.

## To show/hide the center rectangle

The center rectangle is the box that is drawn around the one sample displayed at center of the screen.

1 In the Listing Properties dialog's Window Properties tab's Center Rectangle area, check or uncheck **Display Rectangle** to specify whether the center rectangle is shown or hidden.

If **Display Rectangle** is checked, click the color selection button and select the desired center rectangle color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click OK to apply the changes and close the Listing Properties dialog.

# **Changing Bus/Signal Column Properties**

In the Listing display window, you can change the color, width, alignment, or number base of bus/signal data columns.

To change the properties of a bus/signal data column in the Listing window:

1 Right-click on a bus/signal name or on a waveform, and choose **Properties...**.

Or, highlight the buses/signals whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the bus/signal names), and choose **Edit>Window Properties...** from the main menu.

2 In the Listing Properties dialog's Column Properties tab:

| Listing Properties   | 6                        |                   |  |  |  |
|----------------------|--------------------------|-------------------|--|--|--|
| Window Properties    | Column Properties        | Marker Properties |  |  |  |
| Bus/Signal           | My Bus 1                 |                   |  |  |  |
| Color                |                          | ] •               |  |  |  |
| Width                | 113 🔳 — (                | +                 |  |  |  |
| Alignment            | Right                    | ×                 |  |  |  |
| Base                 | Hex                      | ×                 |  |  |  |
| Time Column Op       | tions                    |                   |  |  |  |
| Marker               | Marker Beginning Of Data |                   |  |  |  |
| Use Fixed Unit       |                          |                   |  |  |  |
| OK Cancel Apply Help |                          |                   |  |  |  |

You can:

• Select the **Bus/Signal** to which the property changes apply. You can select:

- Any bus/signal name that has been assigned (see Defining Buses and Signals (see page 104)).
- **<all>** buses/signals.
- **<selected>** buses/signals if more than one column is highlighted.
- Change a bus/signal's data color (see page 266)
- Change the width of a bus/signal column (see page 266)
- Change the alignment of a bus/signal column (see page 267)
- Change a bus/signal's number base (see page 267)
- Select the marker for marker-relative times (see page 268)
- Select fixed time units (see page 268)
- 3 Click OK to apply the changes and close the Listing Properties dialog.
- See Also Changing Listing Window Properties (see page 263)

## To change a bus/signal's data color

1 In the Listing Properties dialog's Column Properties tab, click the **Color** selection button and select the desired bus/signal data color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click OK to apply the changes and close the Listing Properties dialog.

## To change the width of a bus/signal column

TIP You can autosize individual columns by placing the mouse pointer over the right border of the column header box; then, when the pointer icon changes to a resizing pointer,

# TIP

If your keyboard has a numeric keypad, you can autosize all columns by selecting any column header box (to highlight it) and by pressing **Ctrl** and "+" on the numeric keypad.

1 In the bus/signal headings row of the listing display window, position the mouse pointer over a column separator line; when the cursor changes to a resizing cursor, drag the column border.

Or:

double-click.

1 In the Listing Properties dialog's Column Properties tab, enter the **Width** value in pixels.

The minimum column width is 1 pixel, while the maximum width is 1000 pixels.

2 Click OK to apply the changes and close the Listing Properties dialog.

## To change the alignment of a bus/signal column

The Alignment property sets the display of data to be left-justified, right-justified, or centered within the column.

- 1 In the Listing Properties dialog's Column Properties tab, select the **Alignment** from:
  - Left
  - Center
  - Right
- 2 Click OK to apply the changes and close the Listing Properties dialog.

## To change a bus/signal's number base

The base property specifies the number base to use when displaying the captured data.

- 1 In the Listing Properties dialog's Column Properties tab, select the desired number **Base** from:
  - Binary
  - Hex
  - Octal
  - Decimal
  - Signed Decimal (two's complement)
  - Ascii
  - Symbol (see Displaying Names (Symbols) for Bus/Signal Values (see page 269))

### NOTE

If the **Time** column has been selected instead of a data column, your choices change from a numeric format to **Absolute**, **Relative Previous**, or **Relative Marker**.

**NOTE** If an analog signal from an external oscilloscope module (see "External Oscilloscope Time Correlation and Data Display" (in the online help)) column has been selected instead of a data column, **Voltage** is the only choice for number base.

2 Click OK to apply the changes and close the Listing Properties dialog.

# To select the marker for marker-relative times

In the Listing window, you can display times relative to a marker.

- 1 In the Listing Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
- 2 For the Base property, select Relative Marker.
- **3** For the **Marker** property, select the marker to which relative times should be displayed.
- 4 Click OK to apply the changes and close the Listing Properties dialog.

# To select fixed time units

In the Listing window, you can display time column values with a fixed unit.

- 1 In the Listing Properties dialog's Column Properties tab, use the **Bus/Signal** selection to select the **Time** column.
- 2 In the Time Column Properties box, check Use Fixed Unit; then, select the desired time unit from the drop-down list.
- 3 Click OK to apply the changes and close the Listing Properties dialog.

# **Displaying Names (Symbols) for Bus/Signal Values**

You can display a bus or signal using meaningful names rather than numeric values.

Symbols can be displayed in Waveform, Listing, Compare, and Source windows.

To display symbols:

- 1 Set up the symbols (see page 139).
- 2 Change the number base (see page 267) of the bus or signal to Symbols.

|      | _  |
|------|--|
| Data |  |
| =.×  | Undo   |
|      | Insert Column Before<br>Insert Column After<br>Delete Column |
|      | Assign Channels<br>Rename                                    |
|      | Symbols  |
|      | Find<br>Find Next<br>Find Previous                           |
|      | Display  |
|      | Properties   |

| Listing Properties | ×   |
|--------------------|---|
| Window Properties  | Column Properties Marker Properties                 |
| Bus/Signal         | Data  |
| Color              |   |
| Width              | a<br>a  |
| Alignment          | Right   |
| Base               | Hex   |
| Marker             | Binary<br>Hex<br>Octal<br>Decimal<br>Signed Decimal |
|                    | Ascii<br>Symbol Help                                |

If the symbol is defined as a range, values in the range will be displayed with an offset from the lowest end of the range.

If the definitions of several symbols overlap, the first one listed in the Symbols dialog has precedence over the others.

In the Waveform display, "..." will be shown when the full name of the symbol will not fit into the space available.

Once you have set up symbols, it's usually a good idea to save (see page 206) the logic analyzer configuration. The symbol definitions will be stored as part of the configuration.

**Example** Here is what "My Bus 1" looks like before defining any symbols:



When the symbols have been defined, they are shown in the Symbols dialog:



Here is what the bus looks like after the symbols are defined:



# Marking, and Measuring Between, Data Points

Once a marker is created, you can use it as a reference point in the data when measuring intervals or viewing the data value at the marker.

- To read the markers display and overview bars (see page 272)
- To create new markers (see page 272)
- To place markers in data (see page 274)
- To go to a marker (see page 276)
- To center the display about a marker pair (see page 277)
- To change a marker's snap to edge setting (see page 277)
- To delete a marker (see page 278)
- To create a new time interval measurement (see page 279)
- To create a new sample interval measurement (see page 280)
- To create a new value at measurement (see page 282)
- To rename a marker (see page 282)
- To send a marker to the back (see page 283)
- Changing Marker Properties (see page 284)
  - To change a marker's background color (see page 285)
  - To change a marker's foreground color (see page 285)
  - To hide/show a marker (see page 285)
  - To change a marker's lock in viewer setting (see page 285)
  - To lock a marker relative to another marker (see page 286)
  - To add comments to a marker (see page 286)
- Using Voltage Markers for Analog Signals (in the Waveform Display) (see page 286)
  - To create new voltage markers (see page 287)
  - To place voltage markers (see page 288)
  - To delete voltage markers (see page 289)
  - To create a new voltage interval measurement (see page 290)
  - To rename a voltage marker (see page 291)
  - To send a voltage marker to the back (see page 291)
  - To change voltage marker properties (see page 292)
- **See Also** Markers Display Bar (see page 480)
  - Marker Measurement Display Bar (see page 475)
  - Markers Menu (see page 460)

• Markers Toolbar (see page 472)

# Arrows point to markers relative to display region Color matching bars show location relative to data set

# To read the markers display and overview bars

In the upper markers display bar (see page 480), markers are color coded and displayed with arrows that point to the marker's location relative to the displayed data.

In the lower markers overview bar (see page 481), markers are displayed as color coded bars that show the location relative to the complete captured data set.

In the Waveform window (as shown above), the markers display and overview bars appear on the top and bottom of the window. In the Listing window, the markers display and overview bars appear on the left and right sides of the window in a similar way.

You can quickly display a different region of data by clicking on the markers overview bar at the bottom (waveform) or right side (listing) and selecting **Go To Here** from the popup menu.

# To create new markers

TIP

When creating a new marker, you can give it a name, specify its color, position it in the data, and add comments. Up to 1024 markers can be created.

- 1 From the menu bar, select Markers>New....
- 2 In the New Marker dialog, enter the marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the marker display bar (see page 480) while the long name appears in the marker *tool tip* (see page 795).

| New Marker                  | ×        |
|-----------------------------|----------|
| Name M5                     | OK       |
| Background Color            | Cancel   |
| Foreground Color            |          |
| Position                    |          |
| Time 💌 685 ns 🔳 - + from Tr | rigger 💌 |
| Comments                    |          |
|                             |          |
|                             |          |

- 3 Select the marker's background and foreground colors.
- **4** Specify the position of the new marker in the data by:
  - **Time** positions the marker by a time value from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
  - **Sample** positions the marker by a number of samples from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
  - **Value** positions the marker at an occurrence of a bus/signal pattern. Click **Occurs...** to specify the bus/signal pattern value.

Bus/signal pattern specification is the same as when searching the captured data (see page 294).

**5** Enter comments for the marker.

Comments appear in the marker's tool tip (see page 795).

- 6 Click OK.
- **See Also** To place markers in data (see page 274)
  - To go to a marker (see page 276)
  - To read the markers display and overview bars (see page 272)
  - To center the display about a marker pair (see page 277)
  - To delete a marker (see page 278)
  - To rename a marker (see page 282)
  - To send a marker to the back (see page 283)
  - To change a marker's snap to edge setting (see page 277)
  - Changing Marker Properties (see page 284)

# To place markers in data

Use Place Markers to quickly position a marker in the data. Depending on how you access the Place Markers feature, the marker is placed in the data a little differently. You can also move markers by dragging them with the mouse or by using the front-panel knobs.

**NOTE** An enabled **Snap to Edge** property affects a marker's placement in the Waveform window if the mouse cursor is over a waveform when dragging and dropping or when placing at the mouse cursor.

|                                     | • To drag and drop markers in data (see page 274)   |
|-------------------------------------|---|
|                                     | • To place marker at the mouse cursor (see page 274)  |
|                                     | • To place marker at center screen (see page 274)   |
|                                     | • To change a marker's position property (see page 275)   |
|                                     | • You can also place markers where data is found when searching (see To specify "found" marker placement (see page 304)).   |
| To drag and drop<br>markers in data | Using the drag and drop feature you can move markers to new positions in the data.  |
|                                     | 1 Click and hold down the mouse button on the marker you wish to move.  |
|                                     | <b>2</b> Move the mouse cursor to the new position.   |
|                                     | When moving a marker in the Waveform display window, if the mouse<br>cursor is over a waveform and the marker's <b>Snap to Edge</b> property is<br>enabled, the cursor changes to a green "direction arrow" indicating the<br>direction of the next valid edge. A yellow "cross hair" target is placed<br>on the edge at which the marker will be placed if you decide to release<br>the mouse button. If you don't want the marker to snap to an edge,<br>move the mouse cursor so that it is not over any waveforms before<br>releasing the mouse button. |
|                                     | <b>3</b> Release the mouse button to reposition the marker.   |
| To place marker                     | <b>1</b> Point the mouse to the desired data point in the display.  |
| at the mouse<br>cursor              | 2 Right-click, and select Place Marker>Time>(desired marker).   |
|                                     | If the mouse cursor is over a waveform and the marker's <b>Snap to Edge</b> property is enabled, the marker is placed at nearest waveform edge; otherwise, the marker is placed at the mouse cursor location.   |
| To place marker                     | 1 From the menu bar click Markers>Place On Screen   |
| at center screen                    | 2 In the Place Marker dialog, select the desired marker.  |
|                                     |   |

| Name                  | Position   | Comment             |  |
|-----------------------|------------|---------------------|--|
| <new marker=""></new> |            | Create a new marker |  |
| M1                    | -1.402 us  |                     |  |
| 42                    | 2.926 us   |                     |  |
| 43                    | -12.422 ns |                     |  |
| v14                   | 9.688 ns   |                     |  |
|                       |            |                     |  |
|                       |            |                     |  |
|                       |            |                     |  |
|                       |            |                     |  |
|                       |            |                     |  |
|                       |            |                     |  |

You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click OK.

The marker will be placed at mid-screen.

To change a marker's position property

1 Right-click on a marker, and choose **Properties...**.

Or, when viewing a display window that has markers, choose **Markers>Properties...** from the main menu.

- 2 In the display window properties dialog's Time Marker Properties tab, select the **Marker** to which the property changes apply.
- 3 In the **Position** box, select what to position the marker by:
  - **Time** positions the marker by a time value from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
  - **Sample** positions the marker by a number of samples from a reference point. Reference points are the Trigger, Beginning of Data, End of Data, or another marker.
  - **Value** positions the marker at an occurrence of a bus/signal pattern. Click **Occurs...** to specify the bus/signal pattern value.

Bus/signal pattern specification is the same as when searching the captured data (see page 294), except you can click **Properties...** to open the Value Properties dialog. In the Value Properties dialog:

- Check **Stop repetitive run** if you want to stop a repetitive run when the specified bus/signal pattern is found (or not found).
- Check **Send e-mail** if you want to send an e-mail when the specified bus/signal pattern is found (or not found); then, click the **E-mail...** button. In the E-mail dialog (see page 504), enter the address to which e-mail will be sent, the subject, and the text of the message.
- 4 Click OK to apply the changes and close the properties dialog.

## 7 Analyzing the Captured Data

- **See Also** To specify "found" marker placement (see page 304) (for placing markers where data is found)
  - To create new markers (see page 272)
  - To go to a marker (see page 276)
  - To read the markers display and overview bars (see page 272)
  - To center the display about a marker pair (see page 277)
  - To delete a marker (see page 278)
  - To rename a marker (see page 282)
  - To send a marker to the back (see page 283)
  - To change a marker's snap to edge setting (see page 277)
  - Changing Marker Properties (see page 284)

# To go to a marker

To quickly find a previously set marker in the data, or to go to the beginning of data, end of data, or the trigger point:

• Click in the markers display bar (see page 480) or the markers overview bar (see page 481), and choose **Go To** from the popup menu.

Or:

- 1 From the menu bar, select Markers>Go To... or select the *i* icon in the markers toolbar (see page 472).
- 2 In the Go To Marker dialog, select the marker you wish to find from the list provided.

| Name              | Position     | Comment |  |
|-------------------|--------------|---------|--|
| Beginning Of Data | -20.732582   |         |  |
| End Of Data       | 20.665746 ms |         |  |
| Trigger           | 0 s          |         |  |
| M1                | -1.402 us    |         |  |
| M2                | 2.926 us     |         |  |
| M3                | -12.422 ns   |         |  |
| M4                | 9.688 ns     |         |  |
|                   |              |         |  |
|                   |              |         |  |
|                   |              |         |  |
|                   |              |         |  |

You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

3 Click OK.

The selected marker appears at the center of the display.

**See Also** • To create new markers (see page 272)

- To place markers in data (see page 274)
- To center the display about a marker pair (see page 277)
- To delete a marker (see page 278)
- To rename a marker (see page 282)
- To send a marker to the back (see page 283)
- To change a marker's snap to edge setting (see page 277)
- Changing Marker Properties (see page 284)

# To center the display about a marker pair

Use the center about feature to center the display around a selected marker pair. If the marker pair is separated by a large time or sample amount, the scale of the display is automatically changed so both markers appear on screen.

Since the center about feature centers the display around a pair (two) markers, if you have three or more markers defined, you will have available choices for all possible combinations of two.

- 1 From the menu bar, select Markers>Center About....
- 2 In the Center About dialog, select the desired marker combination.
- 3 Click OK.

The data between the two markers is displayed.

- **See Also** To create new markers (see page 272)
  - To place markers in data (see page 274)
  - To go to a marker (see page 276)
  - To delete a marker (see page 278)
  - To rename a marker (see page 282)
  - To send a marker to the back (see page 283)
  - To change a marker's snap to edge setting (see page 277)
  - Changing Marker Properties (see page 284)

# To change a marker's snap to edge setting

1 In a display window with markers, right-click on the marker, and choose **Snap to Edge**.

Or, in the display window properties dialog's Time Marker Properties tab, check or uncheck **Snap to Edge** to enable or disable the marker's snap to edge behavior.

**See Also** • To place markers in data (see page 274)

• Changing Marker Properties (see page 284)

# To delete a marker

• In the markers display bar (see page 480), click the marker you want to delete, and choose **Delete** from the popup menu (or choose **Delete All** to delete all markers).

Or:

- 1 From the menu bar, select Markers>Delete....
- 2 In the Delete Marker dialog, select the markers you wish to delete.

| Name | Position   | Comment |  |
|------|------------|---------|--|
| M1   | -1.402 us  |         |  |
| M2   | 2.926 us   |         |  |
| M3   | -12.422 ns |         |  |
| M4   | 9.688 ns   |         |  |
|      |            |         |  |

You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

- 3 Click OK.
- **See Also** To create new markers (see page 272)
  - To place markers in data (see page 274)
  - To go to a marker (see page 276)
  - To center the display about a marker pair (see page 277)
  - To rename a marker (see page 282)
  - To send a marker to the back (see page 283)
  - To change a marker's snap to edge setting (see page 277)
  - Changing Marker Properties (see page 284)

# To create a new time interval measurement

Use the new time interval measurement feature to measure a time interval between two specified points in the captured data. Measurement results are displayed in the marker measurement display bar (see page 475).

- 1 From the menu bar select Markers>New Time Interval Measurement, or click the <sup>™</sup> icon in the markers toolbar (see page 472).
- 2 In the Time Interval dialog, select the markers you want to measure time between.

| Time Interval |               | ×      |
|---------------|---------------|--------|
| From M1       | ▼ to M2       | •      |
|               | Properties OK | Cancel |

#### NOTE

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 520). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3 To specify interval properties, click Properties....

| Interval Properties               | ×            |
|-----------------------------------|--------------|
| Run Until<br>When interval >      | OK<br>Cancel |
| Show statistics Show as frequency |              |

In the Interval Properties dialog:

- Check **Stop repetitive run** if you want to stop a repetitive run when the specified interval value is measured.
- Check **Send e-mail** if you want to send an e-mail when the specified interval value is measured; then, click the **E-mail...** button. In the E-mail dialog (see page 504), enter the address to which e-mail will be sent, the subject, and the text of the message.
- Check Show statistics if you want to show repetitive run statistics.

# CAUTION

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker as one of the markers you want to measure time between, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 520). Otherwise, during the repetitive run, the system trigger could switch from one module to another, causing you to lose all the statistical data you have accumulated.

- Check **Show as frequency** if you want to show the measured frequency of changes in the interval.
- Click **OK** when you are done specifying interval properties.
- 4 Click OK to close the Time Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:

Beginning Of Data, to Trigger = 3.860812 ms (511.164 us / 3.860812 ms / 2.279915 ms)

If statistics are shown, the low, high, and average interval measurements are included.

- See Also
  - **Iso** To create a new sample interval measurement (see page 280)
    - To create a new value at measurement (see page 282)

# To create a new sample interval measurement

Use the new sample interval measurement feature to measure the number of samples between two specified points in the captured data. Measurement results are displayed in the marker measurement display bar (see page 475).

- 1 From the menu bar select Markers>New Sample Interval Measurement, or click the 🔀 icon in the markers toolbar (see page 472).
- 2 In the Sample Interval dialog, select the markers you want to measure samples between, and select the bus/signal.



# **NOTE** If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 520). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3 To specify interval properties, click Properties....

| Interval Properties   | ×            |
|---|--------------|
| Run Until       When interval       Stop repetitive run       Send e-mail | OK<br>Cancel |
| Show statistics Show as frequency   |              |

In the Interval Properties dialog:

- Check **Stop repetitive run** if you want to stop a repetitive run when the specified interval value is measured.
- Check **Send e-mail** if you want to send an e-mail when the specified interval value is measured; then, click the **E-mail...** button. In the E-mail dialog (see page 504), enter the address to which e-mail will be sent, the subject, and the text of the message.
- Check Show statistics if you want to show repetitive run statistics.

# CAUTION

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker as one of the markers you want to measure samples between, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 520). Otherwise, during the repetitive run, the system trigger could switch from one module to another, causing you to lose all the statistical data you have accumulated.

- Click **OK** when you are done specifying interval properties.
- 4 Click **OK** to close the Sample Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:

M1 to M2 = 1442011 (393733 / 1442011) [My Bus 1]

If statistics are shown, the low and high interval measurements are included.

- **See Also** To create a new time interval measurement (see page 279)
  - To create a new value at measurement (see page 282)

# To create a new value at measurement

Use the new value at measurement feature to measure the value of a bus/signal at a specified marker location in the captured data. Measurement results are displayed in the marker measurement display bar (see page 475).

- 1 From the menu bar select Markers>New Value At Measurement, or click the *♥* icon in the markers toolbar (see page 472).
- **2** In the Value At dialog, select the numeric base of the data, the bus/signal, and the marker.

| /alue At     |                    | ×      |
|--------------|--------------------|--------|
| Hex value of | My Bus 1 🛛 😽 at M1 | ОК     |
|              |                    | Cancel |

# NOTE

If you have selected a "System Trigger - (module)" or "Trigger - (module)" marker, make sure you uncheck the **First module to trigger designates the System Trigger** option in the Module Skew and System Trigger dialog (see page 520). Otherwise, during a run, the system trigger could switch from one module to another, causing the module markers to be re-assigned and any measurements using these markers to be deleted.

3 Click OK.

The result of the value at measurement  $My Bus 10^{ML} = 48$  is displayed in the marker measurement display bar.

- **See Also** To create a new time interval measurement (see page 279)
  - To create a new sample interval measurement (see page 280)

# To rename a marker

You can give markers any name you choose.

1 In a display window with markers, right-click on the marker, and choose **Rename...**.

Or, in the display window properties dialog's Time Marker Properties tab, select the **Marker**, and click **Rename...**.

2 In the Rename dialog, enter the new marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the marker display bar (see page 480) while the long name appears in the marker *tool tip* (see page 795).

3 Click OK.

**See Also** • To create new markers (see page 272)

- To place markers in data (see page 274)
- To go to a marker (see page 276)
- To center the display about a marker pair (see page 277)
- To delete a marker (see page 278)
- To send a marker to the back (see page 283)
- To change a marker's snap to edge setting (see page 277)
- Changing Marker Properties (see page 284)

# To send a marker to the back

When markers overlap on the display, you can send the visible marker to the back in order to see the marker underneath.

1 Click the marker you wish to send to the back, and choose **Send to Back** from the pop-up menu.



**See Also** • To create new markers (see page 272)

- To place markers in data (see page 274)
- To go to a marker (see page 276)
- To center the display about a marker pair (see page 277)
- To delete a marker (see page 278)
- To rename a marker (see page 282)
- To change a marker's snap to edge setting (see page 277)
- Changing Marker Properties (see page 284)

# **Changing Marker Properties**

Once a marker is created, you can modify any of its attributes from the Time Marker Properties tab..

1 Right-click on a marker, and choose Properties....

Or, when viewing a display window that has markers, choose **Markers>Properties...** from the main menu.

2 In the display window properties dialog's Time Marker Properties tab:

| Waveform Properties  | ×  |
|--|--|
| Window Properties Row Properties<br>Time Marker Properties Volta | Column Properties  |
| Marker M1 Rename   | <ul> <li>☐ Hide</li> <li>✓ Lock in Viewer</li> <li>☐ Lock to Relative</li> </ul> |
| Foreground Color       Position       Time     0 s               | ✓ Snap to Edge n System Trigger • ▼  |
| Comments   |  |
| OK Cancel  | Apply Help   |

You can:

- Select the Marker to which the property changes apply.
- Rename a marker (see page 282)
- Change a marker's background color (see page 285)
- Change a marker's foreground color (see page 285)
- Change a marker's position property (see page 275)
- Hide/show a marker (see page 285)
- Change a marker's lock in viewer setting (see page 285)
- Lock a marker relative to another marker (see page 286)
- Change a marker's snap to edge setting (see page 277)
- Add comments to a marker (see page 286)
- 3 Click OK to apply the changes and close the properties dialog.

**See Also** • To create new markers (see page 272)

- To place markers in data (see page 274)
- To go to a marker (see page 276)
- To center the display about a marker pair (see page 277)
- To delete a marker (see page 278)

- To rename a marker (see page 282)
- To send a marker to the back (see page 283)
- To read the markers display and overview bars (see page 272)

#### To change a marker's background color

1 In the Marker Properties tab, click the **Background Color** selection button and select the desired color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

- 2 Click OK to apply the changes and close the properties dialog.
- **See Also** To change voltage marker properties (see page 292)

# To change a marker's foreground color

1 In the Marker Properties tab, click the **Foreground Color** selection button and select the desired color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

- 2 Click OK to apply the changes and close the properties dialog.
- **See Also** To change voltage marker properties (see page 292)

#### To hide/show a marker

1 In the Marker Properties tab, check or uncheck **Hide** to hide or show the marker.

When a marker is hidden, all other marker properties are retained; the marker is just hidden from view in the display.

- 2 Click **OK** to apply the changes and close the properties dialog.
- **See Also** To change voltage marker properties (see page 292)

#### To change a marker's lock in viewer setting

When a marker's **Lock in Viewer** setting is enabled, moving or placing the marker in one display window causes other display windows to be updated so that the marker appears in them as well.

# **NOTE** The lock in viewer behavior applies only when a marker is dragged within the immediate data viewing area. If a marker is moved by defining a new position in the Time Markers Properties tab, the marker is not guaranteed to be visible in other display windows.

## 7 Analyzing the Captured Data

- 1 In the Time Marker Properties tab, check or uncheck **Lock in Viewer** to enable or disable the setting.
- 2 Click OK to apply the changes and close the properties dialog.

#### To lock a marker relative to another marker

When a marker is positioned relative to another marker and the marker's **Lock to Relative** setting is enabled, moving or placing either marker causes both to move such that the time between the markers remains the same. Both markers must be movable.

- 1 In the Marker Properties tab's **Position** box:
  - a Select Time.
  - **b** Select the relative marker.
  - c Enter the relative time between markers.
- 2 Check or uncheck **Lock to Relative** to lock or unlock relative marker movements.
- 3 Click OK to apply the changes and close the properties dialog.

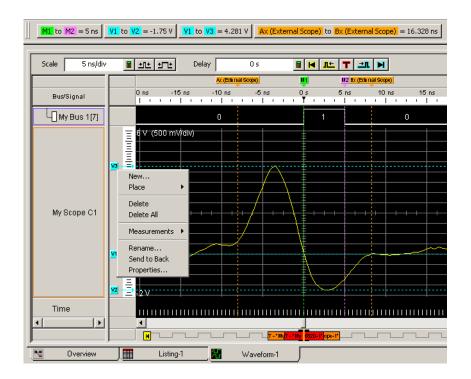
#### To add comments to a marker

You can add comments to a marker that appear in the marker's *tool tip* (see page 795).

- 1 In the Marker Properties tab's Comments box, enter your comments.
- 2 Click **OK** to apply the changes and close the properties dialog.
- **See Also** To change voltage marker properties (see page 292)

# Using Voltage Markers for Analog Signals (in the Waveform Display)

When analog signals are added to the Waveform display window (from an external oscilloscope module), you can add voltage markers and voltage interval measurements.



- To create new voltage markers (see page 287)
- To place voltage markers (see page 288)
- To delete voltage markers (see page 289)
- To create a new voltage interval measurement (see page 290)
- To rename a voltage marker (see page 291)
- To send a voltage marker to the back (see page 291)
- To change voltage marker properties (see page 292)
- See Also
- "External Oscilloscope Time Correlation and Data Display" (in the online help)

# To create new voltage markers

When creating a new voltage marker, you can give it a name, specify its color, position it, and add comments.

1 In an analog signal row's voltage marker/vertical scale display bar (to the left of the waveform), click (where you would like to place the marker) and choose **New...** 

Or, right-click on an analog signal waveform (where you would like to place the marker) and choose **Place Marker>Voltage>New Marker...** 

2 In the New Voltage Marker dialog, enter the marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the voltage marker display bar while the long name appears in the marker *tool tip* (see page 795).

| New Voltage Marker                | ×      |
|-----------------------------------|--------|
| Name 777 📓                        | ОК     |
| Background Color                  | Cancel |
| Foreground Color                  |        |
| Position                          |        |
| Voltage 2.469 V 📓 - + from Ground | •      |
| Comments                          |        |
|                                   |        |
|                                   |        |

- 3 Select the marker's background and foreground colors.
- **4** Specify the position of the new voltage marker by its voltage from ground or another voltage marker.
- 5 Enter comments for the voltage marker.

Comments appear in the marker's tool tip (see page 795).

6 Click OK.

#### **See Also** • To place voltage markers (see page 288)

- To delete voltage markers (see page 289)
- To create a new voltage interval measurement (see page 290)
- To rename a voltage marker (see page 291)
- To send a voltage marker to the back (see page 291)
- To change voltage marker properties (see page 292)

#### To place voltage markers

Use Place Markers to quickly position a voltage marker. Depending on how you access the Place Markers feature, the marker is placed in the data a little differently. You can also move markers by dragging them with the mouse or by using the front-panel knobs. Where voltage markers intersect time markers, you can drag both markers at the same time.

- To drag and drop voltage markers (see page 289)
- To place a voltage marker at the mouse cursor (see page 289)
- To change a voltage marker's position property (see page 289)

| To drag and drop<br>voltage markers   | Using the drag and drop feature you can move voltage markers to new positions in the data.   |
|---------------------------------------|--|
|                                       | 1 Click and hold down the mouse button on the marker you wish to move.   |
|                                       | 2 Move the mouse cursor to the new position.   |
|                                       | <b>3</b> Release the mouse button to reposition the marker.  |
| To place a voltage                    | <b>1</b> Point the mouse to the desired data point in the display.   |
| marker at the<br>mouse cursor         | 2 Right-click, and select Place Marker>Voltage>(desired marker).   |
| To change a                           | 1 Right-click on a voltage marker, and choose Properties   |
| voltage marker's<br>position property | Or, when viewing a display window that has voltage markers, choose <b>Markers&gt;Properties</b> from the main menu.  |
|                                       | <b>2</b> In the Waveform Properties dialog's Voltage Marker Properties tab, select the <b>Marker</b> to which the property changes apply.  |
|                                       | <b>3</b> In the <b>Position</b> box, position the marker by its voltage from ground or another voltage marker.   |
|                                       | 4 Click <b>OK</b> to apply the changes and close the properties dialog.  |
| See Also                              | • To create new voltage markers (see page 287)   |
|                                       | • To delete voltage markers (see page 289)   |
|                                       | • To create a new voltage interval measurement (see page 290)  |
|                                       | • To rename a voltage marker (see page 291)  |
|                                       | • To send a voltage marker to the back (see page 291)  |
|                                       | • To change voltage marker properties (see page 292)   |
|                                       | To delete voltage markers  |
|                                       | • In an analog signal's voltage markers/vertical scale display bar (to the left of the waveform), click the voltage marker you want to delete, and choose <b>Delete</b> from the popup menu (or choose <b>Delete All</b> to delete all voltage markers). |
|                                       | Or:  |
|                                       | 4 Error the many has all the Markens Dalate  |

- 1 From the menu bar, select Markers>Delete....
- 2 In the Delete Marker dialog, select the markers you wish to delete.

### 7 Analyzing the Captured Data

| Name | Position Comment |
|------|------------------|
| M1   | 0 s              |
| M2   | 5 ns             |
| V1   | 0 V              |
| V2   | -1.75 V          |
| V3   | 4.281 V          |
|      |                  |
|      |                  |
|      |                  |
|      |                  |
|      |                  |
|      |                  |

You can sort the list of markers by clicking on the Name, Position, or Comment column headings.

- 3 Click OK.
- **See Also** To create new voltage markers (see page 287)
  - To place voltage markers (see page 288)
  - To create a new voltage interval measurement (see page 290)
  - To rename a voltage marker (see page 291)
  - To send a voltage marker to the back (see page 291)
  - To change voltage marker properties (see page 292)

### To create a new voltage interval measurement

Use the voltage interval measurement feature to measure a voltage between two voltage markers. Measurement results are displayed in the marker measurement display bar (see page 475).

1 In an analog signal row's voltage marker/vertical scale display bar (to the left of the waveform), click and choose Measurements>New Voltage Interval Measurement.

Or, right-click in the marker measurement display bar and choose New Voltage Interval Measurement>(analog signal name).

2 In the Voltage Interval dialog, select the markers you want to measure voltage between.

| Voltage Interval |       | ×      |
|------------------|-------|--------|
| From V1          | to V2 | •      |
|                  | ОК    | Cancel |

3 Click OK to close the Voltage Interval dialog.

The result of the interval measurement is displayed in the marker measurements display bar:

#### **V1** to **V2** = -1.75 V

#### To rename a voltage marker

You can give voltage markers any name you choose.

1 In a Waveform window with voltage markers, right-click on the marker, and choose **Rename...**.

Or, in the display window properties dialog's Voltage Marker Properties tab, select the **Marker**, and click **Rename...**.

2 In the Rename dialog, enter the new marker name.

You can specify both a *long name* and an *abbreviated name* by using the "Long name[abbreviated name]" syntax; for example, "Location A[A]". When an abbreviated name is used, it appears on the marker in the voltage marker display bar while the long name appears in the marker *tool tip* (see page 795).

- 3 Click OK.
- **See Also** To create new voltage markers (see page 287)
  - To place voltage markers (see page 288)
  - To delete voltage markers (see page 289)
  - To create a new voltage interval measurement (see page 290)
  - To send a voltage marker to the back (see page 291)
  - To change voltage marker properties (see page 292)

#### To send a voltage marker to the back

When voltage markers overlap on the display, you can send the visible marker to the back in order to see the marker underneath.

1 Click the voltage marker you wish to send to the back, and choose **Send to Back** from the pop-up menu.

| <u> </u>  | New            |   |  |
|-----------|----------------|---|--|
|           | Place          | • |  |
|           | Delete         |   |  |
|           | Delete All     |   |  |
|           | Measurements   | • |  |
| VI        | Rename         |   |  |
| -         | Send to Back   |   |  |
|           | Properties     |   |  |
| <u>v2</u> | <u>=</u><br>2V |   |  |

**See Also** • To create new voltage markers (see page 287)

- To place voltage markers (see page 288)
- To delete voltage markers (see page 289)
- To create a new voltage interval measurement (see page 290)
- To rename a voltage marker (see page 291)
- To change voltage marker properties (see page 292)

### To change voltage marker properties

Once a voltage marker is created, you can modify any of its attributes from the Voltage Marker Properties tab..

1 Right-click on a voltage marker, and choose Properties....

Or, when viewing a Waveform display window that has voltage markers, choose **Markers>Properties...** from the main menu.

2 In the Waveform Properties dialog's Voltage Marker Properties tab:

| Waveform Properties  | x |
|--|---|
| Window Properties Row Properties Column Properties<br>Time Marker Properties Voltage Marker Properties | 1 |
| Time Marker Properties Voltage Marker Properties   |   |
| Marker V3 Rename Hide  |   |
| Background Color   |   |
| Foreground Color   |   |
| Position   |   |
| Voltage 4.281 V 📓 - + from Ground 💌  |   |
| Comments   |   |
|  |   |
|  |   |
| OK Cancel Apply Help   |   |

You can:

- Select the Marker to which the property changes apply.
- Rename a voltage marker (see page 291)
- Change a marker's background color (see page 285)
- Change a marker's foreground color (see page 285)
- Change a voltage marker's position property (see page 289)
- Hide/show a marker (see page 285)
- Add comments to a marker (see page 286)
- 3 Click **OK** to apply the changes and close the properties dialog.
- See Also To create new voltage markers (see page 287)
  - To place voltage markers (see page 288)

- To delete voltage markers (see page 289)
- To create a new voltage interval measurement (see page 290)
- To rename a voltage marker (see page 291)
- To send a voltage marker to the back (see page 291)

### 7 Analyzing the Captured Data

# **Searching the Captured Data**

You can search for bus/signal patterns in the captured data.

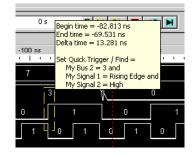
- To quickly find bus/signal patterns (see page 294)
- To find bus/signal patterns in the captured data (see page 296)
- To find packet patterns in the captured data (see page 298)
- To find complex patterns in the captured data (see page 302)
- To store, recall, or delete favorite find patterns (see page 303)
- To specify "found" marker placement (see page 304)

# To quickly find bus/signal patterns

In the Waveform or Listing windows, you can quickly draw a rectangle and find the next or previous occurrence of that bus/signal pattern.

- 1 In the Waveform window, make sure the Fast Zoom In (see page 252) option is not selected.
- **2** Using the mouse, point to the upper-left corner of your desired bus/signal pattern.
- **3** While holding down the mouse button, drag the mouse pointer to the lower-right corner of your bus/signal pattern.

As you draw the rectangle, a tool tip shows the selected bus/signal pattern.



As you move the mouse left-to-right and top-to-bottom, the signal edge/level or bus value in contact with the **left of the rectangle** becomes the bus/signal pattern.

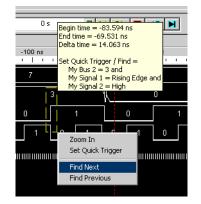
Only one edge can be set.

If a bus is expanded into its separate signals, three conditions apply:

- **a** If drawing starts on a bus, none of its expanded signals can be included.
- **b** If drawing starts on a signal, the bus cannot be included.
- **c** Edges and levels are mutually exclusive. That is, either one edge can be set, or all levels can be set, but not both at the same time.

**NOTE** In the Waveform display window, it may be necessary to redraw the rectangle if you do not get your desired bus/signal pattern dictated by the left-side line of the rectangle. You could also try drawing the rectangle backwards leaving the left-side rectangle line set last.

**4** When the desired bus/signal pattern has been selected, release the mouse button, and select **Find Next** or **Find Previous** from the popup menu.



5 Click the Previous 脑 or Next 🛋 icons to see more occurrences.

General Guidelines • Any bus/signals with overlapping bits are not included within the bus/signal pattern.

**Example:** Bus\_1 has channels 0 through 7 of pod 1 assigned and Bus\_2 has channels 3 through 6 of pod 1 assigned. At this point, you have the same probed signals (channels 3 through 6 of pod 1) assigned in both Bus\_1 and Bus\_2. Now, you draw the rectangle over both bus\_1 and bus\_2. Because Bus\_1 channels 3 through 6 are repeated (overlapped) on Bus\_2, they will not be included in the bus/signal pattern.

See Also

- To find bus/signal patterns in the captured data (see page 296)
  - To find packet patterns in the captured data (see page 298)
- To find complex patterns in the captured data (see page 302)
- To store, recall, or delete favorite find patterns (see page 303)

# To find bus/signal patterns in the captured data

This search option locates a specified data pattern. You can qualify your search by specific bits, data patterns, equality, and range operators. The search result is placed at the center of the display.

- 1 From the menu bar, choose Edit>Find..., or click the A icon in the standard toolbar (see page 469).
- 2 In the **Find** dialog, enter the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.

| 🔆 Find   |
|--|
| Find 1 I -+ occurrence searching Forward v from Display Center   |
| Image: Bus/Signal     Image: My Bus 1     All bits     Image: Bus/Signal     Image: My Bus 1       When     Present     Image: Bus/Signal     Image: My Bus 1     All bits     Image: Bus/Signal |
| Store Favorite ¥ Recall Favorite ¥ Clear Options Find Close Help   |

- 3 In the event specification area, select the Bus/Signal pattern type.
- 4 Specify the bus/signal pattern event you wish to locate.

In addition to the usual pattern matching operators (=, !=, <, >, <=, >=, **In Range**, and **Not In Range**), there are three additional operators you can use:

- **Entering** the first sample of one or more consecutive samples that match the pattern. (By comparison, the "=" equals operator considers every sample that matches the pattern as an occurrence.)
- **Exiting** the sample after one or more consecutive samples that match the pattern.
- **Transitioning** entering or exiting one or more consecutive samples that match the pattern.

You can find analog signal values as well as digital signal values.

- **5** Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator):
  - Present
  - Not Present
  - **Present>** (time duration)
  - **Present>=** (time duration)
  - **Present**< (time duration)
  - **Present<=** (time duration)

- Present for Range (of time)
- Not Present for Range (of time)
- Entering
- Exiting
- Transitioning
- 6 Click Find.
- 7 Click the Previous in or Next in icons to see more occurrences.

# TIP

As you configure the find function, try to think of it as constructing a sentence that reads left-to-right. For example: "Find 1 occurrence **Forward** from the **Display Center** of a bus named **My Bus 1**, and on **All bits** a pattern that **Equals XX Hex**, display the event When all criteria is **Present**."

## NOTE

#### The find qualifiers:

- Present>
  Present>=
- Present<
- Present<=</li>
- Present for Range
- Not Present for Range

allow you to specify a time duration. This means that the find event specified in the expression area will be found based upon the given time and operator.

The other qualifiers:

- Present
- Not Present
- Entering
- Exiting
- Transitioning

do not allow a time duration.

#### **See Also** • To quickly find bus/signal patterns (see page 294)

- To find packet patterns in the captured data (see page 298)
- To find complex patterns in the captured data (see page 302)
- To store, recall, or delete favorite find patterns (see page 303)
- To specify "found" marker placement (see page 304)

# To find packet patterns in the captured data

In the Protocol Viewer window, you can search for packets, packet errors, and field values.

- 1 With the Protocol Viewer window open, choose Edit>Find... from the menu bar or click the **M** icon in the standard toolbar (see page 469).
- 2 In the **Find** dialog, enter the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.
- 3 In the event specification area, select the **Packet**, **Packet Error**, or **Field** pattern type.

| 🔆 Find  | X |
|---|---|
| Find 1 I -+ occurrence searching Forward V from Display Center  | ~ |
| Image: Second |   |
| Store Favorite 🖇 Recall Favorite 🖏 Clear Options Find Close Help  |   |

- To find packet events (see page 298)
- To find packet errors (see page 299)
- To find field values (see page 300)

To find packet 1 You can click packet type button to open a selection dialog. events

| ** Select        |              |
|------------------|--------------|
| Packet Decoder W | OK<br>Cancel |
|                  | .:           |

2 Click the packet event button to open the Event Editor dialog.

| Event Editor  |             |                   |   |
|---|-------------|-------------------|---|
| Events  | Name        | 3DW Memor         | ry Write Request 🔳 Add to Favorites           |
| PCI Express     Favorites     Ordered Sets     Packets  |             | press : Physical  | STP   |
| Any Packet     DLLP Packets     TLP Packets   | PCI Ex      | press : Data Link | X 1. Hex ¥                                    |
| Any TLP Packet  3DW Packets  3DW Memory Read Request  |             | nce Number        | XXX THex V                                    |
| - 3DW Memory Request-Locked<br>- 3DW I/O Read Request<br>- 3DW Configuration Read Type          | Reser       |                   |   |
| - 3DW Configuration Read Type<br>- 3DW Completion without Data<br>- 3DW Completion, Lck Mem Rea | Fmt<br>Type |                   | 3DW header, with data<br>Memory Write Request |
| 3DW Memory Write Request  | Reser       | ved2              | X II Bin V X                                  |
| Organize Favorites  | < l         | 10                |   |
|   | Cle         | ar View as Bits   | . OK Cancel Help                              |

For more information, see Using the Packet Event Editor (see page 175)

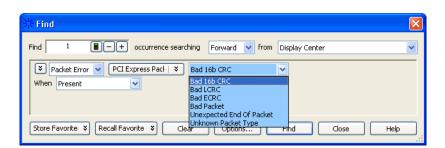
- **3** Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 296).
- 4 Click **Find**.
- **5** Click the Previous **i** or Next **i** icons to see more occurrences.
- To find packet 1 You can click packet type button to open a selection dialog.

#### errors

| 🔆 Select         |              |
|------------------|--------------|
| Packet Decoder W | OK<br>Cancel |
|                  |              |

2 Select the packet error value:

### 7 Analyzing the Captured Data



- **3** Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 296).
- 4 Click Find.
- **5** Click the Previous **1** or Next **1** icons to see more occurrences.

#### To find field 1 Select the field name. values

Clicking  $\blacksquare$  lets you select from recently used field names. Clicking elsewhere on a field name button opens a Select dialog for selecting a different name.

|            |                           | _ |        |
|------------|---------------------------|---|--------|
| 🖃 🔂 Packet | : Decoder W               | ^ | OK     |
| 📄 🚊 Da     | ta Link                   |   |        |
| 📄 📩 🚞 Ph   | ysical                    |   | Cancel |
| 📄 🚖 Tra    | insaction                 | Ξ |        |
|            | Address                   |   |        |
|            | Attributes                |   |        |
|            | Bus Number                | - |        |
|            | Bus Number (Completer)    |   |        |
|            | Bus Number (Requester)    |   |        |
|            | Byte Count                |   |        |
|            | Byte Count Modified       |   |        |
|            | Completer ID              |   |        |
|            | Completion Status         |   |        |
|            | Device Number             |   |        |
|            | Device Number (Completer) |   |        |
|            | Device Number (Requester) |   |        |
|            | EP                        | v |        |
| <          |                           |   |        |
|            |                           | _ |        |

**2** Specify the field value:

If a single-bit field has been selected, select the signal pattern value (High, Low, or Dont Care).

ar a state of the state of the

| 🕸 Find   |
|--|
| Find 1 I - Cccurrence searching Forward V from Display Center  |
| Image: Second system     Image: Second system       Image: Second system     Ima |
| Store Favorite V Recall Favorite V Clear Options Find Close Help   |

If a multiple-bit field has been selected:

a Select one of the operators: = (equal to), != (not equal to), < (less than), > (greater than), <= (less than or equal to), >= (greater than or equal to), In Range, or Not In Range.

| Sti Find  |                          |
|---|--------------------------|
| Find 1 I -+ occurrence searching Forwa                        | rd 💌 from Display Center |
| Field     Completion State     >       When     Present     = | X Hex X                  |
| Store Favorite V Recall Favorite V Cle In Range               | Find Close Help          |

b Select the number base (Binary, Hex, Octal, Decimal, or Signed Decimal, also known as two's complement).

| 🔆 Find   |                           | X    |
|--|---------------------------|------|
| Find 1 II-+ occurrence searching Forward v from  | Display Center            | ~    |
|  | Hex V                     |      |
| When Present                                     | Binary<br>✓ Hex           |      |
|  | Octal                     |      |
| Store Favorite 🕏 Recall Favorite 🕏 Clear Options | Decimal<br>Signed Decimal | Help |

- **c** Enter the pattern value(s).
- **3** Select the desired **When** find qualifier (which further qualifies the find criteria with a time duration or other operator). For more information, see To find bus/signal patterns in the captured data (see page 296).
- 4 Click Find.
- 5 Click the Previous 🛍 or Next 🛋 icons to see more occurrences.

**See Also** • To quickly find bus/signal patterns (see page 294)

• To find bus/signal patterns in the captured data (see page 296)

- To find complex patterns in the captured data (see page 302)
- To store, recall, or delete favorite find patterns (see page 303)
- To specify "found" marker placement (see page 304)

## To find complex patterns in the captured data

You can expand search criteria to include more than one event describing data patterns.

- 1 From the menu bar, choose Edit>Find..., or click the A icon in the standard toolbar (see page 469).
- 2 In the **Find** dialog, select the number of the occurrences you wish to find, select whether you want to search forward or backward from the start location; then, select the start location.
- 3 Select the pattern event drop down menu to choose Insert Event After (AND/OR) or Insert Event Before (AND/OR) to insert new find events.

| Find 1                  | -+ occurrence se  | arching  | Forward    | 💽 from [ | Display Center    | ×      |
|-------------------------|-------------------|----------|------------|----------|-------------------|--------|
| (ADDR And DATA) C       | r (ADDR And DATA) |          |            |          |                   |        |
| 🖲 Bus/Signal 🔽          | ADDR 🛛 💙          | All bits | ✓ =        | *        | target_temp Sym ¥ | And 🐱  |
| 🖲 Bus/Signal 🔽          | DATA 🛛 💙          | All bits | <b>~</b> = | *        | 20XX XXXX 🔳 Hex   | 💙 Or 🔽 |
| 🖲 Bus/Signal 🔽          | ADDR 🛛 💙          | All bits | <b>~</b> = | *        | target_temp Sym ¥ | And 🐱  |
| 🖲 Bus/Signal 🔽          | DATA 🛛 💙          | All bits | <b>~</b> = | *        | 21XX XXXX 📕 Hex   | *      |
| Insert Event Af         | ter (AND/OR)      |          |            |          |                   |        |
| Insert Event <u>B</u> e | fore (AND/OR)     |          |            |          |                   |        |
| Delete Event            |                   |          |            |          |                   |        |
|                         |                   |          |            |          |                   |        |
| Store Favorite 🛛 🗧      | Recall Favorite 🛛 | Clear    | _ Op       | tions    | Find Close        | Help   |

The **Delete Event** option will delete the current event only if there is more than one event present.

**4** For each event you add, select either **And** or **Or** to specify how the event patterns are combined.

AND'ed searches find occurrences of both events, while OR'ed searches find occurrences of either event.

When you have AND'ed and OR'ed events, a button appears above the events for changing the event evaluation order.

- **5** For each event, select the bus or signal name and enter the value you want to locate.
- 6 Click Find.
- **See Also** To quickly find bus signal patterns (see page 294)

- To find bus/signal patterns in the captured data (see page 296)
- To find packet patterns in the captured data (see page 298)
- To store, recall, or delete favorite find patterns (see page 303)
- To specify "found" marker placement (see page 304)

## To store, recall, or delete favorite find patterns

- To store a favorite pattern (see page 303)
- To recall a favorite pattern (see page 303)
- To delete a favorite pattern (see page 304)

#### To store a favorite 1 From the menu bar select, Edit>Find..., or click the M icon.

- 2 Set up the pattern you want to find (see To find bus/signal patterns in the captured data (see page 296) or To find complex bus/signal patterns in the captured data (see page 302)).
- 3 Click Store Favorite.

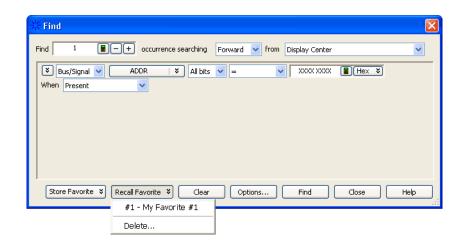


- **4** Enter the name of the find pattern.
- 5 Click OK to save the find pattern.

#### To recall a 1 H favorite pattern

pattern

- **1** From the menu bar select, **Edit>Find...**, or click the **M** icon.
- 2 Select **Recall Favorite**; then, select the find pattern you want to use from the drop down menu.



3 Click Find.

| To delete a      | 1 From the menu bar select, Edit>Find, or click the <b>M</b> icon.  |
|------------------|---|
| favorite pattern | 2 Select Recall Favorite; then, select Delete   |
|                  | <b>3</b> In the Delete Favorites dialog, select the find patterns you wish to delete; then, click <b>Delete</b> . |
| See Also         | • Searching the Captured Data (see page 294)  |
|                  | • To specify "found" marker placement (see page 304)  |

# To specify "found" marker placement

When searching for a pattern, you can place an existing marker on the last occurrence, or you can place a new marker on the last occurrence or on all occurrences.

- 1 From the menu bar select, **Edit>Find...**, or click the **M** icon in the standard toolbar (see page 469).
- 2 In the Find dialog, set up the pattern you want to find.
- 3 Click Options....

| Find Options   | X            |
|--|--------------|
| When Found         Place       Found         Image: Place new marker named:       MyMarker         Image: On the 3rd occurrence         Image: On the 3rd occurrence         Image: On all 3 occurrences | OK<br>Cancel |

| To place an                    | 1 Select the <b>Place</b> option.   |
|--------------------------------|---|
| existing marker<br>on the last | 2 Select the marker you want to place from the drop down menu.  |
| occurrence                     | 3 Click OK.   |
| To place a new                 | 1 Select Place new marker named:.   |
| marker                         | 2 Enter the name of the new marker.   |
|                                | <b>3</b> Select whether you want to place the new marker <b>on the last occurrence</b> or <b>on all occurrences</b> . |
|                                | The <b>on all occurrences</b> option is only available when you are finding more than one occurrence.                 |
|                                | 4 Click OK.   |
| See Also                       | • Searching the Captured Data (see page 294)  |
|                                | • To store, recall, or delete favorite find patterns (see page 303)   |
|                                | • To place markers in data (see page 274)   |

# **Comparing Captured Data to Reference Data**

By comparing data from different acquisitions, you can look for differences between a known-good device under test and a device under test with a problem or one that is operating under different conditions.

To compare captured to reference data:

- 1 Capture (or load) the data you want to use as the reference data.
- 2 Select Window>New Compare... to open a new Compare display window.
- 3 In the Compare display window, click the **Copy...** button to select the current data that should be copied to the reference buffer.
- 4 Capture (or load) the data that you want to compare to the reference.

Differences are highlighted in the Compare window.

For more information on comparing captured data to reference data, see:

- To copy data to the reference buffer (see page 305)
- To find differences in the compared data (see page 306)
- To compare only a range of samples (see page 306)
- To offset the reference data (see page 306)
- To run until a number of compare differences (see page 307)
- To set Compare window properties (see page 307)
- **See Also** Compare Display Window (see page 485)
  - Capturing Data from the Device Under Test (see page 149)
  - Loading Saved Data and Setups (see page 220)

### To copy data to the reference buffer

- 1 In the Compare display window, click the **Copy...** button.
- 2 In the Select Buses/Signals dialog:
  - **a** From the available buses and signals, select the ones to be copied to the reference buffer and click **Add>>**.

To remove buses and signals from the selected list, select them and click **<<Remove**.

- **b** Select either All data or a range of data using markers.
- 3 When you are ready to begin the copy, click OK.

```
NOTE
```

Copying generated bus/signal columns, such as those created by an inverse assembler or an analysis tool, takes longer because of the extra processing to re-create the data.

### NOTE

If your logic analyzer has deep memory, it takes a while to copy data to the reference buffer.

# To find differences in the compared data

In the Compare display window:

- Click the >> button to find the next difference (below the center reference).
- Click the << button to find the previous difference (above the center reference).
- Click a blue tick mark in the **Compare Overview** bar (between the vertical scroll bar and the Marker Overview bar on the right side of the window) to go to that difference.

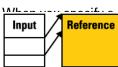
## NOTE

When a difference occurs on a subrow (for example, when the data is inverse-assembled or decoded by an analysis tool), the next and previous buttons go to the sample row instead of the subrow.

# To compare only a range of samples

- 1 In the Compare display window, click the Range & Offset... button.
- 2 In the Range & Reference dialog, select either *All* data or a range of data using markers.
- 3 Click OK.





erence data has been offset (see page 306) by a number of samples) ge in the reference buffer as you might expect. This behavior allows input data to be compared with the reference data.

# To offset the reference data

When there are differences in the number of samples captured before the trigger, or when you are comparing a range of samples, you can offset the reference data so that the samples being compared are properly aligned.

- 1 In the Compare display window, click the Range & Offset... button.
- 2 In the Range & Reference Offset dialog, enter the number of samples to offset the reference by.
- 3 Click OK.
- **See Also** To compare only a range of samples (see page 306)

## To run until a number of compare differences

The Compare display lets you stop comparing, stop a repetitive run, or send e-mail after a run has more than a specified number of differences when compared to the reference data.

- 1 In the Compare display window, click **Compare Until...**.
- 2 In the Difference Properties tab of the Compare Properties dialog, enter the number of differences that will stop comparing, stop a repetitive run, or send an e-mail message.
- **3** To stop a compare after the number of differences have been found, select the **Stop comparing** check box.
- **4** To stop a repetitive run after the number of differences have been found, select the **Stop repetitive run** check box.
- **5** To send e-mail after the number of differences have been found, select the **Send e-mail** check box; then, click the **E-mail...** button. In the E-mail dialog (see page 504), enter the address to which e-mail will be sent, the subject, and the text of the message.
- 6 Click OK in the Compare Properties dialog.
- 7 Start the repetitive run measurement.
- **See Also** Running/Stopping Measurements (see page 203)

## To set Compare window properties

- 1 In the Compare display window, right-click on the bus/signal column name; then, select **Properties...** from the popup menu.
- 2 In the Compare Properties dialog:
  - The **Window Properties** tab lets you select the reference data background color, the background color that indicates no reference data, and the difference foreground and background colors.
  - The **Column Properties** tab's Display field lets you display **All** of the reference data, just the reference data where a difference was found (**Difference Pair**), or only the highlighted differences in the data being compared (**Input Only**).
  - The **Difference Properties** tab lets you select the options for running until a number of compare differences are found.

All other Compare property options are the same as in the Listing window.

#### **See Also** • To set Listing window properties (see page 263)

• To run until a number of compare differences (see page 307)

# **Viewing Source Code Associated with Captured Data**

- **1** Add and configure the appropriate inverse assembler tool (see "Using Inverse Assembler Tools" (in the online help)).
- **2** Load line number symbols (see To load symbols from a file (see page 141)).
- 3 Select Window>New Source... to open a new Source display window.
- **4** In the Add New Window after dialog, select the inverse assembler or filter/colorize tool that the Source window should be added after.

Generally, you want the Source window getting the same data as other display windows (Listing, Waveform, etc.).

- **5** In the source display pane of the Source window, right-click, and choose **Properties...**.
- **6** In the Source Viewer Properties dialog's Source Code Directories tab, click **Add...** tab.
- 7 In the Browse for Folder dialog, select the directory that contains the source files, and click **OK**.
- 8 Click OK to close the Source Viewer Properties dialog.

For more information on viewing the source code associated with captured data, see:

- To step through captured data by source lines (see page 309)
- To go to captured data associated with a source line (see page 309)
- To browse source files (see page 310)
- To search for text in source files (see page 310)
- To set a Quick Trigger in the Source window (see page 154)
- To go to the source line associated with the listing center rectangle (see page 311)
- To edit the source code directory list (see page 311)
- To select the correlation bus (see page 312)
- Changing Source Window Properties (see page 313)
  - To change the source background color (see page 314)
  - To change the source text color (see page 314)
  - To change the source font size (see page 314)
  - To change the source tab width (see page 315)
  - To show/hide source line numbers (see page 315)
  - To change the "Set Quick Trigger" alignment (see page 315)
- **See Also** Analyzing Listing Data (see page 259)

• Source Display Window (see page 486)

## To step through captured data by source lines

| Displa            | ayed File C:\My Documents\source\ecs2.c 💌 Browse 💐 🚺 🕻 🔱 | { t <sub>in</sub> t <sub>in</sub> |
|-------------------|--|-----------------------------------|
| 145               | <pre>proc_spec_init();</pre>                             | <b>A</b>                          |
| 146               |  |                                   |
| 147               | for (;;)   |                                   |
| 148               | (  |                                   |
| 149               | update system(num checks);                               |                                   |
| 150               | num checks++;  |                                   |
| 151               | update_display(num_checks);                              |                                   |
| 150<br>151<br>152 | proc specific();   |                                   |
| 4                 |  | •                                 |

 In the Source window's source pane, click the <u>₩</u> step to next source line or <u>↑</u> step to previous source line buttons.

The listing pane is updated to show the captured data associated with the next or previous source line, and the source pane is updated to show the next or previous source line.

**See Also** • Viewing Source Code Associated with Captured Data (see page 308)

# To go to captured data associated with a source line

| Display                         | red File | C:\My Documents\source\ecs2.c                               | ▼ Browse   | ⇒{ <b>1</b> { <b>↓</b> { | 1 <sub>68</sub> 0 <sub>68</sub> |
|---------------------------------|----------|---|--|--------------------------|---------------------------------|
| 147<br>148<br>149<br>150        | for<br>{ | <pre>(;;) update system(num checks); num_checks++;</pre>    |  |                          | <b>A</b>                        |
| 151<br>152<br>153<br>154 }<br>◀ | }        | <pre>update display(num checks);<br/>proc_specific();</pre> | Set Quick Trigger<br>Find in Source<br>Find Next Selected Source Line<br>Find Prev Selected Source Line<br>Symbols<br>Properties |                          | ×<br>>                          |

- 1 In the Source window's source pane, click the source line whose associated captured data you want to view.
- 2 Click the sind next selected source line or selected source line buttons.

Or, right-click the selected source line and choose **Find Next Selected Source Line** or **Find Prev Selected Source Line**.

If captured data associated with the source line is found, the listing pane is updated to show the captured data, and the source pane is updated to show the selected source line. If captured data associated with the source line is not found, an information dialog is displayed.

See Also • Viewing Source Code Associated with Captured Data (see page 308)

## To browse source files

1 In the Source window's source pane, click Browse....

| Displayed File | C:\My Documents\source\ecs2.c | Browse |
|----------------|-------------------------------|--------|
|                |                               |        |

**2** In the Select Source File to Open dialog, select the source file to browse, and click Open.

The selected source file appears in the source pane.

- See Also • To search for text in source files (see page 310)
  - To set a Quick Trigger in the Source window (see page 154)
  - To go to the source line associated with the listing center rectangle (see page 311)
  - Viewing Source Code Associated with Captured Data (see page 308)

# To search for text in source files

1 In the Source window's source pane, right-click choose Find in Source....

| Displa | ayed File C:\My Documents\source | ecs2.c                         | ▼ Browse | ⇒{ <b>1</b> { <b>↓</b> { | t <sub>été</sub> Q <sub>été</sub> |
|--------|----------------------------------|--------------------------------|----------|--------------------------|-----------------------------------|
| 145    | <pre>proc_spec_init();</pre>     |                                |          |                          |                                   |
| 146    |                                  |                                |          |                          |                                   |
| 147    | for (;;)                         | Set Quick Trigger              |          |                          |                                   |
| 148    | {                                | Find in Source                 |          |                          |                                   |
| 149    | update system(:                  | Find Next Selected Source Line |          |                          |                                   |
| 150    | num checks++;                    | Find Prev Selected Source Line |          |                          |                                   |
| 151    | update display                   |                                | _        |                          |                                   |
| 152    | proc specific(                   |                                |          |                          | <u> </u>                          |
| •      |                                  | Properties                     | -        |                          | •                                 |

2 In the Find dialog, enter the text to search for, select the direction to search, and click Find Next.

If the text is found, the source line is highlighted.

If the text is not found, an information dialog is displayed.

See Also

- To set a Quick Trigger in the Source window (see page 154)
  - To go to the source line associated with the listing center rectangle (see page 311)

• Viewing Source Code Associated with Captured Data (see page 308)

## To go to the source line associated with the listing center rectangle

After browsing or searching for text in source files, you may want to return to displaying the source line associated with the captured data displayed in the listing pane.

| Displaye                        | ed File C:\My Documents\source\ecs2.c   Browse  F( \ \ | 4       |
|---------------------------------|--|---------|
| 145<br>146<br>147               | <pre>proc_spec_init();</pre>                           | <b></b> |
| 146                             |  |         |
| 147                             | for (;;)   |         |
| 148                             | (  |         |
| 149                             | update system(num checks);                             |         |
| 150                             | num_checks++;  |         |
| 148<br>149<br>150<br>151<br>152 | update_display(num_checks);                            |         |
| 152                             | proc specific();                                       |         |
| •                               |  | •       |

In the Source window's source pane, click the ⇒
 show correlated source line button.

The source pane is updated to show either the source line associated with the listing center rectangle or "No matching symbol found.".

**See Also** • Viewing Source Code Associated with Captured Data (see page 308)

## To edit the source code directory list

Because source file paths specified in the symbol file may not be valid if you compile on one computer and debug on another, you can specify the directories where source code is located.

- 1 In the Source window display areas, right-click, and choose **Properties...**.
- 2 Or, choose Edit>Window Properties... from the main menu.
- 3 In the Source Viewer Properties dialog's Source Code Directories tab:

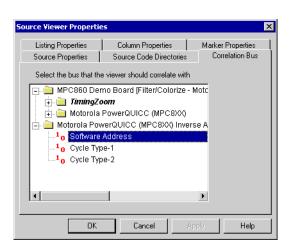
| Search subdirectories |  | Add                  |
|-----------------------|--|----------------------|
|                       |  |                      |
|                       |  | Move Up<br>Move Down |

You can:

- Add a directory to the search list by clicking Add ....
- Specify whether subdirectories are included in or excluded from the search by checking or unchecking **Search subdirectories**.
- Change a directory's order in the search list by highlighting a directory and clicking **Move Up** or **Move Down**.
- Delete directory from the search list by highlighting a directory and clicking **Delete**.
- 4 Click **OK** to apply the changes and close the Source Viewer Properties dialog.
- See Also Viewing Source Code Associated with Captured Data (see page 308)

# To select the correlation bus

- 1 In the Source window display areas, right-click, and choose **Properties...**.
- 2 Or, choose Edit>Window Properties... from the main menu.
- **3** In the Source Viewer Properties dialog's Correlation Bus tab, select the bus on which the Source window should look for line number symbols.



Typically, you will select the "software address" bus generated by an inverse assembler tool or another address bus.

- **4** Click **OK** to apply the changes and close the Source Viewer Properties dialog.
- **See Also** Viewing Source Code Associated with Captured Data (see page 308)

# **Changing Source Window Properties**

You can change properties that affect the source code pane of the Source display window.

- 1 In the source display pane of the Source window, right-click, and choose **Properties...**.
- 2 Or, choose Edit>Window Properties... from the main menu.
- 3 In the Source Viewer Properties dialog's Source Properties tab:

| Source Viewer Propertie                 | s 🔉  |
|---|--|
| Listing Properties<br>Source Properties | Column Properties Marker Properties<br>Source Code Directories Correlation Bus   |
| Background Source Text                  | Display Options<br>Tab Width 1 1 - +<br>Tab Width 1 - +<br>Topological Display Line Numbers<br>Trigger Options<br>Address Alignment 4-byte |
| ОК                                      | Cancel Apply Help  |



- Change the source background color (see page 314)
- Change the source text color (see page 314)
- Change the source font size (see page 314)
- Change the source tab width (see page 315)
- Show/hide source line numbers (see page 315)
- Change the "Set Quick Trigger" alignment (see page 315)
- **4** Click **OK** to apply the changes and close the Source Viewer Properties dialog.
- **See Also** Changing Listing Window Properties (see page 263)
  - Changing Bus/Signal Column Properties (see page 265)

#### To change the source background color

1 In the Source Viewer Properties dialog's Source Properties tab, click the **Background** color selection button and select the desired background color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

#### To change the source text color

1 In the Source Viewer Properties dialog's Source Properties tab, click the **Source Text** selection button and select the desired color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

#### To change the source font size

1 In the Source Viewer Properties dialog's Source Properties tab, enter the desired **Font Size**.

Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

### To change the source tab width

1 In the Source Viewer Properties dialog's Source Properties tab, enter the desired **Tab Width**.

Tab widths can range from 1 to 10 spaces.

2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

### To show/hide source line numbers

- 1 In the Source Viewer Properties dialog's Source Properties tab, check or uncheck **Display Line Numbers** to specify whether source file line numbers are shown or hidden.
- 2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.

## To change the "Set Quick Trigger" alignment

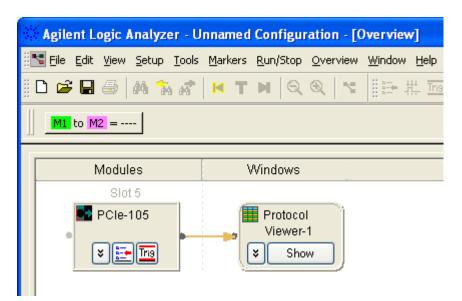
For microprocessors that fetch blocks of instructions at a time (from block boundary addresses only), the address alignment property lets you adjust the source line symbol values to be on block boundary addresses when setting up Quick Triggers on a source line.

- 1 In the Source Viewer Properties dialog's Source Properties tab, select the desired **Address Alignment**.
- 2 Click **OK** to apply the changes and close the Source Viewer Properties dialog.
- See Also To set a Quick Trigger in the Source window (see page 154)

# 7 Analyzing the Captured Data

# **Analyzing Packet Data**

You can use a Protocol Viewer window to display the captured data. The following screen displays an instance of Protocol Viewer added to the U4301A PCIe Gen3 Analyzer module to display the PCIe data captured by this module.



Unlike the Listing window, the Protocol Viewer windows let you view summarized and detailed packet information at the same time within two panes. The following screen displays the captured packets in a Protocol Viewer window.

| Sample Numbe                                       | er Time                           |                          | PCI-Ex                   | xpress                   | Packe                    | t                        | Link                 | Speed          |                | Dire           | ction      |                | Sec                                       |
|--|-----------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|----------------------|----------------|----------------|----------------|------------|----------------|---|
| .0   | 8 ns                              |                          | Ack                      |                          |                          |                          | Gen3 I               | Field I        | )ecode         | PCIe-          | 101        |                | 32A                                       |
| 0  | 14 n                              | 3                        | Cpl                      |                          |                          |                          | Gen3 I               | rield I        | ecode          | PCIe-          | 102        |                | 343                                       |
| 1  | 21 n                              | 3                        | Update                   | FC-Cpl                   |                          |                          | Gen3 I               | rield I        | ecode          | PCIe-          | 102        |                | -<br>//////////////////////////////////// |
| l  | 28 n                              | 3                        | Cpl                      |                          |                          |                          | Gen3 I               | ield I         | )ecode         | PCIe-          | 101        |                | F70                                       |
| 2  | 30 n                              |                          | 1 ck                     |                          |                          |                          | Gen3 I               | Tield I        | ecode          | PCTe-          | 102        |                | FSC                                       |
| Is Header Payl                                     | oad Lane                          | s Traffi                 | ic Overvi                | ew LTS                   | SSM Ove                  | rview                    |                      |                |                |                |            |                | • ×                                       |
| ls Header Payl                                     | oad Lane                          |                          | ic Overvi                | ew LTS                   | SSM Ove                  | rview                    |                      |                |                |                |            |                | • ×                                       |
|  |                                   |                          | ic Overvi                | ii                       | SM Ove                   | rview                    | Lane 5               | Lane 6         | Lane 7         | Lane 8         | Lane 9     |                | -1  |
| Time   | PCIe-102                          | s Traffi                 | Newson                   | ii                       |                          | Name                     | Lane 5               | Lane 6         | Lane 7         | Lane 8         | Lane 9     |                | -1  |
| Time<br>( Symbol Time )                            | PCIe-102<br>Sample                | Lane 0                   | Lane 1                   | Lane 2                   | Lane 3                   | Lane 4                   | Construction and the | Succession.    | HERE STREET    | Action of      | stands and | L              | -1  |
| Time<br>( Symbol Time )<br>14ns                    | PCIe-102<br>Sample                | Lane 0                   | Lane 1                   | Lane 2<br>63             | Lane 3<br>43             | Lane 4                   | 00                   | 00             | 00             | 00             | 00         | L:<br>21       | -1  |
| Time<br>( Symbol Time )<br>14 ns<br>15 ns          | PCIe-102<br>Sample<br>0           | Lane 0                   | Lane 1<br>00<br>4D       | Lane 2<br>63<br>DC       | Lane 3<br>43<br>E3       | Lane 4<br>0A<br>00       | 00                   | 00             | 00             | 00             | 00         | L:<br>20<br>00 | -1  |
| Time<br>( Symbol Time )<br>14 ns<br>15 ns<br>16 ns | PCIe-102<br>Sample<br>0<br>0<br>0 | Lane 0<br>5F<br>68<br>00 | Lane 1<br>00<br>4D<br>00 | Lane 2<br>63<br>DC<br>00 | Lane 3<br>43<br>E3<br>00 | Lane 4<br>0A<br>00<br>00 | 00<br>00<br>00       | 00<br>00<br>00 | 00<br>00<br>00 | 00<br>00<br>00 | 00         | L:<br>21<br>00 | -1  |

The upper packet summary pane is similar to a Listing window except that its columns display packets and fields instead of bus/signal values. Like a Listing window, you can insert time or pattern markers.

The lower pane contains tabs for viewing selected packet details, header, payload, and lane information.

The Protocol Viewer window is customized for the protocol family for which the data is displayed.

You can add new Protocol Viewer windows using the Window menu. You can view Protocol Viewer windows that have already been added by choosing from the open window names at the bottom of the menu. If tabbed windows (see page 353) are turned on, you can also view Protocol Viewer windows by selecting the tab at the bottom of the window.

- Viewing the Packet Summary (see page 319)
  - To go to different locations in the displayed data (see page 320)
  - To re-arrange packet columns (see page 321)
  - To insert or delete packet columns (see page 321)
  - To show/hide parts of the packet summary display (see page 326)
  - To lockstep Protocol Viewer with other display windows (see page 327)

- Viewing a Selected Packet (see page 328)
  - To view and compare packet details (see page 329)
  - To view a packet header (see page 332)
  - To view a packet payload (see page 333)
  - To view a packet's lanes (see page 334)
  - To show/hide Protocol Viewer panes (see page 337)
- Changing Packet Summary Event Colors (see page 337)
- Changing Protocol Viewer Window Properties (see page 338)
  - To change the selected row box color (see page 339)
  - To change the Protocol Viewer font size (see page 340)
  - To lock scrolling with other display windows (see page 340)
- Changing Packet Summary Column Properties (see page 340)
  - To change the directions of a packet column (see page 342)
  - To change the width of a packet column (see page 342)
  - To change the alignment of a packet column (see page 342)
  - To change a packet column's number base (see page 343)
  - To select the marker for marker-relative times (see page 344)
  - To select fixed time units (see page 344)
- Viewing LTSSM States and Transitions (in the U4301 PCIe Gen3 Analyzer Online help).
- Viewing Decoded Transactions (in the U4301 PCIe Gen3 Analyzer Online help)
- Viewing Offline Performance Summary (in the U4301 PCIe Gen3 Analyzer Online help)
- Viewing PCIe Gen3 Packets (in the U4301 PCIe Gen3 Analyzer Online help)
- Customizing Protocol Descriptions for Protocol Viewer (in the online help)
- See Also To specify packet events (in "Find a packet" trigger function) (see page 175)
  - To find packet patterns in the captured data (see page 298)
  - "To specify packet patterns to filter" (in the online help)
  - Marking, and Measuring Between, Data Points (see page 271)
  - Displaying Names (Symbols) for Packet Summary Column Values (see page 269)
  - Searching the Captured Data (see page 294)

# **Viewing the Packet Summary**

The upper packet summary pane of the Protocol Viewer window is similar to a Listing window except that its columns display packets and fields instead of bus/signal values. Like a Listing window, you can insert time or pattern markers.

| Pac | kets         |       |                   |                   |           |              |
|-----|--------------|-------|-------------------|-------------------|-----------|--------------|
|     | Sample Numbe | Time  | PCI-Express Packe | Link Speed        | Direction | Sequence Num |
|     | 0            | 14 ns | Cp1               | Gen3 Field Decode | PCIe-102  | 343 Hex      |
| 2   | •            | 21 ns | UpdateFC-Cpl      | Gen3 Field Decode | PCIe-102  |              |
|     | 1            | 28 ns | Cpl               | Gen3 Field Decode | PCIe-101  | F70 Hex      |

Upper pane of the Protocol Viewer

Click a line to select a packet. Notice that a colored box highlights the selected line. You can use the up-arrow or down-arrow keys to select the previous or next packets.

- "To go to different locations in the displayed data" on page 320
- "To re-arrange packet columns" on page 321
- "To insert or delete packet columns" on page 321
- "To show/hide parts of the packet summary display" on page 326
- To lockstep Protocol Viewer with other display windows (page 327)

See Also • "Changing Packet Summary Event Colors" on page 337

- "Changing Protocol Viewer Window Properties" on page 338
- "Changing Packet Summary Column Properties" on page 340
- "Viewing a Selected Packet" on page 328
- "Marking, and Measuring Between, Data Points" on page 271
- "Searching the Captured Data" on page 294
- Viewing LTSSM States and Transitions (in the U4301 PCIe Gen3 Analyzer Online help).
- Viewing PCIe Gen3 Packets (in the U4301 PCIe Gen3 Analyzer Online help)

## To go to different locations in the displayed data

In the Protocol Viewer window, you can go to different locations in the captured data by using the vertical scroll bars, by using the Go To buttons on the standard toolbar, or by choosing Go To commands from popup menus.

To go to different 1 locations using toolbar buttons

 $\label{eq:click} 1 \ \ \ Click \ one \ of \ the \ Go \ \ To \ buttons \ in \ the \ standard \ toolbar.$ 

🗅 🖙 🖬 🎒 🖓 💏 📜 🔫 T 💌 🔍 🔍 🔫

| K | Go to Beginning — centers the beginning of the displayed data.   |
|---|--|
| T | Go to Trigger — centers the trigger point in the displayed data. |
| M | Go to End — centers the end of the displayed data.               |

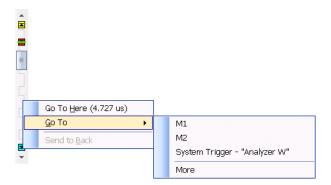
To go to different locations using popup/context menus 1 Right-click in the packet summary display area, and choose one of the **Go To** commands.

#### Packets

| Sample Number | Time   | PCI-Express Packet |                   | Link Speed | Sequence Number         | Dire     |  |
|---------------|--------|--------------------|-------------------|------------|-------------------------|----------|--|
| 9             | 114 ns | MemRd_             | 32 Gen3           |            | 347                     | Downs    |  |
| 10            | 118 ns | Ack                |                   | Gen3       | F5F                     | Downs    |  |
| 12            | 122 ns | MemRd_             | 32                | Gen3       | F75                     | Upsti    |  |
| 13            | 126 ns | Ack                | Copy Cell         |            | 32E                     | Upsti    |  |
| 11            | 130 ns | Mem                | Pin Row           |            | 348                     | Downs    |  |
| 14            | 139 ns | Mem                | PITROW            |            | F76                     | Upst     |  |
| 12            | 146 ns | IO I               | Goto              | •          | Time                    |          |  |
| 13            | 151 ns | Ack                | Goto Beginning of | Data       | Sample                  |          |  |
| 15            | 155 ns | IO I               | Goto End of Data  |            | M1                      |          |  |
| 16            | 159 ns | Ack                | Place Marker      | •          | System Trigger - "Downs | stream"  |  |
| 14            | 164 ns | Upd                |                   |            | Trigger - "Upstream"    | ci odini |  |
| 15            | 165 ns | Upd                | Find              |            | M2                      |          |  |
| 17            | 171 ns | Meml               | Find Next         |            | mz                      |          |  |
| 16            | 175 ns | Ack                | Find Previous     |            | More                    |          |  |
| 18            | 175 ns | Ack                | Properties        |            | 331                     | Upst:    |  |

You can choose **Beginning Of Data**, **End Of Data**, **Trigger**, a marker, a **Time**, or a **Sample**.

Or, click in the marker overview bar, and choose one of the Go To commands.



#### To re-arrange packet columns

- **1** Position the mouse pointer over the packet field column you want to move.
- 2 Click and hold the mouse button.
- 3 Drag-and-drop the packet decode column to its new position.

The column is placed to the left of the red position indicator that appears.

#### To insert or delete packet columns

- To insert packet<br/>columns1In the Protocol Viewer window, right-click in the column headings;<br/>then, choose Insert Column..., Insert Column Before..., or Insert<br/>Column After....
  - **2** In the Insert dialog, select the packet fields/column(s) you want to insert.

## 7 Analyzing the Captured Data

| 💥 Insert After PC   | l Express Packet 🛛 🔀                         |
|---|--|
| PCI Express     Control Express     Contr | k<br>ion<br>ad Fields                        |
| Search  | ٩  |
| Insert Options  |  |
| Insert Order:   | PCI Express Packet                           |
| Column Channels:  | Downstream Packet Decoder, Upstream Packet [ |
| Overlay Fields:   |  |
| Column Name:  | PCI Express Packet                           |
|   | OK Cancel                                    |

3 In the Insert Options area of the Insert dialog, you can:

- Specify the **Insert Order** by dragging items in the list to the desired order. (Clicking the "X" in the list removes the item.)
- Specify the **Column Channels** (directions) associated. For a more in-depth discussion, see: "Understanding Column Channels (Directions)" on page 322.
- Choose to **Overlay Fields**; that is, you can choose to include multiple fields in one column.
- When fields are overlaid, you can specify the Column Name.
- 4 Click OK.
- To delete selected<br/>packet columns1Highlight the headings of the columns you want to delete (by clicking,<br/>Shift-clicking, or Ctrl-clicking the column names).
  - 2 Right-click in (one of) the selected column heading(s); then, choose Delete>Column(s).

**Understanding Column Channels (Directions)** When a column is inserted into a Protocol Viewer, the Insert column dialog lets you optionally select the channels whose data is shown in the column:

a Proto

| 💥 Insert After PC   | l Express Packet 🛛 🔀                           |
|---|--|
| PCI Express     PCI Expre | k<br>ion<br>ad Fields                          |
| Search  | ٩  |
| Insert Options  |  |
| Insert Order:   | PCI Express Packet                             |
| Column Channels:  | Downstream Packet Decoder, Upstream Packet [ 💌 |
| Overlay Fields:   |  |
| Column Name:  | PCI Express Packet                             |
|   | OK Cancel                                      |

Figure 1 The Insert column dialog from the Protocol Viewer context menu

By default, columns are inserted with all channels selected. This means the new column will display the data for any of the available channels attached to the Protocol Viewer.

Channels are associated with directions which are simply another name for unidirectional links and represent the directional flow of protocol data along a particular network within the target platform's topology.

For example, say we have a bidirectional communication path between two PCI Express components: a root complex and a device as seen below:

|                 | Direction 1 (Upstream)   |        |
|-----------------|--------------------------|--------|
| Root<br>Complex | ,                        | Device |
| complex         | Direction 2 (Downstream) |        |
|                 |                          |        |

Figure 2 Two directions of PCI Express traffic

Assume that we are probing both directions of PCIe traffic by using a single PCIe Gen3 Analyzer module. In this case, we have two directions of PCI Express packet traffic being generated and then displayed using Protocol Viewer.

When inserting a new column within the Protocol Viewer window, you can specify for which of the channels the data in the inserted column should appear:

| 💥 Insert Before P   | CI-Express Packet                  | × |
|---|------------------------------------|---|
| PCI-Express<br>PCI-Exp<br>PCI-Exp<br>Packet F<br>Packet F | ress Packet<br>Fields<br>ed Fields |   |
| Search  |                                    | P |
| Insert Options  |                                    |   |
| Insert Order:   |                                    |   |
| Column Channels:  | All Channels                       |   |
| Overlay Fields:   |                                    |   |
| Column Name:  |                                    |   |
|   | OK Cancel                          |   |

Figure 3 Insert a PCI Express Packet column for both directions

For example, if you specify that a new PCI Express Packet column should show data for All Channels (directions), it looks like:

| Packets       |        |                        |            |
|---------------|--------|------------------------|------------|
| Sample Number | Time   | PCI-Express Packet     | Direction  |
| 10            | 112 ns | UpdateFC-NP (Gen3)     | Upstream   |
| 11            | 113 ns | UpdateFC-Cpl (Gen3)    | Upstream   |
| 9             | 114 ns | Memory Read 32b (Gen3) | Downstream |
| 10            | 118 ns | Ack (Gen3)             | Downstream |
| 12            | 122 ns | Memory Read 32b (Gen3) | Upstream   |
| 13            | 126 ns | Ack (Gen3)             | Upstream   |
| 11            | 130 ns | Memory Write 32b (Gen… | Downstream |
| 14            | 139 ns | Memory Write 32b (Gen… | Upstream   |
| 12            | 146 ns | I/O Read (Gen3)        | Downstream |
| 13            | 151 ns | Ack (Gen3)             | Downstream |
| 15            | 155 ns | I/O Read (Gen3)        | Upstream   |
| 16            | 159 ns | Ack (Gen3)             | Upstream   |

**Figure 4** A PCI Express Packet column that displays data for both the Upstream and Downstream directions

Alternatively, you can specify that a column be dedicated to certain channels (directions). Dedicating a column to certain channels (directions) can be useful when trying to visualize the flow of packets across a topology. For example, viewing the packets flow across both directions can be accomplished by creating two PCI Express Packet columns, each dedicated to a unique direction like:

| Packet | s      |                    |                    |            |
|--------|--------|--------------------|--------------------|------------|
| Sampl  | Time   | PCI-Express Packet | PCI-Express Packet | Direction  |
| 10     | 112 ns |                    | UpdateFC-NP        | Upstream   |
| 11     | 113 ns |                    | UpdateFC-Cpl       | Upstream   |
| 9      | 114 ns | MemRd_32           |                    | Downstream |
| 10     | 118 ns | Ack                |                    | Downstream |
| 12     | 122 ns |                    | MemRd_32           | Upstream   |
| 13     | 126 ns |                    | Ack                | Upstream   |
| 11     | 130 ns | MemWr_32           |                    | Downstream |
| 14     | 139 ns |                    | MemWr_32           | Upstream   |
| 12     | 146 ns | IO Rd              |                    | Downstream |
| 13     | 151 ns | Ack                |                    | Downstream |
| 15     | 155 ns |                    | IO Rd              | Upstream   |
| 16     | 159 ns |                    | Ack                | Upstream   |

Figure 5 Two PCI Express Packet columns that are each dedicated to a unique direction

Note that you can also use the **Show:Channels** button drop-down to specify the channels (directions) that should be displayed in the Packet summary.

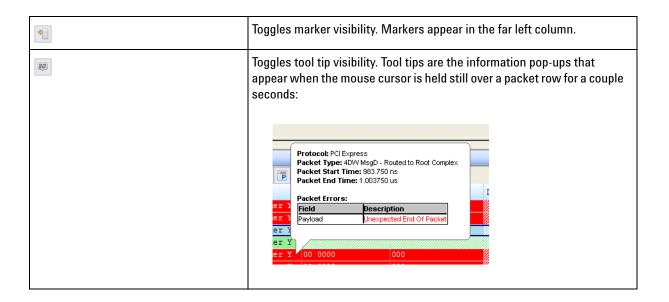
#### To show/hide parts of the packet summary display

1 Click one of the Show: buttons in the Packet Summary toolbar.



The Packet Summary toolbar contains the following Show buttons:

| Show: All Channels | Displays the column channels (directions) and allows you to select the<br>required directions for which data will be displayed in Protocol Viewer.<br>The channels you select here are displayed in the Direction column of<br>Summary pane. For more information, see "Understanding Column<br>Channels (Directions)" on page 322. |
|--------------------|---|
| <b>*</b>           | Resize columns based on column content.   |
| <b>*</b>           | Resize columns based on column headers.   |



The Packet Summary toolbar also contains the following Show buttons to show/hide Protocol Viewer panes (see page 337).

| H        | Toggles Header pane visibility from the Details pane.           |
|----------|---|
| P        | Toggles Payload pane visibility from the Details pane.          |
| <b>B</b> | Toggles Details pane visibility from the Details pane.          |
|          | Toggles Lanes pane visibility from the Details pane.            |
| 7        | Toggles Traffic Overview pane visibility from the Details pane. |
| 1        | Toggles LTSSM Overview pane visibility from the Details pane.   |

You can also make these selections in the **Pane Display Options** area of the Protocol Viewer Properties dialog box.

See Also • "Changing Protocol Viewer Window Properties" on page 338

#### To lockstep Protocol Viewer with other display windows

You can use the *Lockstep windows* feature to ensure that when a Protocol Viewer window is scrolled, other lockstepped windows are scrolled as well, such that the same time is centered in each lockstepped display window. This allows you to easily map and view correlated data in multiple display windows.

You can lockstep a Protocol Viewer window with display windows such as another Protocol Viewer, Waveform, Listing, or Compare.

- 1 From the Protocol Viewer toolbar, click the Lockstep windows toolbar button.
- 2 In the **Lockstep Windows** dialog, select the display window(s) whose scrolling should be locked with this window and specify any offset from this window.
- 3 Click OK to close the Lockstep Windows dialog.

**NOTE**: In Waveform Viewer and Listing, you can access the Lockstep Windows dialog by clicking Lockstep Windows... from the Window Properties tab of the display window's **Properties** dialog,

### **Viewing a Selected Packet**

When a packet is selected in the upper packet summary portion of the Protocol Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line), information about the selected packet appears in the lower part of the window.

| Show only Favorite Fields 🔽     | Favorites. Show-only-Favorite-Fields  |
|---------------------------------|---|
| Generated Fields                | <u> </u>  |
| Direction = PCle-102            |   |
| Size (Bytes) = 8 Decimal        | and the second se |
| -Link Speed = Gen3 Field Decode |   |
| Link Width = 16 Field Decode    |   |
| PCI-Express                     |   |
| Packet Fields                   |   |
| - SDP Token = F0AC Hex          |   |
| DLLP Type = UpdateFC-Cpl        | × .   |

Lower pane of the Protocol Viewer

- "To view and compare packet details" on page 329
- "To view a packet header" on page 332
- "To view a packet payload" on page 333
- "To view a packet's lanes" on page 334
- "To view LTSSM States and Transitions" on page 336
- "To show/hide Protocol Viewer panes" on page 337
- See Also "Viewing the Packet Summary" on page 319

#### To view and compare packet details

To view packet<br/>details1Select a packet in the upper packet summary portion of the Protocol<br/>Viewer window (by clicking on a line or by using the up arrow or down<br/>arrow keys to highlight the previous or next line).

2 Select the **Details** tab in the lower portion of the window.

| Show only Favorite Fields 🗸     | Favorites. Show-only-Favorite Fields V  |
|---------------------------------|---|
| Generated Fields                |   |
| Direction = PCle-102            |   |
| —Size (Bytes) = 8 Decimal       | car line in the second s |
| -Link Speed = Gen3 Field Decode |   |
| Link Width = 16 Field Decode    |   |
| PCI-Express                     |   |
| Packet Fields                   |   |
| SDP Token = FOAC Hex            |   |
| DLLP Type = UpdateFC-Cpl        | ×   |

Packet details are displayed in the left pane of the lower portion of the window.

If you hold the mouse pointer motionless for a second over one of the packets, a *tool tip* (that is, a small box with text) appears with more information.

**3** You can expand or collapse the displayed information by clicking "+" or "-" in the packet hierarchy tree.

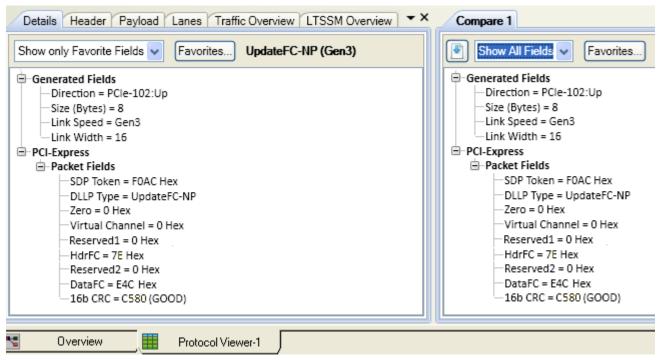
**To compare packet details** 1 In the lower pane of the window, display the details of the packet that you want to compare. To do this, select the required packet from the list of packets in the upper pane.

The details of the packet are now displayed in the lower-left pane. The Compare buffer in the lower-right pane is currently empty.

#### 7 Analyzing the Captured Data

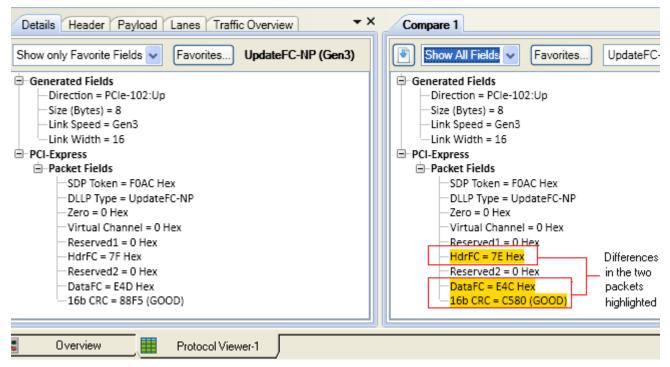
| Details Header Payload Lanes Traffic Overview LTSSM Overview - ×   | Compare 1                   |
|--|-----------------------------|
| Show only Favorite Fields Favorites UpdateFC-NP (Gen3)   | Show All Fields V Favorites |
| Generated Fields Direction = PCle-102:Up Size (Bytes) = 8 Link Speed = Gen3 Link Width = 16 PCI-Express Packet Fields SDP Token = FOAC Hex DLLP Type = UpdateFC-NP Zero = 0 Hex Virtual Channel = 0 Hex Reserved1 = 0 Hex HdrFC = 7E Hex Reserved2 = 0 Hex Reserved2 = 0 Hex |                             |
| DataFC = E4C Hex<br>—16b CRC = C580 (GOOD)   |                             |

2 Click the 🗾 button displayed in the Compare buffer in the lower-right pane. Clicking this button copies the details of the packet currently displayed in the lower-left pane to the compare buffer at the right.

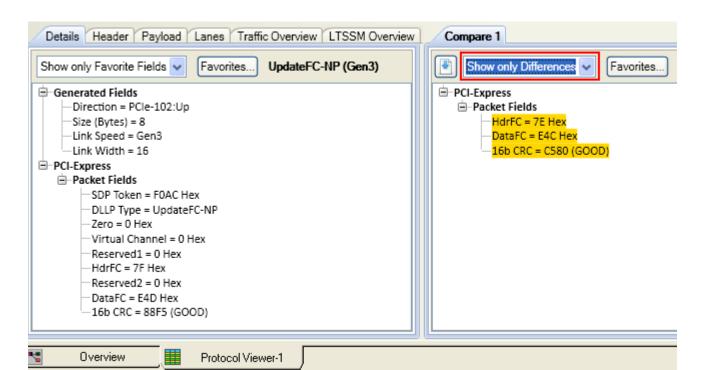


**3** From the list of the packets displayed in the upper pane, select the other packet with which you want to compare the packet already displayed in the compare buffer.

The details of the selected packet are now displayed in the lower-left pane and the differences between the two packets are highlighted in the compare buffer in the lower-right pane.



- **4** You can customize the display of packet information in the compare buffer as per the following options available in the compare buffer.
  - If you want to display only the differences between the two packets, then select the **Show only Differences** option from the listbox in the compare buffer.



- If you want to display only a few selected fields in the comparison, then click the **Favorites** button in the compare buffer, uncheck the fields that you do not want to display, and click **OK**. Finally, select the **Show only Favorite Fields** option from the listbox in the compare buffer. Doing so, displays only those fields in the lower pane that you selected for display. If you want to display the differences in only the favorite fields of the two packets, then select the **Show only Favorite Differences** option from the listbox in the compare buffer.
- If desired, you can change the name for the packet information displayed in the compare buffer. A text field next to the Favorites button in the compare buffer displays the packet type. You can alter this text while comparing packets.
- **See Also** "To view a packet header" on page 332
  - "To view a packet payload" on page 333
  - "To view a packet's lanes" on page 334
  - "To view LTSSM States and Transitions" on page 336

#### To view a packet header

- 1 Select a packet in the upper packet summary portion of the Protocol Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).
- 2 Select the Header tab in the lower portion of the window.

|      |        | -             | +0      | +1              |      | +2      |       |     | +3          |  |  |  |
|------|--------|---------------|---------|-----------------|------|---------|-------|-----|-------------|--|--|--|
|      | 7 6    | 5 4           | 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7654 | 3       | 2 1 0 | 7 6 | 5 4 3 2 1 0 |  |  |  |
|      | 0-04-0 | SDP Token     |         |                 |      |         | VC    | R   | HdrFC[7:2]  |  |  |  |
| e 0  |        | 0xF0AC        |         |                 |      |         | 0x0   | 0x0 | x0 0x19     |  |  |  |
|      | H[1:0] | R DataFC      |         |                 | 10   | 16b CRC |       |     |             |  |  |  |
| te 4 | 0x1    | 0x1 0x0 0x400 |         |                 |      | 0xEB24  |       |     |             |  |  |  |

If you hold the mouse pointer motionless for a second over one of the header fields, a *tool tip* (that is, a small box with text) appears with more information about the field.

3 If desired, you can select a different number Base.

• "To view and compare packet details" on page 329

#### See Also

- "To view a packet payload" on page 333
- "To view a packet's lanes" on page 334
- "To view LTSSM States and Transitions" on page 336

#### To view a packet payload

- 1 Select a packet in the upper packet summary portion of the Protocol Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).
- 2 Select the Payload tab in the lower portion of the window.

| Layout<br>Bytes Per Column: 1           | Columns I   | Per Row: 4  Column Byte Order Big Endian Uittle Endian |   |
|---|-------------|--|---|
| 000000000000000000000000000000000000000 | 00 01 02 03 |  |   |
| 000000000000000000004                   | 04 05 06 07 |  |   |
| 8000000000000000                        | 08 09 OA OB |  |   |
| 0000000000000000000000                  | OC OD OE OF |  |   |
| 000000000000000000000000000000000000000 | 10 11 12 13 |  |   |
| 0000000000000014                        | 14 15 16 17 |  |   |
| 00000000000000018                       | 18 19 1A 1B |  |   |
| 000000000000001C                        | 1C 1D 1E 1F |  |   |
| 000000000000000000000000000000000000000 | 20 21 22 23 | !"#  |   |
| 00000000000000024                       | 24 25 26 27 | \$% &'   |   |
| 0000000000000028                        | 28 29 2A 2B | () *+  |   |
| 000000000000002C                        | 2C 2D 2E 2F |  |   |
|   | 30 31 32 33 | 0123   | + |

Payload data bytes are displayed in the selected number of bytes per column and columns per row. The right-most column displays the row data in ASCII format.

- 3 You can format the display of payload bytes by selecting the **Bytes Per Column, Columns Per Row,** and **Column Byte Order** (when there is more than one byte per column).
- **See Also** To view and compare packet details (see page 329)
  - To view a packet header (see page 332)
  - To view a packet's lanes (see page 334)
  - "To view LTSSM States and Transitions" on page 336

#### To view a packet's lanes

- 1 Select a packet in the upper packet summary portion of the Protocol Viewer window (by clicking on a line or by using the up arrow or down arrow keys to highlight the previous or next line).
- 2 Select the Lanes tab in the lower portion of the window.

#### Lanes view in Protocol Viewer

The Lanes view in Protocol Exerciser shows vertical listing of packet data with respect to the logical lanes. In this view, you can see not just the packet data for the packet selected in the Summary pane but also the post packet data represented by different color codes. This helps you identify the start and end of data. The packet data in the lanes view is shown by the same color as used for the packet in the summary pane.

|             | Sample Numbe   | er Time   |  | PCI-Express Packet                               |  |  |  | Link Speed                             |  |  | Direction  |  |  |
|-------------|--|---|--|--|--|--|--|--|--|--|--|--|--|
| T           | 0  | 8 ns  |  | Ack  |  |  |  | Gen3 Field Decode                      |  |  | PCIe-101   |  |  |
|             | 0  | 14 n:   | 3  | Cpl  |  |  |  | Gen3 F                                 | ield I                                 | ecode                                  | PCIe-  | 102                                    |  |
|             | 1  | 21 n:   | 3  | UpdateFC-Cpl<br>Cpl                              |  |  |  | Gen3 Field Decode<br>Gen3 Field Decode |  |  |  |  |  |
|             | 1  | 28 n:   | 5  |  |  |  |  |  |  |  |  |  |  |
|             | 2  | 30 n.   | a<br>  | Lev  |  |  |  | Gen3 Field Decode                      |  |  | PCTe-102   |  |  |
|             | ils Header Payl  | PCIe-102  | s Traffi   | ic Overvi  | ew   LTS   | SM Ove   | rview  |  |  |  |  |  |  |
|             | 1  | 1   | Lane 0   | Lane 1   | ew   LTS   |  |  | Lane 5                                 | Lane 6                                 | Lane 7                                 | Lane 8   | Lane 9                                 |  |
|             | Time   | PCIe-102  | Ň  |  |  |  |  | Lane 5                                 | Lane 6                                 | Lane 7                                 | Lane 8   | Lane 9                                 |  |
|             | Time<br>( Symbol Time )  | PCIe-102<br>Sample  | Lane 0   | Lane 1   | Lane 2   | Lane 3   | Lane 4   | , costh crase                          | 4444.200                               | PLACE A                                | and the second s | 20010.000                              |  |
|             | Time<br>(Symbol Time)<br>14ns  | PCIe-102<br>Sample  | Lane 0<br>5F                                     | Lane 1<br>00                                     | Lane 2<br>63                                     | Lane 3<br>43   | Lane 4<br>0A   | 00                                     | 00                                     | 00                                     | 00   | 00                                     |  |
|             | Time<br>(Symbol Time)<br>14 ns<br>15 ns  | PCIe-102<br>Sample<br>0   | Lane 0<br>5F<br>68                               | Lane 1<br>00<br>4D                               | Lane 2<br>63<br>DC                               | Lane 3<br>43<br>E3                                     | Lane 4<br>0A<br>00                                     | 00                                     | 00                                     | 00                                     | 00   | 00                                     |  |
|             | Time<br>(Symbol Time)<br>14 ns<br>15 ns<br>16 ns   | PCIe-102<br>Sample<br>0<br>0<br>0                               | Lane 0<br>5F<br>68<br>00                         | Lane 1<br>00<br>4D<br>00                         | Lane 2<br>63<br>DC<br>00                         | Lane 3<br>43<br>E3<br>00                               | Lane 4<br>0A<br>00<br>00                               | 00<br>00<br>00                         | 00                                     | 00<br>00<br>00                         | 00<br>00<br>00   | 00<br>00<br>00                         |  |
|             | Time<br>( Symbol Time )<br>14 ns<br>15 ns<br>16 ns<br>17 ns  | PCIe-102<br>Sample<br>0<br>0<br>0<br>0                          | Lane 0<br>5F<br>68<br>00<br>00                   | Lane 1<br>00<br>4D<br>00<br>00                   | Lane 2<br>63<br>DC<br>00<br>00                   | Lane 3<br>43<br>E3<br>00<br>00                         | Lane 4<br>0A<br>00<br>00<br>00                         | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00   | 00<br>00<br>00<br>00                   |  |
|             | Time         ( Symbol Time )         14 ns         15 ns         16 ns         17 ns         18 ns                             | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0<br>0                | Lane 0<br>5F<br>68<br>00<br>00<br>00             | Lane 1<br>00<br>4D<br>00<br>00<br>00             | Lane 2<br>63<br>DC<br>00<br>00<br>00             | Lane 3<br>43<br>E3<br>00<br>00<br>00                   | Lane 4<br>0A<br>00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00   | 00<br>00<br>00<br>00<br>00             |  |
| <b>7</b> _r | Time           ( Symbol Time )           14 ns           15 ns           16 ns           17 ns           18 ns           19 ns | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0<br>0<br>0           | Lane 0<br>5F<br>68<br>00<br>00<br>00<br>00       | Lane 1<br>00<br>4D<br>00<br>00<br>00<br>00       | Lane 2<br>63<br>DC<br>00<br>00<br>00<br>00       | Lane 3<br>43<br>E3<br>00<br>00<br>00<br>00             | Lane 4<br>0A<br>00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00   | 00<br>00<br>00<br>00<br>00<br>00       |  |
| Deta        | Time         ( Symbol Time )         14 ns         15 ns         16 ns         17 ns         18 ns         19 ns         20 ns | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | Lane 0<br>5F<br>68<br>00<br>00<br>00<br>00<br>00 | Lane 1<br>00<br>4D<br>00<br>00<br>00<br>00<br>00 | Lane 2<br>63<br>DC<br>00<br>00<br>00<br>00<br>00 | Lane 3<br>43<br>63<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 4<br>0A<br>00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00   | 00<br>00<br>00<br>00<br>00<br>00<br>00 |  |

#### Context-menu of the Lanes view

If you right-click anywhere in the Lanes view, a context-menu is displayed.

| м1 | Time          | PCIe-101      |        |         |        |                              |          |        |        |          |        |     |
|----|---------------|---------------|--------|---------|--------|------------------------------|----------|--------|--------|----------|--------|-----|
|    | (Symbol Time) | Sample Number | Lane 0 | Lane 1  | Lane 2 | Lane 3                       | Lane 4   | Lane 5 | Lane 6 | Lane 7   | Lane 8 | Lan |
| M2 | 21 ns         | 0             | 00     | 00      | 00 00  |                              | 00       | 00     | 00     | 00       | 00     | 00  |
|    | 22 ns         | 0             | 00 00  |         | 00     | 00                           | 00       | 00     | 00     | 00       | 00     | 00  |
|    | 23 ns         | 0             | 00     | 00 00   |        | 00                           | 00       | 00     | 00     | 00       | 00     | 00  |
|    | 24 ns         | 0             | 00     | 00 00 🧰 |        | Lockstep •                   |          |        | Enable |          | d      | 00  |
|    | 25 ns         | 0             | 00     | 00      |        |                              |          |        |        | )isabled |        | 00  |
|    | 26 ns         | 0             | 00     | 00      | 10.00  | Channels<br>Color packets by |          |        | 00     | 00       | 00     | 00  |
|    | 27 ns         | 0             | 00     | 00      |        |                              |          | - t    | 00     | 00       | 00     | 00  |
|    | 28 ns         | 1             | 5F     | 00      |        | Display m                    | y mode i |        | 00     | 00       | 00     | 00  |
|    | 29 ns         | 1             | 26     | 3F      | AC     | 41                           | 00       | 00     | 00     | 00       | 00     | 00  |
|    | 30 ns         | 1             | 00     | 00      | 00     | 00                           | 00       | 00     | 00     | 00       | 00     | 00  |

You can use this menu to customize the display of data in the Lanes view. For instance, if you disable the Lockstep option, then the upper summary pane and the lower Lanes view of Protocol viewer are not synchronized. Clicking on a packet in the summary view does not show its details in the Lane view and vice versa. You can also choose to color the packet data in the Lanes view with the color of the packet in the Summary pane or not to color the packets data.

- **See Also** To view and compare packet details (see page 329)
  - To view a packet header (see page 332)
  - To view a packet payload (see page 333)

#### **To view LTSSM States and Transitions**

You can use the *LTSSM Overview* tab to display the LTSSM states and their transitions as detected from the PCIe data captured in a trace. To know more about how to view these states, refer to the topic **Viewing LTSSM States and Transitions** in the U4301 PCIe Gen3 Analyzer online help.

| Details Header Pa<br>Settings Data Rar | ayload  | Lanes Traffic Overvie | w LT | SSM | Overview                      |   |  |  |  |  |
|--|---|-----------------------|------|-----|-------------------------------|---|--|--|--|--|
|  | Setup Beginning Of Data 🗸 to: End Of Data 🔍 Compute 🚺 🛃 Go 1-+ out        |                       |      |     |                               |   |  |  |  |  |
| PCle-101:Down                          | PCIe-101:Down PCIe-101:Up CISSM from Beginning Of Data to PCIe-101:Down F |                       |      |     |                               |   |  |  |  |  |
| LO                                     |   | 10                    |      | ^   | Start of Trace -> L0          | 1 |  |  |  |  |
| Rcvr.RcvrLock                          | Gen3  | LO                    | Gen3 |     | L0 -> Rcvr.RcvrLock           | 8 |  |  |  |  |
| Rcvr.Speed                             |   | Rcvr.RcvrLock         | Gens | _   | Rcvr.RcvrLock -> Rcvr.Speed   | 4 |  |  |  |  |
|  |   | Rcvr.Speed            |      |     | Rcvr.Speed -> Rcvr.RcvrLock   | 4 |  |  |  |  |
| Rcvr.RcvrLock                          |   | Rcvr.RcvrLock         |      |     | Revr.RevrLock -> Revr.RevrCfg | 8 |  |  |  |  |
|  |   | Revr.RevrCfg          |      |     | Rcvr.RcvrCfg -> Rcvr.Idle     | 8 |  |  |  |  |
| Rcvr.RcvrCfg                           |   | Rcvr.Idle             |      |     | Rcvr.Idle -> L0               | 8 |  |  |  |  |
| Rcvr.Idle<br>L0                        |   | LO                    |      | ~   |                               |   |  |  |  |  |
| <                                      |   |                       | >    |     |                               |   |  |  |  |  |
| Noverview                              |   | Protocol Viewer-1     |      |     |                               |   |  |  |  |  |

#### To show/hide Protocol Viewer panes

1 Click the toolbar buttons in the Packet Summary toolbar to toggle the visibility of various panes.

|                    |   | 11 million | - |      | 1 |   |   |   | 2 | S. 7 |   |    |
|--------------------|---|------------|---|------|---|---|---|---|---|------|---|----|
| Show: All Channels | - |            | 相 | 1010 | D | H | P | L | T | τ    | đ | CS |

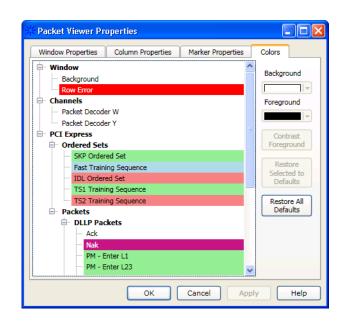
Alternatively, make these selections in the Pane Display Options area of the Window Properties tab in the Packet Viewer Properties dialog box.

**See Also** • Changing Protocol Viewer Window Properties (see page 338)

## **Changing Packet Summary Event Colors**

To change the colors associated with events in the Protocol Viewer window:

- **1** Right-click in the packet summary portion of the window, and choose **Properties...**.
- 2 In the Protocol Viewer Properties dialog, select the Colors tab.



- **3** In the Colors tab:
  - a Select the packet event type whose color you want to change.
  - **b** Select the **Background** color.
  - **c** Select the **Foreground** color or click **Contrast Foreground** to automatically get a color with good contrast to the selected background color.
- **4** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

To restore event<br/>color defaults1In the Protocol Viewer Properties dialog's Colors tab, click Restore All<br/>Defaults or Restore Selected Defaults.

- **2** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.
- See Also "Changing Protocol Viewer Window Properties" on page 338
  - "Changing Packet Summary Column Properties" on page 340

#### **Changing Protocol Viewer Window Properties**

You can change properties that affect the entire Protocol Viewer display window.

- 1 Right-click in the packet summary portion of the window, and choose **Properties...**.
- 2 In the Protocol Viewer Properties dialog, select the **Window Properties** tab.

| Packet Viewer Pr   | operties          |   |         |
|--|-------------------|---|---------|
| Window Properties Row Options Selected Row Font Size Error Display Line Wrap Show Field Name | Column Properties | Marker Properties                                       | Colors  |
| Color  | Packet Type       | Pane Display Packets Details Header                     | Options |
| Overlay Columns     Comma Delimited     Stacked Vertically     Concatenated                  |                   | <ul><li>Payload</li><li>Lanes</li><li>Markers</li></ul> |         |
|  | ОК                | Cancel  | ly Help |

- 3 In the Window Properties tab, you can:
  - Change the selected row box color (see page 339)
  - Change the Protocol Viewer font size (see page 340)
  - Lock scrolling with other display windows (see page 340)
  - Show/hide parts of the packet summary display (see page 326)
  - Show/hide Protocol Viewer panes (see page 337)
- **4** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.
- **See Also** Changing Packet Summary Event Colors (see page 337)
  - Changing Packet Summary Column Properties (see page 340)

#### To change the selected row box color

To highlight the selected line in the upper packet summary area of the Protocol Viewer window, a box is drawn around it.

1 In the Window Properties tab of the Protocol Viewer Properties dialog, click the **Selected Row** color selection button and select the desired highlight box color from the palette.

If you want to use a color that is not on the palette, click **Other...** to access the custom color dialog.

2 Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To change the Protocol Viewer font size

The font size property adjusts the data display and packet decode column heading text size.

1 In the Window Properties tab of the Protocol Viewer Properties dialog, enter the desired **Font Size**.

Fonts can range from size 6 through 72 points.

2 Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

As the font size is changed, the column width may be automatically increased to fit the new text size.

#### To lock scrolling with other display windows

You can lock display windows (for example, Waveform, Listing, Compare, etc.) so that when one window is scrolled, others are scrolled as well, such that the same time is centered in each display.

- 1 In the Window Properties tab of the Protocol Viewer Properties dialog, click Lockstep Windows....
- **2** In the Lockstep Windows dialog, select the display windows whose scrolling should be locked with this window and specify any offset from this window.

| Lockstep Wind      | ows                             |   |               |     |   |   |                        |
|--------------------|---------------------------------|---|---------------|-----|---|---|------------------------|
| Lockstep window(s) | Listing-1, Waveform-1           | - | and offset by | C s | - | + | from Protocol Viewer-1 |
|                    | <pre>empty&gt;  Listing-1</pre> |   |               |     | ( |   | OK Cancel              |

- 3 Click OK to close the Lockstep Windows dialog.
- **4** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### **Changing Packet Summary Column Properties**

In the Protocol Viewer display window, you can change the color, width, alignment, or number base of bus/signal data columns.

To change the properties of a bus/signal data column in the Protocol Viewer window:

1 Right-click on a packet decode column, and choose Properties....

Or, highlight the packet decode columns whose properties you want to change (by clicking, Shift-clicking, or Ctrl-clicking the column headings), and choose **Edit>Window Properties...** from the main menu.

| 🔆 Packet Viewer I | Properties                                 |
|-------------------|--|
| Window Properties | Column Properties Marker Properties Colors |
| Column            | PCI Express Packet  V Overlay              |
| Channels          | Packet Decoder Y                           |
| Color by          | All Channels                               |
| Width             | Packet Decoder W     Packet Decoder W      |
| Alignment         | Packet Decoder Y      Packet Decoder Y     |
| Base              | Packet Summary                             |
| Time Column Opt   | ions                                       |
| Marker            | Beginning Of Data 🐱                        |
| Use Fixed Un      | t 🔍  |
|                   |  |
|                   |  |
|                   |  |
|                   |  |
|                   | OK Cancel Apply Help                       |

2 In the Protocol Viewer Properties dialog's Column Properties tab:

You can:

- Select the **Column** to which the property changes apply. You can select:
  - Any packet decode column that is being displayed.
  - **<all>** packet decode columns.
  - **Overlay...** to include multiple fields in a column.
- "To change the channels (directions) of a packet column" on page 342
- "To change the width of a packet column" on page 342
- "To change the alignment of a packet column" on page 342
- "To change a packet column's number base" on page 343
- "To select the marker for marker-relative times" on page 344
- "To select fixed time units" on page 344
- **3** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.
- See Also "Changing Packet Summary Event Colors" on page 337
  - "Changing Protocol Viewer Window Properties" on page 338

#### To change the channels (directions) of a packet column

1 In the Protocol Viewer Properties dialog's Column Properties tab, check or uncheck the Channels **All Channels** checkbox.

If you want the column to display data for specified channels (directions) only, uncheck **All** and check the desired directions in the drop-down list.

If you want the column to display data for all channels (directions), check **All Channels**.

For more information, see "Understanding Column Channels (Directions)" on page 322.

**2** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To change the width of a packet column

TIP

You can autosize individual columns by placing the mouse pointer over the right border of the column header box; then, when the pointer icon changes to a resizing pointer, double-click.

## TIP

If your keyboard has a numeric keypad, you can autosize all columns by selecting any column header box (to highlight it) and by pressing **Ctrl** and "+" on the numeric keypad.

1 In the packet headings row of the Protocol Viewer window, position the mouse pointer over a column separator line; when the cursor changes to a resizing cursor, drag the column border.

#### Or:

1 In the Protocol Viewer Properties dialog's Column Properties tab, enter the **Width** value in pixels.

The minimum column width is 1 pixel, while the maximum width is 1000 pixels.

**2** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To change the alignment of a packet column

The Alignment property sets the display of data to be left-justified, right-justified, or centered within the column.

- 1 In the Protocol Viewer Properties dialog's Column Properties tab, select the **Alignment** from:
  - Left

- Center
- Right
- **2** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To change a packet column's number base

The base property specifies the number base to use when displaying the decoded packet values.

- 1 In the Column Properties tab of the Protocol Viewer Properties dialog, select the desired number **Base** from:
  - Binary
  - Hex
  - Octal
  - Decimal
  - **Signed Decimal** (two's complement, the only choice for the "Sample Number" column)
  - Ascii
  - Symbol (see Displaying Names (Symbols) for Bus/Signal Values (see page 269))
  - Hardware Address
  - Dot Notation
  - Field Decode

For the main packet decode information column, you can select from:

- Packet Summary
- Packet Bytes

For other generated packet columns, the only choice may be:

• String

If the "Time" column has been selected instead of a data column, your choices change from a numeric format to:

- Absolute
- Relative Previous
- Relative Marker
- **2** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To select the marker for marker-relative times

In the Protocol Viewer window, you can display times relative to a marker.

- 1 In the Column Properties tab of the Protocol Viewer Properties dialog, use the **Bus/Signal** selection to select the **Time** column.
- 2 For the Base property, select Relative Marker.
- **3** For the **Marker** property, select the marker to which relative times should be displayed.
- **4** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

#### To select fixed time units

In the Protocol Viewer window, you can display time column values with a fixed unit.

- 1 In the Column Properties tab of the Protocol Viewer Properties dialog, use the **Bus/Signal** selection to select the **Time** column.
- 2 In the Time Column Properties box, check Use Fixed Unit; then, select the desired time unit from the drop-down list.
- **3** Click **OK** to apply the changes and close the Protocol Viewer Properties dialog.

## Analyzing the Same Data in Different Ways (Using the Overview Window)

The Overview window lets you specify how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows. For example, you can display the same data filtered in one Listing window and unfiltered in another Listing window.

To analyze the same data in different ways:

- **1** Open or display the Overview window.
- 2 Add new windows.

If the Add New Window After dialog appears, select the module or tool that the new window should be placed after.

3 Add new tools.

If the New Tool dialog appears, select where the new tool should be placed.

For more information on using the Overview window, see:

- To open or display the Overview window (see page 345)
- To add, duplicate, or delete windows and tools (see page 346)
- To edit window or tool properties (see page 348)
- To rename windows, tools, and modules (see page 349)
- To redraw the Overview window (see page 350)
- To delete the Overview window (see page 350)
- **See Also** Overview Window (see page 491)
  - Waveform Display Window (see page 476)
  - Listing Display Window (see page 482)
  - Compare Display Window (see page 485)
  - Source Display Window (see page 486)
  - "Filter/Colorize Tool" (in the online help)
  - "Inverse Assembly Tools" (in the online help)
  - "Bus Analysis Tools" (in the online help)
  - "Tools" (in the online help)

#### To open or display the Overview window

- Select Tools>Overview.
- Select Window>Overview.

- If the Overview window is already open and you have Tabbed Windows (see page 353) turned on, you can display the Overview window by selecting the Overview tab at the bottom of the window.
- See Also Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)

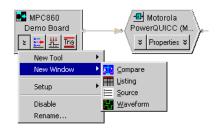
#### To add, duplicate, or delete windows and tools

You can add new listing and waveform display windows to the interface. As new windows are added, they appear in the list under **Window** in the menu bar. The active window will have a check mark. All available windows can be accessed either through the menu bar or through the use of tabs.

When you add a new tool to the logic analyzer's measurement configuration, its name appears at the bottom of the Tools menu. The tools interact with each other, so that you can progressively filter data or color parts of an inverse-assembled listing.

From the menu bar, select Window>New type....
If the windows are tabbed, you can also right-click on the tab and

- In the Overview window, right-click in the background, and select **New Window** from the popup menu.
- In the Overview window, select **New Window** from a module or tool menu.



select Window>New type....

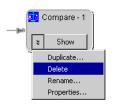
The new window is placed after the module or tool.

To delete

• From the window's menu in the menu bar, select **Delete**.

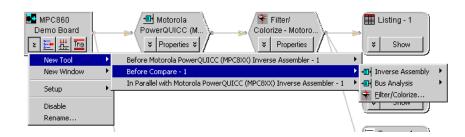
windows

- If the windows are tabbed, you can right-click on the tab and select **Delete**.
- In the Overview window, select **Delete** from the window's menu.



To add new tools • From the menu bar, select Tools>New type....

- In the Overview window, right-click in the background, and select **New Tool** from the popup menu.
- In the Overview window, select New Tool from a module or tool menu.

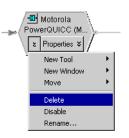


The new tool is placed after the module or tool.

If the tool you want is not listed, make sure that you have "installed" (in the online help) and licensed (see page 361) the tool.

Many tools come with a configuration file. Loading the configuration file will add the tool, as well as set up the bus names, symbols, or filters used by the tool.

To delete tools • In the Overview window, select Delete from the tool's menu.



**To duplicate** In the Overview window, you can duplicate windows from window menus. **windows** Duplicating a window is the same as adding a new window except that the new window has the same properties of the duplicated window.

TIP

#### 7 Analyzing the Captured Data



To delete1In the Overview window, select the connection you wish to delete.connections2Select Delete Connection.

| MPC<br>Dema | Board powerQUICC (M )  |
|-------------|--|
| Agilent Lo  | ogic Analyzer Question 🛛 🕅 🕅   |
| ?           | You are deleting the only connection to 'Filter/Colorize - 1'.<br>If you delete this connection, 'Filter/Colorize - 1' will also be deleted. |
|             | Do you want to continue?   |
|             | Yes No   |
|             |  |

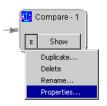
Deleting a connection has the effect of deleting the window or tool at the end of the connection.

**To add** There is no way to draw connections between modules, tools, and windows other than by adding new windows or tools. See: Connection Rules (see page 491).

- See Also Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)
  - To turn window tabs on/off (see page 353)

## To edit window or tool properties

**To edit window properties** In the Overview window, select the **Properties...** command from the window menu.



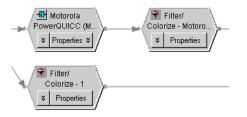
Or, from the menu bar, select the **Properties...** command from the window's menu.

Or, right-click in the display window and select the **Properties...** command from the popup menu.

- In the window's properties dialog, make the desired changes.
- Select **OK** to apply the changes and close the dialog.

**To edit tool** After adding a new tool such as a filter or inverse assembler, you can modify its properties as you refine your analysis of the data.

1 In the Overview window, click **Properties** on the tool.

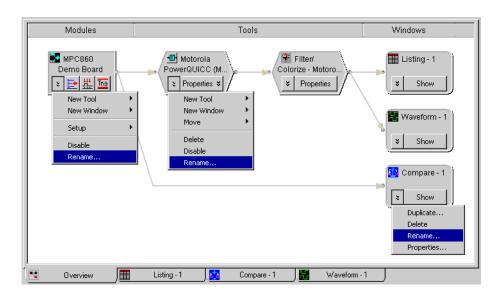


Or, from the menu bar, select Tools>tool name.

- 2 In the tool dialog box, change properties.
- 3 Select OK to apply the changes and close the box.
- See Also Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)
  - To set waveform window properties (see page 249)
  - To set listing window properties (see page 263)
  - To set Compare window properties (see page 307)

## To rename windows, tools, and modules

- **1** Display the Overview window.
- 2 Select the Rename... command from the window, tool, or module menu.



See Also • Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)

### To redraw the Overview window

- **1** Display the Overview window.
- 2 Select the Overview>Redraw command, or:

Right-click in the Overview window and select Redraw.

See Also • Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)

#### To delete the Overview window

- **1** Display the Overview window.
- 2 Select the Overview>Delete command, or:

If Tabbed Windows (see page 353) are turned on, right-click the Overview tab and select **Delete**.

See Also • Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)

## Setting the System Trigger and Skew Between Modules

When there are multiple *module* (see page 790)s in a logic analyzer or logic analysis system, there is a single Time=0 point for all modules. If one module arms another, the second module has a trigger that is not at Time=0 with respect to the first module. Because there is a single Time=0 point, when you see one module captures an event at Time=-435 ns and another module captures an event at -835 ns, you know the two events occurred 400 ns apart.

This means one module's trigger reference point must be designated the *system trigger* (which is *Time=0*).

You can specify the skew between the *system trigger* and the trigger reference points of other modules. When two modules are looking at the same data, you may want to specify skew so that the waveforms from the two modules line up.

In all display windows, there are global, immovable trigger markers for each module. The marker for the *system trigger* has a special icon.

Each display window has its own *Beginning Of Data* and *End Of Data* markers based upon the buses and signals displayed in that window. For example, if Bus1 is acquired on Logic Analyzer-1 and Bus2 is acquired on Logic Analyzer-2 and both buses are included in Viewer1, then the *Beginning Of Data* will be the earliest sample in either Logic Analyzer-1 or Logic Analyzer-2, and the *End Of Data* will be the latest sample in either Logic Analyzer-1 or Logic Analyzer-2. If Viewer1 only contains buses from Logic Analyzer-1, then its beginning and end of data are only based upon Logic Analyzer-1.

To set the system trigger and skew between modules:

- 1 From the main menu, choose Setup>Skew & System Trigger....
- 2 In the Module Skew and System Trigger dialog (see page 520), select the module whose trigger reference point is to be *Time=0* as the **System Trigger**.
- **3** To specify skew for other modules, enter the appropriate values in their **Skew** fields.
- **4** If you want the *system trigger* to be changed after the next run to the first module that triggers, check **First module to trigger designates the System Trigger**.
- 5 Click OK.

If a module is not the *system trigger*, the module icon in the Overview window is the standard logic analyzer icon:

## 7 Analyzing the Captured Data

|   | 16753A - 1 |
|---|------------|
| × | 📴 👯 🌆      |

When a module is designated the  $system \ trigger,$  an additional red "T" icon appears:



## **Using Display Windows**

- To add or delete display windows (see page 353)
- To turn window tabs on/off (see page 353)
- **See Also** To change the "Go to Trigger on Run" option (see page 204)

#### To add or delete display windows

You can add new listing and waveform display windows to the interface. As new windows are added, they appear in the list under **Window** in the menu bar. The active window will have a check mark. All available windows can be accessed either through the menu bar or through the use of tabs.

To add a new<br/>display windows1In the menu bar, click Window>New Listing or New Waveform. If the<br/>windows are tabbed, you can also right-click on the tab, then select<br/>New Listing or New Waveform.

To delete display<br/>windows1From the menu bar, click Window>Close. If windows are tabbed, you<br/>can also right-click on the tab, then select Close.

**See Also** • To turn window tabs on/off (see page 353)

#### To turn window tabs on/off

By default, the Listing and Waveform display windows are tabbed for ease of switching between displays.

To turn on or off window tabs, select View>Tabbed Windows.

| <mark>⊔st</mark> <u>F</u> ile | <u>E</u> dit | ⊻iew           | <u>S</u> etup          | <u>T</u> ools          | <u>M</u> arke | rs <u>R</u> un | /Stop | <u>₩</u> indow | <u>H</u> elp | )    |
|-------------------------------|--------------|----------------|------------------------|------------------------|---------------|----------------|-------|----------------|--------------|------|
|                               | •            | Zoo<br>Zoo     | m (in<br>m <u>O</u> ut |                        |               | <u>?</u> [#    | 0     | ର୍             | *            | 1 7  |
| <u>M1-</u>                    | M2= 5        | <u>I</u> 00    | lbars                  |                        | •             |                |       |                |              |      |
|                               |              | Eull           | Screen                 | F                      | 9             |                |       |                |              |      |
| 9                             | Samp         |                |                        | idows F                | 10<br>11      | E              | Bus 2 |                | Signa        | al 1 |
|                               |              | ✓ <u>S</u> tat | us bar                 | ۲<br>مربه <del>–</del> |               | =, 🖸           | XXXX  |                | $\mathbb{X}$ | -    |
| -                             | -7           |                |                        |                        | FЭ            |                |       | FF9            |              | 1    |
| -                             | -6           |                |                        |                        | FA            |                | 3     | FFA            |              | 1    |

To switch display windows when tabs are turned off, you must select **Window>"***display window name*".

**See Also** • To add or delete display windows (see page 353)

#### 7 Analyzing the Captured Data

## **Printing Captured Data**

There are three ways to create printed documentation of your measurement:

- To print captured data (see page 354)
- To copy text to the clip board (see page 355)
- To copy a screen to the clip board (see page 355)

**See Also** • To install a printer (see page 355)

• To connect a LAN (see page 355)

#### To print captured data

1 From the menu bar, select File>Print....

**NOTE** The first time you access the print dialog, you are asked to install a printer (see page 355). Follow the directions in the printer install dialogs that appear.

- 2 In the Print What section, select the desired display window.
- **3** To change the headers, footers, or margins, click **Options...** and specify the changes in the resulting dialog box. When you are done, click **OK**.
- 4 In the **Print range** section, select either:
  - All

files

- Time range
- Sample range
- Marker range

If you selected **Time**, **Sample**, or **Marker**, set the desired range by entering or selecting the **from** and **to** values.

5 Click **OK** to print the specified data.

Data is printed from the smallest time/sample to the largest.

**To print captured** Set up a generic/text only printer that prints to the "FILE:" port. In the **data to ASCII text** Windows **Add Printer Wizard**:

- **1** Select a **Local** printer. (Do not automatically detect and install a plug and play printer.)
- 2 Select the **FILE:** port.
- **3** Select the **Generic** manufacturer and the **Generic** / **Text Only** printer model.

After you have set up the generic/text only printer, you can print captured data to it just like any other printer.

Note that you can also export captured data to CSV format ASCII text files (see page 207).

- **See Also** To export data to CSV format files (see page 207)
  - To install a printer (see page 355)

#### To copy text to the clip board

- **1** From the listing display area, position the mouse cursor over the upper-left corner of the desired display region.
- 2 Click and hold the left mouse button, then drag the mouse cursor to the lower-right corner. Release the mouse button. A rectangle is drawn around the defined region (snaps to state lines and bus/signal columns).
- 3 From the shortcut list that appears, click Copy Text.
- 4 Open a word processor or spreadsheet program, paste the text into the program, and print the pasted data text.

#### To copy a screen to the clip board

- 1 Click **Edit>Copy Screen**. The currently displayed window is copied into the windows clip board buffer.
- **2** Paste the contents of the clip board buffer into a graphics editing program of your choice.
- **3** Print the screen from the graphics program.

#### To install a printer

Local and network printers are installed outside of the logic analyzer environment using the Windows printer install wizard.

- 1 Click Start>Settings>Printers.
- 2 Click on an existing printer, or click Add Printer.
- **3** Follow the Windows printer install wizard instructions.

**See Also** • To connect a LAN (see page 355)

#### To connect a LAN

Local area networks (LAN) are installed outside of the logic analyzer environment using the Windows network configuration wizard.

- 1 Click Start>Settings>Network and Dial-up Connections.
- 2 Click an existing connection, or click Make New Connection.

- **3** Follow the Windows network install wizard instructions.
- See Also
- , "16900-Series Logic Analysis System Installation Guide"
- > "16800-Series Logic Analyzers Installation/Quick Start Guide"
- > "1680-Series Logic Analyzers Quick Start/Installation Guide"
- "Changing the Windows XP Firewall Settings" (in the online help)
- Network Troubleshooting Guide (see page 402)

## **Extending Data Visualization/Analysis with VBA**

With the integrated Microsoft Visual Basic for Applications (VBA), you can extend the data visualization and analysis capabilities of the logic analyzer. For example:

- You can graph captured data in the VbaView window. You can create:
  - Line graphs.
  - XY scattergrams.
  - Horizontal and vertical bar charts.
  - Stacked horizontal and vertical bar charts.
  - Pie charts.

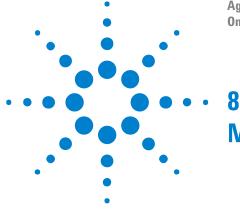
These charts are created in the VbaView window using the new VbaViewWindow and VbaViewChart COM automation objects.

Bar charts let you create histograms of bus values which can be helpful in analyzing system performance.

- You can create macros that perform analysis and compute statistics on captured data. For example, to detect setup and hold problems, you could look at two edges throughout a trace, compute the delta time between them, list the average, minimum, and maximum delta times. You could also automatically place markers on unusual events.
- You can export captured data to external applications (like Microsoft Excel, Microsoft Access, the Agilent 89600 Vector Signal Analyzer, MathWorks MATLAB, etc.) for post-processing and analysis. Using the VbaView window, you can plot post-processed data on the logic analyzer.
- See Also "Displaying Data in VbaView Windows" (in the online help)
  - "Using the Advanced Customization Environment (ACE)" (in the online help)

## 7 Analyzing the Captured Data

Agilent Logic and Protocol Analyzer Online Help



# **Managing Software Licenses**

- To view active software license information (see page 360)
- To activate software licenses (see page 361)
- To access floating license servers (see page 362)
- To borrow floating licenses and return them early (see page 364)

Starting with the 3.20 release of the *Agilent Logic Analyzer* application, you are able to order *floating* (also known as *counted*) licenses for tools and other add-in software. (Previously, all licenses were *node-locked*.)

**NOTE** With the 3.20 release of the *Agilent Logic Analyzer* application, you had to set up the LM\_LICENSE\_FILE environment variable to access floating license servers. Starting with the 3.30 release, license servers are accessed from within the *Agilent Logic Analyzer* application, and you *must not* use the LM\_LICENSE\_FILE environment variable any more.

Before you can use floating licenses, you need to set up a license server.

- See Also ► "License Server Administration Guide" for more information on setting up license servers for the Agilent 16900-series logic analysis systems and the 16800-series or 1680/1690-series logic analyzers.
  - Software Licensing Dialog (see page 534)



#### 8 **Managing Software Licenses**

## To view active software license information

- 1 From the main menu, choose Help>Software Licensing....
- 2 In the Software Licensing dialog's Summary tab (see page 534):

| Software Licensing Summary Activation Floating License Servers Borrow   | X    |
|---|------|
| Active Software Licenses  Active Software Licenses  Advanced Customization Environment - Runtime Package  Advanced Customization Environment - Runtime Package  Advanced Customization Environment - Runtime Package  Advanced Solution Software (ASI) Packet Analysis  Advanced Switching Interface (ASI) Packet Analysis  ARM11 and ARM7/9 ETM Inverse Assembler  ARM779 AHB Inverse Assembler  ABM7/9 Inverse Assembler  ABM7/9 Inverse Assembler  ABM7/9 Inverse Assembler  Copy to Clipboard | <    |
| OK Cancel Apply   | Help |

- You see all the software licenses that can be used.
- Red check marks show floating licenses that are already in use.
- Red "X"s show that software is not installed. •
- You can select a license and click Show Details... to see detailed information about the license.
- You can copy all licensing summary information to the clip board.

| NOTE     | When an "Advanced Customization Environment - Development Package" floating license is used, it is taken for the whole session. You must open a new configuration to return the license.                            |
|----------|---|
| NOTE     | When an "ASCII Remote Programming Interface Package" floating license is used, it is taken for as long as the <i>Agilent Logic Analyzer</i> application runs. You must close the application to return the license. |
| See Also | • To activate software licenses (see page 361)  |

- To activate software licenses (see page 361)
  - To access floating license servers (see page 362)
  - To borrow floating licenses and return them early (see page 364)

# To activate software licenses

- **1** Follow the instructions on the Entitlement Certificate you received with your software purchase.
- 2 From the *Agilent Logic Analyzer* application's main menu, choose Help>Software Licensing....
- **3** In the Software Licensing dialog's Activation tab (see page 535), copy the Licensing Host ID. You will need this when activating licenses.

| Software Licensing                                 |   |                       |                      |      |
|--|---|-----------------------|----------------------|------|
| Summary Activation F                               | loating License Servers                         | Borrow                |                      |      |
| To purchase Entitlement<br>http://www.agilent.com/ | t Certificate(s), contact yo<br>/find/contactus | our Agilent sales rep | resentative or go to |      |
| Licensing Host ID:                                 | 473ecb54  |                       |                      |      |
|  |   |                       |                      |      |
|  |   |                       |                      |      |
|  |   | OK Ca                 | incel Apply          | Help |

**4** Visit the Agilent license redemption web site. The URL should be printed on the Entitlement Certificate.

The license redemption web site will use the order number or other license activation code which is printed on the certificate, along with the Licensing Host ID, to generate a license file. The license file will be e-mailed to you.

**5** To install the license file and enable the software, follow the instructions in the e-mail that contains the license file.

Those instructions will tell you to install the license file in the proper directory on the logic analysis system or floating license server and restart the *Agilent Logic Analyzer* application or license server. On a logic analysis system, the license directory is usually "C:\Program Files\Agilent Technologies\Logic Analyzer\License\". For the proper directory on a license server, see the  $\checkmark$  "License Server Administration Guide".

The license file must have a .lic extension.

- **See Also** To view active software license information (see page 360)
  - To access floating license servers (see page 362)
  - To borrow floating licenses and return them early (see page 364)

# To access floating license servers

Before you can use floating licenses, you need to set up a license server (see  $\checkmark$  "License Server Administration Guide").

- 1 Open the *Agilent Logic Analyzer* application (with the default configuration) so that no floating licenses are in use.
- 2 From the main menu, choose Help>Software Licensing....
- **3** Select the Software Licensing dialog's Floating License Servers tab (see page 536).

| Software Licensing   |
|--|
| Summary Activation Floating License Servers Borrow                               |
| License Servers  |
| 27004@silk     Add Server     27000@dyuga06                                      |
| Delete Server  |
| Move Up  |
| Move Down  |
| Refresh  |
| NOTE: Servers are searched in order from top to bottom for available licenses.   |
| Green/Red status shows presence on network, not that a license server was found. |
| OK Cancel Apply Help   |

To add a floating license server

### 1 Click Add Server....

2 In the Add License Server dialog, enter the port number and name of the floating license server.



The port number is typically 27000, but it can be different depending on how the floating license server was set up.

### CAUTION

Only enter names of computers (or logic analyzers) that are floating license servers. Otherwise, the license manager interface hangs up for many minutes trying to determine if the computer is really a floating license server.

|   | 3 Click <b>OK</b> to close the Add License Server dialog.   |
|---|---|
|   | 4 In the Software Licensing dialog, click Apply.  |
| To move a server                                | 1 In the License Servers list, select the license server you want to move.  |
| up or down in the<br>search order               | 2 Click Move Up or Move Down.   |
|   | 3 Click Apply.  |
| To refresh floating<br>license server<br>status | 1 Click <b>Refresh</b> .  |
|   | The green or red server availability indicators are only a check of<br>whether the computer is on the network, not of whether the license<br>server software is running on that computer. |
| To delete a                                     | 1 In the License Servers list, select the license server you want to delete.  |
| floating license<br>server                      | 2 Click Delete Server.  |
|   | 3 Click Apply.  |
| See Also  | • , "License Server Administration Guide"   |
|   | • To view active software license information (see page 360)  |
|   | • To activate software licenses (see page 361)  |
|   | • To borrow floating licenses and return them early (see page 364)  |

### 8 Managing Software Licenses

# To borrow floating licenses and return them early

You can borrow floating licenses from a server for a period of time, for example, if you're taking a logic analyzer (or a computer running the *Agilent Logic Analyzer* application) out of the office (or just off the network). When a borrowed license's time expires, the license is automatically returned to the server. However, you can also return licenses early.

1 From the main menu, choose Help>Software Licensing....

**2** Select the Software Licensing dialog's Borrow tab (see page 537).

To access the Software Licensing dialog's Borrow tab

 Software Licensing

 Summary Activation Floating License Servers

 Borrow Licenses

 Click on the Borrow button to borrow additional licenses used by this configuration.

 Borrow
 until 11/ 9/2005

 Return Borrowed Licenses

 The following licenses cannot be returned while licenses are still checked out.

 Advanced Customization Environment - Runtime Package (returns 11/02/05 09:56:18)

 Return

 DK
 Cancel

 Apply
 Help

To borrow **1** Set up the configuration (or open a configuration file) that uses the floating licenses software you need to borrow licenses for. 2 Access the Software Licensing dialog's Borrow tab. 3 In the Borrow Licenses area, enter the date and time when the borrowed license will be returned. The default time is seven days. The minimum time is ten minutes. 4 Click **Borrow**. Repeat these steps to borrow additional licenses. To return floating When returning borrowed floating licenses early, all borrowed licenses licenses early must be returned. You are not able to return borrowed licenses while any licenses are checked out. 1 Open the Agilent Logic Analyzer application (with the default configuration).

- 2 Access the Software Licensing dialog's Borrow tab.
- 3 In the Return Borrowed Licenses area, click Return.

| Re | eturn Borrrowed Licenses  |
|----|---|
|    | The following licenses are currently borrowed for exclusive use on this system:                                   |
|    | 🖃 🎥 Advanced Customization Environment - Runtime Package (returns 11/02/05 09:59:37)<br>📒 📒 Borrowed from dvuqa06 |
|    | Return Click on the Return button to return all borrowed licenses early.  |

- **See Also** To view active software license information (see page 360)
  - To activate software licenses (see page 361)
  - To access floating license servers (see page 362)

# 8 Managing Software Licenses

Agilent Logic and Protocol Analyzer Online Help



# **Updating Software**

You may be able to install logic analyzer software from the logic analysis system's hard disk (depending on when it shipped from the factory or the application install CD that was last used).

To update, add, or remove logic analyzer software, or to remove the install packages from previous releases (and free disk space):

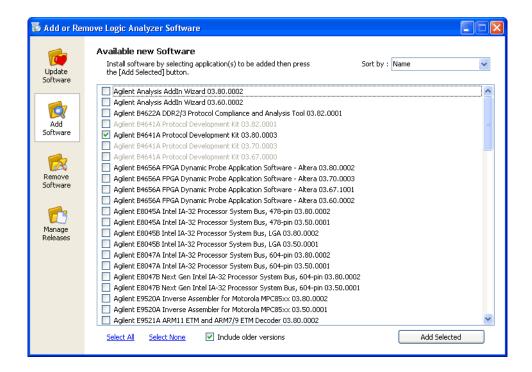
- 1 In the Agilent Logic Analyzer application, choose Help>Software Update....
- 2 In the Add or Remove Agilent Logic Analyzer Software tool:
  - To update software: click **Update Software** and select the software you want to update; then, click **Update Selected**.

| 🐻 Add or Rei                          | nove Logic Analyzer Software   |  |
|---------------------------------------|--|--|
| Update<br>Software                    | Available updates for currently installed software           Apply software updates by pressing the [Update Selected] button.         Sort by : Name   | *  |
|                                       | Name   | Size   |
| Add<br>Software<br>Remove<br>Software | <ul> <li>✓ Agilent B4655A Xilinx FPGA Dynamic Probe / E9524A MicroBlaze Trace Toolset 03.82.0001</li> <li>✓ Agilent Dbc3 Evefinder 03.82.0002</li> <li>✓ Agilent Inverse Assembler for Motorola PowerQUICC (8xx) 03.80.0002</li> <li>✓ Agilent License Manager 03.82.0001</li> <li>✓ Agilent PCI Express Packet Analysis Probe 03.80.0002</li> </ul> | 18.94MB<br>1.82MB<br>0.27MB<br>1.12MB<br>5.69MB<br>49.73MB |
|                                       | Select All Select None Upda  | te Selected  |

• To add software: click **Add New Software** and select the software you want to add; then, click **Add Selected**.

When adding new software, you can show all versions or just the latest version.

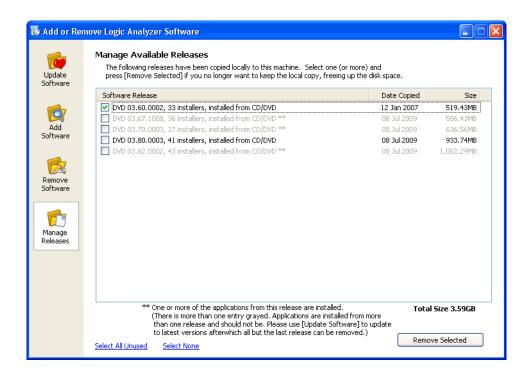




• To remove software: click **Remove Software** and select the software you want to remove; then, click **Remove Selected**.

| <b>.</b>                  | Currently Installed Software Uninstall software by selecting application(s) to be removed then Sort by | Name        |          |
|---------------------------|--|-------------|----------|
| date<br>tware             | press the [Remove Selected] button.  | : Name      |          |
|                           | Name   | Date Instal | Size     |
|                           | Agilent 16900, 16800, 1680, 1690 Logic Analyzer Software 03.82.0002                                    | 08 Jul 2009 | 317.96MB |
| <b>Q</b>                  | Agilent B4655A Xilinx FPGA Dynamic Probe / E9524A MicroBlaze Trace Toolset 03.67                       | 08 Jul 2009 | 18.94MB  |
| Add<br><sup>i</sup> tware | Agilent Bus Decoder for DDR2 and DDR3 03.81.9034   | 21 May 2009 | 1.82MB   |
| tware                     | Agilent DDR3 Eyefinder 03.81.9034  | 21 May 2009 | 0.27MB   |
|                           | Agilent Inverse Assembler for Motorola PowerQUICC (8xx) 03.50.0001                                     | 08 Jul 2009 | 1.12MB   |
|                           | Agilent License Manager 02.00.0000 **  | 08 Jul 2009 | 5.69MB   |
|                           | Agilent Logic Analyzer Demo Center 03.82.0002 **   | 08 Jul 2009 | 28.14MB  |
| move<br>tware             | Agilent Logic Update Tool 03.82.4012 **  | 09 Jul 2009 | 0.65MB   |
| tware                     | Agilent PCI Express Packet Analysis Probe 03.67.0000   | 08 Jul 2009 | 49.73MB  |
| inage<br>leases           |  |             |          |
|                           |  |             |          |
|                           |  |             |          |

• To remove old releases and free disk space: click **Manage Releases** and select the release whose files you want to remove; then, click **Remove Selected**.



Note that, when adding updating, or removing software, you can select all software or none, and you can sort the software list by name, version, size, or date.

- **See Also** You can also download and install the latest versions of logic analyzer software from the Agilent web site:
  - "http://www.agilent.com/find/la-sw-download"

# 9 Updating Software

Agilent Logic and Protocol Analyzer Online Help

# 10 Solving Problems

When troubleshooting problems or looking for more information, see:

- Software Installation Problems (see page 372)
- If starting in offline mode is unexpected (see page 373)
- If an ALA format configuration file won't open (see page 374)
- Interpreting Error Messages (see page 375)
- License Problems (see page 390)
- Translating Configuration Files from Other Logic Analyzers (see page 392)
- Running Self Tests (see page 395)
- Accessing Japanese Online Help (Windows XP) (see page 397)
- Network Troubleshooting Guide (see page 402)
- Remote Desktop Set Up (see page 405)
- If there are problems writing CDs on a 16900A, 16902A, or 16903A frame (see page 400)
- Hibernation Is Not Supported (see page 401)
- **See Also** For More Information (see page 406)
  - Intrinsic Support (see page 408)
  - Agilent Logic Analyzer Readme



# **Software Installation Problems**

Some problems that can occur when installing the *Agilent Logic Analyzer* application are:

• Installation Errors on 1680-Series Logic Analyzers (see page 372)

# **Installation Errors on 1680-Series Logic Analyzers**

When installing the *Agilent Logic Analyzer* application on a 1680-series logic analyzer, a fragmented hard disk drive can cause installation errors; for example, the version of the acquisition card FPGAs can be reported too slowly, resulting in an error.

Try defragmenting the 1680-series logic analyzer disk and performing the installation again.

# If starting in offline mode is unexpected

When starting the *Agilent Logic Analyzer* application on a logic analysis system or logic analyzer, you expect to connect to local hardware. If you have set up to auto-connect to a remote logic analysis system or logic analyzer, you expect to connect to the remote hardware. If the *Agilent Logic Analyzer* application starts in offline mode instead:

- It could be that the *Agilent Logic Analyzer* application is already running a local session. You can run multiple instances of the application, but if there's a local session is already running, additional instances start in offline mode.
- In the case of 1690-series logic analyzers (either local or remote), it could be:
  - Power to the logic analyzer is off.
  - An unplugged or loose IEEE 1394 cable.
  - A problem with the IEEE 1394 interface card in the personal computer.
- In the case where you have set up to auto-connect to a remote logic analysis system or logic analyzer, it could be:
  - The remote system is powered-down or off the network. In this case, you are given an information dialog about the system being offline before starting in offline mode.
  - The remote system is in the process of having its software updated.
  - The remote system software has been updated, resulting in an "incompatible remote service". In this case, make sure the same version of software is installed on the local computer or logic analysis system.

# If an ALA format configuration file won't open

If an ALA format configuration file won't open because modules are incompatible (that is, not in the same or similar logic analyzer families like the 16740/41/42A and 16750/51/52A/B), you can still load the setup information from the ALA format configuration file:

1 Load the incompatible ALA format configuration file in offline mode.

(If you're only interested in looking at the data, you can ignore the following steps.)

- **2** Save the configuration's setup information as an XML format configuration file (see To save a configuration file (see page 206)).
- 3 Go back online (see Returning to Online Analysis (see page 85)).
- **4** Open the XML format configuration file (see To open a configuration file (see page 220) and possibly To transfer module setups to/from multi-module systems (see page 224)).
- 5 Save the loaded setup information to an ALA format configuration file.

This procedure converts an incompatible ALA format configuration file into one that is compatible.

# **Interpreting Error Messages**

To locate the error you received, use the help window's Search tab to search for key words in the error message.

- Error Messages (see page 375)
- Warning Messages (see page 386)
- Informational Messages (see page 388)
- Eye Finder Info Messages (see page 388)
- **See Also** Solving Problems (see page 371)

## **Error Messages**

- Acquisition Errors (see page 376)
- Bus/Signal Errors (see page 376)
- File Errors (see page 379)
- Hardware Errors (see page 379)
- Help File Errors (see page 380)
- Import/Export and Translator Errors (see page 380)
- Naming Errors (see page 382)
- Tool Errors (see page 383)
- Trigger Errors (see page 384)
- **See Also** Interpreting Error Messages (see page 375)

### **Acquisition Errors**

| An acquisition<br>error has<br>occurred due to<br>state clock edges<br>occurring too<br>close together.<br>This could be the<br>result of: - Poor  | When in the state acquisition mode, the logic analyzer requires a clear clock signal no faster than the maximum state clock speed (see Specifications and Characteristics (see page 714)). Poor state clock quality may be caused by loading in the device under test. It may also be caused by a clock setup (see page 128) in the Sampling Setup dialog that is a combination of several signals which combined together violate the clock specification. When your clock setup uses multiple edges, the logic analyzer's setup/hold time typically increases (see Specifications and |
|--|---|
| state clock<br>quality (signal<br>integrity)<br>Inadequate probe<br>grounding (try   | Characteristics (see page 714)). When you are using a clock speed near the specification, grounding every second or third probe connection is recommended. <b>Bus/Signal Frrors</b>   |
| grounding (try<br>multiple grounds<br>around clock<br>signals) State<br>clock edges<br>spaced closer<br>than<br>specifications<br>allow Multiple<br>clocks selected<br>and spaced<br>closer than<br>specifications<br>allow. | Bus/Signal Errors   |
| Maximum of 128<br>channels per Bus.  | The logic analyzer cannot handle buses that contain more than 128 channels (signals). If you require wider buses, try breaking the bus into two or more buses, for example Data_HI and Data_LO.   |
| Cannot group into<br>Bus. Maximum of<br>128 channels per<br>Bus.   | The logic analyzer cannot handle buses that contain more than 128 channels (signals). If you require wider buses, try breaking the bus into two or more buses, for example Data_HI and Data_LO.   |

| The following<br>Bus/Signals are<br>required to have a<br>specific number<br>of assigned<br>channels because<br>they are locked.<br>Please correct<br>the following<br>Bus/Signals:<br>name (has num1<br>channels,<br>requires num2<br>channels) | Some tools may "lock" buses and signals that are necessary to produce<br>their output. The locked buses and signals may have their specific channel<br>assignments changed, but the total number of channels on each bus or<br>signal must stay the same. Please change the channel assignment for each<br>indicated bus or signal so that the width is <i>num2</i> . This message<br>sometimes appears in combination with the next one. In these cases, you<br>may have changed a configuration to use half the pods for sampling. Check<br>the sampling tab.  |
|--|--|
| Every Bus/Signal<br>requires at least<br>one assigned<br>channel. Please<br>assign channels<br>to the following<br>Bus/Signals:  | Every bus or signal requires at least one channel. If you do not see the Bus/Signal named in the error dialog, try scrolling the Bus/Signal listing. Certain tools may also have created buses or signals within folders. If you are trying to avoid showing extra information on the viewer, delete the row (see page 247) or column (see page 262) the bus or signal is in. This removes the information from the viewer without losing the bus/signal setup information. This message sometimes appears in combination with the previous one. In these cases, you may have changed a configuration to use half the pods for sampling. Check the sampling tab. |
| Minimum of one<br>Bus/Signal with<br>assigned<br>channels<br>required. Please<br>add a<br>Bus/Signal.  | The bus/signal setup cannot be closed because you have deleted all buses<br>and signals. Folders only contain buses and signals, but do not represent<br>data mappings of themselves. In order to close the dialog, select Add<br>Bus/Signal. Assign at least one channel to the new bus or signal.<br>Alternatively, you can select Cancel and revert to the previous bus and<br>signal assignments.  |
| name is locked<br>and cannot be<br>deleted because<br>it is required by<br>another tool in<br>the application. In<br>order to unlock it,<br>the following<br>tools must be<br>deleted: <i>tool</i>   | Some tools may "lock" buses and signals that are necessary to produce<br>their output. Until the tool is deleted via <b>Tools&gt;Overview</b> , you cannot<br>delete or rename the bus or signal.  |

| <i>name</i> is locked<br>and cannot be<br>renamed because<br>it is required by<br>another tool in<br>the application. In<br>order to unlock it,<br>the following<br>tools must be<br>deleted: <i>tool</i> | Some tools may "lock" buses and signals that are necessary to produce<br>their output. Until the tool is deleted via <b>Tools&gt;Overview</b> , you cannot<br>delete or rename the bus or signal.   |
|---|---|
| Cannot change<br>pod selection<br>while there are<br>locked<br>Bus/Signals.   | Some tools may "lock" buses and signals that are necessary to produce<br>their output. Until the tool is deleted via <b>Tools&gt;Overview</b> , you cannot<br>modify the bus or signal by changing the pod in use.  |
| Cannot delete<br><i>folder</i> because it<br>contains one or<br>more locked<br>children.  | Some tools may "lock" buses and signals that are necessary to produce<br>their output. The folder you have tried to delete contains a unique copy of<br>at least one locked bus or signal. You can move the locked buses or signals<br>outside the folder, and then delete the folder. Alternatively, you can delete<br>the tool locking the buses or signals via <b>Tools&gt;Overview</b> , and then delete<br>the folder. |
| Unable to set<br>setup and hold<br>times for this<br>Bus/Signal since<br>no channels have<br>been assigned.<br>Please assign<br>channels before<br>using setup and<br>hold.                               | The possible valid range of setup and hold values depends on the clock<br>setup used by the pods that the channels are attached to. Without<br>knowing which pods' channels are part of the bus or signal, it is<br>impossible for the logic analyzer to set appropriate ranges. Please assign<br>channels to the bus or signal, and then set setup and hold.   |
| Please enter a<br>user threshold<br>value.  | All pods will be set to the same threshold value. If you select OK without<br>setting a value, the current threshold values (at least one of which is<br>different from the rest) are retained. Please check the dialog and be sure<br>all fields are filled in.  |
| Please enter a threshold value.   | All pods will be set to the same threshold value. If you select OK without<br>setting a value, the current threshold values (at least one of which is<br>different from the rest) are retained. Please check the dialog and be sure<br>all fields are filled in.  |

### **File Errors**

Error trying to remove file: "*directory/*hardw are\_log.txt". When the logic analyzer is started up, it replaces the old hardware\_log.txt file. For some reason, this time the old hardware log was not able to be deleted. This could indicate a problem with the disk that the file is stored on.

File "*filename*" could not be opened. When the logic analyzer is started up, it creates a new hardware\_log.txt file. For some reason, this time the log was not able to be opened after creation. This could indicate a file system or disk problem.

### **Hardware Errors**

| Analyzer<br>Calibration Failed<br>[ <i>time</i> ] -<br>Instrument may<br>need service.   | The logic analyzer's pre-measurement calibration failed. Any data collected after receiving this error message is possibly incorrect. If the failure is transient, cycling power may fix the problem. If the failure is persistent, run <b>Help&gt;Self Test</b> or call your Agilent Sales Office to arrange for service.                                    |
|--|---|
| High speed<br>system clock<br>failure -<br>Instrument may<br>need service.<br>Sleep Duration<br>and Count:<br><i>duration,</i><br><i>counted</i> .                         | The internal 100 MHz clock did not pass initialization tests. Any measurements are likely to be faulty. Please contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus" for information on getting the instrument repaired.   |
| Contact with the<br>analyzer<br>hardware has<br>been lost. This<br>application will<br>be terminated.<br>You will have an<br>opportunity to<br>save your<br>configuration. | [1690A-series analyzers only] Something has interrupted the IEEE-1394 connection between the computer and the logic analyzer. Save your current work in a configuration (*.ala) file, then check the power to the logic analyzer hardware and the connections. A lost connection cannot be resumed; you will need to re-start the logic analyzer application. |
| I/O Channel<br>Error: Invalid<br>Request<br>Argument.  | [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.   |
| I/O Channel<br>Error: Offset Out<br>of Bounds.   | [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.   |
| I/O Channel<br>Error: Timeout.   | [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.   |

| I/O Channel<br>Error: System I/O<br>Error.   | [1690A-series analyzers only] There is a problem with the data being sent via the IEEE-1394 connection.   |
|--|---|
| I/O Channel<br>Error.  | [1690A-series analyzers only] There is an unspecified problem with the data being sent via the IEEE-1394 connection.  |
|  | Help File Errors  |
| Help file<br>information was<br>not found in the<br>registry. You may<br>need to reinstall<br>the tool.      | The logic analyzer could not find a registry entry for the help file<br>associated with the tool. If you have done a custom installation of the<br>tool, you must also install the help file to access help. If the problem<br>persists after re-installing, please contact Agilent Technologies sales or<br>support at "http://www.agilent.com/find/contactus" for assistance. |
| Help file<br>information not<br>found in registry.<br>Cannot display<br>help.                                | The logic analyzer could not find a registry entry for the help file<br>associated with the tool. If you have done a custom installation of the<br>tool, you must also install the help file to access help. If the problem<br>persists after re-installing, please contact Agilent Technologies sales or<br>support at "http://www.agilent.com/find/contactus" for assistance. |
| Help file not<br>found. Cannot<br>display help.  | The help file was not found where specified by the registry. It may have<br>been deleted or moved. You can search the drive where the logic analyzer<br>software is installed for .chm files, or re-install the tool.   |
| The HTML Help<br>file " <i>filename</i> "<br>was not found.<br>You may need to<br>re-install the<br>product. | The help file was not found where specified by the registry. It may have<br>been deleted or moved. You can search the drive where the logic analyzer<br>software is installed for the file, or re-install. To re-install, close the logic<br>analyzer application and run the setup program on the logic analyzer CD.   |
| The HTML Help<br>file " <i>filename</i> "<br>was not found.<br>You may need to                               | The help file for the tool was not found where specified by the registry. It may have been deleted or moved. You can search the drive where the logic analyzer software is installed for .chm files, or re-install the tool.  |
| re-install the tool.   | Import/Export and Translator Errors   |
| Refer to the<br>import files: <i>file1</i><br>and <i>file2</i> for more<br>details.                          | The configuration translator could not complete the translation. An explanation will be listed in <i>file1</i> or <i>file2</i> between " " and " " delimiters.  |
| The specified file<br>is NOT a 167xG<br>Analyzer<br>configuration file:<br><i>filename</i>                   | The configuration translator was not able to translate the specified file because it was not in an understood format. The configuration translator only translates configuration files generated by 1670G, 1671G, 1672G, and 1673G logic analyzers.   |

| Cannot read<br>configuration file<br><i>filename</i>   | The configuration translator was unable to read the configuration file<br>indicated due to an internal error in the configuration file.   |
|--|---|
| Cannot import an<br>empty file. Import<br>terminated.  | The file you tried to import has no content.  |
| Invalid non-ascii<br>character read.<br>Import<br>terminated.  | The logic analyzer only imports ASCII files. The file you tried to import<br>contains a non-ascii character. You can edit the file in any text editing<br>program, such as Notepad, to remove the character. Be careful to not<br>change header data or the number of samples.  |
| There are one or<br>more locked<br>bus/signals<br>required by<br>tool(s) currently<br>loaded in the<br>application. In<br>order to unlock<br>any of these<br>bus/signals, you<br>must unload<br>every tool listed<br>for that<br>bus/signal<br>Import<br>terminated. | Some tools may "lock" buses and signals that are necessary to produce<br>their output. Until the tool is deleted via <b>Tools&gt;Overview</b> , you cannot<br>delete, rename, or modify the bus or signal. A side effect of this is that<br>you cannot import a file that uses different buses and signals, or analyzer<br>channel count. |
| There were fewer<br>time data<br>samples than<br>indicated by the<br>NumberOfSample<br>s attribute of<br>Module tag.<br>Import<br>terminated.  | When you import a saved data file, the logic analyzer verifies that the data<br>is consistent. To fix this error, you can edit the file in any text editing<br>program, such as Notepad.  |
| Syntax error in<br>import file: <i>error.</i><br>Import<br>terminated.   | The error description indicates the syntax problem. Most often, it results from mismatched tags. Check the import file for any accidental deletions.  |
| No bus/signals<br>were valid for<br>importing. Import<br>terminated.   | The import file was created on a logic analyzer model with more pod pairs<br>than this one, and all the buses and signals were defined on pod pairs<br>this model does not possess. You can attempt to modify the file by<br>changing the assigned channels for the buses and signals. You can use any                                    |

text editing program (such as Notepad) to edit import files. For more information on the format of import files, see "XML Format" (in the online help) .

**Could not create file for export** The logic analyzer was unable to create the file. Possible reasons include not enough disk space or insufficient permissions to create the file where indicated.

Could not find<br/>required tag1The import file is required to have a section with the heading tag1<br/>completely contained within the section delimited by <tag2> and </tag2>.section contained<br/>within tag2You can repair the import file by adding <tag1></tag1> at the beginning of<br/>the tag2 section. You can use any text editing program (such as Notepad)<br/>to edit import files. For more information on the format of import files,<br/>see "XML Format" (in the online help) .

Invalid or missing<br/>attribute in tagThe import file requires the XML tag to include the keyword attribute and<br/>a value. For example, if attribute is Acquisition and tag is Sampling, the<br/>file has an XML tag of the form <Sampling></Sampling> but requires<br/><Sampling Acquisition="State"></Sampling></Sampling> but requiresSampling Acquisition="State"></Sampling>. You can repair the import<br/>file by adding attribute to the specified tag and giving it a value. (Try<br/>exporting a similar configuration to see standard values.) You can use any<br/>text editing program (such as Notepad) to edit import files. For more<br/>information on the format of import files, see "XML Format" (in the online<br/>help) .

Invalid attribute value for attribute in tag XML tag in the tag in tag in the tag in tag in tag in tag XML tag in tag XML tag in tag in

### **Naming Errors**

The object name<br/>cannot be an<br/>empty string.When you rename a viewer, tool, or bus, you must give it a name at least<br/>one character in length. The blank or empty name you tried was not<br/>accepted by the logic analyzer.

**Object name must**<br/>be unique.You have tried to rename a viewer, tool, or bus, but the name you entered<br/>is already being used and so was not accepted by the logic analyzer. You<br/>may appear to have identical names on some buses or signals, but these<br/>either are truncated or refer to the same bus (aliases).

| The name<br>" <i>toolname</i> " is<br>already in use.<br>Please choose a                         | You have tried to rename a tool, but the name you selected is already in<br>use. If you do not rename the tool, it will revert back to its previous<br>name.   |
|--|--|
| different name.  | Tool Errors  |
|  | For errors generated by specific inverse assemblers or bus analysis tools, go to the appropriate tool help.  |
| Could not load the<br>component - you<br>may need to<br>reinstall                                | This error occurs when there is a problem with the tool file. Possible<br>reasons are the tool file was renamed, or permissions changed so that the<br>logic analyzer cannot open it. To reinstall the tool file, close the logic<br>analyzer and run the setup program on the logic analyzer CD.                      |
| Could not get<br>license<br>information for<br>component   | The logic analyzer attempted to determine if the tool was licensed or<br>freely available, but could not find the information. Try re-installing the<br>tool.  |
| Could not obtain<br>license<br>information for<br>component                                      | This error means the logic analyzer is missing some information it needs<br>in order to check the license. Licenses are created by the lmtools.exe<br>program. You can run this to see what information is missing, and to<br>check licenses.  |
| Could not obtain a<br>license for<br>component   | This error occurs when the license is not in the expected directory. When<br>the tool is installed, the license is written into a predefined directory.<br>Moving or deleting the file prevents you from using the component. If you<br>do not believe the license was deleted, check your hard drive for *.lic files. |
| License for<br>component is<br>invalid   | This error means that a license file exists, but that the information in it does not match. Licenses are specific to equipment; you cannot transfer a license for a tool or a logic analyzer between tools or logic analyzers.   |
| Could not create<br>licensed<br>component  | There was a valid license for the tool earlier in the install process, but<br>something has gone wrong. Start the tool installation process over again. If<br>this error persists, please contact Agilent Technologies sales or support at<br>"http://www.agilent.com/find/contactus" for assistance.                  |
| Could not create<br>component -<br>unknown error   | A license for the tool exists in the proper directory, but the internal<br>information is inconsistent. Licenses are specific to equipment; you cannot<br>transfer a license between tools or between logic analyzers. If this is a<br>corrupt license, try reinstalling the tool again.                               |
| The stored tool<br>could not be<br>restored from file.<br>The tool may have<br>been uninstalled. | The configuration file you are trying to load includes a licensed tool. The logic analyzer was not able to find this tool, so some information will be missing. All buses and signals that were based on physical data will be loaded; buses and signals created by the tool will not.                                 |

| The selected tool:    | The configuration file you are trying to load includes a licensed tool. The |
|-----------------------|---|
| <i>Name</i> could not | logic analyzer was not able to find this tool, so some information will be  |
| be loaded.            | missing. All buses and signals that were based on physical data will be     |
|                       | loaded; buses and signals created by the tool will not.                     |

The selected tool<br/>could not be<br/>loaded.The configuration file you are trying to load includes a licensed tool. The<br/>logic analyzer was not able to find this tool, so some information will be<br/>missing. All buses and signals that were based on physical data will be<br/>loaded; buses and signals created by the tool will not.

The tool could not<br/>be created - you<br/>may need toThe configuration file you are trying to load includes a licensed tool. The<br/>logic analyzer was not able to find this tool, so some information will be<br/>missing. All buses and signals that were based on physical data will be<br/>loaded; buses and signals created by the tool will not.

The analysis tool<br/>(toolname) could<br/>not be restored<br/>from theThe configuration file you are trying to load includes a licensed tool. The<br/>logic analyzer was not able to find this tool, so some information will be<br/>missing. All buses and signals that were based on physical data will be<br/>loaded; buses and signals created by the tool will not.configuration file.

### **Trigger Errors**

Only one action per timer per branch is allowed.
A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 584), may have multiple branches. Within a branch, only one of Start from reset, Stop and reset, Pause, or Resume is allowed per timer. For more on timers, see To configure a timer (see page 165).

Only one action per counter per branch is allowed.
A branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 584), may have multiple branches. Within a branch, you can not both Increment and Reset the same counter. You can increment one and reset the other. For more on counters, see To configure a counter (see page 166).

Only one store action per branch is the collection of actions after a "Then" in an Advanced Trigger step. Some steps, such as Advanced 2-Way Branch (see page 584), may have multiple branches. Within a branch, you can set Store sample or Don't store sample but not both in the same branch. If you do not specify any store actions, default storage (see page 179) is used.

Only one reset<br/>occurrenceA branch is the collection of actions after a "Then" in an Advanced Trigger<br/>step. Some steps, such as Advanced 2-Way Branch (see page 584), may<br/>have multiple branches. Within a branch, you can only specify Reset<br/>occurrence counter once.

No more edge resources available for this pod pair.

allowed.

The logic analyzer hardware can only handle two edge statements per pod pair in *Full Channel Timing Mode* (see page 635) or *Half Channel Timing Mode* (see page 635), or one edge statement per pod pair in *Transitional* / *Store Qualified Timing Mode* (see page 635). If the edges are on different signals, try probing one of the signals with another channel on another pod pair. If all the edges are being used on the same signal, replace the "either edge" terms with "rising edge OR falling edge". See To insert events (see page 185) for how to replace "either edge".

No more pattern resources available for this pod pair

BranchThe expression in one of the branches of the trigger specification is too<br/>complicated for the logic analyzer. The logic analyzer first combines all<br/>AND terms and then ORs the expressions together. AND terms that have<br/>more than 4 events use twice the resources. Try rewriting the branch<br/>expression to use more OR terms, or delete some events.

One situation that leads to this error is using the **In Range** and **Not In Range** operators with buses that span more than 2 pod pairs. These operators are limited to buses that span 2 or fewer pod pairs (up to 64 bits wide).

TriggerAlthough no single branch expression is too complex, the total number ofSpecification is<br/>too complexANDs and ORs has exceeded the logic analyzer's resources. Try simplifying<br/>some expressions in some steps, or removing steps altogether.

Replacement<br/>failed. Maximum<br/>number of<br/>sequence stepsThe logic analyzer translates the trigger you specified into internal<br/>sequence steps. Different trigger functions use different numbers of<br/>internal sequence steps. Also, the "trigger and fill memory" action requires<br/>an additional internal sequence step each time it is used in state<br/>acquisition mode. One possible way to simplify the trigger specification is<br/>to replace all other "trigger and fill memory" actions with a "goto N" action<br/>that points to a "Find anything then trigger and fill memory" step.

Unable to insert<br/>step. The<br/>maximum<br/>number of<br/>sequence stepsThe logic analyzer translates the trigger you specified into internal<br/>sequence steps. Different trigger functions use different numbers of<br/>internal sequence steps. Also, the "trigger and fill memory" action requires<br/>an additional internal sequence step each time it is used in state<br/>acquisition mode. One possible way to simplify the trigger specification is<br/>to replace all other "trigger and fill memory" actions with a "goto N" action<br/>that points to a "Find anything then trigger and fill memory" step.

**Too many sequence steps.** The logic analyzer translates the trigger you specified into internal sequence steps. Different trigger functions use different numbers of internal sequence steps. Also, the "trigger and fill memory" action requires an additional internal sequence step each time it is used in state acquisition mode. One possible way to simplify the trigger specification is to replace all other "trigger and fill memory" actions with a "goto N" action that points to a "Find anything then trigger and fill memory" step.

| Goto action<br>specifies an<br>undefined step.                                     | The last step in the trigger sequence includes the action "Goto next".<br>Because there is no next step, the logic analyzer cannot run and look for<br>a trigger. Select <b>Setup&gt;(Logic Analyzer Module)&gt;Advanced Trigger</b> , and<br>change the action for the last trigger step.   |
|--|--|
| Counter event<br>specified both<br>true and false in<br>the same product<br>term   | In the trigger specification, at least one branch ANDs together "bus equals X" and "bus not equal X". Because this condition can never be true, the logic analyzer will not trigger and does not start the acquisition. If you intend to have it run until you press stop, use the trigger function Run Until User Stop, found under the "Other" tab in advanced trigger.                                |
| Cannot use <,<br><=, >, >= for a<br>bus with clock<br>bits that spans<br>pod pairs | You have defined a bus that both spans pod pairs and includes a clock bit. The clock bits are numbered the same as the pod they are located on, and it is possible for them to be the channel that is not on the same pod pair as the others. Check the channel assignment in the Buses/Signals (see page 499) tab of the Setup dialog. The logic analyzer will not run until this problem is corrected. |
| Cannot specify a<br>range on a bus<br>with clocks bits<br>that spans pod<br>pairs  | You have defined a bus that both spans pod pairs and includes a clock bit. The clock bits are numbered the same as the pod they are located on, and it is possible for them to be the channel that is not on the same pod pair as the others. Check the channel assignment in the Buses/Signals (see page 499) tab of the Setup dialog. The logic analyzer will not run until this problem is corrected. |

# **Warning Messages**

You are currently running "Offline," so running the analyzer is not possible. If you wish to create "fake" data while offline, go to "Edit -> Options" and select "Create **Data When Offline**". Note: This setting is persistent from session to session.

The logic analyzer is running in offline mode. Offline mode means that the logic analyzer software does not have access to logic analyzer or logic analysis system hardware. If you have a logic analyzer attached, please check the connection. For more on running with fake data, see Options Dialog (see page 522). Fake data is useful when learning how to use the logic analyzer software.

| This module is<br>already being<br>used by another<br>instance of the<br>application. You<br>are now working<br>Offline.                                     | The logic analyzer hardware is attached to an open instance of the logic<br>analyzer software. If you need to acquire data, locate that instance from<br>the Windows taskbar. The Local/Remote/Offline indicator is at the bottom<br>of the application window. In offline mode, the software can still work<br>with saved data.  |
|--|---|
| Event specified<br>both true and<br>false in the same<br>product term  | In the Advanced Trigger dialog, one of the branches for one of the steps<br>checks that an event is both true and not true. An event may be a bus or<br>signal equal to a value, a timer expiring, or a count exceeding some value.<br>Because of the AND combination, the branch cannot be true. You may<br>want to modify the trigger to use either an OR combination of the events,<br>or separate them into different branches or steps. For more on<br>constructing complex triggers, see To replace or insert trigger functions<br>into trigger sequence steps (see page 169). For more on how to interpret<br>the trigger sequence, see Reading Event and Action Statements (see<br>page 165). |
| Timer <i>n</i> value<br>checked as an<br>event, but no start<br>action specified.  | In the Advanced Trigger dialog, the trigger sequence checks the value of a timer that was never started. Timers need to be explicitly started in a previous trigger step. See To configure a timer (see page 165) for more information.   |
| Counter <i>n</i> value<br>checked as an<br>event, but no<br>increment action<br>specified.   | In the Advanced Trigger dialog, the trigger sequence checks the value of a counter that is never incremented. Counters need to be incremented in the action statements of a trigger step. See To configure a counter (see page 166) for more information.   |
| The Bus/Signals<br>listed below<br>could not be<br>loaded from the<br>configuration file.<br>Please recheck<br>your Trigger since<br>it may have<br>changed. | The configuration file you just loaded was created on a logic analyzer with<br>more pods than this model. Because of this, some buses and signals which<br>rely on the additional pods could not be loaded. If these buses or signals<br>were used in the trigger sequence, the trigger sequence will have changed.<br>You may be able to work around this by assigning different channels to<br>the affected buses and signals, and re-creating the trigger sequence.  |
| Slow or missing<br>clock in Trigger<br>Step <i>n</i>   | The logic analyzer is not able to detect the state clock, and is therefore<br>unable to take samples and evaluate the trigger sequence. If your device<br>under test's clock is bursty, this may be expected behavior. If it is not,<br>please check all probing connections. To verify the clock signal is being<br>received, you can assign the clock channels to a bus in timing acquisition   |

mode and acquire data.

### **Informational Messages**

- **Filling memory after trigger...** The logic analyzer has triggered and is filling memory. Due to either a slow clock or storage qualification in state acquisition mode, or infrequent transitions in transitions-only timing acquisition mode, the logic analyzer is taking enough time to fill memory that this message is showing.
- **Trigger inhibited** The logic analyzer is in timing acquisition mode. In timing acquisition **during prestore...** The logic analyzer fills the designated amount of memory before searching for the trigger. If this message is showing, the logic analyzer is filling memory and has not yet begun to compare data to the trigger sequence. To capture triggers that happen during the beginning of a device under test's boot sequence, be sure to set the trigger position in the Sampling tab to 100% poststore.
- Waiting in TriggerThe logic analyzer is waiting for a sample that matches the events defined<br/>in step n of the trigger sequence. Sometimes the event is rare, causing<br/>long waits. If you feel that the logic analyzer should have triggered already,<br/>check the trigger sequence in Advanced Trigger. For more on triggering,<br/>see Specifying Advanced Triggers (see page 163).

### **Eye Finder Info Messages**

|  | These messages appear in the Thresholds and Sample Positions dialog (a page 550) after an <i>eye finder</i> measurement is run.   |  |  |
|--|---|--|--|
| "Clock signal in<br>Fast State Mode<br>is divided by<br>two."                | This message only appears with 16753/54/55/56 and 16950 logic analyzers.  |  |  |
| "Demo: Results<br>will not be used<br>for analysis."                         | This channel was measured when "Demo Mode (no probes required)" was<br>selected in the Run Mode tab of the Eye Finder Advanced Options dialog<br>(see page 555). The data shown are typical of <i>eye finder</i> operation, but<br>the sample position setting shown is NOT used. (The manual setting is still<br>in use.)  |  |  |
| "No signal<br>activity. Check<br>connection,<br>threshold, and<br>stimulus." | <ul> <li>This channel appears to be completely quiet.</li> <li>Check the probe connection between the analyzer and the device under test.</li> <li>Check the threshold voltage setting (see Setting the Logic Analyzer Threshold Voltage (see page 102)).</li> <li>Check that the device under test is turned on and is running the appropriate diagnostic or other stimulus program.</li> <li>If all these things are set up correctly, activity will be shown in the</li> </ul> |  |  |

If all these things are set up correctly, activity will be shown in the Analyzer Setup dialog's Buses/Signals tab (see page 499).

| "No stable   | Two common possibilities exist:   |
|--|---|
| regions. Check<br>clock and<br>thresholds."                            | <ol> <li>The signal on this channel is asynchronous to the clock defined for the logic analyzer. If this is the case, there is no stable relationship between the times when the signal switches and when the clock arrives.</li> </ol>   |
|  | If you expect the signal to be sampled synchronously you must redefine<br>the clock for this signal.  |
|  | <b>2</b> The stable region(s) are too small for <i>eye finder</i> to detect.  |
|  | In this case you must resort to adjusting the sample position manually<br>and checking its validity by running an ordinary analyzer measurement<br>to see if the data values you expect are sampled. You can adjust the<br>sample position manually by selecting the arrow buttons or by dragging<br>the blue sampling position indicator in the display. |
| "No voltage scan:<br>Channel in pod<br>with assigned<br>clock."        |   |
| "One or more<br>stable regions<br>found."                              |   |
| "Only a few<br>transitions<br>detected. Change<br>stimulus or          | The signal on this channel was observed to toggle fewer than 500 times.<br>The characterization may be accepted as it stands or you may wish to<br>change the stimulus program or diagnostic in the device under test to<br>increase the toggle rate.   |
| increase<br>measurement<br>duration."                                  | Another option is to select "Long" in the Measurement Duration tab of the Eye Finder Advanced Options dialog (see page 555). Using the "Long" setting won't necessarily make the message go away, but it will ensure that <i>eye finder</i> has the opportunity to observe a more significant number of transitions on the channel.                       |
| "Stable region at<br>N ns is an<br>estimate."                          | This message only appears for certain bus probes (not general purpose probes).  |
| "The stable<br>region extends<br>beyond the limits<br>of the display." | This channel is active, but the signal does not switch within 5 ns before or after the clock. For example, this could occur if the propagation delay in the device under test from clock to data is greater than 5 ns and the clock period is greater than 10 ns (slower than 100 MHz).   |

# **License Problems**

Some problems that can occur with licenses are:

- License Not Available (see page 390)
- Floating License Server Communication Timeout (see page 390)

### License Not Available

If you attempt to use a software feature that requires a license, and a license is not available, the License Not Available dialog appears.

Depending on the situation, there are several ways to solve this problem:

- If all licenses are in use, you can wait until one of them becomes available again. If there is only one license, the License Not Available dialog shows you who is using the license. If there are multiple licenses, you can view the active software license information (see page 360) to see the license users.
- If all licenses are in use or there are no licenses, you may be able to get a license from another license server (see To access floating license servers (see page 362)).
- If the license management software detects that one of your license servers is unavailable, make sure the computer or logic analyzer hosting the license server is running, is accessible over the network, and is running the license service. For more information, see the > "License Server Administration Guide".
- If an expected node-locked license is not found, make sure the license file is located in the "License" subdirectory under the installation directory (typically C:\Program Files\Agilent Technologies\Logic Analyzer), and make sure the license file has the .lic extension.
- If you decide to purchase additional licenses, contact Agilent Technologies (see "http://www.agilent.com/find/contactus"). When you get your Entitlement Certificate, activate your licenses by using the License Activation Wizard (see To activate software licenses (see page 361)).
- **See Also** Managing Software Licenses (see page 359)

### **Floating License Server Communication Timeout**

When floating licenses are used, the license subsystem checks for communication with the license server every two minutes.

After 10 minutes of communication loss (6 checks), licenses are considered lost, and you are given a message about the server that is no longer communicating and the features that are disabled.

Depending on the feature, you may be able to continue working in the *Agilent Logic Analyzer* application, or you may be forced to exit the application. In either case, you are able to save your setup and data to a configuration file.

If you are able to continue using the *Agilent Logic Analyzer* application with disabled features, the communication checks continue every two minutes. If communication with the license server is re-established, an information dialog tells you about the server and features that have been re-enabled.

When communication with a floating license server is lost, make sure the computer or logic analyzer hosting the license server is running, is accessible over the network, and is running the license service. For more information, see the  $\downarrow$  "License Server Administration Guide".

# **Translating Configuration Files from Other Logic Analyzers**

Included with the *Agilent Logic Analyzer* application are utilities for translating configuration files from 167xG and 16700-series logic analyzers. These configuration file translators move setup information from other logic analyzer configuration files into generic XML format configuration files that can be loaded into the *Agilent Logic Analyzer* application.

The configuration file translators can be run without any logic analyzer hardware.

NOTE Only setup information is translated, not saved data.

- To translate 167xG logic analyzer configuration files (see page 392)
- To translate 16700-series logic analyzer configuration files (see page 393)

See Also

- "XML Format" (in the online help)
  - To open a configuration file (see page 220)

### To translate 167xG logic analyzer configuration files

- 1 From the Windows Start menu, choose Start>All Programs>Agilent Logic Analyzer>Utilities>167xG Configuration File Translator.
- **2** In the 167xG Configuration File Translator dialog, enter the name of the 167xG configuration file you want to translate.

| C 167xG Configuration File T  | ranslator  | X            |
|---|--|--------------|
| The Configuration File Translator con<br>configuration file into generic configu<br>168x/9x Logic Analyzer.<br>This application will output two .xml<br>machines of the 167xG logic analyze<br>corresponding machine number app | uration files (.xml) for use by the<br>files corresponding to the two<br>er. The two files will have the | Exit<br>Help |
| 167xG Configuration File:<br>168x/9x Generic Configuration  |  | Browse       |

### NOTE

167xG configuration files end in .\_A, but this suffix is also used by other models. If possible, confirm that it has a file type of 167xdn\_config when viewed on a 1670-series logic analyzer.

3 Type in the name you want to save the new configuration files under.

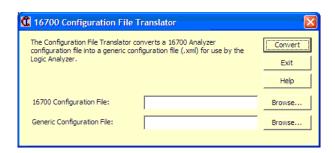
- Because the 1670-series logic analyzers split resources between two measurement engines by default, two output files are created. The default filename is the same as the 167xG configuration file, but has 1.txt or 2.txt appended. Both files are created even if the configuration only used one of the measurement engines.
- Files are saved in the same directory as the input file unless otherwise specified.
- The output files are in XML format, and can be opened like other XML configuration files.
- 4 Click Convert.

Information not converted from file:

- In timing acquisition mode, the sampling period and sampling option.
- In state acquisition mode, the clock mode and clock description.
- All data.
- Any tool information.
- Interface layout.
- Marker information.

### To translate 16700-series logic analyzer configuration files

- 1 From the Windows Start menu, choose Start>All Programs>Agilent Logic Analyzer>Utilities>167xx Configuration File Translator.
- **2** In the 16700 Configuration File Translator dialog, enter the name of the 16700 configuration file you want to translate.



When you have a 16700-series logic analysis system with modules in slots B and C, you get three files when you save a configuration: an xxx.\_\_B, xxx.\_\_C, and xxx.\_\_. Of these three files, only the xxx.\_\_B and xxx.\_\_C can be translated into XML. The xxx.\_\_ cannot be translated.

- **3** Type in the name you want to save the new configuration files under.
  - Files are saved in the same directory as the input file unless otherwise specified.

- The output files are in XML format, and can be opened like other XML configuration files.
- 4 Click Convert.

Information not converted from file:

- All data.
- Any tool information.
- Interface layout.
- Marker information.

**To translate** multi-module **configurations** For example, if you have a 16700-series logic analysis system with modules in slots B and C:

1 On the 16700-series logic analysis system, save the configuration to file "setup1". This generates files setup1.\_\_B, setup1.\_\_C and setup1.\_\_.

(The setup1.\_\_B and setup1.\_\_C files each contain the setup for a single module. In order to translate the entire two-module configuration, you need to translate both files.)

- 2 Copy the setup1.\_\_B and setup1.\_\_C files to the logic analyzer or personal computer on which the *Agilent Logic Analyzer* application runs. (You can ignore the setup1.\_\_\_ file.)
- **3** Use the configuration file translator (as described above) on setup1.\_\_B and setup1.\_\_C to generate the files setup1B.XML and setup1C.XML.
- **4** In the *Agilent Logic Analyzer* application, open the setup1B.XML file. When asked "Do you want to clear all modules before loading?", click **Yes**.
- **5** Open the setup1C.XML file. When asked "Do you want to clear all modules before loading?", click **No**.

In general, clear all modules when loading the first XML file, and do not clear all modules when loading subsequent XML files.

# **Running Self Tests**

The Self Test menu checks the major hardware functions of the logic analysis system to verify that it is working correctly.

CAUTION

Because the most recently acquired data will be lost, be sure to save important data before running self tests.

1 From the menu bar select Help>Self Test....

If you have acquired data, a warning message appears, "Running self-tests will invalidate acquired data"; click **OK** to continue.

| Analysis System Self Tests  |   |  |  |  |
|---|---|--|--|--|
| Select options  | Set reporting level: Current = 0                                      | Progress & Statistics<br>Overall<br>Tests selected: 1<br>Remaining: 0<br>Failures: 0   |  |  |
| Select instruments  | Select suites (slots)   | Select tests   |  |  |
| <all>     16900A Logic Analysis System (1)     16902A Logic Analysis System (1)</all>   | <all><br/>16752A Logic Analyzer(B)<br/>16950A Logic Analyzer(D)</all> | Call> Interface FPGA Register Test Load Memory FPGAs Test Memory FPGA Register Test EEPROM Test ADC Test Probe ID Read Test Memory Data Bus Test ✓ |  |  |
|   | Results   |  |  |  |
| 16950A Logic Analyzer(D) ended. Result: Passed<br>16900A Logic Analyzis System (1) ended. Result: Passed<br>mtx13.cos.agilent.com ended. Result: Passed<br>Stop time: 2004/01/12 12:25:16 |   |  |  |  |
| All tests passed.   |   |  |  |  |
| End of Analysis System Self Test Run  |   |  |  |  |
| Start Stop  | Reset Logs.   | Help Close   |  |  |

- 2 In the Analysis System Self Tests dialog, select the self test options:
  - **Include interactive tests** causes interactive tests to appear in the selection lists.
  - **Run repetitively** runs the selected tests repetitively until you click **Stop**.
  - **Stop on fail** if you are running multiple tests or running tests repetitively, this causes the tests to stop if there is a failure.
  - Double-click item to start lets you double-click a test to start it.
- **3** Set the reporting level.

Higher levels produce increasingly verbose output.

- **4** If you have a multiframe configuration, select the instruments you want to test.
- 5 If you have a slotted instrument, select the suites you want to run.
- 6 Select the tests you want to run.
- 7 Click Start.

As the tests are running, the results are reported in the lower part of the dialog and saved to a log file.

To stop running test, click Stop.

To reset the self-test options, click Reset.

To view the log file, click **Logs...**, select the log file you want to view, and click **Open**.

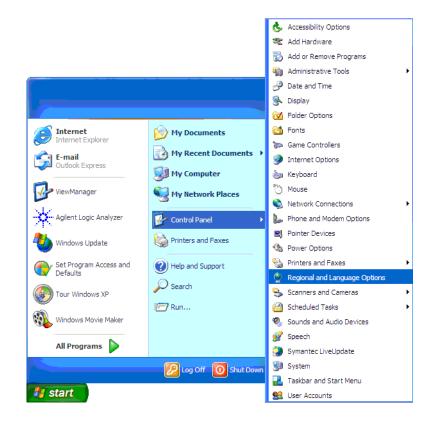
If, after completing the self tests, you have failures or you have questions about the performance of the logic analysis system, contact Agilent Technologies sales or support at "http://www.agilent.com/find/contactus".

**See Also** • For More Information (see page 406)

## **Accessing Japanese Online Help**

#### On Windows XP

1 From the Windows Start menu, choose **Start>Control Panel>Regional** and Language Options.



- 2 In the Advanced tab of the Regional and Language Options dialog:
  - a In the "Language for non-Unicode programs" box, select Japanese.

| Regional and Language Options   |
|---|
| Regional Options Languages Advanced   |
| Clanguage for non-Unicode programs  |
| This system setting enables non-Unicode programs to display menus<br>and dialogs in their native language. It does not affect Unicode<br>programs, but it does apply to all users of this computer. |
| Select a language to match the language version of the non-Unicode<br>programs you want to use:   |
| Japanese 🗸  |
| Code page conversion tables   |
| ✓ 10000 (MAC - Roman)   |
| <ul> <li>✓ 10001 (MAC - Japanese)</li> <li>✓ 10002 (MAC - Traditional Chinese Big5)</li> </ul>  |
| ✓ 10003 (MAC - Korean)  |
| 10004 (MAC - Arabic)     10005 (MAC - Hebrew)   |
| Default user account settings   |
| Apply all settings to the current user account and to the default<br>user profile   |
|   |
| OK Cancel Apply   |

- **b** Click **OK** to close the Regional and Language Options dialog.
- 3 In the dialog that appears, select the files to copy:
  - On a logic analyzer or logic analysis system, the dialog asks if you would like to use existing files or recopy files from the Windows CD-ROM; click **Yes** to use the existing files.
  - On a personal computer running the *Agilent Logic Analyzer* application for a 1690-series logic analyzer, offline analysis, or remote connection to a logic analysis system, you may have to copy files from your Windows CD-ROM.
- **4** A dialog appears asking if you would like to restart your computer; click **Yes** to restart your computer.
- 5 After your computer restarts, start the *Agilent Logic Analyzer* application, and choose **Help>Help Language>Japanese**.

| <u>H</u> elp            |    |                   |
|-------------------------|----|-------------------|
| <u>H</u> elp Topics     | F1 |                   |
| Help On <u>W</u> indows | I  |                   |
| Help On <u>T</u> ools   | I  |                   |
| Help <u>L</u> anguage   | l  | <u>]</u> apanese  |
| <u>S</u> elf Test       |    | ✓ <u>E</u> nglish |
| Status<br>Upgrade       |    | -                 |

Now, when you access the online help, you get the Japanese version.

On Windows 7:

- 1 From the Windows Start menu, choose **Start>Control Panel>Region** and Language.
- 2 In the Administrative tab of the Region and Language dialog, click the Change system locale button.
- 3 In the **Region and Language settings** dialog box, select **Japanese** from the **Current system locale** listbox.
- 4 Click OK and then click Apply.
- **5** After your computer restarts, start the Agilent Logic Analyzer application, and choose Help>Help Language>Japanese.

## If there are problems writing CDs on a 16900A, 16902A, or 16903A frame

#### CAUTION

When writing to a 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive, the logic analysis system must be oriented horizontally; otherwise, the resulting CD-R/RW disc may not be readable on *any* CD-ROM drive.

The 16900A, 16902A, or 16903A logic analysis system's DVD-ROM & CD-R/RW combination drive supports:

- 24x speed CD-R writing.
- 24x speed CD-RW writing.
- 24x speed CD-ROM reading.
- 8x speed DVD-ROM reading.
- Can read DVD-RAM, DVD-R, and DVD-RW.

And it supports the following writing methods:

- Disc at Once.
- Session at Once.
- Track at Once.
- Multi-Session.
- Fixed/Variable Packet Writing.

## **Hibernation Is Not Supported**

No standalone Agilent logic analysis system supports Windows *hibernation* power state.

Power management is controlled through the "Power Options" icon under the control panel. In the "Power Options" dialogs you will find a tab entitled, "Hibernate." Within this window is a check box that lets you turn on/off hibernation. Please do not check this box. The logic analysis system ships from the factory with hibernation disabled.

If you enable hibernation and the logic analysis system attempts to enter hibernation when the *Agilent Logic Analyzer* application is installed, Windows will produce a dialog stating something like the following:

"The device driver for the 'Agilent 16800/16900 Logic Analyzer' device is preventing the machine from entering hibernation. Please close all applications and try again. If the problem persists, you may need to update this driver."

Please note that this message only indicates that the logic analysis system does not support hibernation—not that there is something wrong with the software or drivers.

# **Network Troubleshooting Guide**

|                          | • Network Setup (see page 402)  |
|--------------------------|---|
|                          | • Network Access Issues (see page 402)  |
|                          | • Login Issues (see page 402)   |
|                          | • Using with Multiframe (see page 403)  |
|                          | • Network Hardware and Configuration (see page 403)   |
|                          | • Network Topology (see page 403)   |
|                          | • Known OS Issues (see page 403)  |
|                          | Logic Analyzer Specific Issues (see page 404)   |
|                          | • Keep System Protected, Up-To-Date (see page 404)  |
| Network Setup            | For information on setting up 16900-series logic analysis systems on the network (and in multiframe configurations), refer to the $ \downarrow$ "16900-Series Logic Analysis System Installation Guide".                                |
|                          | • Is the logic analysis system registered with DNS?   |
|                          | • Is the logic analysis system registered with DHCP?  |
| Network Access<br>Issues | • The link activity light must be on. If these LEDs are not on, the LAN segment may be dead.  |
|                          | • Can system be accessed on the network from another computer?  |
|                          | • Note: if on a network without a DHCP server, it can take up to 5 minutes before auto-negotiation configures an IP address. Use <b>ipconfig</b> to verify that the IP address is not 0.0.0.0 before trying to do any network activity. |
|                          | • What IP address does <b>ping</b> <i>hostname</i> yield?   |
|                          | • What IP address does <b>nslookup</b> <i>hostname</i> yield?   |
|                          | • Can system be accessed via UNC in a Windows Explorer (\\hostname)?  |
|                          | • Are the systems all in the same subnet? If not, do they have normal IP address (that is, not one of the following 'unroutable' IP addresses):   |
|                          | • 10.x.x.x  |
|                          | • 172.16.x.x  |
|                          | • 192.168.x.x   |
|                          | • 224.0.0.0 (multicast-reserved)  |
|                          | • Is the Windows Network Firewall enabled? If so, is it configured correctly? (See "Changing the Windows Firewall Settings" (in the online help))   |

#### Login lssues • How are you logged-in? (Workgroup vs. Domain).

• Are there different behaviors between workgroup and domain logins?

| Using with              | • Is the agLogicSvc.exe service running on each system?   |
|-------------------------|---|
| Multiframe              | • If you changed any network cables, you need to re-initialize the agLogicSvc.exe service by stopping it and restarting it or by rebooting. Has this been done?   |
|                         | • All Gbit LAN cards on a Gbit LAN must use the same "Jumbo Frames" setting (see the LAN cards' advanced properties dialog). Also, if a switch/hub is used, you must make sure it supports the same size "Jumbo Frames" setting.                    |
| Network<br>Hardware and | <ul> <li>Which OS is running? (Windows XP, Windows 7, Windows 8, or<br/>Windows Vista)</li> </ul>   |
| Configuration           | <ul> <li>How many network cards? (Motherboard built-in 100Base-T, gigabit<br/>LAN)</li> </ul>   |
|                         | • From command prompt, run <b>ipconfig /all</b> for detailed configuration info.  |
|                         | • From command prompt, run <b>ipconfig</b> / <b>release</b> to release current IP addresses.  |
|                         | • From command prompt, run <b>ipconfig</b> / <b>renew</b> to re-obtain IP addresses.  |
| Network<br>Topology     | • On public LAN? On private LAN? Cross-over cable? Multiple networks?   |
|                         | Configurations:   |
|                         | Stand-alone   |
|                         | • 1 network adapter - LAN.  |
|                         | • 1 network adapter - cross-over cable.   |
|                         | • 1 network adapter - private (switch or hub).  |
|                         | • 2 network adapters - LAN + cross-over cable.  |
|                         | • 2 network adapters - LAN + private (switch or hub).   |
| Known OS Issues         | • Are the <b>SSDP</b> and <b>UPnP</b> services running? (SSDP = Manual, UPnP = Automatic).  |
|                         | On some systems, the SSDP Discovery Service suddenly wakes up and<br>starts using a lot of CPU time. This is a 'manual' service, which listens<br>for a Universal Plug-n-Play request, and is thus started when a<br>particular packet is received. |
|                         | When this happens, the SSDPSRW task starts, stops, and starts again in a loop.  |
|                         | To disable the service, choose <b>My Computer&gt;Manage&gt;Services&gt;SSDP</b><br><b>Discovery Service&gt;Properties</b> and set to <b>Disable</b> .   |
|                         | Then, set the SSDP service back to manual.  |
|                         | Failure to do this can cause the system logger to fill up and other nasty side effects  |

side effects.

|   | • Is the <b>Computer Browser</b> service running? If all systems are Windows XP, or if there is a DHCP server on the network, it may not be necessary for Computer Browser to be running. Furthermore, if the domain name server is NT 4.0, running computer browser on the network can lock out the 'real' domain server making it impossible for people on the network to log in reliably. |
|---|--|
| Logic Analyzer<br>Specific Issues       | • Are there any <i>Agilent Logic Analyzer</i> application specific problems (application or service) being seen? (Connection error dialogs, crashes, other).   |
| Keep System<br>Protected,<br>Up-To-Date | <ul> <li>Use Windows Update to keep up-to-date on critical updates and service packs.</li> <li>Keep the virus definitions up-to-date in your anti-virus software.</li> </ul>   |
|   | <ul> <li>Install any Agilent Logic Analyzer application updates using their<br/>InstallShield packages.</li> </ul>   |
|   | <ul> <li>The local Administrator password should not be empty.</li> </ul>  |

## **Remote Desktop Set Up**

If your logic analysis system has the Windows XP Professional or Windows 7/8 operating system, it supports Remote Desktop Protocol (RDP) connections.

To enable Remote Desktop connections to the logic analysis system, see the Remote Desktop topics in the Windows XP / Windows 7/8 online help:

- 1 From the Windows Start menu, choose Start>Help and Support.
- 2 In the Help and Support Center window, enter "Remote Desktop" in the Search field; then, click the green arrow button to start the search.
- **3** Go to the topic on setting up the computer to use Remote Desktop, and follow its instructions.

When you set up a computer to use Remote Desktop, it is enabled as an exception in the operating system's firewall.

- **See Also** " Changing Windows Firewall Settings, XP Service Pack 2" (in the online help)
  - " Changing Firewall Settings, XP Service Pack 1" (in the online help)
  - " Changing Firewall Settings, Windows 7 " (in the online help)

# For More Information

#### Documentation

| Quick<br>Start/Installation<br>Guide | <ul> <li>The Quick Start/Installation Guide gives you information on how to connect system peripherals and probing. Also included is an overview of the interface and information on installing software upgrades. Use this guide to quickly get familiar with the analyzer and also as a future reference for keeping your analyzer up-to-date and running properly.</li> <li> <i>x</i> "16900-Series Logic Analysis System Installation Guide" </li> <li> <i>x</i> "16800-Series Logic Analyzers Installation/Quick Start Guide" </li> </ul> |
|--------------------------------------|--|
|                                      | • 😕 "1680-Series Logic Analyzers Quick Start/Installation Guide"   |
|                                      | • 😕 "1690-Series Logic Analyzers Quick Start/Installation Guide"   |
| Probing<br>Documentation             | For more information on general-purpose probing, QFP package probing, target connector and connectorless probing, and other probing options, see:  |
|                                      | <ul> <li>         "Probing Selection Quick Reference Card"     </li> </ul>   |
|                                      | • > "Probing Solutions for Logic Analyzers" ( latest version on web")  |
|                                      | Ga "Logic Analyzer Probing Solutions"  |
|                                      | For more information on analysis probes and other processor and bus solutions, see:  |
|                                      | <ul> <li>         "Processor and Bus Support for Logic Analyzers" (</li></ul>  |
|                                      | • 🝙 "Processor, Bus, and FPGA Support for Logic Analyzers"   |
| Online Help<br>System                | The online help gives you product reference and feature information. Also included is a tutorial (see page 60) showing you how to make a basic measurement and containing links to time-saving features and concepts.  |
| Agilent<br>Technologies<br>Web Sites |  |
| Corporation/Cont                     | <ul> <li>Corporation - "http://www.agilent.com"</li> </ul>   |
| act                                  | Contact Us - "http://www.agilent.com/find/contactus"   |
|                                      | • Email Updates - "http://www.agilent.com/find/emailupdates"   |
| Product                              | <ul> <li>Logic Analysis - "http://www.agilent.com/find/logic"</li> </ul>   |
| Information                          | <ul> <li>Logic Analysis Software Download -<br/>"http://www.agilent.com/find/la-sw-download"</li> </ul>  |
|                                      | • Software on CD - "http://software.cos.agilent.com/LogicAnalyzerSW"   |
| See Also                             | • Tutorial - Getting to know your logic analyzer (see page 60)   |

• Intrinsic Support (see page 408)

## **Intrinsic Support**

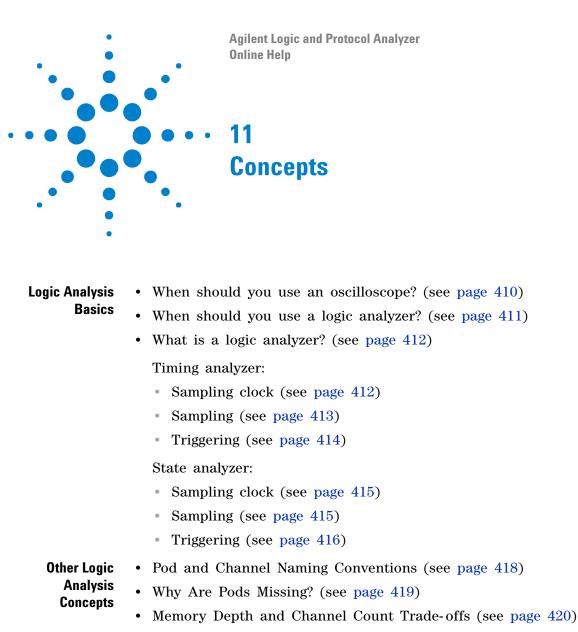
Because the Agilent 16900-series logic analysis systems and 1680A/AD-series logic analyzers operate in a Microsoft Windows XP Professional environment, intrinsic support shall only cover the *Agilent Logic Analyzer* application. Intrinsic support shall also cover any Windows XP Professional operating system services utilized by the *Agilent Logic Analyzer* application:

- Print from the Agilent Logic Analyzer application.
- Networking.
- File management from the Agilent Logic Analyzer application.

Because the Agilent 1690A/AD-series logic analyzers operate on a hosted desktop PC, support shall only cover the *Agilent Logic Analyzer* application and the IEEE 1394 interface to the host PC. Intrinsic support shall not cover any other Windows XP Professional operating system issues other than those listed above. Other Windows XP Professional issues shall be considered Microsoft issues.

**NOTE** Any customer-installed applications on an Agilent 1680A,AD-series product shall not be supported by Agilent. Customers must contact the software vendor for support.

- **See Also** Solving Problems (see page 371)
  - For More Information (see page 406)



- Transitional Timing (see page 422)
- Understanding State Mode Sampling Positions (see page 424)
- Understanding Logic Analyzer Triggering (see page 431)
- ALA vs. XML, When to Use Each Format (see page 445)
- Multiframe Logic Analysis Systems (see page 446)
- Agilent Logic Analyzer vs. 16700 Terminology (see page 449)



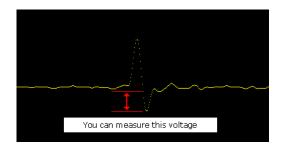
## When should you use an oscilloscope?

[ Tutorial Home (see page 60) ] [ Next Topic (see page 411) ] [ Previous Topic (see page 60) ]

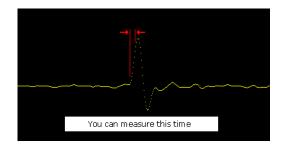
Generally, an oscilloscope is used when you need precise parametric information such as time intervals and voltage readings.

More specifically:

• When you need to measure small voltage excursions on your signals such as undershoot or overshoot.



• When you need high time-interval accuracy. Oscilloscopes can capture precise parametric information such as the time between two points on a rising edge of a pulse with very high accuracy.



### When should you use a logic analyzer?

[ Tutorial Home (see page 60) ] [ Next Topic (see page 412) ] [ Previous Topic (see page 410) ]

Generally, a logic analyzer is used to view timing relationships among many signals, or if you need to trigger on patterns of logic highs and lows. A logic analyzer reacts the same way as the logic circuits do when a voltage threshold is crossed by a signal in the device under test. It will recognize the signal to be either low or high.

More specifically:

• When you need to see many signals at once.

Logic analyzers are very good at organizing and displaying multiple signals. A common task is to group multiple signals into a bus and assign a custom name. Good examples are address, data, and control buses.

• When you need to look at signals in your system the same way your hardware does.

Signals are displayed on a time axis so you can see when transitions occur relative to other bus signals or clock signals.

• When you need to trigger on a unique bus pattern or signal edge.

Logic analyzers can be configured to store data when the high or low values of a group (bus) of signals match a predefined pattern.

Logic analyzers can be configured to store data when a specific edge or level is detected on a single signal.

## What is a logic analyzer?

[ Tutorial Home (see page 60) ] [ Next Topic (see page 412) ] [ Previous Topic (see page 411) ]

Now that we've talked a little about when to use a logic analyzer, let's look in more detail at what a logic analyzer is. Up to now, we've used the term "logic analyzer" rather loosely. In fact, most logic analyzers are really two analyzers in one.

What is a timing A timing analyzer is the part of a logic analyzer that is analogous to an oscilloscope. As a matter of fact, they can be thought of as close cousins.

The timing analyzer displays information in the same general form as an oscilloscope, with the horizontal axis representing time and the vertical axis as voltage amplitude. Because the waveforms on both instruments are time-dependent, the displays are said to be in the "time domain".

The basic areas of functionality in a timing analyzer are as follows:

- Sampling clock in the timing analyzer (see page 412)
- Sampling in the timing acquisition mode (see page 413)
- Triggering the timing analyzer (see page 414)
- What is a state analyzer is very good at tracking down bugs in software or defective components in hardware. It can help eliminate the question whether a problem is in the software code or some hardware device.

Most often, state analyzers are used to find out what logic levels are present on a bus when a particular clock signal occurs. In other words, you want to know what "state of activity" is present when the clock occurs and data is suppose to be valid. Data captured in memory is displayed in a listing format with a time tag attached to every state.

The basic areas of functionality in a state analyzer are as follows:

- Sampling clock in the state analyzer (see page 415)
- Sampling in the state acquisition mode (see page 415)
- Triggering the state analyzer (see page 416)

#### Sampling clock in the timing analyzer

[ Tutorial Home (see page 60) ] [ Next Topic (see page 413) ] [ Previous Topic (see page 412) ]

The timing analyzer uses its own internal clock to control the sampling of data. This type of clocking makes the sampling of data in the logic analyzer *asynchronous* to the clocking in the device under test.

More specifically:

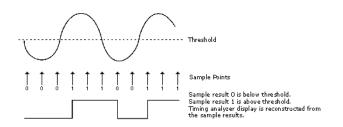
- A timing analyzer is good at showing you "When" signal activity occurs "Relative to other signals".
- A timing analyzer is more interested in viewing the timing relationships between individual signals, than the timing relationships to the signals that are controlling execution in the device under test.
- This is why a timing analyzer can sample data "out of sync", or asynchronous to the device under test clock signals.

#### Sampling in the timing acquisition mode

[ Tutorial Home (see page 60) ] [ Next Topic (see page 414) ] [ Previous Topic (see page 412) ]

In the timing acquisition mode, the logic analyzer works by sampling the input waveforms to determine whether they are high or low. It determines a high or low by comparing the voltage level of the incoming signal to a user-defined voltage threshold. If the signal is above that threshold when it samples, it will be displayed as a 1 or high by the analyzer. By the same criterion, any signal sampled that is below threshold is displayed as a 0 or low.

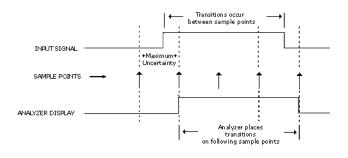
The figure below illustrates how a logic analyzer samples a sine wave as it crosses the threshold level.



The sample points are then stored in memory and used to reconstruct a more squared-off digital waveform.

This tendency to square everything up would seem to limit the usefulness of a timing analyzer. However, a timing analyzer is not intended as a parametric instrument. If you want to check rise time of a signal, use an oscilloscope. If you need to verify timing relationships among several or hundreds of signals by seeing them all together, a timing analyzer is the right choice.

**Sampling** When the timing analyzer samples an input channel, it is either high or **accuracy** low. If the channel is at one state (high or low) on one sample, and the opposite state on the next sample, the analyzer "knows" that the input signal has transitioned sometime between the two samples. It doesn't know when, so it places the transition point at the next sample, as shown in the figure below.



This presents some ambiguity as to when the transition actually occurred and when it is displayed by the analyzer.

Worst case for this ambiguity is one sample period, assuming that the transition occurred immediately after the previous sample point.

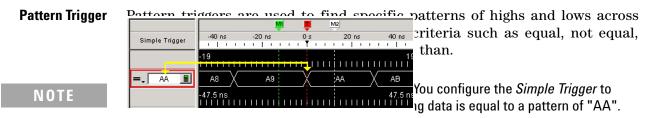
With this technique however, there is a trade-off between resolution and total acquisition time. Remember that every sampling point uses one memory location. Thus, the higher the resolution (faster sampling rate), the shorter the acquisition window.

#### Triggering the timing analyzer

[ Tutorial Home (see page 60) ] [ Next Topic (see page 415) ] [ Previous Topic (see page 413) ]

At some point in a measurement, the logic analyzer has to know when to capture (store) the data that is flowing through its memory. This is know as the trigger point.

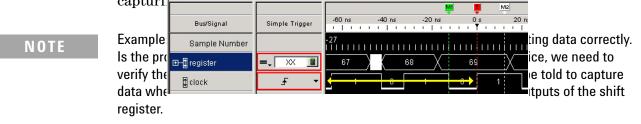
One way to get the analyzer to trigger is to configure the analyzer to look for either a pattern of highs and lows from a group of signals (bus), or a rising or falling edge from a single signal. When the analyzer sees the specified patterns or edges in data, it triggers.



To make things easier for some users, the trigger point on most analyzers can be set not only in Hex, but in binary (1's and 0's), octal, ASCII, or decimal. For instance, the Hex trigger value of AA could also be set to an equivalent binary trigger value of 1010 1010. However, using hex for the trigger point is particularly helpful when looking at buses that are 16, 24, 32, or 64 bits wide.

**Edge Trigger** Edge triggering is a familiar concept to those accustomed to using an oscilloscope. When adjusting the "trigger level" knob on an oscilloscope, you could think of it as setting the level of a voltage comparator that tells the oscilloscope to trigger when the input voltage crosses that level. A timing analyzer works essentially the same on edge triggering except that the trigger level is preset to a logic threshold.

While many logic devices are level dependent, clock and control signals of these devices are often edge-sensitive. Edge triggering allows you to start capturing and the sensitive of the sensiti



#### Sampling clock in the state analyzer

[ Tutorial Home (see page 60) ] [ Next Topic (see page 415) ] [ Previous Topic (see page 414) ]

The state analyzer requires a sampling clock signal from the device under test. This type of clocking makes the sampling of data in the logic analyzer *synchronous* to the clocked events on the device under test.

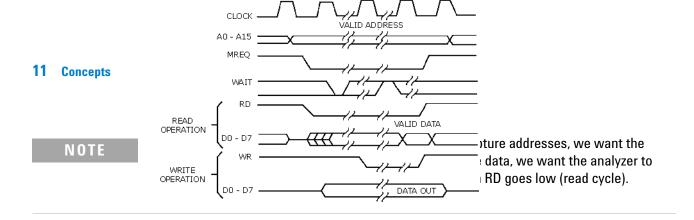
More specifically:

- A state analyzer is good at showing you "What" the signal activity is during a "Valid clock or control signal".
- A state analyzer is more interested in viewing signal activity during specified times of execution, than signal activity unrelated to the timing.
- This is why a state analyzer wants to sample data that is "synchronized" or synchronous to the device under test clock signals.

#### Sampling in the state acquisition mode

[ Tutorial Home (see page 60) ] [ Next Topic (see page 416) ] [ Previous Topic (see page 415) ]

In the world of microprocessors, you can have both data and address appearing on the same signal lines. To capture the correct data, the logic analyzer has to restrict the sampling of data to times when only the desired data is valid and appears on the signal lines. It does this by sampling data from the same signal lines but with different sampling clocks from the device under test.

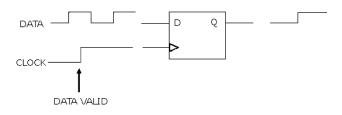


#### Triggering the state analyzer

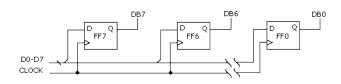
[ Tutorial Home (see page 60) ] [ Next Topic (see page 61) ] [ Previous Topic (see page 415) ]

Similar to a timing analyzer, a state analyzer has the capability to qualify the data we want to store. If we are looking for a specific pattern of highs and lows on the address bus, we can tell the analyzer to start storing when it finds that pattern and to continue storing until the analyzer's memory is full.

Simple Trigger<br/>ExampleLooking at the "D" flip-flop shown below, data on the "D" input is not<br/>valid until after a positive-going clock edge occurs. Thus, a valid state for<br/>the flip-flop is when the clock input is high.



Now imagine that we have eight of these flip-flops in parallel. All eight are connected to the same clock signal as shown below.



When a high level occurs on the clock line, all eight capture data at their "D" inputs. Again, a valid state occurs each time there is a positive level on the clock line.

The following simple trigger tells the analyzer to collect data on lines D0 - D7 when a high level is on the clock line.

| Sample Number | D0-D7  | Clock |
|---------------|--------|-------|
|               | =, 🖂 🗉 | 1 -   |
| -10           | OODB   | 1     |
| -9            | OODF   | 1     |
| -8            | 0062   | 0     |
| -7            | 0065   | 1     |

Advanced Trigger<br/>ExampleYou want to see what data is stored in memory at the address value<br/>406F6. You configure the advanced trigger to look for the pattern 406F6<br/>(hexadecimal) on the address bus and a high level on the RD (memory<br/>read) clock line.

| Step 1 ¥ Edge and Pattern      |      |                               |
|--------------------------------|------|-------------------------------|
| Find 🛛 Bus/Signal 💌            | RD   | Rising Edge                   |
| And 🛛 Bus/Signal 💌             | ADDR | × All bits ▼ = ▼ 4 06F6 Hex × |
| Then 🙁 Trigger and fill memory | ,    | <b>_</b>                      |

As you configure the Edge And Pattern trigger dialog, try to think of it as constructing a sentence that reads left-to-right.

"Find the first occurrence of a **Bus** named **ADDR**, and on **All bits** a pattern that **Equals406F6 Hex**, And a **Signal** named **RD** with a **High** level. Then **Trigger and fill memory** with **Anything**.

## **Pod and Channel Naming Conventions**

In 16900-series logic analysis systems:

- Slots are named "A" through "F" starting with the top slot.
- There is a cable marked "Pod 2" connected to every logic analyzer card. It is important to know which slot a pod is connected to because if you have logic analyzer cards in slots A and B, there will be two pod cables labeled "Pod 2", but the *Agilent Logic Analyzer* application will refer to one as "Slot A Pod 2" and the other as "Slot B Pod 2". It's important not to mix up the two cables.
- Slot A Pod 2 is the same as "Pod A2". "A2" is used interchangeably with "Slot A Pod 2"; likewise, "D1" is used interchangeably with "Slot D Pod 1".

In 16900-series logic analysis systems and 1680/1690-series logic analyzers:

- The Clock Pod consists of the all of the clock channels for all of the pods in this module.
- Each pod has a clock channel. All of the clock channels are numbered Clk1, Clk2, Clk3, etc. If there is a logic analyzer module with two logic analyzer cards with four pods each, the clocks will be labeled Clk1 through Clk8.
- Clock channels are also labeled "C1" as well as "Clk1". "C1" and "Clk1" are the same.

In 16900-series logic analysis systems, don't confuse clock channel "C2" with Pod 2 in Slot C which is referred to as "Pod C2". For clock channels, the "C" is short for "Clock" and not Slot C.

See Also • Pod and Channel Naming Conventions in U4154A Logic Analyzer (see page 680)

## Why Are Pods Missing?

There are a number of reasons all pods are not available to a logic analyzer module:

- In the state sampling mode, with the *General State Mode* (see page 636) sampling option selected, choosing the maximum acquisition memory depth requires one pod pair to be reserved for time tag storage. In this case, setting the memory depth to half of the maximum (or less) will return the pods.
- In the state sampling mode, with the *Turbo State Mode* (see page 636) sampling option selected, one pod pair is reserved for time tag storage.
- In the timing sampling mode, with the *Transitional / Store Qualified Timing Mode* (see page 635) sampling option selected:
  - When the smallest sampling period is selected, one pod pair is reserved for time tag storage.
  - When sampling periods other than the smallest are selected, choosing the maximum acquisition memory depth requires one pod pair to be reserved for time tag storage. In this case, setting the memory depth to half of the maximum (or less) will return the pods.
- The module is part of a logic analyzer that has been split. In this case, the pods are in the module that is the other half of the split analyzer.

See Also

- **so** Memory Depth and Channel Count Trade-offs (see page 420)
  - Configuring Logic Analyzer Modules (see page 98)

## **Memory Depth and Channel Count Trade-offs**

This topic describes the interaction between channel count, memory depth, and triggering in the:

- State Sampling Mode (see page 420)
- Transitional Timing Sampling Mode (see page 421)

# **NOTE** The memory depth and channel count trade-offs are somewhat different in the 16760 logic analyzer (see 16760 Logic Analyzer Memory Depth and Channel Count Tradeoffs (see page 648)).

| State Sampling<br>Mode   |  |
|--|--|
| Time Tag Storage<br>Requires 1 Pod<br>Pair or 1/2<br>Acquisition<br>Memory         | <ul> <li>In the Agilent Logic Analyzer application, all modules are time-correlated; you cannot turn off time tag storage (as you could with previous Agilent logic analysis systems).</li> <li>To use more than 1/2 of a module's acquisition memory, one pod pair must be reserved for time tag storage. To use all pod pairs, you must use 1/2 (or less) of a module's acquisition memory.</li> </ul> |
|  | • In general, the number of timers available = the number of pod pairs<br>not reserved for time tag storage (refer to your logic analyzer<br>characteristics (see page 714) for the actual number of timers<br>available).   |
| Default Settings   | <ul> <li>Time tag storage is always on (and cannot be turned off).</li> <li>Memory depth is set at 1/2 of the total acquisition memory.</li> <li>All pod pairs are available for capturing data.</li> <li>If full memory is selected, the default pod pair to be used for time tag storage is the leftmost, but any pod pair without buses or signals assigned can be used.</li> </ul>                   |
| Selecting Full<br>Memory Depth<br>when No<br>Channels<br>Assigned to a Pod<br>Pair | • The pod pair is automatically reserved for time tag storage.   |
| Selecting Full<br>Memory Depth<br>when Channels<br>Assigned to All<br>Pod Pairs    | <ul><li>A dialog appears to caution you that:</li><li>Bus/signals will lose assigned channels.</li><li>Trigger specifications that use timer resources may be affected.</li></ul>  |

| Going from Full<br>Memory Depth to<br>Half Memory<br>Depth                 | • The pod pair reserved for time tag storage is automatically freed (assigned to the logic analyzer) so it can be used to capture data.  |
|--|--|
| Splitting an<br>Analyzer   | <ul><li>In the Split Analyzer Setup dialog (see page 541) you can:</li><li>Specify whether pod pairs should be reserved for time tag storage.</li></ul>  |
| Transitional<br>Timing Sampling<br>Mode                                    |  |
| Time Tag Storage<br>Requires 1 Pod<br>Pair or 1/2<br>Acquisition<br>Memory | <ul> <li>The transitional timing sampling mode also requires <i>time tag storage</i>.</li> <li>When the smallest sampling period is chosen, one <i>pod pair</i> must be <i>reserved for time tag storage</i>. In this case, you cannot use 1/2 (or less) of a module's acquisition memory to gain back the <i>pod pair</i>.</li> <li>With other sampling periods, the memory depth and channel count trade-offs are the same as in the state sampling mode. That is, to use more than 1/2 of a module's acquisition memory, one <i>pod pair</i> must be <i>reserved for time tag storage</i>. To use all pod pairs, you must use 1/2 (or less) of a module's acquisition memory.</li> <li>In general, the number of timers available = the number of pod pairs not reserved for time tag storage (refer to your logic analyzer characteristics (see page 714) for the actual number of timers available).</li> </ul> |
| Default Settings   | <ul> <li>Time tag storage is required.</li> <li>If full memory is selected, the default pod pair to be used for time tag storage is the leftmost, but any pod pair without buses or signals assigned can be used.</li> </ul>   |
| See Also   | <ul> <li>Configuring Logic Analyzer Modules (see page 98)</li> <li>To set acquisition memory depth (see page 135)</li> <li>Choosing the Sampling Mode (see page 119)</li> <li>Logic Analyzer Notes, Channels and Memory Depth (see page 635)</li> </ul>  |

## **Transitional Timing**

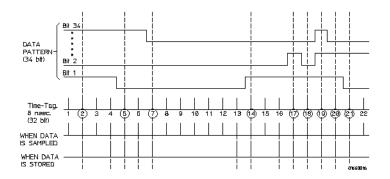
In the **Transitional / Store qualified** timing mode, the timing analyzer samples data at regular intervals, but only stores data when there is a signal transition across the threshold voltage level. Each time a transition occurs on any of the bits in the defined buses/signals (that haven't been excluded), data on all channels is stored. A *time tag* is stored with each stored data sample so the measurement can be reconstructed and displayed later.

# More on Storing

Transitions

MinimumNormally, transitions do not occur at each sample point. This is illustratedTransitionsbelow with time tags 2, 5, 7, and 14. When transitions do occur, twoStoredsamples are stored for every transition. Therefore, with 2K samples of<br/>memory, 1K transitions are stored. You must subtract one, which is<br/>necessary for a starting point, for a minimum of 1023 stored transitions.

MaximumIf transitions occur at a fast rate, such that there is a transition at each<br/>sample point, only one sample is stored for each transition as shown by<br/>time tags 17 through 21 below. If this continues for the entire trace, the<br/>number of transitions stored is 2K samples. Again, you must subtract the<br/>starting point sample, which then yields a maximum of 2047 stored<br/>transitions.



In most cases a transitional timing trace is stored by a mixture of the minimum and maximum cases. Therefore, in this example the actual number of transitions stored will be between 1023 and 2047.

| Transitional<br>Timing<br>Considerations                             |  |
|--|--|
| Data Storage   | When an edge is detected, two samples are stored across all channels<br>assigned to the timing analyzer. Two samples are needed to avoid data loss<br>if a second edge occurs (after the first edge) before the edge detectors can<br>reset.   |
| Sequence Step<br>Branching   | In transitional timing, only 2 branches are available per sequence step.   |
| <b>Global Counters</b>   | In transitional timing, only one global counter is available.  |
| Storing Time Tags  | Transitional timing requires time tags to recreate the data. Time tags are<br>stored by interleaving them with measurement data in memory.   |
| Increasing<br>Duration of<br>Storage (Amount<br>of Time<br>Measured) | By default, the analyzer looks for transitions on all buses/signals defined<br>for the logic analyzer module. However, to increase usable memory depth<br>and acquisition time, you can, in the Advanced Trigger dialog (see<br>page 496), exclude certain bus/signal transitions from being stored (like<br>clock or strobe signal transitions that add little useful information to the<br>measurement). |
| Data on<br>Unassigned<br>Channels                                    | When you run a measurement, data is captured on all logic analyzer channels, whether buses/signals are defined and assigned to those channels or not. In the transitional timing mode, captured samples are saved if there are transitions on the <i>defined</i> buses/signals (that haven't been excluded).   |
|  | After a transitional timing measurement has been run, if you define new<br>buses/signals for previously unassigned logic analyzer channels, the data<br>captured on those channels appears, but it is unlikely that all transitions<br>on those buses/signals have been stored; the data that appears is as if the<br>new buses/signals had been excluded before the measurement was run.                  |
| Trigger Position   | In transitional timing, no data prestore (samples acquired before trigger) is<br>required. Therefore, much like state mode, the trigger position<br>(start/center/end) indicates the percentage of memory filled with samples<br>after the trigger. The number of samples acquired/displayed before the<br>trigger will vary between measurements.   |

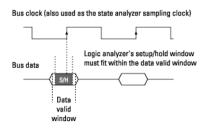
## **Understanding State Mode Sampling Positions**

Synchronous sampling (state mode) logic analyzers are like edge-triggered flip-flops in that they require input logic signals to be stable for a period of time before the clock event (setup time) and after the clock event (hold time) in order to properly interpret the logic level. The combined setup and hold time is known as the setup/hold window.

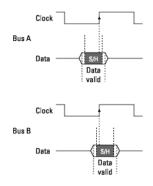
A device under test (because of its own setup/hold requirements) specifies that data be valid on a bus for a certain length of time. This is known as the data valid window. The data valid window on most buses is generally less than half of the bus clock period.

To accurately capture data on a bus:

• The logic analyzer's setup/hold time must fit within the data valid window.



• Because the location of the data valid window relative to the bus clock is different for different types of buses, the position of the logic analyzer's setup/hold window must be adjustable (relative to the sampling clock, and with fine resolution) within the data valid window. For example:



To position the setup/hold window (sampling position) within the data valid window, a logic analyzer has an adjustable delay on each sampling input (to position the setup/hold window for each channel).

Sample Position<br/>Adjustments on<br/>Individual<br/>ChannelsWhen you can make sampling position adjustments on individual channels,<br/>you can make the logic analyzer's setup/hold window smaller because you<br/>can correct for the skew effects caused by the probe cables and the logic<br/>analyzer's internal circuit board traces, and you are left with the<br/>setup/hold requirements of the logic analyzer's internal sampling circuitry.

However, the process of manually positioning the setup/hold window for each channel is time consuming. For each signal in the device under test and each logic analyzer channel, you must measure the data valid window in relation to the bus clock (with an oscilloscope), repeatedly position the setup/hold window and run measurements to see if the logic analyzer captures data correctly, and finally position the setup/hold window in between the positions where data was captured incorrectly.

With Agilent Technologies logic analyzers that have the *eye finder* / eyescan feature, in a small fraction of the time that it takes to make the adjustments manually (and without the extra test equipment), you can automatically:

- Position the setup/hold window on each channel.
- Adjust the threshold voltage setting for the widest possible data valid window.

*Eye finder* and eyescan are an easy way to get the smallest possible logic analyzer setup/hold window.

#### NOTE

You use the Eye Finder feature with 16960/62 series of Agilent Logic Analyzers. You use the Eyescan feature with the U4154A Logic Analyzer to automatically adjust sample positions on individual channels. Refer to the topic "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690 to know more about the eyescan feature.

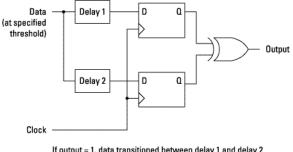
**Eye Finder** For the state sampling clock specified, *eye finder* locates data signal transitions (threshold voltage crossings) in a fixed range of time before and the after clock edges and gives you a display that helps set up the best sampling positions.

To understand the *eye finder* display, imagine, for each active clock edge, one "picture" of the data signal transitions around that edge is taken. Think of this as a snapshot or freeze-frame or stroboscope (centered on, or synchronized with, the clock edge). The time of arrival of the clock edge is T=0.

For example, if you select the rising edge of the clock input on Pod 1 as the state sampling clock, imagine a "picture" is snapped each time a rising edge on the Pod 1 clock arrives. It doesn't matter if the time between Pod 1 clock edges is the same or not. If you elect to sample on both rising and falling edges, then a "picture" is snapped on each. Again, it doesn't matter how much time elapses between active edges. A "picture" is taken on each one.

To build the *eye finder* display, hundreds of thousands of these "pictures" are stacked on top of each other. Each "picture" is aligned at T=0, which is when the active clock edge arrived. It doesn't matter if the pictures are from rising edges or falling edges; they are aligned at T=0. Once the display is built, you cannot tell whether a given signal transition region is associated with clock rising edges or falling edges (or both).

How Eye FinderEye finder measurements are made possible by the logic analyzer's ability<br/>to double-sample each channel using slightly offset delays and by<br/>comparing the delayed samples using an exclusive-OR operation.



If output = 1, data transitioned between delay 1 and delay 2 If output = 0, data did not transition between delay 1 and delay 2. Output is collected for many clocks.

When the exclusive-OR output is high, the delayed samples are different, and a transition is detected between the delay times.

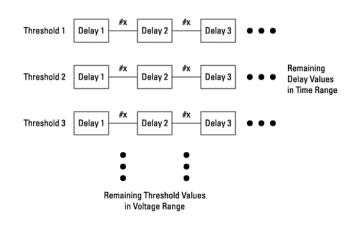
Because of jitter and other variations in the sampled signal, an *eye finder* measurement checks many clocks for each pair of delay values so that it can report how often transitions occur between the two delay times.

Then, another pair of delay values is checked, and so on, until a whole range of time is scanned for transitions.



(#x = Number of Transitions)

Because the logic analyzer is able to adjust the threshold voltage for channels, an *eye finder* measurement is able to repeat the scan for transitions over time at many threshold voltage levels.



By adjusting threshold voltages and watching activity indicators, *eye finder* is able to find the signal activity envelope and determine the optimal threshold voltage; then, by performing a full time scan at that threshold, *eye finder* is able to suggest the sample position.

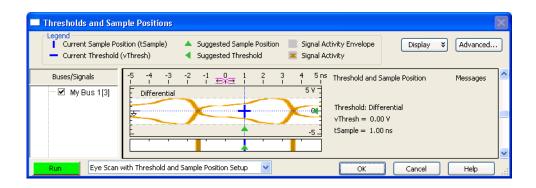
| Legend<br>Current Sample Pos<br>Current Threshold ( |  |
|---|--|
| Buses/Signals                                       | -5 -4 -3 -2 -1 0 1 2 3 4 5 ns<br>Threshold and Sample Position Messages<br>5 V -<br>Threshold: Differential<br>vThresh = 0.00 V<br>tSample = 1.00 ns |

You can also run a full time scan at the current threshold voltage setting to automatically set sampling positions only.

| Legend<br>Current Sample Pos<br>Current Threshold ( |          | <br>al Activity Envelope Display ¥        | Advanced |
|---|----------|---|----------|
| Buses/Signals                                       | -5 -4 -3 | 5 ns Sample Position<br>tSample = 1.00 ns | Messages |

The Auto Threshold and Sample Position Setup scan is usually enough to make sure data is captured accurately, but it may also identify signals that you want to look at in more detail (for example, if you notice delay, damping, etc.).

By performing full time scans across the full signal activity envelope, *eye finder* is able to give you a map of transitions detected in small windows of time and voltage. These scans are called *eye scans*. Oscilloscope-like eye diagrams are used to display the measurement data. The number of transitions in each window is indicated by brightness. This gives you a rough picture of the data eye and may tell you whether you need to look at signals in even more detail with an oscilloscope.



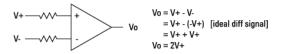
You can run *eye scans* that result in the automatic setting of threshold voltages and sampling positions or *eye scans* that result only in automatic setting of sampling positions.

The number of channels on which an *eye finder* measurement collects data affects how long the measurement takes. The exception is when there are multiple logic analyzer cards in a module; in this case, measurements run simultaneously in parallel.

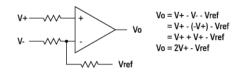
- See Also To automatically adjust state sampling positions and threshold voltages (see page 130)
  - To manually adjust state sampling positions (see page 133)
  - Selecting the State Mode (Synchronous Sampling) (see page 122)
  - Thresholds and Sample Positions Dialog (see page 550)
  - "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690

#### Eye Scan in Logic Analyzers that Support Differential Signals

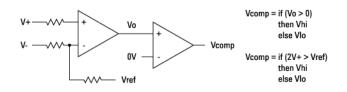
Logic analyzers that support differential signals (like the 16753/54/55/56, 16760, and 16950 logic analyzers) use true differential receivers on their inputs:



A programmable reference voltage is summed into the negative input. This is the threshold voltage when the analyzer is used with single ended probes. The reference is normally programmed to 0V for operation with differential probing:

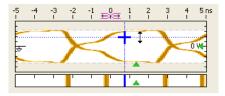


The output of the receiver is then compared to 0V to produce the internal logical signal from the differential input signal. Note that the final comparison produces the answer to the question "Is the differential signal above or below Vref?":



The *eye scan* measurement of the eye opening is performed by doing a series of *eye finder* measurements with different Vref settings. The default *eye finder* measurement for a differential input uses Vref=0V. By raising Vref above zero, we find where the signal crosses the elevated Vref value. If Vref is raised high enough, then the top rail of the signal goes through Vref, and we see the top of the eye. Raising Vref a bit more causes Vcomp to be constant at Vlo, meaning the signal never rises to that level. Conversely, moving Vref below zero finds the lower half of the eye.

The eye scan/eye finder display shows this relationship between eye finder and eye scan by showing the eye finder cross section below the eye scan diagram for each signal. By moving the horizontal Vth line in the eye scan diagram up and down you can obtain the eye finder view at that offset from the center of the eye.



The differential inputs to the logic analyzer are *always* applied to the receiver, regardless of threshold setting in the user interface. This means you can allow for a common mode voltage in the differential pair by

#### **11** Concepts

manually setting the threshold voltage to a nonzero value. *Eye scan* will do this automatically if the center of the signal swing is more than about 100 mV from ground.

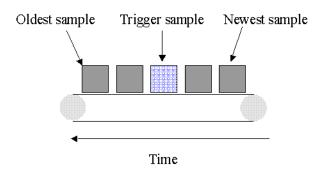
## **Understanding Logic Analyzer Triggering**

Setting up logic analyzer triggers can be difficult and time-consuming. You could assume that if you know how to program, you should be able to set up a logic analyzer trigger with no difficulty. However, this is not true because there are many concepts that are unique to logic analysis. The purpose of this section is to describe these key concepts and how to use them effectively.

- The Conveyor Belt Analogy (see page 431)
- Summary of Triggering Capabilities (see page 432)
- Sequence Steps (see page 433)
- Boolean Expressions (see page 435)
- Branches (see page 436)
- Edges (see page 436)
- Ranges (see page 437)
- Flags (see page 437)
- Occurrence Counters and Global Counters (see page 437)
- Timers (see page 438)
- Storage Qualification (see page 439)
- Strategies for Setting Up Triggers (see page 440)
- Conclusions (see page 444)
- **See Also** Capturing Data from the Device Under Test (see page 149)

#### The Conveyor Belt Analogy

The memory of a logic analyzer can be compared to a very long conveyor belt, and the samples acquired from the device under test (DUT) as boxes on the conveyor belt. At one end, new boxes are placed on the conveyor belt, and at the other end the boxes fall off. In other words, because logic analyzer memory is limited in depth (number of samples), whenever a new sample is acquired the oldest sample currently in memory is thrown away if the memory is full. This is shown in the following figure.



The conveyor belt analogy

A logic analyzer trigger is similar to someone standing at the beginning of the conveyor belt placing more boxes on it. They are told to "look for a special box and to stop the conveyor belt when that box reaches a particular position on the belt". Using this analogy, the special box is the trigger. Once a logic analyzer detects a sample that matches the trigger condition, this is the indication that it should stop acquiring more samples when the trigger is located appropriately in memory.

The location of the trigger in memory is known as the *trigger position*. Normally, the trigger position is set to the middle so that the maximum number of samples that occurred before and after the trigger are in memory. However, you can set the trigger position to any point in memory.

The concepts in this analogy are summed up in the following table.

Mapping of concepts in the Conveyor Belt Analogy to a Logic Analyzer

| Conveyor Belt<br>Analogy                  | Logic Analyzer                              |
|---|---|
| Boxes on the belt                         | Samples acquired from the device under test |
| Number of boxes that will fit on the belt | Memory depth                                |
| Special box                               | Trigger point                               |

Next: Summary of Triggering Capabilities (see page 432)

#### **Summary of Triggering Capabilities**

Because logic analyzer triggering provides a great deal of functionality, the following table provides a brief summary of the capabilities covered in this article. Each of these capabilities will be described.

Summary of Logic Analyzer Triggering Capabilities

| Capability            | Examples   |
|-----------------------|--|
| Edges                 | If there is rising edge on SIG1 then Trigger<br>If there is falling edge on SIG1 then Trigger  |
| Boolean expressions   | If $ADDR = 1000$ and $DATA = 2000$   |
| Ranges                | If ADDR in range 1000 to 2000  |
| Storage qualification | <pre>1. If<br/>Else If ADDR in range 1000 to 2000 then<br/>Store Sample<br/>Go to 1<br/>Else If ADDR not in range 1000 to 2000 then<br/>Don't Store Sample<br/>Go to 1</pre> |
| Counters              | <ol> <li>If DATA = 1000 Then<br/>Increment Counter 1<br/>Go to 2</li> <li>If Counter 1 &gt; 2 Then<br/>Trigger</li> </ol>  |
| Timers                | <ol> <li>If DATA = 1000 Then<br/>Start Timer 1<br/>Go to 2</li> <li>If Timer 1 &gt; 500 ns Then<br/>Trigger</li> </ol>   |

Next: Sequence Steps (see page 433)

## **Sequence Steps**

While logic analyzer triggers are often simple, they can require complex programming. For example, you may want to trigger on the rising edge of one signal that is followed by the rising edge of another signal. This means that the logic analyzer must first find the first rising edge before it begins looking for the next rising edge. Because there is a sequence of steps to find the trigger, this is known as a *trigger sequence*. Each step of the sequence is called a *sequence step*.

Each sequence step consists of two parts; the conditions and the actions. The conditions are Boolean expressions such as "If ADDR = 1000" or "If there is a rising edge on SIG1". The actions are what the logic analyzer should do if the condition is met. Examples of actions include triggering the logic analyzer, going to another sequence step, or starting a timer. This is similar to an If/Then statement in programming.

Each step in the trigger sequence is assigned a number. The first sequence step to be executed is always Sequence Step 1, but because of the Go To actions, the rest of the sequence steps can be executed in any order. When a sequence step is executed and none of the Boolean expressions are true, the logic analyzer acquires the next sample and executes the same sequence step again. As a simple example, consider the following trigger sequence:

1. If DATA = 7000 then Trigger

If the following samples were acquired, the logic analyzer would trigger on sample #6.

| Sample # | ADDR | DATA |  |
|----------|------|------|--|
| 1        | 1000 | 2000 |  |
| 2        | 1010 | 3000 |  |
| 3        | 1020 | 4000 |  |
| 4        | 1030 | 5000 |  |
| 5        | 1040 | 6000 |  |
| 6        | 1050 | 7000 | <- This is where the logic analyzer triggers |
| 7        | 1060 | 2000 |  |

In essence, Sequence Step 1 is equivalent to "Keep acquiring more samples until DATA=7000, then trigger".

If a Boolean expression in a sequence step is met, another sample is always acquired before the next sequence step is executed. In other words, if a sample meets the condition in Sequence Step 1, another sample will be acquired before executing Sequence Step 2. This means that it is not possible for a single sample to be used to meet the conditions of more than one sequence step. Each sequence step can be thought of as representing events that occur at different points in time. Two sequence steps can never be used to specify two events that happen simultaneously.

For example, consider the following trigger sequence:

1. If ADDR = 1000 then Go to 2 2. If DATA = 2000 then Trigger

If the following samples were acquired, the logic analyzer would trigger on sample #7.

| Sample # | ADDR | DATA |   |
|----------|------|------|---|
| 1        | 1000 | 2000 | <- This meets the condition in Sequence step #1 |
| 2        | 1010 | 3000 |   |
| 3        | 1020 | 4000 |   |
| 4        | 1030 | 5000 |   |
| 5        | 1040 | 6000 |   |
| 6        | 1050 | 7000 |   |
| 7        | 1060 | 2000 | <- This is where the logic analyzer triggers    |

Note that the logic analyzer will not trigger on Sample #1 because a new sample is acquired between the time that the condition in Sequence Step 1 is met and when the condition in Sequence Step #2 is tested. A good way to think of this trigger sequence is "Find ADDR = 1000 followed by DATA = 2000 and then trigger". Multiple sequence steps in a trigger sequence imply a "followed by".

Once a logic analyzer triggers, it does not trigger again. In other words, even if more than one sample meets the trigger condition, the logic analyzer still only triggers once. For example, using "ADDR=1000" as our trigger, if the logic analyzer acquires the following samples, it will trigger on Sample #2 and only on Sample #2.

Sample # ADDR 1 0000 2 1000 <- The logic analyzer triggers here 3 2000 4 1000 <- The logic analyzer does NOT trigger again here 5 1040

A frequently asked question is "What happens if the conditions in a sequence step are not met?" For example, if there is a condition that says "If ADDR = 1000 Then Trigger", what happens if the current sample has ADDR = 2000? The logic analyzer simply acquires the next sample and tries to execute this sequence step again. In essence, if the trigger condition is "ADDR = 1000", this is equivalent to "Keep acquiring more samples until you find one that has ADDR=1000". Therefore, if you set up a trigger condition that is never met, the logic analyzer will never trigger.

When the conditions are met in a sequence step, it is clear which sequence step will be executed next when a "Go To" action is used, but it is not necessarily clear if there is no "Go To". On some logic analyzers, if there is no "Go To", this means that the next sequence step should be executed. On other logic analyzers, it means the same sequence step should be executed again. Because of this confusion, it is good practice to always use a "Go To" action rather than relying on the default. The state and timing modules deal with this problem by automatically including a "Go To" or "Trigger" action in every sequence step. For example:

If ADDR = 1000 and DATA = 2000 then Go to 1 <- This is automatically added

Next: Boolean Expressions (see page 435)

### **Boolean Expressions**

While multiple sequence steps imply a "followed by", within a sequence step Boolean expressions can be used. An example is:

If ADDR = 1000 and DATA = 2000

This expression means that for this expression to be met, ADDR must equal 1000 in the same sample that DATA equals 2000. In other words, ADDR equals 1000 at the same time that DATA equals 2000. Therefore, if you want to trigger on two events that occur at the same time, a Boolean expression should be used. It's a common mistake to try to use two sequence steps when a Boolean expression should be used or to use a Boolean expression when two sequence steps should be used.

NOTE

Boolean expressions are used for events that happen at the same time, and multiple sequence steps are used when one event follows another.

Next: Branches (see page 436)

### **Branches**

Branches are similar to the *Switch* statement in the C programming language and the *Select Case* statement in Basic. They provide a method for testing multiple conditions. Each branch has its own actions. An example of multiple branches is shown below:

| 1. | If ADDR < 1000 then Go To 2        | <- This is a branch of Level 1     |
|----|------------------------------------|------------------------------------|
|    | Else If ADDR > 2000 then Go To 3   | <- This is a 2nd branch of Level 1 |
|    | Else If DATA = 2000 then Trigger   | <- This is a 3rd branch of Level 1 |
| 2. | If DATA <= 7000 then Trigger       |                                    |
| 3. | If there is a Rising Edge on SIG1, | then Trigger                       |

In sequence step 1, there are three branches, so there are three possible actions that can be taken.

When the condition of one branch is met, none of the branches below it are tested. In other words, there is no way for more than one branch to be executed based upon a single sample, even if the sample causes the conditions for more than one branch to be met. In other words, each branch is an "Else If".

Next: Edges (see page 436)

#### Edges

Edges represent a transition from low to high or high to low on a single signal. Typically, edges are specified as "rising edge", "falling edge", or "either edge", where "rising edge" indicates a transition from a low to a high. On most logic analyzers, up to two edges can be included in the trigger sequence although some allow only one.

Next: Ranges (see page 437)

### Ranges

Ranges are a convenient method for specifying a range of values, such as "ADDR in range 1000 to 2000". Most logic analyzers also support a "not in range" function as well. Ranges are a convenient shortcut so that you don't have to specify "ADDR  $\geq$  1000 and ADDR  $\leq$  2000".

Next: Flags (see page 437)

## Flags

Flags are Boolean variables that are used to send signals from one module to another. They can be set when a condition occurs in one module and tested later by another module. In the example below, flag 1 is used to keep track of what happens in the trigger sequence of Module 1 so that this information can be used in Module 2.

Trigger Sequence for Module 1:

```
    If ADDR < 5000 then
Set Flag 1
Trigger and fill memory
```

Trigger Sequence for Module 2:

1. If DATA = 5000 and Flag 1 is set then Trigger Else if DATA = 1000 and not Flag 1 then Trigger

#### NOTE

Flags are not available in 1680/1690-series logic analyzers.

Next: Occurrence Counters and Global Counters (see page 437)

## **Occurrence Counters and Global Counters**

Occurrence Counters are used in situations where you want to find the Nth occurrence of an event. For example, if you want to trigger on the 5th time that ADDR = 1000, you could set up the trigger as:

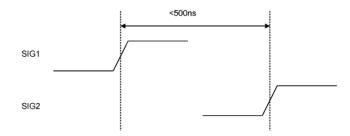
If ADDR = 1000 occurs 5 times then Trigger

Global Counters are like integer variables. They are more flexible than Occurrence Counters because they can be used to count complex events such as an edge followed by another edge. Global Counters can be incremented, tested, and reset. By default, Global Counters begin with zero and don't need to be reset unless they have already been used in the trigger sequence. In general, Occurrence Counters should be used in place of Global Counters, if possible, because they are easier to use and because there is a limited number of Global Counters. Next: Timers (see page 438)

### Timers

Timers are used to check the amount of time that has elapsed between events. For example, if you want to trigger on one edge followed by another edge that occurs within 500 ns, use a timer. The most critical point to remember in using timers is that they need to be started before they are tested. In other words, timers do not start automatically.

The key to setting up a timer is to identify where it should be started and where it should be tested. Consider the example in the following figure. The timer should be started when the rising edge on SIG1 is detected and it should be tested when the rising edge occurs on SIG2.



An edge followed by an edge with a time limit

An example trigger sequence to set up this measurement is:

```
    If there is a Rising Edge on SIG1, then
Start Timer1
Go to 2
    If there is a Rising Edge on SIG2 AND Timer1 < 500ns then
Trigger
```

While the above trigger sequence seems correct, it actually has a critical flaw. What happens if there is a rising edge on SIG1 but SIG2 doesn't occur within 500 ns? The logic analyzer will never trigger, because timer1 will keep running and condition "Timer1 < 500 ns" will never be met. There might be another rising edge on SIG1 that is followed within 500 ns by the rising edge on SIG2 that occurs later on, so this situation is unacceptable.

To fix this problem, whenever the timer exceeds 500 ns without triggering, the sequence should loop back to Level 1 to look for another rising edge on SIG1. The following shows an example of the correct sequence:

```
    If there is a Rising Edge on SIG1, then
Start Timer1
Go to 2
    If there is a Rising Edge on SIG2 AND Timer1 < 500ns then
Trigger
```

```
Else If Timer1 >= 500ns then
Reset Timer1
Go to 1
```

Occasionally, you may run out of timers. A counter can be used in place of a timer if the logic analyzer is sampling at regular intervals (that is, if it's in the timing sampling mode). A timer can be simulated by counting the number of samples that are acquired. For example, if the logic analyzer acquires a new sample every 10 ns and seven samples are acquired, this represents 70 ns.

Next: Storage Qualification (see page 439)

## **Storage Qualification**

Storage qualification is used to determine if an acquired sample should be stored (that is, placed in memory) or thrown away. This keeps the logic analyzer memory from being filled with samples that are not needed.

**Default Storage** The simplest method to set up storage qualification is by setting up the Default Storage. Default Storage means "unless a sequence step specifies otherwise, this is what should be stored". As an example, you may want to only store samples if ADDR is in the range 1000 to 2000, so you should set the Default Storage to:

ADDR In Range 1000 to 2000

By default, the Default Storage is set to store all samples acquired. You can also set the Default Storage to store nothing, which means that no samples will be stored unless a sequence step overrides the default storage.

Sequence Step Sequence step storage qualification means that within a particular sequence step only certain samples will be stored. This means that until a "Go To" or "Trigger" action is used to leave this sequence step, the storage qualification applies. This is useful when you want different storage qualification for each sequence step. For example, you may want to store nothing until ADDR = 1000 and then store only samples with ADDR in the range 1000 to 2000 for the rest of the measurement.

Setting up sequence step storage requires the use of an additional branch. For example, if you want to store only samples with ADDR in the range 5000 to 6FFF while looking for DATA = 005E, the following sequence step could be used in some situations:

```
1. If DATA = 005E then Trigger
Else If ADDR in range 5000 to 6FFF then
Store Sample
Go to 1
```

Note the use of the store sample action. This means "store the most recently acquired sample in memory now". It does *not* mean, "From now on, start storing". It should be noted that since the store sample action is never executed unless ADDR is in the range 5000 to 6FFF, this branch essentially means "While in this sequence step, store only samples with ADDR between 5000 and 6FFF".

The above example seems to imply that only samples with ADDR between 5000 and 6FFF will be stored. However, this depends upon how the default storage has been set up. Using the previous example, if the default storage is set to "Store Everything", and a sample is outside of the range 5000 to 6FFF, then the Else If branch is not executed and the Default Storage is applied. In essence, the sequence step has said what to do when a sample has a value in a particular range, but it doesn't say what to do for samples outside the range. Therefore, if you want to specify the sequence step storage unambiguously, use the following:

```
1. If DATA = 005E then Trigger
Else If ADDR in range 5000 to 6FFF then
Store Sample
Go to 1
Else If ADDR not in range 5000 to 6FFF then
Don't Store Sample
Go to 1
```

Alternatively, if the default storage is set to "Store Everything", use the following:

```
1. If DATA = 005E then Trigger
Else If ADDR not in range 5000 to 6FFF then
Don't Store Sample
Go to 1
```

In summary, Sequence Step Storage always overrides the Default Storage, but only for the conditions specifically mentioned in the Sequence Step Storage. You must be very careful that you account for the interaction between Default Storage and Sequence Step Storage.

Next: Strategies for Setting Up Triggers (see page 440)

## Strategies for Setting Up Triggers

- Trigger Functions (see page 440)
- Setting Up Complex Triggers (see page 443)
- Save and Document Your Trigger Sequences (see page 443)

#### **Trigger Functions**

While setting up logic analyzer triggers can be difficult, *trigger functions* can greatly simplify the process. Trigger functions are commonly-needed building blocks that can be combined to set up a trigger. Because the

functions cover most common triggers, you can set up your trigger simply by selecting the appropriate function and filling in the data. The logic analyzer trigger user interface is shown in the following figure. Note that trigger functions are prominently located at the left of the screen.

| tell Adv.                       | anced Trigger fo   | r 1674x/5x Logic Analyzer - 1   |
|---------------------------------|--|---|
| Trig                            | ger Functions  | Trigger Sequence  |
| Adhenced Other Bus Pattern Edge | Pattern<br>present for<br>>t time<br>Pattern<br>or <t time<br="">Pattern<br/>absent for<br/>&gt;t time</t> | Step 1 × Pattern present for >t time         Find × Bus/Signal • My Bus 1         All bits • = • 45 • Hex ×         present for > 6 ns • - +         Then × Trigger and fill memory |

The trigger user interface

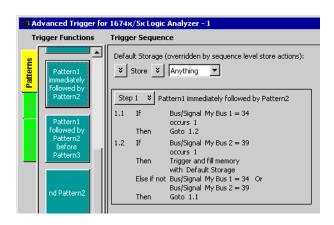
Note that a picture (which corresponds to the selected function) is provided by hovering over the trigger function button.

For example, if you want to trigger when a bus pattern is immediately followed by another bus pattern, you can drag-and-drop the "Pattern1 immediately followed by Pattern2" trigger function onto a trigger sequence step, as shown in the following figure.

| tin Ac          | lvanced Trigger fo  | r 1674x/5x Logic Analyzer - 1  |
|-----------------|---|--|
| Tr              | igger Functions   | Trigger Sequence   |
| <b>Patterns</b> | Pattern1<br>immediately<br>followed by<br>Pattern2        | Default Storage (overridden by sequence level store actions):          Image: Store ima |
| Advanced Other  | Pattern1<br>followed by<br>Pattern2<br>before<br>Pattern3 | Find       >       Bus/Signal       >       My Bus 1       >       All bits       =       >       34       Hex ×         Followed immediately by ×       Bus/Signal       >       My Bus 2       ×       All bits       =       >       39       Hex ×         Then       ×       Trigger and fill memory       ×        ×       >   |

Pattern1 immediately followed by Pattern2

Once you have selected this function, you simply fill in the names of the buses and the patterns. Contrast the previous figure with the following figure, which is the same trigger created using If/Then statements. The trigger function is easier to use because the additional details of the If/Then statements have been hidden. However, if you want to see the details, you can show trigger step as if/then.



The same trigger as If/Then statements

Trigger functions can be modified. For example, if you start with the function "Find Edge", you can add another event, and it becomes the same as "Find Edge and Pattern". Therefore, a function that is not exactly correct can often be converted into the desired trigger. It is also possible to convert a trigger sequence step to advanced If/Then trigger functions and modify them.

Trigger functions are like building blocks because they can be used together in a trigger sequence. For example, if you want to set up a trigger as "Find edge followed by pattern", you can use a "Find Edge" function for Level 1 and a "Find Pattern" function for Sequence Level 2 (see the following figure). So, functions are useful both as an entire trigger sequence and as one step in a trigger sequence.

| ta Ac        | dvanced Trigger fo  | r 1674x/5x Logic Analyzer - 1   |
|--------------|---------------------|---|
| Tr           | igger Functions     | Trigger Sequence  |
| Pattern Edge | Pattern             | Step 1 * Edge       Find * Bus/Signal • My Signal 1 * Rising Edge •       Then * Goto • Next •  |
| d Other Bus  | Edge and<br>Pattern | Step 2       > Pattern         Find        > Bus/Signal          My Bus 1       > All bits          Then        > Trigger and fill memory |

"Find Edge" and "Find Pattern" together

Next: Setting Up Complex Triggers (see page 443)

### **Setting Up Complex Triggers**

Frequently, the most difficult part of setting up a complex trigger is breaking down the problem. In other words, how do you map a complex trigger into sequence steps, branches, and Boolean expressions? Here are step by step instructions:

- **1** Break down the problem into events that don't happen simultaneously. These correspond to the sequence steps.
- **2** Scan the list of trigger functions to try to find some that match the events identified in Step #1.
- **3** Within all remaining events, break them down into Boolean expressions and their corresponding actions. Each Boolean expression/Action pair corresponds to a separate branch within a sequence step. Remember that "Store" branches may exist that are used only to handle storage qualification for that sequence step.

Next: Save and Document Your Trigger Sequences (see page 443)

#### Save and Document Your Trigger Sequences

If a trigger sequence is important at one time, it is likely to be important again. This is why saving and documenting trigger sequences is so valuable. Complex trigger sequences generally are too difficult to understand without some accompanying explanation.

In Advanced If/Then trigger functions, you can include comments with the "If" clauses in a trigger sequence step. See "To display or hide "If" clause comments" on page 190.

When saving a trigger specification to a file, you can enter a description of the trigger sequence in the file header information (see "To store a trigger" on page 201 and the following figure).

| a <b>ve As</b><br>Save in: 🚮 🛙 | Desktop 💌 🗢 🚞  | ?<br>* 🗐 🕈 |
|--------------------------------|--|------------|
| My Documer                     | its  |            |
| 🖳 My Compute                   |  |            |
| 📴 My Network<br>🚞 adjbuild     | Places   |            |
|                                |  |            |
|                                |  |            |
|                                |  |            |
| 1                              |  |            |
| File name:                     | *.xml  | Save       |
| Save as type:                  | Logic Analyzer Trigger Specification (*.xml) 💌   | Cancel     |
| Source:                        |  |            |
| Jource.                        | <u> </u>   |            |
|                                |  |            |
|                                |  |            |
| File Header Inf                | ormation   |            |
| Owner:                         | Project:   |            |
| Description:                   |  | <u> </u>   |
| Description:                   |  | <u> </u>   |
| File Options                   |  |            |
|                                | i Setup 💿 Setup Only   |            |
|                                | a south of the sou |            |
|                                |  | Help       |
|                                |  |            |

Also, because the trigger specification file is in XML format, you edit the file and annotate steps with additional HTML-style comments (for example, <!-- Comment. -->).

Next: Conclusions (see page 444)

## Conclusions

Setting up logic analyzer triggers is very different than writing software. The job can be greatly simplified if other work can be leveraged by using pre-defined trigger functions and well-documented triggers that were written earlier. Only write your own trigger setup if there's nothing else available. Finally, when faced with a difficult trigger to set up, break down the problem into smaller chunks and deal with each one individually.

| If you want to:  | Then use:  |
|--|--|
| Save and load sessions from a logic analysis system.                       | <b>ALA Format</b> — ALA format files are more complete, and the format is more efficient for saving and loading logic analyzer information.  |
| Share captured data.   | <ul> <li>ALA Format — In offline mode, you can read ALA format configuration files in any instance of the Agilent Logic Analyzer application, without having licenses for licensed tools, windows, etc. that may be used in the configuration. This provides "read-only" capability; licenses are required to go online or add any licensed tools, windows, etc.</li> <li>XML Format — You can also share captured data using XML format configuration files. When loading an XML format file with data, you are forced into offline mode. Also, when viewing data from XML format configuration files, you need licenses for any licensed tools that may be used in the configuration.</li> </ul> |
| Transfer module setup<br>information between similar<br>logic analyzers.   | <b>ALA Format</b> — ALA format configuration files can only be<br>loaded by logic analysis systems with compatible modules (for<br>example, modules in the same or similar logic analyzer families<br>like the 16740/41/42A and 16750/51/52A/B).   |
| Transfer module setup<br>information between different<br>logic analyzers. | <b>XML Format</b> — If you want to transfer setup information between incompatible modules, you must use XML format configuration files.   |
| Transfer only part of a logic analyzer setup.                              | <b>XML Format</b> — You can load edited XML format configuration files.  |
| Control the logic analysis<br>system remotely using COM<br>automation.     | <b>XML Format</b> — The COM automation interface has commands<br>for setting up parts of the logic analysis system with XML<br>format strings. You can get these strings from XML format<br>configuration files. (You can also load complete setups from<br>ALA format configuration files using COM automation.)  |
| Insert symbol information<br>from software development<br>tools.           | <b>XML Format</b> — When a compiler-generated output file can't be<br>loaded, you can save the configuration to an XML format file,<br>edit it to include the symbol information (which has been<br>translated into the logic analyzer's XML format), and open the<br>XML format file again.   |

# ALA vs. XML, When to Use Each Format

#### See Also

- To save a configuration file (see page 206)
- To open a configuration file (see page 220)
- To transfer module setups to/from multi-module systems (see page 224)
- ALA Format (see page 588)
- "XML Format" (in the online help)

# Multiframe Logic Analysis Systems

If you need to make time-correlated measurements with more logic analysis channels than can be installed in a single frame/chassis, you can connect multiple 16900A, 16901A, 16902A, 16902B, and 16800 Series logic analyzer frames or U4002A, M9502A or M9595A chassis together.

#### NOTE

Not all logic analysis systems have multiframe capability. If the back of your instrument does not have an "Input" and "Output" connector, it does not support multiframe. For example, the 16903A logic analysis system and the 1680/1690-series logic analyzers do not support multiframe.

The  $\checkmark$  "16900-Series Logic Analysis System Installation Guide" describes how to connect multiple frames/chassis. Basically, each 16900A, 16901A, 16902A, 16902B, 16800 Series frame or U4002A, M9502A or M9595A chassis has two multiframe connectors, labeled "Input" and "Output". A multiframe cable connects the output of one frame to the input of another frame. You can chain as many frames as you like together this way. The master frame is the one with the open input connector; all other frames are slave frames, and the one with the open output connector is the terminating slave frame.

## CAUTION

Failing to follow one of the recommended multiframe configurations in the installation guide can result in unpredictable software behavior and/or poor analyzer performance!

In addition to the multiframe cables, the frames must also be connected to a network. Usually, this is a Gbit LAN network. It can be a private or public network (see installation guide). The multiframe cable is used for time correlation, cross-triggering, and multiframe setup; all other inter-frame communication and data transfer take place over the network.

### NOTE

If (and only if) you encounter problems after changing multiframe connections, try rebooting all frames in the multiframe set.

To ensure the smoothest multiframe startup, the following startup sequence is recommended:

- First, start up the system configured as the master frame. Let it fully boot and then log in as the preferred user. Once the desktop is available, wait until the Agilent Notification Center Icon (viewable in the system Tray) is displayed and in the green "ready" state.
- Proceed to start the next intermediate slave system in the multiframe chain, again waiting until the instrument is in the ready state.
- Continue sequentially with the rest of the slave systems, allowing each to get to the ready state.
- · Lastly, start the terminating slave system and allow it to reach the ready state.

You may now start the controlling Logic Analyzer application, which can run on the master system, any of the slave systems, or even remotely from another personal computer.

A "System" is considered to be a combination of the host controller and the instrument chassis. For the 16900A, 16901A, 16902A, 16902B or 16800 series of standalone instruments, the host controller and instrument chassis is contained in one, single frame package. For the U4002A, M9502A or M9505A chassis with one or more instrument modules installed, "system" is the combination of the chassis connected via some network connection to either an external remote host computer or an embedded host controller module installed in the chassis.

Remotely hosted systems may have their own boot sequence requirements. Usually this is to boot the chassis first and then the host computer.

## CAUTION

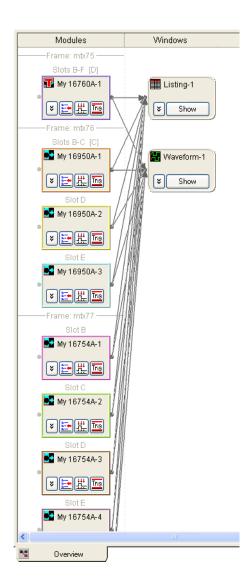
Changing multiframe cables and/or network cables while a user is connected (online) with the multiframe set will force them offline—losing any unsaved changes.

#### NOTE

When an operating application on an instrument is forced offline due to a multiframe connection being made, multiple offline warning messages are displayed which require a user response to continue. For smoother multiframe startup, it is recommended to remove any startup menu shortcuts for the Logic Analysis application from all systems in the multiframe scenario so that no instrument systems can auto-start at login and enter online mode.

Some things to consider when using multiframe logic analysis systems:

• Use the Overview window to tell which frames are connected and which modules are in each frame.



- When triggering from, or sending a trigger to, an external, non-multiframe instrument, you must use the **Trigger In** or **Trigger Out** BNC connectors on the *master frame*.
- When you arm between modules in different frames, an unused flag line is implicitly used to facilitate the arming. (Flag lines already used in the trigger setup or to arm the external Trigger Out are not used.)
- The *Agilent Notification Center Icon* (lower, right-hand corner of the desktop) will be present when logged onto any standalone instrument. You can double-click this icon to get frame and module details on all frames in the multiframe set. If connected remotely from a PC, this information is available via the Overview window (mentioned above) and the System Summary dialog.

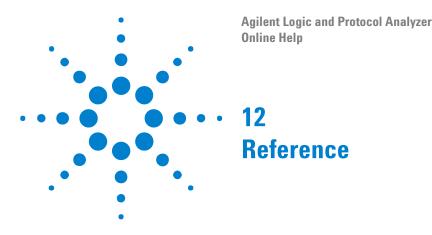
# Agilent Logic Analyzer vs. 16700 Terminology

If you are familiar with the 16700-series logic analysis system, note that some of the terminology in the *Agilent Logic Analyzer* application is different:

| 16700 Term   | Agilent Logic Analyzer Term  |
|--|--|
| label  | bus or signal (see page 104)   |
| Workspace  | Overview window (see page 491)   |
| machine  | analyzer, module, and split analyzer (see page 98)   |
| IMB  | arming (see page 193) (Advanced Trigger dialog)  |
| Source Correlation<br>Toolset                                  | Source window (see page 486)   |
| Compare tool   | Compare window (see page 485)  |
| trigger level  | trigger step (see page 163)  |
| trigger <i>macro</i> (see<br>page 790)                         | trigger function (see page 560)  |
| Config   | pod assignment (see page 98)   |
| load   | open (see page 220)  |
| Filter tool  | "Filter/Colorize tool" (in the online help)  |
| Chart tool, Chart<br>display tool, Chart<br>window, chart mode | view waveform bus data as chart (see page 245), or "chart data in<br>VbaView windows" (in the online help) |

See Also • , "Quick Start for 16700-Series Users"

## Concepts



- Menus (see page 453)
- Toolbars (see page 469)
- Marker Measurement Display Bar (see page 475)
- Windows (see page 476)
- Dialogs (see page 494)
- Trigger Functions (see page 560)
- Data Formats (see page 588)
- Object File Formats Supported by the Symbol Reader (see page 600)
- General-Purpose ASCII (GPA) Symbol File Format (see page 601)
- Product Overviews (see page 608)
  - 1680/1690-Series Logic Analyzer Product Overview (see page 608)
  - 16800-Series Logic Analyzer Product Overview (see page 614)
  - 16900-Series Logic Analysis System Product Overview (see page 617
  - U4154A Logic Analyzer Product Overview (see page 626)
  - 16850-Series Logic Analyzer Product Overview (see page 628)
  - Agilent Logic Analyzer Application Product Overview (see page 631)
- Logic Analyzer Notes (see page 635)
  - 1680/1690-Series Logic Analyzer Notes (see page 637)
  - 16740/41/42 Logic Analyzer Notes (see page 638)
  - 16750/51/52 Logic Analyzer Notes (see page 640)
  - 16753/54/55/56 Logic Analyzer Notes (see page 643)
  - 16760 Logic Analyzer Notes (see page 645)
  - 16800-Series Logic Analyzer Notes (see page 651)
  - 16910/11 Logic Analyzer Notes (see page 654)
  - 16950/51 Logic Analyzer Notes (see page 656)
  - 16960 Logic Analyzer Notes (see page 658)
  - U4154A Logic Analyzer Notes (see page 676)



- 16850-Series Logic Analyzer Notes (see page 711)
- Specifications and Characteristics (see page 714)
  - 1680/1690-Series Logic Analyzer Specifications and Characteristics (see page 714)
  - 16740/41/42 Logic Analyzer Specifications and Characteristics (see page 717)
  - 16750/51/52 Logic Analyzer Specifications and Characteristics (see page 722)
  - 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 727)
  - 16760 Logic Analyzer Specifications and Characteristics (see page 734)
  - 16800-Series Logic Analyzer Specifications and Characteristics (see page 742)
  - 16910/11 Logic Analyzer Specifications and Characteristics (see page 749)
  - 16950/51 Logic Analyzer Specifications and Characteristics (see page 757)
  - 16960 Logic Analyzer Specifications and Characteristics (see page 764)
  - 16900-Series Logic Analysis System Frame Characteristics (see page 774)
  - U4154A Logic Analyzer Specifications and Characteristics (see page 775)
  - 16850-Series Logic Analyzer Specifications and Characteristics (see page 779)

# Menus

- File Menu (see page 453)
- Edit Menu (see page 454)
- View Menu (see page 456)
- Setup Menu (see page 456)
- Tools Menu (see page 458)
- Markers Menu (see page 460)
- Run/Stop Menu (see page 461)
- Overview Menu (see page 462)
- Listing Menu (see page 462)
- Waveform Menu (see page 462)
- Compare Menu (see page 463)
- Source Menu (see page 464)
- Protocol Viewer Menu (see page 464)
- VbaView Menu (see page 465)
- Window Menu (see page 466)
- Help Menu (see page 467)

## File Menu

| Eile   |              |
|--|--------------|
| 🗋 New  | Ctrl+N       |
| 🗃 Open   | Ctrl+O       |
| ⊆lose  | Ctrl+F4      |
| 📕 <u>S</u> ave   | Ctrl+S       |
| Save <u>A</u> s  |              |
| Import   | Ctrl+I       |
| Export   | Ctrl+Shift+E |
| <u>G</u> o Offline   |              |
| <u>G</u> o Online To   |              |
| 🖨 Print  | Ctrl+P       |
| <recent configur<="" th=""><th>ation Files&gt;</th></recent> | ation Files> |
| E⊻it   |              |

| New                 | Creates a new logic analyzer configuration file.                |
|---------------------|---|
| Open                | Opens a previously saved logic analyzer configuration file.     |
| Close               | Closes the active window after asking whether to save its data. |
| Save (see page 206) | Saves changes to the currently open configuration file.         |

| Save As (see<br>page 206)                    | Saves the currently open configuration file to a new name.   |
|--|--|
| Import                                       | Opens the Import Dialog (see page 514) for importing fast binary output data from 16700-series logic analyzers (for offline analysis) or for importing pattern generator stimulus vectors. |
| Export (see<br>page 207)                     | Saves captured data to comma-separated value (CSV) files. CSV files can be imported into spreadsheet, database, or other data analysis programs.   |
| Go Offline                                   | Disconnects the <i>Agilent Logic Analyzer</i> application from the currently connected frame.  |
| Go Online To Local<br>Frame                  | Connects the <i>Agilent Logic Analyzer</i> application to the local frame. If there is no local frame, the Offline Startup Options dialog (see page 521) opens.                            |
| Go Online To                                 | Opens the Select System to Use dialog (see page 531) for choosing a frame to connect the <i>Agilent Logic Analyzer</i> application to.   |
| Print  | Opens the Printing Data dialog (see page 525) for printing displayed data within a defined range.  |
| Recent Configuration<br>Files (see page 222) | Lists recently opened files for quick reference or access.   |
| Exit   | Closes the logic analyzer user interface window.   |

# Edit Menu

| Edit                          |          |
|-------------------------------|----------|
| 🔊 Undo                        | Ctrl+Z   |
| 🐰 Cu <u>t</u>                 | Ctrl+X   |
| В ⊂ору                        | Ctrl+C   |
| Copy <u>S</u> creen           |          |
| 🔁 Paste                       | Ctrl+V   |
| Insert Bus/Signal Into Window | Alt+I    |
| Remove Bus/Signal From Window |          |
| Window Properties             | Alt+P    |
| Symbols                       |          |
| 🙀 Eind                        | Ctrl+F   |
| 🙀 Find Pr <u>e</u> vious      | Shift+F3 |
| 🙀 Find <u>N</u> ext           | F3       |
| K Go To Beginning             | Ctrl+B   |
| T Go To <u>I</u> rigger       | Ctrl+T   |
| ▶ Go To <u>E</u> nd           | Ctrl+E   |
| Options                       |          |

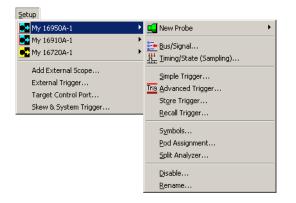
| Undo                                | Undo the last user action. This includes any properties that have<br>changed such as column color, column width, column move, column<br>insert, column delete, etc. Items that cannot be undone include scrolling,<br>acquisition runs and simple trigger modifications. |
|-------------------------------------|--|
| Cut                                 | Cuts the selection from alphanumeric fields in listing and waveform windows. Alphanumeric fields in lower level modal dialogs are cut using keyboard commands (see page 632) (accelerator keys). Cut selections are pasted to the clip board.                            |
| Сору                                | Copies the selection from alphanumeric fields in listing and waveform windows. Alphanumeric fields in lower level modal dialogs are copied using keyboard commands (see page 632) (accelerator keys). Copied selections are pasted to the clip board.                    |
| Copy Screen (see<br>page 355)       | Copies the current screen to a bitmap and places it on the system clip board.  |
| Paste                               | Pastes the cut or copied data that is stored in the clip board into the alphanumeric field. Alphanumeric data is pasted into fields in lower level modal dialogs using keyboard commands (see page 632) (accelerator keys).  |
| Insert Bus/Signal<br>Into Window    | Inserts a predefined bus or signal into the display.   |
| Remove Bus/Signal<br>From Window    | Deletes the highlighted bus or signal from the display window.   |
| Window Properties<br>(see page 526) | Accesses the window properties dialog.   |
| Symbols                             | Opens the Symbols dialog (see page 545) for setting up symbols for the selected bus/signal.  |
| Find (see page 294)                 | Locates specific data in the acquisition.  |
| Find Previous (see<br>page 294)     | Locates the previous occurrence of the specified data.   |
| Find Next (see<br>page 294)         | Locates the next occurrence of the specified data.   |
| Go To Beginning (see<br>page 276)   | Places the beginning of the captured data trace at center screen.  |
| Go To Trigger (see<br>page 276)     | Places the trigger point at center screen.   |
| Go To End (see<br>page 276)         | Places the end of the captured data trace at center screen.  |
|                                     | Accesses the System Options dialog (see page 522).   |

## **View Menu**

| View                    |              |                             |
|-------------------------|--------------|-----------------------------|
| Com Out Eul             | Ctrl+Shift+F |                             |
| Q Zoom Out              | Shift+O      |                             |
| 🔍 Zoom <u>I</u> n       | Shift+I      |                             |
| <u>T</u> oolbars        | •            | Standard                    |
| E Full Screen           | F9           | Pattern Generator           |
| ✓ Tabbed <u>Windows</u> | F11          | 🖌 Analyzer Setup            |
|                         |              | External Oscilloscope Setup |
| ✓ <u>S</u> tatus Bar    | F12          | – Data Import               |
|                         |              | ✓ Probes                    |
|                         |              | ✓ Markers                   |
|                         |              | Run/Stop                    |
|                         |              | Visual Basic                |
|                         |              | <u>C</u> ustomize           |

| Zoom Out Full                 | Zooms out on an active window as far as possible. |
|-------------------------------|---|
| Zoom Out (see<br>page 240)    | Zooms out on an active window.                    |
| Zoom In (see<br>page 240)     | Zooms in on an active window.                     |
| Toolbars (see<br>page 469)    | Access the Toolbar dialog window.                 |
| Full Screen                   | Enables or disables full screen display.          |
| Tabbed Windows (see page 353) | Enables or disables Listing and Waveform tabs.    |
| Status Bar                    | Enables or disables the status bar.               |

# Setup Menu



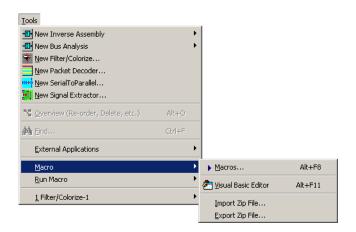
| New Probe  | Lets you set up the FPGA Dynamic Probe (for probing signals internal to<br>an FPGA) or set up definitions for other probes that are used (see<br>"Setting Up Probes" (in the online help)).   |
|--|---|
| Bus/Signal                                       | Accesses the Buses/Signals (see page 499) tab of the Analyzer Setup dialog (see page 498).  |
| Timing/State<br>(Sampling)                       | Accesses the Sampling (see page 500) tab of the Analyzer Setup dialog (see page 498).   |
| Simple Trigger                                   | See Specifying Simple Triggers (see page 156).  |
| Advanced Trigger                                 | Accesses the Advanced Trigger (see page 496) dialog.  |
| Store Trigger                                    | Stores current trigger.   |
| Recall Trigger (see<br>page 527)                 | Accesses a list of most recently used triggers.   |
| Symbols  | Opens the Symbols dialog (see page 545) for setting up symbols for the selected bus/signal.   |
| Pod Assignment                                   | Opens the Pod Assignment dialog (see page 524) for reserving pods or<br>pod pairs for time tag storage. When a <i>module</i> (see page 790) has been<br>split into two modules, this dialog can also be used to re-assign<br>channels to the split modules. |
| Split Analyzer                                   | Opens the Split Analyzer Setup dialog (see page 541) for splitting a logic analyzer module into two modules.  |
| Unsplit Analyzer                                 | This item appears when a logic analyzer module has been split into two modules; it re-combines the split modules (see page 100) into one module.  |
| Disable/ Enable                                  | Disabling a module prevents its captured data from being sent to tools<br>and display windows; this will speed up the processing of data from<br>other modules.   |
| Rename   | Lets you rename the logic analyzer module.  |
|  |   |
| " Add External<br>Scope" (in the<br>online help) | Runs the <i>Add External Oscilloscope</i> wizard for connecting an external oscilloscope to the logic analyzer.   |
| Delete External<br>Scope                         | Removes the setup for an externally connected oscilloscope.   |
| External Trigger                                 | Opens the External Trigger dialog (see page 510) for setting up triggers between the logic analyzer and other, external instruments.  |
|  |   |

### 12 Reference

| Target Control Port      | Opens the Target Control Port dialog (see page 549) for outputting signals on the logic analysis system frame's <i>target control port</i> .   |
|--------------------------|--|
| Skew & System<br>Trigger | Opens the Module Skew and System Trigger dialog (see page 520) for specifying which <i>module</i> (see page 790) is the <i>system trigger</i> (that is, which module's trigger reference point is <i>Time=0</i> ) and for specifying the trigger reference point skew for modules that are not the <i>system trigger</i> . |

## **Tools Menu**

| Tools   |        | · ····   |
|---|--------|--|
| New Inverse Assembly                            | •      | <u>A</u> RM Inverse Assembler                            |
| + New Bus Analysis                              | +      | Motorola PowerQUICC (MPC8XX) Inverse Assembler           |
| 👻 New Filter/Colorize                           |        | IBM PowerPC 405 Inverse Assembler                        |
| New Packet Decoder                              |        | Freescale MPC555 Inverse Assembler                       |
| <mark>™•</mark> • <u>N</u> ew SerialToParallel… |        | Motorola 74xx 60xbus Inverse Assembler                   |
| 📶 New Signal Extractor                          |        | ARM11 ETM Decoder  |
| 🕆 Overview (Re-order, Delete, etc.)             | Alt+O  | Motorola PowerQUICC II (MPC8260) Inverse Assembler       |
|   | HICTO  | Ereescale M-CORE Nexus Decoder and Inverse Assembler     |
| 🚧 Eind  | Ctrl+F | PowerPC 6xx/7xx Inverse Assembler                        |
| External Applications                           | •      | Motorola 6833x/6837x Inverse Assembler                   |
| Excernal upplications                           |        | Ereescale StarCore140 Nexus Decoder                      |
| Macro   | +      | Ibm405TracePort Inverse Assembler                        |
| <u>R</u> un Macro                               | +      | Motorola PowerQUICC III (MPC85xx) GPCM Inverse Assemble  |
| 1 Filter/Colorize-1                             | •      | Motorola 74xx MPXbus Inverse Assembler                   |
|   |        | ARM AHB Inverse Assembler                                |
|   |        | Ereescale MXC Memory Bus Decoder                         |
|   |        | ARM7/9 ETM Decoder                                       |
|   |        | Motorola PowerQUICC III (MPC85xx) DDR Inverse Assembler. |
|   |        | LPC Bus Decoder  |



All add-in tools are grouped under the tools menu. The *Agilent Logic Analyzer* application comes with a filter/colorize tool built in. If you are using inverse assemblers, bus analysis tools, or other third-party tools, the tools will show up in the Tools menu under New.

 $\underline{X}ilin \times MicroBlaze Inverse Assembler \dots$ 

As tools are created, they are added to the bottom of the Tools menu. The menus above show one active tool.

| New (see page 346)                   | Creates a new inverse assembly, bus analysis, filter/colorize, packet decoder, serial to parallel, or signal extractor tool.  |
|--------------------------------------|---|
| Overview (see<br>page 345)           | Lets you manage the active tools.   |
| Find (see page 294)                  | Locates specific data in the acquisition.   |
| External<br>Applications>            | Lets you run external applications from the <i>Agilent Logic Analyzer</i> application's menu. <b>Setup</b> on the submenu opens the External Application Setup dialog (see page 508) that lets you add, edit, arrange, or remove items from the submenu.  |
| Macro>                               | <ul> <li>Lets you:</li> <li>Open the Macros dialog for "choosing a Visual Basic macro to run"<br/>(in the online help).</li> <li>Open the Visual Basic Editor for "editing programs" (in the online<br/>help).</li> <li>"Import VBA project code from .zip files" (in the online help).</li> <li>"Export VBA project code to .zip files" (in the online help).</li> <li>For more information, refer to the Visual Basic online help.</li> </ul>   |
| Run Macro>                           | <ul> <li>Opens the Add-In Manager dialog which lets you register an add-in (a customized tool that adds capabilities to the Visual Basic development environment), load or unload it, and set its load behavior. For more information, click Help in the Add-In Manager dialog.</li> <li>Runs a sample macro. As shipped from the factory, the submenu contains: <ul> <li>FindEdges (macro for displaying the time between two edges and placing markers on certain edge pairs).</li> <li>RepetitiveSaveToFile (macro for saving data from repetitive runs to incrementing file names).</li> <li>SendToExcel (macro for sending logic analyzer data to Microsoft Excel).</li> <li>SendToPatternGeneratorModule (macro for sending logic analyzer data to a pattern generator module as stimulus vectors).</li> <li>You can add your own VBA macros to this submenu by placing VBA project code .zip files in the directory:</li> <li><drive letter="">:\<install directory="">\VBA\</install></drive></li> </ul> </li> <li>C:\Program Files\Agilent Technologies\Logic Analyzer\VBA\</li> </ul> |
| 1 <i>tool name</i> (see<br>page 348) | Edit an existing tool.  |

See Also • To add a new tool (see page 346)

- To change a tool (see page 348)
- To delete a tool (see page 346)
- "Using the Filter/Colorize Tool" (in the online help)

# **Markers Menu**

| Markers                            |
|------------------------------------|
| ⁺∕∕ <u>N</u> ew                    |
| 🤣 Place On Screen                  |
| 🎾 <u>G</u> o To                    |
| 🍟 <u>C</u> enter About             |
| Delete                             |
| 🥍 New Time Interval Measurement    |
| 🧏 New Sample Interval Measurement  |
| 🎾 New <u>V</u> alue At Measurement |
| 🦻 Hide Measurements List           |
| Pg Properties                      |

| New (see page 272)                                   | Creates a new marker.   |
|--|---|
| Place on Screen<br>(see page 274)                    | Places a new or selected (existing) marker at the middle of the screen. |
| Go To (see<br>page 276)                              | Goes to a selected marker.  |
| Center About (see page 277)                          | Centers the display around a selected marker.                           |
| Delete   | Deletes selected markers.   |
| New Time Interval<br>Measurement (see<br>page 279)   | Creates a new time interval measurement.                                |
| New Sample Interval<br>Measurement (see<br>page 280) | Creates a new sample interval measurement.                              |
| New Value At<br>Measurement (see<br>page 282)        | Creates a new value at measurement.                                     |
| Hide/Show<br>Measurements List                       | Hides or shows the marker measurement display bar.                      |
| Properties (see page 284)                            | Accesses the markers properties dialog                                  |

# Run/Stop Menu

| Run                          | F5            |   |
|------------------------------|---------------|---|
| -<br>Run Re <u>p</u> etitive | Ctrl+F5       |   |
| Stop                         |               |   |
| My 16720A-1                  |               | <u> <u> </u> </u> |
| Cancel                       | Shift+F8      | <u> 3</u> Run Repetitive  |
| Resume                       | Shift+Ctrl+F8 | <u>S</u> tep  |
| Status                       |               |   |
|                              |               | Reset   |

| <u>R</u> un/Stop                  |               |
|-----------------------------------|---------------|
| ▶ <u>R</u> un                     | F5            |
| & Run Re <u>p</u> etiti           | ve Ctrl+F5    |
| ■ <u>S</u> top                    | F8            |
| ⊠ <u>C</u> ancel                  | Shift+F8      |
| R <u>e</u> sume                   | Shift+Ctrl+F8 |
| Run Pr <u>o</u> perties<br>Status |               |

| Run                            | Starts sampling, fills logic analyzer memory with samples around the trigger, and stops.   |
|--------------------------------|--|
| Run Repetitive                 | Starts sampling, fills logic analyzer memory with samples around the trigger, and repeats.   |
| Stop                           | Stops a logic analyzer measurement that is in progress.  |
| (Pattern Generator<br>Module)> | Provides access to the " pattern generator module's run/stop commands" (in the online help).   |
| Cancel                         | When searching, using a filter, or exporting captured data, Cancel stops the operation.  |
| Resume                         | If you have used Cancel to stop a filter tool operation, Resume continues the filter operation.  |
| Run Properties                 | Opens the Run Properties dialog (see page 529) which lets you enable,<br>and set the options for, saving captured data after each run and stopping<br>after a certain number of repetitive runs. |
| Status                         | Opens the Status dialog (see page 542).  |

# **Overview Menu**

| Overview        |       |
|-----------------|-------|
| <u>R</u> edraw  |       |
| System Summary. |       |
| Duplicate       |       |
| Delete          |       |
| Disable         |       |
| <u>R</u> ename, |       |
| Properties      | Alt+P |

| Redraw         | Re-paints the Overview window.   |
|----------------|--|
| System Summary | Opens the System Summary dialog (see page 546) which displays<br>information about the <i>frames</i> (see page 789), <i>modules</i> (see page 790),<br><i>cards</i> (see page 788), and <i>slots</i> (see page 793) in the logic analysis<br>system. |
| Delete         | Closes the Overview window.  |

# **Listing Menu**

| Listing        |       |
|----------------|-------|
| Duplicate      |       |
| Delete         |       |
| <u>R</u> ename |       |
| Properties     | Alt+P |

| Duplicate  | Adds a new Listing window with the same properties as the window being displayed. |
|------------|---|
| Delete     | Closes the Listing window.  |
| Rename     | Lets you rename the Listing window.   |
| Properties | Lets you change Listing window properties.  |

See Also • Analyzing Listing Data (see page 259)

• To set listing window properties (see page 263)

# Waveform Menu

| Waveform       |       |
|----------------|-------|
| Duplicate      |       |
| <u>D</u> elete |       |
| <u>R</u> ename |       |
| Properties     | Alt+P |

| Duplicate  | Adds a new Waveform window with the same properties as the window being displayed. |
|------------|--|
| Delete     | Closes the Waveform window.  |
| Rename     | Lets you rename the Waveform window.   |
| Properties | Lets you change Waveform window properties.  |

- **See Also** Analyzing Waveform Data (see page 239)
  - To set waveform window properties (see page 249)

## **Compare Menu**

| ⊆ompare                 |       |
|-------------------------|-------|
| ⊆ору                    |       |
| Range & Offset          |       |
| <u>N</u> ext Difference |       |
| Previous Difference     |       |
| Duplicate               |       |
| <u>D</u> elete          |       |
| Disable                 |       |
| <u>R</u> ename          |       |
| Properties              | Alt+P |

| Сору                | Copies data to the reference buffer.  |
|---------------------|---|
| Range & Offset      | Lets you compare a range of samples and offset the reference data.                |
| Next Difference     | Finds the next difference (below the center reference).                           |
| Previous Difference | Finds the previous difference (above the center reference).                       |
| Duplicate           | Adds a new Compare window with the same properties as the window being displayed. |
| Delete              | Closes the Compare window.  |
| Disable, Enable     | Lets you disable or re-enable the Compare window.                                 |
| Rename              | Lets you rename the Compare window.   |
| Properties          | Lets you change Compare window properties.  |

#### See Also

- Compare Display Window (see page 485)
- Comparing Captured Data to Reference Data (see page 305)
- To set Compare window properties (see page 307)

# Source Menu

| Source         |       |
|----------------|-------|
| Duplicate      |       |
| <u>D</u> elete |       |
| <u>R</u> ename |       |
| Properties     | Alt+P |

| Duplicate  | Adds a new Source window with the same properties as the window being displayed. |
|------------|--|
| Delete     | Closes the Source window.  |
| Rename     | Lets you rename the Source window.   |
| Properties | Lets you change Source window properties.  |

### **See Also** • Source Display Window (see page 486)

- Viewing Source Code Associated with Captured Data (see page 308)
- To set Source window properties (see page 313)

## **Protocol Viewer Menu**

| Duplicate      |       |
|----------------|-------|
| <u>D</u> elete |       |
| <u>R</u> ename |       |
| Properties     | Alt+P |

| Duplicate  | Adds a new Protocol Viewer window with the same properties as the window being displayed. |
|------------|---|
| Delete     | Closes and deletes the Protocol Viewer window.  |
| Rename     | Lets you rename the Protocol Viewer window.   |
| Properties | Lets you change Protocol Viewer window properties.  |

- **See Also** Protocol Viewer Display Window (see page 487)
  - Analyzing Packet Data (see page 316)
  - Changing Protocol Viewer Window Properties (see page 338)

# VbaView Menu

| VbaView        |       |
|----------------|-------|
| <u>R</u> edraw |       |
| ⊻iew Code…     |       |
| Duplicate      |       |
| Delete         |       |
| Disable        |       |
| <u>R</u> ename |       |
| Properties     | Alt+P |

| Redraw          | Redraws the chart in the VbaView window.  |
|-----------------|---|
| View Code       | Views the code associated with the VbaView window in the Visual Basic Editor.     |
| Duplicate       | Adds a new VbaView window with the same properties as the window being displayed. |
| Delete          | Closes the VbaView window.  |
| Disable, Enable | Lets you disable or re-enable the VbaView window.                                 |
| Rename          | Lets you rename the VbaView window.   |
| Properties      | Lets you change VbaView window properties.  |

**See Also** • VbaView Window (see page 490)

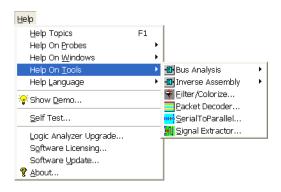
# Window Menu

| Window                  |                            |
|-------------------------|----------------------------|
| 👫 New <u>C</u> ompare   |                            |
| New Listing             |                            |
| New Protocol Viewer     |                            |
| New Source              |                            |
| 🔥 New VbaView 🔹 🕨       | <u>B</u> us vs Bus Sample  |
| 🏪 New <u>W</u> aveform  | Distribution Sample        |
| Noverview Alt+O         | Export to IE               |
| _                       | External Scope Web Control |
| ₽ <u>N</u> ext F6       | Hello World Sample         |
| Previous Shift+F6       | Timing Compare             |
| 🖶 Ca <u>s</u> cade      |                            |
| Tile Horizontally       |                            |
| Tile <u>V</u> ertically |                            |
| <u>A</u> rrange Icons   |                            |
| 1. Or unem size u       |                            |
| <u>1</u> Overview       |                            |
| 2 Listing               |                            |
| ✓ <u>3</u> Waveform     |                            |

| New Compare            | Creates a new Compare window (see page 485).                 |
|------------------------|--|
| New Listing            | Creates an additional Listing window (see page 482).         |
| New Protocol<br>Viewer | Creates an additional Protocol Viewer window (see page 487). |
| New Source             | Creates a new Source window (see page 486).                  |

| Creates a new VbaView window (see page 490) and populates it with  |
|--|
| <ul> <li>custom code. As shipped from the factory, the submenu contains:</li> <li>Bus vs Bus Sample (simple XY scattergram chart example).</li> <li>Distribution Sample (simple data distribution bar chart example).</li> <li>Export to IE (simple export data to another application example).</li> <li>External Scope Web Control (opens web control window for external oscilloscope).</li> <li>Hello World Sample (simple text output example).</li> <li>Timing Compare (compares timing analyzer data with a specified tolerance).</li> <li>You can add your own VbaView windows (and code) to this submenu by placing VBA project code .zip files in the directory:</li> <li><drive letter="">:\<install directory="">\VBA\</install></drive></li> <li>For example:</li> <li>C:\Program Files\Agilent Technologies\</li> <li>Logic Analyzer\VBA\</li> </ul> |
| Creates an additional Waveform window (see page 476).  |
| Opens or displays the Overview window (see page 491).  |
| Displays the next window.  |
| Displays the previous window.  |
| Displays all opened windows in an overlaid and offset format.  |
| Displays all opened windows so the horizontal display space is equally divided.  |
| Displays all opened windows so the vertical display space is equally divided.  |
| All minimized listing and waveform windows are arranged at the bottom of the analyzer window.  |
|  |

# Help Menu



| Help Topics               | Accesses the online help.  |
|---------------------------|--|
| Help On Probes            | Opens online help for probes.  |
| Help On Windows           | Opens online help for the Waveform, Listing, Compare, or Source windows.   |
| Help On Tools             | Opens online help for tools.   |
| Help Language             | Lets you choose between the English and Japanese versions of the online help (see Accessing Japanese Online Help (Windows XP) (see page 397)).       |
| Show Demo                 | Launches the Demo Center (see page 78) application that demonstrates logic analysis system features.   |
| Self Test                 | Accesses the Logic Analyzer Self-Tests dialog (see Running Self Tests (see page 395)).   |
| Logic Analyzer<br>Upgrade | Accesses the Agilent Logic Analyzer Upgrade dialog (see page 497)<br>which provides information for upgrading hardware in logic analyzer<br>modules. |
| Software Licensing        | Opens the Software Licensing dialog (see page 534) for managing software licenses used by the logic analysis system.                                 |
| Software Update           | Opens the Add or Remove Agilent Logic Analyzer Software (see page 367) tool for managing your logic analyzer software and keeping it up to date.     |
| About                     | Displays product version and copyright information.  |

# **Toolbars**

Toolbars are located under the menu bar, and are used to quickly access a function or perform a task. By default, not all toolbars, or individual tools within a given toolbar are displayed. For a complete list of all available toolbars, choose **View>Toolbars>**. For a complete list of all tools within a given toolbar, choose **View>Toolbars>**Customize...; then, select the **Commands** tab in the Customize dialog.

- Standard (see page 469)
- Pattern Generator (see page 470)
- Analyzer Setup (see page 471)
- External Oscilloscope Setup (see page 471)
- Data Import (see page 472)
- Probes (see page 472)
- Markers (see page 472)
- Run/Stop (see page 473)
- Visual Basic (see page 473)
- Customize... (see page 474)

## **Standard Toolbar**

D 🖆 🖬 🎒 🖓 🙀 📜 🗖 🕨 🔍 🔍 🔧

|            | New - Creates a new logic analyzer configuration file.                                |
|------------|---|
| <b></b>    | Open - Opens a previously saved logic analyzer configuration file.                    |
|            | Save - Saves changes to the currently open configuration file.                        |
| 4          | Print (see page 525) - Prints displayed data within a defined range.                  |
| <i>#</i> 1 | Find (see page 294) - Locates specific data in the acquisition.                       |
| H          | Find Previous (see page 294) - Locates the previous occurrence of the specified data. |
| ส์         | Find Next (see page 294) - Locates the next occurrence of the specified data.         |
| K          | Go to Beginning (see page 276) - Centers the beginning of the acquisition data.       |
| T          | Go to Trigger (see page 276) - Centers the trigger point of the acquisition.          |
| M          | Go to End (see page 276) - Centers the end of the acquisition data.                   |

| Q | Zoom Out (see page 240) - Zooms in on an active window.          |
|---|--|
| • | Zoom In (see page 240) - Zooms out on an active window.          |
| * | Overview - Opens or displays the Overview window (see page 491). |

## NOTE

The following are optional standard toolbar icons.

| ж        | Cuts the selection and places it on the clip board.                                   |
|----------|---|
|          | Copies the selection and places it on the clip board.                                 |
| â        | Pastes the data that is stored on the clip board.                                     |
| 8        | Provides online help information about the <i>Agilent Logic Analyzer</i> application. |
| ŝ        | Undo last user action.  |
|          | Enables or disables full screen display.  |
| ₽        | Activate the next window.   |
| æ        | Activates the previous window.  |
| <b>•</b> | Arranges windows as cascaded overlapping tiles.                                       |
|          | Arranges windows as non-overlapping horizontal tiles.                                 |
|          | Arranges windows as non-overlapping vertical tiles.                                   |

**See Also** • To create a custom toolbar (see page 474)

# **Pattern Generator Toolbar**

| E c | Seg Mac | <u>.</u> | ₿. | • | 3 | - <del>-}-</del> | Ĵ |
|-----|---------|----------|----|---|---|------------------|---|
|-----|---------|----------|----|---|---|------------------|---|

| 8<br>8      | Sets up the pattern generator bus/signal attributes attributes. |
|-------------|---|
| <del></del> | Sets up the pattern generator clocking attributes.              |
| Seg         | Sets up the pattern generator sequence.                         |
| Mac         | Sets up the pattern generator macros.                           |

| ₹  | Runs the pattern generator.                                    |
|----|--|
| 3  | Runs the pattern generator repetitively.                       |
|    | Stops the pattern generator.                                   |
|    | Steps through the pattern generator vector sequence.           |
| •+ | Resumes pattern generator vector sequence output.              |
|    | Resets the pattern generator vector sequence to the beginning. |

**See Also** • "Using the Pattern Generator" (in the online help)

# **Analyzer Setup Toolbar**



| 8    | Bus/Signal - Accesses the Buses/Signals (see page 499) tab of the Setup dialog.         |
|------|---|
| #    | Timing/State (Sampling) - Accesses the Sampling (see page 500) tab of the Setup dialog. |
| Tris | Advanced Trigger - Accesses the Advanced Trigger (see page 496) dialog.                 |

See Also • To create a custom toolbar (see page 474)

## **External Oscilloscope Setup Toolbar**

### 🗄 🖸 🌆

| 23   | Sets up the external oscilloscope connection attributes. |
|------|--|
| D    | Sets up the external oscilloscope option attributes.     |
| Trig | Sets up the external oscilloscope trigger attributes.    |

**See Also** • "Infiniium Oscilloscope Time Correlation" (in the online help)

# **Data Import Toolbar**

🗄 😭 🔁

| 6<br>6   | Lets you edit the data import module bus/signal definitions. |
|----------|--|
| <b>P</b> | Displays data import module file information.                |
| <b>i</b> | Re-reads the data import module file.                        |

| See Also | ٠ | Using | Data | Import | Modules | (see     | page | 227) |
|----------|---|-------|------|--------|---------|----------|------|------|
|          |   | - 0   |      | T      |         | <b>C</b> | 1.0  |      |

# **Probes Toolbar**

|  | Opens the properties dialog for a particular probe.<br>• "Using the Xilinx FPGA Dynamic Probe" (in the online help)<br>• "Using the FPGA Dynamic Probe for Altera FPGAs" (in the online help)<br>• "Using General Purpose Probes" (in the online help)<br>• "PCI Express Analysis Probe" (in the online help)<br>• "Serial ATA Analysis Probe" (in the online help) |
|--|---|
|--|---|

# **Markers Toolbar**

## +/ →/ °F/ ₩/,

| */ | New (see page 272) - Creates a new marker.                             |
|----|--|
| */ | Go To (see page 276) - Centers the display around the selected marker. |
| of | Creates a new value at a measurement (see page 282).                   |
| H  | Creates a new time interval measurement (see page 279).                |

## NOTE

The following are optional markers toolbar icons.

| */  | Place Maker (see page 274) - Places a new or selected (existing) marker at the middle of the screen. |
|-----|--|
| ")/ | Center About (see page 277) - Centers the display around two selected markers.                       |
| H/  | Creates a new sample interval measurement (see page 280).  |
| 1   | Hides or shows the marker measurement display bar.   |
| P   | Accesses the markers properties (see page 284) dialog.   |

**See Also** • To create a custom toolbar (see page 474)

## **Run/Stop Toolbar**



|           | Starts sampling, fills logic analyzer memory with samples.  |
|-----------|---|
| <b>\$</b> | Starts Sampling, fills logic analyzer memory with samples around the trigger, and repeats.            |
|           | Stops a logic analyzer measurement in progress, for example, when the trigger condition is not found. |
| ×         | Cancels the current operation.  |
|           | Resumes the cancelled operation.  |

**See Also** • To create a custom toolbar (see page 474)

# **Visual Basic Toolbar**

#### ۰ 🔁 🔹

| • | Runs a Visual Basic for Applications (VBA) macro. |
|---|---|
| 2 | Opens the Visual Basic Editor.                    |

**See Also** • "Using the Advanced Customization Environment (ACE)" (in the online help)

# To customize toolbars

|                                  | • To add icons to a toolbar (see page 474)  |
|----------------------------------|---|
|                                  | • To remove icons from a toolbar (see page 474)   |
|                                  | • To create a new toolbar (see page 474)  |
|                                  | • To restore a toolbar to its original icons (see page 474)   |
| To add icons to a                | 1 From the menu bar, select View>Toolbars>Customize   |
| toolbar                          | 2 Select the Commands tab.  |
|                                  | 3 Select the <b>Category</b> that you want to add icons from.   |
|                                  | <b>4</b> Drag the desired icon from the <b>Buttons</b> area to the desired position on the toolbar; then, release the mouse button to insert the tool icon. |
|                                  | <b>5</b> Repeat for any other icons you wish to add.  |
| To remove icons                  | 1 From the menu bar, select View>Toolbars>Customize   |
| from a toolbar                   | 2 Select the <b>Commands</b> tab.   |
|                                  | <b>3</b> Drag the icon from the toolbar and drop it onto the <b>Buttons</b> area of the Customize dialog.   |
|                                  | 4 Repeat for any other icons you wish to remove.  |
| To create a new                  | 1 From the menu bar, select View>Toolbars>Customize   |
| toolbar                          | 2 In the Customize dialog's Toolbars tab, click New   |
|                                  | 3 In the New Toolbar dialog, enter the name of the new toolbar, and click OK.   |
|                                  | <b>4</b> Drag the new toolbar window to the desired position in the toolbar dock.   |
|                                  | A second row of toolbars can be created by dragging a toolbar to the bottom of an existing toolbar row.   |
|                                  | If a toolbar is hidden off-screen, drag a visible toolbar to create a second row of toolbars; that should then reveal the hidden toolbar.                   |
|                                  | Once you have created a new toolbar, you can add or remove icons as described above.  |
| To restore a                     | 1 From the menu bar, select View>Toolbars>Customize   |
| toolbar to its<br>original icons | <b>2</b> In the Customize dialog's Toolbars tab, select the name of the <b>Toolbar</b> you want to restore.   |
|                                  | 3 Click Reset.  |

# **Marker Measurement Display Bar**

Marker "interval" and "value at" measurements are displayed below the menu bar with the other toolbars.



- To create a new time interval measurement (see page 279)
- To create a new sample interval measurement (see page 280)
- To create a new value at measurement (see page 282)
- To hide/show measurement display bar (see page 460)

# Windows

- Waveform Display Window (see page 476)
  - Markers Display Bar (see page 480)
  - Markers Overview Bar (see page 481)
- Listing Display Window (see page 482)
- Compare Display Window (see page 485)
- Source Display Window (see page 486)
- Protocol Viewer Display Window (see page 487)
- VbaView Window (see page 490)
- Overview Window (see page 491)

### **Waveform Display Window**

|                | Delay 5 ns 📓 🖊 🕂 🕇 🛏            |
|----------------|---------------------------------|
|                |                                 |
| Simple Trigger | -5 ns 0s 5 ns 10 ns 15 ns       |
| = * XX 🖩       | B2 X B3 X B4 X B5 X B6 X B7 X A |
| X ×            |                                 |
|                | Х вз Ж в4 В5 Х в6 в7 ХХ         |
|                |                                 |
|                | -8.75 ns 18.75 ns               |
|                |                                 |
| •   <u>)</u>   |                                 |
|                | Simple Trigger                  |

The Waveform window is accessed through the menu bar's **Window>Waveform**. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

The Waveform window displays captured data as a digital waveform. You can configure the window to display selected buses and signals with time or pattern markers in the data. You can also set up bus pattern triggers and signal trigger options.

The Waveform window consists of the following areas:

- Bus/Signal Configuration (see page 477)
- Simple Trigger (see page 156)
- Markers Display Bar (see page 480)
- Waveform Display Area (see page 478)
- Markers Overview Bar (see page 481)

- Delay Controls (see page 242)
- Scale (time/division) Controls (see page 240)

**Bus/Signal** To access the following Bus/Signal configuration options, right-click on any bus or signal name in the Bus/Signal column.



| Undo                          | Undo the last action performed.  |
|-------------------------------|--|
| Insert Row Before             | Inserts a bus/signal before the highlighted row.   |
| Insert Row After              | Inserts a bus/signal after the highlighted row.  |
| Delete>                       | Deletes the bus/signal in the highlighted row or deletes all buses/signals.  |
| Expand                        | Expands the highlighted bus into separate displayed channels.  |
| Collapse                      | Collapses displayed channels to a single displayed bus.  |
| Assign Channels               | Access to the Buses/Signals tab of the Analyzer Setup dialog for mapping (assigning) the highlighted bus/signal to the desired pod and channel connection of the probes. |
| Rename                        | Access a keypad to rename the highlighted bus/signal.  |
| Group into Bus (see page 248) | Groups highlighted signals into a bus.   |
| Overlay (see<br>page 244)     | Overlays the highlighted bus or signal with another selected bus or signal.  |
| Overlay Remove                | Separates overlaid bus/signals.  |
| Symbols                       | Opens the Symbols dialog (see page 545) for setting up symbols for the selected bus/signal.  |

| Find                         | Opens the Find dialog for searching the captured data (see page 294).                                      |
|------------------------------|--|
| Find Bus/Signal              | Searches for a bus/signal row.   |
| View As Chart (see page 245) | Opens the View As dialog for viewing the bus data as a chart or a bus.                                     |
| Display>                     | Lets you show or hide parts of the Waveform window (see page 247).   |
| Properties (see page 249)    | Access to properties dialog for waveform window, bus/signal row, bus/signal column, and marker properties. |

WaveformTo access waveform display options, right-click anywhere in the displayDisplay Areaarea.

| F6 | Undo                    | F9  |
|----|-------------------------|-----|
| 1  | Zoom Out Full           | 1   |
| 6  | Zoom Out                | a   |
| •  | Zoom In                 | -   |
| 1  | Go To                   | ▶ 1 |
|    | Go To Beginning Of Data |     |
|    | Go To End Of Data       |     |
|    | Place Marker            | •   |
|    | Center About            | •   |
|    | Find                    |     |
|    | Find Next               |     |
|    | Find Previous           |     |
|    | Properties              |     |
|    |                         |     |

| Undo                         | Undo the last action performed.  |
|------------------------------|--|
| Zoom Out (see<br>page 240)   |  |
| Zoom In (see<br>page 240)    |  |
| Go To (see page 242)         |  |
| Place Marker> (see page 274) |  |
| Center About>                | Centers the display about a marker pair (see page 277) or waveform edges (see page 241). |
| Find (see page 294)          |  |
| Find Next (see<br>page 294)  |  |

| Find Previous (see page 294) |  |
|------------------------------|--|
| Properties (see page 249)    |  |

#### Drawing Rectangle in Data

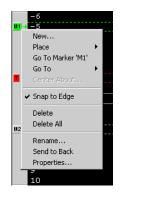


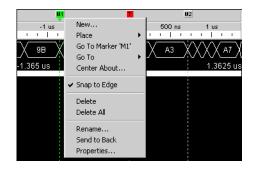
| Zoom In (see<br>page 241)        |   |
|----------------------------------|---|
| Set Quick Trigger (see page 152) | Alternative way to set a Simple Trigger.  |
| Find Next                        | Data value on left edge of rectangle becomes Find search (see page 294) criteria and next occurrence of that data value is placed at center screen.     |
| Find Previous                    | Data value on left edge of rectangle becomes Find search (see page 294) criteria and previous occurrence of that data value is placed at center screen. |

### See Also • Analyzing Waveform Data (see page 239)

- Marking, and Measuring Between, Data Points (see page 271)
- Specifying Advanced Triggers (see page 163)
- Setting Up Symbols (see page 139)
- To add or delete display windows (see page 353)
- To turn window tabs on/off (see page 353)

## **Markers Display Bar**





To access these tasks, right-click anywhere in the marker display bar.

| To create new markers.                      |
|---|
| To place markers in data.                   |
| To go to a marker.                          |
| To center the display about a marker pair.  |
| To toggle a marker's snap to edge property. |
| To delete a marker.                         |
| To delete all markers.                      |
| To rename a marker.                         |
| To send a marker to the back.               |
| To set marker properties.                   |
|   |

#### **See Also** • To read the markers display and overview bars (see page 272)

- Markers Menu (see page 460)
- Markers Toolbar (see page 472)
- Markers Overview Bar (see page 481)

#### Markers Overview Bar

| Go To Here (-2.<br>Go To<br>Send to Back                | 39157874 ms)          | Beginning Of Data<br>End Of Data<br>Trigger<br>M1<br>M2 |
|---|-----------------------|---|
|   | Go To Here (-3)       | 6.13844526 ms)  |
| Beginning Of Data<br>End Of Data<br>Trigger<br>M1<br>M2 | Go To<br>Send to Back |   |

To access these menus, click anywhere in the marker overview bar.

| Go To (see page 276)        | To go to a marker.            |
|-----------------------------|-------------------------------|
| Send to back (see page 283) | To send a marker to the back. |

- **See Also** To read the markers display and overview bars (see page 272)
  - Markers menu (see page 460)
  - Markers toolbar (see page 472)

# **Listing Display Window**

|       | Sample Number | Bus 1   | Bus 2      | Signal 1 | Signal 2 | Time            |
|-------|---------------|---------|------------|----------|----------|-----------------|
|       |               | =, XX 🏢 | =, XXX III | - ⊠      | - ⊠      |                 |
|       | -7            | КА      | 3449       | 1        | 1        | -350            |
|       | -6            | FA      | 3FFA       | 1        | 1        | -300 <b>-</b> 8 |
| M1 -) | -5            | FB      | 3FFB       | 1        | 1        | -250            |
|       | -4            | FC      | 3FFC       | 1        | 1        | -200            |
|       | -3            | FD      | 3FFD       | 1        | 1        | -150            |
|       | -2            | FE      | 3FFE       | 1        | 1        | -100            |
|       | -1            | FF      | 3 F F F    | 1        | 1        | -50             |
| ∎→    | 0             | 00      | 0000       | 0        | 0        | 0 — M           |
|       | 1             | 01      | 0001       | 0        | 0        | 50              |
|       | 2             | 02      | 0002       | 0        | 0        | 100             |
|       | 3             | 03      | 0003       | 0        | 0        | 150             |
|       | 4             | 04      | 0004       | 0        | 0        | 200             |
| M2 -  | 5             | 05      | 0005       | 0        | 0        | 250             |
|       | 6             | 06      | 0006       | 0        | 0        | 300 _1 🛯        |
|       | 7             | 07      | 0007       | <u> </u> | <u> </u> | 350             |
|       | 4             |         |            |          |          |                 |

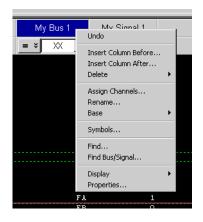
The Listing window is accessed through the menu bar's **Window>Listing**. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

The Listing window displays your captured data as a state listing. You configure the window to display selected buses and signals in columns. Within the listed data, you can insert time or pattern markers. You can also configure the bus pattern triggers and signal trigger options.

The Listing window consists of the following areas:

- Column Configuration (see page 482)
- Simple Trigger (see page 156)
- Markers Display Bar (see page 480)
- Listing Display Area (see page 483)
- Markers Overview Bar (see page 481)

**Column** To access the following column configuration options, right-click on any bus or signal name in the column head.



| Undo                                      | Undo the last action performed.   |
|---|---|
| Insert Column<br>Before (see<br>page 262) |   |
| Insert Column After<br>(see page 262)     |   |
| Delete> (see<br>page 262)                 |   |
| Assign Channels<br>(see page 104)         |   |
| Rename                                    | Access a keypad to rename the highlighted bus/signal.                                       |
| Base> (see page 267)                      |   |
| Symbols                                   | Opens the Symbols dialog (see page 545) for setting up symbols for the selected bus/signal. |
| Find                                      | Opens the Find dialog for searching the captured data (see page 294).                       |
| Find Bus/Signal                           | Searches for a bus/signal column.   |
| Display>                                  | Lets you show or hide parts of the Listing window (see page 262).                           |
| Properties (see page 263)                 | Access to properties dialog for Listing window, bus/signal column, and marker properties.   |

Listing Display To access the Listing display options, right-click anywhere in the display area.



| Undo                         | Same as Edit>Undo (see page 454). |
|------------------------------|-----------------------------------|
| Go To (see page 260)         |                                   |
| Place Marker> (see page 274) |                                   |
| Find (see page 294)          |                                   |
| Find Next (see<br>page 294)  |                                   |
| Find Previous (see page 294) |                                   |
| Properties (see page 263)    |                                   |

#### Draw Rectangle in Data

| My Bus 1 | Set Quick Trigger / Find =<br>My Bus 1 = F6 and<br>My Signal 1 = High |
|----------|---|
| = * XX 🔳 | X ×   |
|          | 1   |
| F6       | 1   |
| F7       | Set Quick Trigger   |
| F7       | Find Next   |
| F 1      |   |
| F8       | Find Previous   |
| F8       | Copy Text 🕨 🕨   |
| F8       | ±   |

| Set Quick Trigger (see page 152) | Alternative way to set a simple trigger.   |
|----------------------------------|--|
| Find Next                        | Data value on top edge of rectangle becomes Find search (see page 294) criteria and next occurrence of that data value is placed at center screen.     |
| Find Previous                    | Data value on top edge of rectangle becomes Find search (see page 294) criteria and previous occurrence of that data value is placed at center screen. |
| Copy Text (see<br>page 354)      | Copies data as text into the system clip board.  |

#### **See Also** • Analyzing Listing Data (see page 259)

- Setting Up Symbols (see page 139)
- Marking, and Measuring Between, Data Points (see page 271)
- To add or delete display windows (see page 353)
- To turn window tabs on/off (see page 353)

### **Compare Display Window**

| <<       | : >>       | <u>⊆</u> ору | <u>R</u> ange 8 | & Offset.          |         | ompare | <u>U</u> ntil    |      |           |         |   |
|----------|------------|--------------|-----------------|--------------------|---------|--------|------------------|------|-----------|---------|---|
|          | Sample     | e Number     |                 | My E               | Bus 1   |        | Time             |      |           |         |   |
|          |            |              | = *             | 111                | 1 1111  |        |                  |      |           |         |   |
| <b>Å</b> |            | 76           | 0100            | 1011               | 0100    | 1011   | 38               | ) ns |           | <b></b> |   |
| <u></u>  |            | 77           | 0100            | 1100               | 0100    | 1100   |                  | 5 ns |           |         |   |
|          |            | 78           | 0100            | 1101               | 0100    | 1101   | 390              | ) ns |           |         |   |
|          |            | 79           | 0100            | 1110               | 0100    | 1110   | 39               | 5 ns |           |         |   |
|          |            | 80           | 0100            | 1111               | 0100    | 1111   | 40               | ) ns |           |         |   |
|          |            | 81           | 0101            | <mark>1</mark> 000 | 0101    | 0000   | 40               | 5 ns |           |         |   |
|          |            | 82           | 0101            | 0001               | 0101    | 0001   |                  | ) ns |           |         |   |
|          |            | 83           | 0101            |                    | 0101    | 0010   | 41               | 5 ns |           |         |   |
|          |            |              | 0101            |                    | 0101    | 0011   |                  | 2 ns |           |         |   |
|          |            |              | 0101            |                    |         |        | 42               | 5 ns |           |         |   |
|          |            | 86           | 0101            | 0101               | 0101    | 0101   | 430              | ) ns |           | -       |   |
|          | •          |              |                 |                    |         |        |                  | -    |           | Þ       | k |
| Sar      | mples Corr | npared: 1310 | 72 0            | olumns (           | Compare | :d: 1  | Comparisons: 131 | 072  | Differenc | es: 194 |   |

The Compare window lets you compare acquired (input) data to data that has been saved in a reference buffer. The reference data has a colored background, and differences between between the input data and the reference data are highlighted.

The Compare window is accessed through the menu bar's **Window>Compare**. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

Except for the Compare window's ability to display the differences between captured data and reference data, and its inability display colorized data (from the Filter/Colorize tool), the Compare window is just like the Listing window.

- **See Also** Comparing Captured Data to Reference Data (see page 305)
  - To copy data to the reference buffer (see page 305)
  - To find differences in the compared data (see page 306)
  - To compare only a range of samples (see page 306)
  - To offset the reference data (see page 306)
  - To run until a number of compare differences (see page 307)

- To set Compare window properties (see page 307)
- Analyzing Listing Data (see page 259)

## **Source Display Window**

| Dis              | played File C:\My D | ocuments\source\ecs2.c |        |                   |                         | ▼ B       | rowse  | ⇒{  <b>1</b> { ↓ |
|------------------|---------------------|------------------------|--------|-------------------|-------------------------|-----------|--------|------------------|
| 45               | proc_spe            | c_init();              |        |                   |                         |           |        |                  |
| 46               |                     |                        |        |                   |                         |           |        |                  |
| 47               | for (;;)            |                        |        |                   |                         |           |        |                  |
| .48              | {                   |                        |        |                   |                         |           |        |                  |
| 49               |                     | ite system(num checks  | );     | Set Quick Trigger |                         |           |        |                  |
| 50               | _                   | checks++;              |        |                   |                         |           |        |                  |
| 51<br>52         | -                   | te_display(num_check   | 3);    | Find in Source    |                         |           |        |                  |
| 54<br>53         | ) proc              | _specific();           |        |                   | urce Line in Listing (f |           |        |                  |
| i i i            | · ·                 |                        |        | Find Selected Sou | urce Line in Listing (B | Backward) |        | •                |
|                  | - · · ·             | 4000                   |        | Symbols           |                         |           |        |                  |
|                  | Sample Number       | ADDR                   | MPC8   |                   |                         |           | Time   | Sc               |
|                  |                     | = > FFF0 34D8          |        | Properties        |                         | ]         |        |                  |
|                  |                     | num_checks+1           | mem    | read Ox2e         |                         |           | -1.052 | us 🔺             |
| • -              | 6                   | num_checks+2           | mem    | read Oxaa         |                         |           | -936   | ns               |
|                  | 5                   | num_checks+3           |        | read Ox42         |                         |           | -816   | ns               |
| l→ <mark></mark> | 1                   | main+23                | bl     | update s          | system                  |           | -192   |                  |
| 3                |                     | update_system+3        | mfspr  | r0,d8             |                         |           | 352    |                  |
| 2                |                     | update_system+7        | or     | r11,r1,1          |                         |           | 976    |                  |
| 12               | 1                   | update_system+B        | stwu   | r1,0xffe          | 8(r1)                   |           | 1.600  | us 🔻             |
| 4                |                     |                        |        |                   |                         |           |        |                  |
| 4                | Overview            | Listing - 1            | Wavefo | orm - 1 📃         | Source - 1              |           |        |                  |

The Source window lets you view the high-level source code that is associated with captured data.

The Source window is accessed through the menu bar's **Window>Source** command. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

The Source window has two panes: the top pane displays the high-level source code associated with the captured data, and the bottom pane is the same as a Listing window.

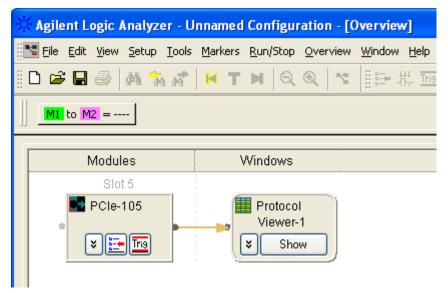
**See Also** • Viewing Source Code Associated with Captured Data (see page 308)

- To step through captured data by source lines (see page 309)
- To go to captured data associated with a source line (see page 309)
- To browse source files (see page 310)
- To search for text in source files (see page 310)
- To set a Quick Trigger in the Source window (see page 154)
- To go to the source line associated with the listing center rectangle (see page 311)
- To edit the source code directory list (see page 311)
- To select the correlation bus (see page 312)
- Changing Source Window Properties (see page 313)

• Analyzing Listing Data (see page 259)

## **Protocol Viewer Display Window**

You can use a Protocol Viewer window to display data captured by an Agilent instrument module such as the U4301A PCIe Gen3 Analyzer module. The following screen displays an instance of Protocol Viewer added to the U4301A module in the Logic Analyzer application to display the PCI Express data captured by the module.



On clicking the **Show** button on Protocol Viewer, the Protocol Viewer window is displayed with the captured data in the Logic Analyzer application.

|      | Sample Numbe   | r Time   |  | PCI-ES   | press  | Packe  | t  | Link :                                 | õpeed                                  |  | Dire                                   | ction  |  | Se  | quence Number          | Ta      |
|------|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|------------------------|---------|
| T    | 0  | 8 ns   |  | Ack  |  |  |  | Gen3 Field Decode                      |  |  | PCIe-                                  | 101  |  | 322 | A Hex                  |         |
|      | 0  | 14 na  | ,  | Cpl  |  |  |  | Gen3 F                                 | ield I                                 | ecode  | PCIe-                                  | 102  |  | 34: | 3 Hex                  | 06      |
| • 1  |  | 21 ns  | ;  | UpdateFC-Cp1   |  |  | Gen3 Field Decode                                |  | PCIe-102                               |  |  |  |  |     |                        |         |
|      | 1 28 ns  |  | ,  | Cp1  |  |  | Gen3 Field Decode                                |  | PCIe-101                               |  | F70 Hex                                |  | 04                                     |     |                        |         |
|      | 2  | 30 ns  | 1  | 1.ck   |  |  |  | Gen3 B                                 | ield T                                 | ecode  | PCTe-                                  | 102  |  | FS  | C Hev                  |         |
| etai | ls Header Paylo  | PCIe-102   | s (Traffi  | ic Overvi  | ew <sup>P</sup> LTS                                    | SSM Ove  | rview  |  |  |  |  |  |  | ×   | Compare 1<br>Show only | Favori  |
| a    |  |  | s Traffi   |  |  |  | 1-1-<br>   | Lane 5                                 | Lane 6                                 | Lane 7                                       | Lane 8                                 | Lane 9                                       |  |     |                        | Favori  |
|      | Time   | PCIe-102   | Marine and a state                                     |  |  |  | 1-1-<br>   | Lane 5                                 | Lane 6                                 | ST GALLON                                    | Lane 8                                 | Lane 9                                       |  | 1   |                        | Favori  |
|      | Time<br>( Symbol Time )  | PCIe-102<br>Sample   | Lane 0   | Lane 1   | Lane 2   | Lane 3   | Lane 4   | 2610.0.0                               | 450.0707                               | 00   | ACTION - TO                            | 2041002401                                   | L                                      | 1   |                        | Favori  |
|      | Time<br>(Symbol Time)<br>14 ns   | PCIe-102<br>Sample<br>0                                    | Lane 0   | Lane 1   | Lane 2<br>63   | Lane 3<br>43   | Lane 4<br>0A                                     | 00                                     | 00                                     | 00   | 00                                     | 00   | L;<br>21                               | 1   |                        | Favori  |
|      | Time<br>( Symbol Time )<br>14 ns<br>15 ns  | PCIe-102<br>Sample<br>0                                    | Lane 0<br>5F<br>68                                     | Lane 1<br>00<br>4D                                     | Lane 2<br>63<br>DC                                     | Lane 3<br>43<br>E3                                     | Lane 4<br>0A<br>00                               | 00                                     | 00                                     | 00   | 00                                     | 00   | L;<br>2(<br>0(                         | 1   |                        | Favorit |
|      | Time<br>(Symbol Time)<br>14 ns<br>15 ns<br>16 ns   | PCIe-102<br>Sample<br>0<br>0<br>0                          | Lane 0<br>5F<br>68<br>00                               | Lane 1<br>00<br>4D<br>00                               | Lane 2<br>63<br>DC<br>00                               | Lane 3<br>43<br>E3<br>00                               | Lane 4<br>0A<br>00<br>00                         | 00<br>00<br>00                         | 00                                     | 00<br>00<br>00<br>00                         | 00                                     | 00<br>00<br>00                               | L:<br>21<br>0(<br>0(                   | 1   |                        | Favorit |
|      | Time<br>(Symbol Time)<br>14 ns<br>15 ns<br>16 ns<br>17 ns  | PCIe-102<br>Sample<br>0<br>0<br>0<br>0                     | Lane 0<br>5F<br>68<br>00<br>00                         | Lane 1<br>00<br>4D<br>00<br>00                         | Lane 2<br>63<br>DC<br>00<br>00                         | Lane 3<br>43<br>E3<br>00<br>00                         | Lane 4<br>0A<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                   | 00<br>00<br>00<br>00                         | L:<br>2(<br>0(<br>0(                   | 1   |                        | Favorit |
|      | Time           ( Symbol Time )           14 ns           15 ns           16 ns           17 ns           18 ns                                 | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0                | Lane 0<br>5F<br>68<br>00<br>00                         | Lane 1<br>00<br>4D<br>00<br>00<br>00                   | Lane 2<br>63<br>DC<br>00<br>00<br>00                   | Lane 3<br>43<br>E3<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 4<br>0A<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00             | 00<br>00<br>00<br>00<br>00                   | L:<br>2(<br>0(<br>0(<br>0(             | 1   |                        | Favorit |
|      | Time           ( Symbol Time )           14 ns           15 ns           16 ns           17 ns           18 ns           19 ns                 | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | Lane 0<br>5F<br>68<br>00<br>00<br>00<br>00             | Lane 1<br>00<br>4D<br>00<br>00<br>00<br>00             | Lane 2<br>63<br>DC<br>00<br>00<br>00<br>00             | Lane 3<br>43<br>E3<br>00<br>00<br>00<br>00             | Lane 4<br>0A<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00       | 00<br>00<br>00<br>00<br>00<br>00             | L:<br>2(<br>0(<br>0(<br>0(<br>0(       | 1   |                        | Favorit |
|      | Time           ( Symbol Time )           14 ns           15 ns           16 ns           17 ns           18 ns           19 ns           20 ns | PCIe-102<br>Sample<br>0<br>0<br>0<br>0<br>0<br>0<br>0<br>0 | Lane 0<br>5F<br>68<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 1<br>00<br>4D<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 2<br>63<br>DC<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 3<br>43<br>E3<br>00<br>00<br>00<br>00<br>00<br>00 | Lane 4<br>0A<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00<br>53 | 00<br>00<br>00<br>00<br>00<br>00<br>00 | 00<br>00<br>00<br>00<br>00<br>00<br>00<br>00 | L;<br>2(<br>0(<br>0(<br>0(<br>0(<br>0( | 1   |                        | Favorit |

Unlike the Listing window, the Protocol Viewer window lets you view summarized and detailed packet information at the same time within two panes.

The upper pane lists the captured packets. On selecting a packet in the upper pane, specific details of that packet are displayed in various tabs of the lower pane.

#### Adding a Protocol Viewer window instance

You can add an instance of the Protocol Viewer window to a module or a tool in the Overview tab of the Logic Analyzer application. To do this, right-click the module or tool, select **New Window** and then select **Protocol Viewer**.

If you are using the U4301A PCIe Gen3 Analyzer module, an instance of the Protocol Viewer window is automatically added to this module in the Overview tab of the Logic Analyzer application.

#### Upper pane of Protocol Viewer

The upper pane of Protocol Viewer provides a summarized listing of the captured packets. To know more about how to use the upper pane of Protocol Viewer, refer to the topic "Viewing the Packet Summary" on page 319.

#### Lower pane of Protocol Viewer

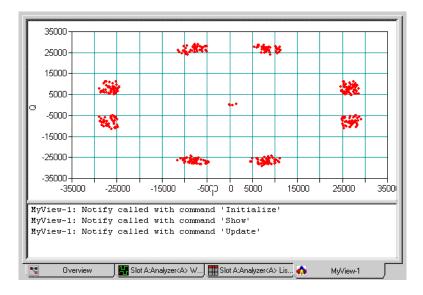
The lower pane displays the details of a packet that you selected in the upper pane. The packet details are organized in the following tabs.

| Details                      | This tab displays the details of a selected packet. You can also compare<br>the details of a packet with another packet's details. To know how to use<br>this tab, refer to the topic "To view and compare packet details" on<br>page 329.   |
|------------------------------|--|
| Header                       | This tab displays the header information for a selected packet. To know how to use this tab, refer to the topic "To view a packet header" on page 332.   |
| Payload                      | This tab displays the payload information for a selected packet. To know how to use this tab, refer to the topic "To view a packet payload" on page 333.   |
| Lanes                        | This tab displays a vertical listing of a selected packet's data with respect to the logical lanes. To know how to use this tab, refer to the topic "To view a packet's lanes" on page 334.  |
| Traffic Overview             | This tab provides an overview of the protocol traffic that is displayed in<br>the upper pane of Protocol Viewer. You can use this tab to get a count of<br>captured packets categorized on the basis of packet types.<br>To know how to use this tab, refer to the topic <b>Viewing the captured</b><br><b>PCIe Traffic statistics</b> in U4301A PCIe Gen3 Analyzer module online<br>help.   |
| LTSSM Overview               | This tab displays a sequential list of the LTSSM states and their<br>transitions and the packets exchanged during each state. You can use<br>the information displayed in this tab to in verify the link training process<br>and find out reasons for any failure in this process.<br>To know how to use this tab, refer to the topic <b>Viewing LTSSM States</b><br><b>and Transitions</b> in the U4301A PCIe Gen3 Analyzer module online help. |
| Transaction Decode           | This tab allows you to compute and view transactions decoded from the captured PCIe traffic. This is a licensed feature.<br>To know how to use this tab, refer to the topic <b>Viewing Decoded</b><br><b>Transactions</b> in the <i>U4301A PCIe Gen3 Analyzer module online help</i> .   |
| PCIe Performance<br>Overview | This tab allows you to perform post processing on the captured PCIe traffic and generate an offline performance summary of bus utilization. This is a licensed feature.<br>To know how to use this tab, refer to the topic <b>Viewing Offline</b><br><b>Performance Summary</b> in the U4301A PCIe Gen3 Analyzer module online help.   |

#### NOTE

You can export the captured packet information to a specified .csv file using Protocol Viewer. You can either export all the data captured and displayed in Protocol Viewer or a specified time/marker based range of data. You do this using the set toolbar button in the Protocol Viewer window.

## **VbaView Window**



The VbaView window works with the integrated Microsoft Visual Basic for Applications (VBA) to provide custom data visualization charts.

The VbaView window is accessed through the menu bar's **Window>VbaView** command. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

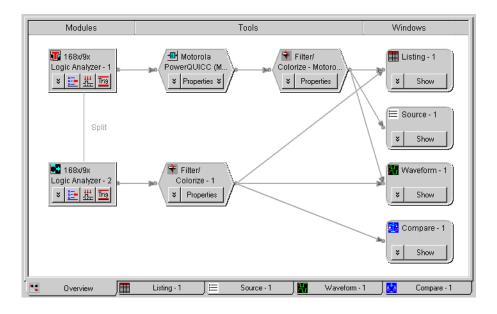
The VbaView window has two panes: the top pane displays the chart, and the bottom pane displays text output.

See Also

• Extending Data Visualization/Analysis with VBA (see page 357)

• "Displaying Data in VbaView Windows" (in the online help)

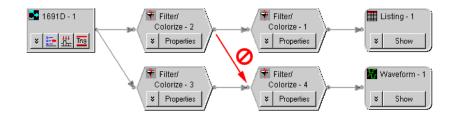
# **Overview Window**



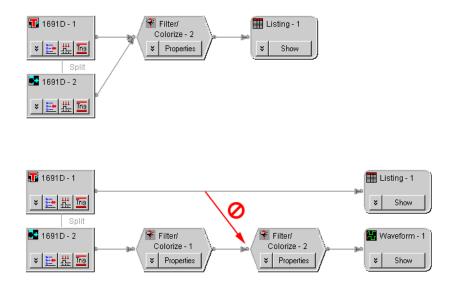
The Overview window lets you specify how the data is sent from the logic analyzer data acquisition module to post-processing tools and display windows.

The Overview window is accessed through the menu bar's **Window>Overview** command. If you have Tabbed Windows (see page 353) turned on, you can also select a tab at the bottom of the window.

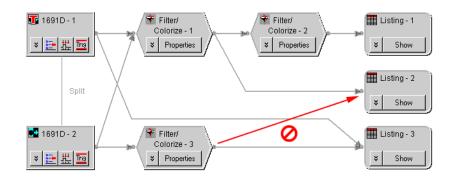
- **Connection Rules** There are a few rules that govern how you are able to add/connect tools and display data.
  - Rule 1: Fan out to tools only occurs directly after modules.



• Rule 2: Fan in to tools occurs only directly after modules.



• Rule 3: Display windows cannot show two versions of the same bus/signal.



Not allowed because "1691D - 2" buses/signals already in data from "Filter/Colorize - 1".

- See Also Analyzing the Same Data in Different Ways (Using the Overview Window) (see page 345)
  - To open or display the Overview window (see page 345)
  - To add, duplicate, or delete windows and tools (see page 346)
    - To add new windows (see page 346)
    - To delete windows (see page 346)
    - To add new tools (see page 347)
    - To delete tools (see page 347)
    - To duplicate windows (see page 347)
    - To delete connections (see page 348)

- To add connections (see page 348)
- To edit window or tool properties (see page 348)
- To rename windows, tools, and modules (see page 349)
- To redraw the Overview window (see page 350)
- To delete the Overview window (see page 350)

# Dialogs

- Advanced Clocking Setup Dialog (see page 495)
- Advanced Trigger Dialog (see page 496)
- Agilent Logic Analyzer Upgrade Dialog (see page 497)
- Analyzer Setup Dialog (see page 498)
- Chat Dialog (see page 501)
- Chat Select Destination Dialog (see page 502)
- Choose a Protocol Family and Bus Dialog (see page 502)
- Create a New Configuration Dialog (see page 503)
- E-mail Dialog (see page 504)
- Event Editor Dialog (see page 505)
- Eye Finder Advanced Options Dialog (see page 555)
- Eye Finder Properties Dialog (see page 557)
- Export Dialog (see page 506)
- Export File Selection Dialog (see page 507)
- External Application Setup Dialog (see page 508)
- External Trigger Dialog (see page 510)
- Find Dialog (see page 511)
- Frame/Module Information Dialog (see page 513)
- "General Purpose Probe Set Dialog" (in the online help)
- Import Dialog (see page 514)
- Import Setup Dialog (see page 515)
- Module Mapping Dialog (see page 517)
- Module Skew and System Trigger Dialog (see page 520)
- Netlist Import Dialog (see page 520)
- Offline Startup Options Dialog (see page 521)
- Options Dialog (see page 522)
- Pod Assignment Dialog (see page 524)
- Printing Data Dialog (see page 525)
- Properties Dialog (see page 526)
- Range Properties Dialog (see page 526)
- Recall Trigger Dialog (see page 527)
- Run Properties Dialog (see page 529)
- Select Symbol Dialog (see page 530)

- Select System to Use Dialog (see page 531)
- Software Licensing Dialog (see page 534)
- Source Viewer Properties Dialog (see page 538)
- Specify Mapping Dialog (see page 540)
- Split Analyzer Setup Dialog (see page 541)
- Status Dialog (see page 542)
- Symbols Dialog (see page 545)
- System Summary Dialog (see page 546)
- Target Control Port Dialog (see page 549)
- Thresholds and Sample Positions Dialog (see page 550)
- TimingZoom Setup Dialog (see page 558)

### Advanced Clocking Setup Dialog

The Advanced Clocking Setup dialog lets you specify more complex clock setups than you can with the normal Master or Slave selections. If you want to use a specific clock channel both as an edge and a qualifier in the same clock description, you need to use advanced clocking.

| Advanced Clocking Setup<br>Clock spec: [(Clk11) AND (Clk3=0)] OR [(Clk34) AND | (Clk1=1)) | X   |
|---|-----------|---|
| Edges<br>Clk1 <b>F v</b> Or Clk2 <b>X v</b>                                   | (         | Clk3 2 0r Clk4 X 3                        |
| AND   | OR        | AND                                       |
| Qualifiers<br>Q1 Clk3 Low  And Q2 Off   |           | Qualifiers<br>Q3 Clk1 High V And Q4 Off V |
|   |           | OK Cancel Help                            |

| Clock spec: | A textual description of the clocking setup.  |
|-------------|---|
| Edges       | Lets you choose from <b>Don't Care</b> , <b>Rising Edge</b> , <b>Falling Edge</b> , or <b>Both</b><br><b>Edges</b> for each of the available clock inputs.              |
| Qualifiers  | Lets you turn <b>Off</b> clock qualifiers or select <b>Low</b> or <b>High</b> levels from the available clock inputs for each of the clock qualifier resources (Q1-Q4). |
| And/Or      | Lets you toggle the boolean operators for the clock qualifiers.   |

#### See Also

- To set up advanced clocking (see page 129)
- Pod and Channel Naming Conventions (see page 418)

# **Advanced Trigger Dialog**

The Advanced Trigger dialog lets you set up complex trigger specifications that cannot be set up with simple triggers (for example, you can trigger on a sequence of events in the device under test).

| ta an    | lvanced Trigger               |   | _ 🗆 × |
|----------|-------------------------------|---|-------|
| т        | rigger Functions              | Trigger Sequence  |       |
| Patterns | Pattern n<br>times            | Default Storage (overridden by sequence level store actions):                                 |       |
| other    |                               | Step 1 💙 Pattern n times  |       |
| ð        |                               | Find 1 I occurrence of  |       |
| loed     | N consecutive<br>samples with | ▼     Bus/Signal     My Bus 1     ▼     All bits     ▼     =     ▼     XX     ■     Hex     ▼ |       |
| Advanced | Pattern1                      | Then 👻 Trigger and fill memory  |       |
|          |                               | 👻 with 🞽 Default Storage 💌  |       |
|          | Pattern1 💌                    |   |       |
|          |                               | Simple Trigger Store Recall Clear OK Cancel   | Help  |

| Trigger Functions | Trigger functions are pre-defined trigger setups for common<br>measurements. Trigger functions are drag-and-dropped into the Trigger<br>Sequence area in the desired order; then, you fill-in the fields that<br>specify the <i>events</i> to look for in the sampled data and the <i>actions</i> to take<br>when the events are found. |
|-------------------|---|
| Trigger Sequence  | The trigger sequence describes the steps to take when searching for a sequence of events that will trigger the logic analyzer.<br><i>Default storage</i> specifies which samples to store unless there are overriding <i>storage control</i> actions within the trigger sequence steps.   |
| Simple Trigger    | Opens an information dialog that explains how to specify simple triggers (see page 156).  |
| Store             | Opens the Store Trigger dialog for saving a trigger sequence setup as a favorite or saving it to a file.  |
| Recall            | Opens the Recall Trigger dialog (see page 527) for recalling favorite, recently used, and stored trigger sequence setups.   |
| Clear             | Clears the current trigger sequence and sets up a default trigger sequence.   |

#### See Also

- Specifying Advanced Triggers (see page 163)
  - Trigger Functions (see page 560)
  - Specifying Simple Triggers (see page 156)
  - Storing and Recalling Triggers (see page 201)

# **Agilent Logic Analyzer Upgrade Dialog**

#### NOTE

When installing licensed hardware upgrades, you must run the *Hardware Update Utility* program on the frame that contains the cards you want to upgrade. In other words:

- In a multiframe logic analysis system, you must run the *Hardware Update Utility* program on each frame that has cards to be upgraded.
- You cannot install module upgrades over a remote connection (including remote connections via Remote Desktop, NetOp, or RealVNC).

Determine if a Logic Analyzer is 🎘 Agilent Logic Analyzer Upgrade **Upgradeable Tab** Determine if a Logic Analyzer is Upgradeable Install a Logic Analyzer Upgrade - For some logic analyzers, state speed or memory depth can be upgraded via software The table below shows which logic analyzers are upgradeable Note: If the module(s) that will be upgraded are in a frame that is connected to other 16900/902 frame(s), see Help - To order a state speed or memory depth upgrade, contact your Agilent sales representative or go to www.agilent.com/find/contactus for product purchase information. The following shows this system's upgrade status. If an upgrade license-file is present, the 'Yes' in the 'Upgradeable' column is replaced with the maximum state speed and/or memory depth of pending upgrades. To install a pending upgrade, select the "Install a Logic Analyzer Upgrade" tab and follow the instructions. Serial Number Current Depth Current State Speed Slot Card Type Upgradeable 256K Samples 256K Samples MY46000132 250 MHz State 16910A Master D Yes 16950A Master MY46000246 300 MHz (600 MHz Turbo) State Pending upgrade(s): 1Meg Samples Е 16Meg Samples 150 MHz (300 MHz Turbo) State No F 16720A Master Unknown < > Close Help

> This tab lists the logic analyzers and other cards in a frame and shows you whether they are upgradeable or if an upgrade is pending.

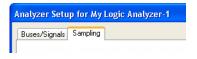
Install a Logic Analyzer Upgrade Tab

| Agil   | ent Logic Analyzer  | Upgrade                                     |   |   |                                 | X          |
|--------|---|---|---|---|---------------------------------|------------|
| Determ | nine if a Logic Analyzer is   | s Upgradeable Ir                            | nstall a Logic Analyz                         | er Upgrade  |                                 |            |
|        | o obtain a license file, fol<br>(The serial number(s) rec   |   |   | t Certificate you received with your<br>wn below.)                        | upgrade purchase.               |            |
|        |   |   |   | ns provided in the email to install the<br>ologies\Logic Analyzer\License | e license file on the logic ana | lyzer.     |
|        |   | in the 'Upgradeab                           |   | grade license file has been installe<br>n replaced with the maximum state |                                 |            |
|        | an upgrade is pending, o<br>a. Complete any acquis<br>(The logic analyzer<br>b. Select the row that h | itions and save da<br>will be taken offline | ta prior to doing an<br>e in order to perform | the upgrade.)   |                                 | Upgrade    |
| Slot   | t Card Type   | Serial Number                               | Current Depth                                 | Current State Speed   | Upgradeable                     |            |
| D      | 16910A Master   | MY46000132                                  | 256K Samples                                  | 250 MHz State   | Yes                             |            |
| F      | 16950A Master<br>16720A Master  | MY46000246<br>Unknown                       | 256K Samples<br>16Meg Samples                 | 300 MHz (600 MHz Turbo) State<br>150 MHz (300 MHz Turbo) State            |                                 | eg Samples |
|        |   |   |   |   |                                 |            |
|        |   |   |   |   |                                 |            |
|        |   |   |   |   |                                 |            |
|        |   |   |   |   | Close                           | Help       |
|        |   |   |   |   |                                 |            |

Upgrade... Performs the pending upgrade for the selected card.

See Also • Installing Licensed Hardware Upgrades (see page 147)

# **Analyzer Setup Dialog**



The Analyzer Setup dialog is accessed through the main menu's Setup>(Logic Analyzer Module)>Bus/Signal... or Setup>(Logic Analyzer Module)>Timing/State (Sampling)... commands.

The dialog consists of the following two tabs.

- **Buses/Signals** The Buses/Signals tab is used to map bus and signal names in the interface to the pod and channel connections of the probes. Also, you can set a pod threshold, and assign a default number base and polarity to the bus or signal. See Buses/Signals Tab (see page 499).
- **Sampling** The Sampling tab is used to name the analyzer, and select and configure the acquisition mode. In the timing acquisition mode, you set the channel width and sampling rate. In the state acquisition mode you configure the state clocks and qualifiers. See Sampling Tab (see page 500).

#### **Buses/Signals Tab**

The Buses/Signals tab is used to map (assign) bus and signal names in the interface to the pod and channel connections of the probes. You also use the Buses/Signal tab to set up thresholds, polarity, default number base, and enter user comments.

| Enter buses and signals and                                     | Pot                  | Pod 2 |             |          |   |   | Slot D Pod 1<br>Threshold: TTL |   |   |   |   |   |   | ~  | Display ¥ 🔍 ඁ<br>✓ Channels Assigned |   |           |          |             |          |     |                                  |
|---|----------------------|-------|-------------|----------|---|---|--------------------------------|---|---|---|---|---|---|----|--------------------------------------|---|-----------|----------|-------------|----------|-----|----------------------------------|
| Bus/Signal Name   | Channels<br>Assigned | Width | <u>old:</u> | TTL<br>‡ | 1 | 1 | 1                              | 1 | 1 | ‡ | 1 | 1 | 1 | 1  | 1                                    | 1 | Thre<br>‡ | esh<br>‡ | old:<br>  ‡ | TTL<br>‡ | · * | <u>W</u> idth<br>Balasite        |
|   | Ŭ                    |       | 7           | 6        | 5 | 4 | 3                              | 2 | 1 | 0 |   |   |   | 12 |                                      |   |           | 8        | 7           | 6        | -   | <u>P</u> olarity<br>Default Base |
| C My Bus 1  | Pod D1[7:0]          | 8     |             |          |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          | 1           | 1        |     | -                                |
| C My Bus 2  | Pod D1[9:8]          | 2     |             |          |   |   |                                |   |   |   |   |   |   |    |                                      |   | ~         | 1        |             |          |     | C <u>o</u> mment                 |
| — 💭 My Bus 3  | Pod D1[11:10         | 2     |             |          |   |   |                                |   |   |   |   |   |   |    | 1                                    | ~ |           |          |             |          | ~   | Threshold                        |
| My Signal 1   | Pod D1[12]           | 1     |             |          |   |   |                                |   |   |   |   |   |   | 1  |                                      |   |           |          |             |          |     | <br>Activity                     |
| My Signal 2   | Pod D1[13]           | 1     |             |          |   |   |                                |   |   |   |   |   | 1 |    |                                      |   |           |          |             |          |     | Channel Numbers                  |
| My Signal 3   | Pod D1[14]           | 1     |             |          |   |   |                                |   |   |   |   | 1 |   |    |                                      |   |           |          |             |          | Ļ   |                                  |
| 🖨 🚔 My Folder 1   |                      |       |             |          |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
| ——————————————————————————————————————                          | Pod D2[1:0],         | 3     |             |          |   |   |                                |   | √ | 1 | √ |   |   |    |                                      |   |           |          |             |          |     |                                  |
| My Signal 4   | Pod D2[2]            | 1     |             |          |   |   |                                | ~ |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
| 😑 🚔 My Folder 2   |                      |       |             |          |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
| ——————————————————————————————————————                          | Pod D2[5:3]          | 3     |             |          | 1 | 1 | 1                              |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
| My Signal 5   | Pod D2[6]            | 1     |             | 1        |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
|   |                      |       | <           |          |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |
| Add Bus/Signal) Delete Delete All Import Netlist System Summary |                      |       |             |          |   |   |                                |   |   |   |   |   |   |    |                                      |   |           |          |             |          |     |                                  |

The Buses/Signals tab is accessed through the menu bar's **Setup>(Logic Analyzer Module)>Bus/Signal...** command.

Through the **Display** button, you can select what bus/signal setup information is displayed.

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

**Read Only** The following fields are read only and cannot be edited. The display of these items can be turned on/off under the **Display** button.

| Width           | The Width column displays the number of assigned channels on each bus.  |
|-----------------|---|
| Activity        | <ul> <li>The Activity row displays the type of signal activity on each channel.</li> <li>Low bar = A stable low level.</li> <li>High bar = A stable high level.</li> <li>Transition arrows = An active signal transition between low and high.</li> </ul> |
| Channel Numbers | The Channel Numbers row displays pod channel numbers  |

| NOTE     | In previous versions of the <i>Agilent Logic Analyzer</i> application, the Buses/Signals setup tab had a <b>Define Probes</b> button; now, probes are defined differently (see "To define probes" (in the online help)).   |
|----------|--|
| NOTE     | If you enable the Advanced Probe settings for U4154A or 16962 logic analyzer, a button named <b>APS</b> is displayed in the Buses/Signals tab. You use this button to enable or disable the peaking for the probing system used for these logic analyzers. See "Changing Advanced Probe Settings for U4154A and 16962 Logic Analyzers" on page 681.  |
| See Also | <ul> <li>Defining Buses and Signals (see page 104)</li> <li>To add a new bus or signal (see page 105)</li> <li>To delete a bus or signal (see page 106)</li> <li>To rename a bus or signal (see page 107)</li> <li>To assign channels in the default bit order (see page 110)</li> <li>To assign channels, selecting the bit order (see page 111)</li> <li>To define buses and signals by importing netlist files (see page 113)</li> <li>To reorder bits by editing the Channels Assigned string (see page 114)</li> <li>To set the default number base (see page 116)</li> <li>To set polarity (see page 117)</li> <li>To add user comments (see page 117)</li> <li>To alias a bus/signal name (see page 118)</li> <li>To sort bus/signal names (see page 118)</li> <li>Pod and Channel Naming Conventions (see page 418)</li> <li>Why Are Pods Missing? (see page 635)</li> </ul> |
|          |  |
|          | Sampling Tab<br>The Sampling tab is access through the menu bar's Setup>(Logic Analyzer<br>Module)>Timing/State (Sampling) command. The Sampling setup tab is  |
|          | used to select and configure the sampling mode.  |

| nalyzer Setup for My Logic Analyzer-1  |   |
|--|---|
| Buses/Signals Sampling   |   |
| Acquisition          Acquisition         Timing - Asynchronous Sampling         State - Synchronous Sampling (500 Mb/s maximum clock rate)         Timing Options         Sampling Options:         Full channel. 500 MHz         Sampling Period:         2 ns         State Options - Specify when the logic analyzer should acquire samples         Sampling Options:         250 MHz         Clock Mode:   | Options       TimingZoom         Trigger Position: 50% poststore       Enable         Setup       Setup         Acquisition Depth:       IM         Thresholds and Sample Positions       Setup |
| Pod:         Pod A4         Pod A3         Pod A2         Pod A1           Clock:         Clk4         Clk3         Clk2         Clk1           Activity:         Image: | Clock Description   |
|  | OK Cancel Help  |

| Acquisition    | Lets you select the Timing or State acquisition mode (see Choosing the Sampling Mode (see page 119)).   |
|----------------|---|
| Timing Options | When the Timing acquisition mode is selected, you can specify its options (see Selecting the Timing Mode (Asynchronous Sampling) (see page 120)).   |
| State Options  | When the State acquisition mode is selected, you can specify its options (see Selecting the State Mode (Synchronous Sampling) (see page 122)).  |
| Options        | Lets you specify options that apply to both the Timing and State<br>acquisition modes (see To specify the trigger position (see page 134) and<br>To set acquisition memory depth (see page 135)). |
| TimingZoom     | Lets you turn the timing zoom feature on or off and specify its settings (see Using Timing Zoom (see page 136)).  |

## **See Also** • Choosing the Sampling Mode (see page 119)

• Logic Analyzer Notes (see page 635)

# **Chat Dialog**

The Chat dialog lets you enter and send messages to other logic analysis system users.

| Chat [w/ AGILENT\dvutest@MTX63] WHITE,PAT (A-ColSprings,ex1) [AGILENT\pw5670@mtx33]            |      |
|--|------|
| > When will the system be available?<br>SHEETS, JACK [AGILENT\dvutest@mtx63]<br>> At 12:00 pm. |      |
|  |      |
|  |      |
|  |      |
|  |      |
| Message to send:   |      |
| Thank you.   |      |
| Send Close Last message received:<br>Wed Mar 22, 2006 - 3:33:3                                 | 2 PM |

| Message to send | Lets you enter a message to send.       |
|-----------------|---|
| Send            | Sends the message.                      |
| Close           | Closes the dialog and the chat session. |

- **See Also** Select System to Use Dialog (see page 531)
  - Chat Select Destination Dialog (see page 502)

# **Chat Select Destination Dialog**

The Chat Select Destination dialog lets you select either the person logged into or the person connected to the logic analysis system.

| ₩ Chat  | X  |
|---|----|
| Select Destination                                  |    |
| Chat with person logged onto machine (mtx63):       |    |
| SHEETS, JACK, AGILENT\dvutest                       | ~  |
| • Chat with person using instrument:                |    |
| SHEETS, JACK, AGILENT\dvutest@mtx63.cos.agilent.com |    |
|   |    |
| OK Cancel   |    |
|   | .: |

Clicking **OK** opens the Chat dialog (see page 501) where you can enter and send your message.

See Also • Select System to Use Dialog (see page 531)

## **Choose a Protocol Family and Bus Dialog**

The Choose a Protocol Family and Bus dialog lets you select a protocol family and bus for the "Find a packet" trigger function.

| 🔆 Choose a Pr    | otocol Family and Bus   | X |
|------------------|---|---|
| Protocol Family: | PCI Express   | ~ |
| Bus:             | <none selected=""></none>   | ¥ |
| ок               | <none selected=""><br/>8B/10B Link - x1<br/>8B/10B Link - x16<br/>8B/10B Link - x2</none>   |   |
|                  | 88/108 Link - x4<br>88/108 Link - x8<br>PIPE 16-bit - x1<br>PIPE 16-bit - x16<br>PIPE 16-bit - x2<br>PIPE 16-bit - x4<br>PIPE 16-bit - x8<br>PIPE 8-bit - x1<br>PIPE 8-bit - x1<br>PIPE 8-bit - x4<br>PIPE 8-bit - x8 |   |

| Protocol Family | Lets you select the protocol family.                        |
|-----------------|---|
| Bus             | Lets you select the type of bus within the protocol family. |

- **See Also** Find a packet (see page 580) trigger function
  - To specify packet events (in "Find a packet" trigger function) (see page 175)

# **Create a New Configuration Dialog**

The Select Offline Hardware dialog appears when you are in *offline mode* and you choose the **File>New** command to create a new logic analyzer configuration file. This dialog lets you specify the type of logic analyzer hardware to model in the configuration file.

| Create a New Configurat  | ion                            | ×      |
|--|--------------------------------|--------|
| Since you are not currently connected to any logic analysis system,<br>you may select the type of logic analysis hardware that should be |                                | ОК     |
| used for a new offline sessi   | DN:                            | Cancel |
| Type of Card:  | 16910-16911 Logic Analyzer 🖉 💌 | Help   |
| Number of Cards in   | One Card Module 💌              |        |
| Starting Slot:   | Slot A                         |        |
|  |                                |        |

| Тур | Type of Card | Selects the type of logic analysis hardware to use in the new offline configuration file.   |
|-----|--------------|---|
|     |              | A Virtual Analyzer is a generic logic analyzer with no hardware options; it<br>is the type of logic analyzer that is used when fast binary format data<br>from 16700-series logic analyzers is imported for offline analysis. |

| Number of Cards in | Specifies the number of cards in the hardware module.                              |
|--------------------|--|
| 5                  | Selects the starting slot of the cards used in the new offline configuration file. |

**See Also** • Offline Analysis (see page 233)

• To set up multiple-modules with XML-format configurations (see page 224)

# **E-mail Dialog**

#### NOTE

E-mail must be set up on the computer running the *Agilent Logic Analyzer* application before this feature will work. Refer to the operating system online help or your mail application's online help for information on setting up e-mail. See also Setting Up Outlook Express on the Logic Analysis System (see page 505).

Some mail applications block e-mail that is sent by running programs, so test this feature with your mail application before you use it.

| E-mail                        | ×      |
|-------------------------------|--------|
| To: First_last@company.com    | ОК     |
| Subject: Logic analyzer event | Cancel |
| Here's the message body.      | Help   |

| То        | Address(es) to which e-mail will be sent. You can specify multiple recipients by separating each e-mail address with a semicolon (;). |  |
|-----------|---|--|
| Subject   | Subject of the e-mail.  |  |
| (message) | Text of the message.  |  |

#### See Also

- To specify a trigger sequence step's goto or trigger action (see page 178)
  - To create a new time interval measurement (see page 279)
  - To create a new sample interval measurement (see page 280)
  - To change a marker's position property (see page 275)
  - To run until a number of compare differences (see page 307)

### Setting Up Outlook Express on the Logic Analysis System

Outlook Express is installed on logic analyzers and logic analysis systems along with Internet Explorer and the Windows XP operating system. If you want to use the logic analysis system's "e-mail on" features (on trigger, on measured interval, on number of compare differences), you can use Outlook Express.

To set up Outlook Express on the logic analysis system:

- 1 Make Outlook Express the default e-mail program in Internet Explorer:
  - a In Internet Explorer, choose Tools>Internet Options....
  - **b** In the Internet Options dialog's Programs tab, for the **E-mail** service, select **Outlook Express**.
- **2** Get e-mail server and account information from your network or system administrator, and configure a mail account in Outlook Express:
  - a In Outlook Express, choose Tools>Accounts....
  - **b** In the Internet Accounts dialog's Mail tab, click Add>Mail....
  - **c** In the **Internet Connection Wizard**, follow the instructions, using the e-mail account information from your system or network administrator.
- **3** Make sure the Security tab settings are set correctly:
  - a In Outlook Express, choose Tools>Options....
  - **b** In the Options dialog's Security tab, uncheck **Warn me when other applications try to send mail as me**.
- 4 Send a test e-mail from Outlook Express.
- 5 Test one of the logic analysis system's "e-mail on" features.
- **See Also** E-mail Dialog (see page 504)

### **Event Editor Dialog**

The Event Editor dialog lets you specify packet events in the "Find a packet" trigger function.



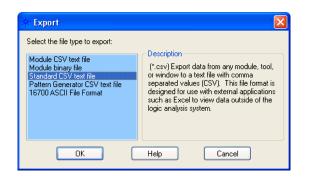
| Events             | Hierarchically lists protocol event types that you can select.  |
|--------------------|---|
| (Fields)           | (On the right side of the dialog). Lets you enter, select, or clear (💌) packet field values.  |
| Name               | Lets you enter or modify the name of the packet event.  |
| Add to Favorites   | Adds the packet event to the favorites list.  |
| Organize Favorites | Opens the Organize Favorites dialog for organizing the packet event favorites list (see To organize favorite packet events (see page 177)).                     |
| Clear              | Clears all packet field values.   |
| View as Bits       | Opens the View as Bits dialog for viewing the packet event in a format similar to specifications documents (see To view a packet event as bits (see page 176)). |

### **See Also** • Using the Packet Event Editor (see page 175)

- Find a packet (see page 580) trigger function
- To specify packet events (in "Find a packet" trigger function) (see page 175)
- To find packet patterns in the captured data (see page 298)
- "To specify packet patterns to filter" (in the online help)

## **Export Dialog**

The Export dialog lets you export certain kinds of data into the *Agilent Logic Analyzer* application.

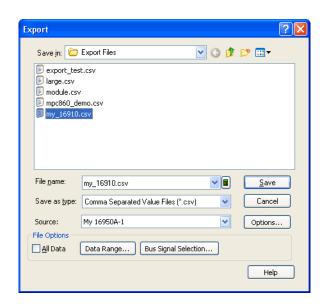


| Module CSV text file               | Lets you export module data only to a comma separated value (CSV) format text file. This file type is for post-processing tools and can be re-imported into the logic analysis system using a <i>data import module</i> (see "To export data to module CSV format files" on page 210).                                   |
|------------------------------------|--|
| Module binary file                 | Lets you export module data only to a binary format file (see "To export<br>data to module binary (ALB) format files" on page 213). Future releases<br>of the <i>Agilent Logic Analyzer</i> application will be able to import module<br>binary files into the logic analysis system using a <i>data import module</i> . |
| Standard CSV text file             | Lets you export data from modules, tools, or windows to a comma<br>separated value (CSV) format text file. This file type is for logic analyzer<br>data that will be imported and viewed in external applications like<br>Microsoft Excel (see "To export data to standard CSV format files" on<br>page 207).            |
| Pattern Generator<br>CSV text file | Lets you export pattern generator vector sequences to a comma<br>separated value (CSV) format file (see "Exporting Vector Sequences to<br>CSV Format Files" (in the online help)).   |
| 16700 ASCII File<br>Format         | Lets you export captured data to a text file that matches the output of<br>the 16700 logic analysis system's "Print to File" format (see "To export<br>data to 16700 ASCII format files" on page 215).   |

# **Export File Selection Dialog**

The Export file selection dialog lets you select the file to which data is exported, the data source, the export options, the range of data samples, and the buses/signals to export.

### 12 Reference



| File name               | Lets you select the file to which data is exported.  |
|-------------------------|--|
| Save as type            | The appropriate type is already selected, based on the file type selected in the previous Export dialog (see page 506).  |
| Source                  | Lets you select the data source. The list of sources you can select from is determined by the file type selected in the previous Export dialog (see page 506). |
| Options                 | Opens the File Export Options dialog where you can select the appropriate options for the file type selected in the previous Export dialog (see page 506).     |
| All Data                | When checked, data from all samples and all buses/signals is exported.   |
| Data Range              | When <b>All Data</b> is not checked, this button opens a Range Properties dialog for selecting the range of data samples to export.                            |
| Bus Signal<br>Selection | When <b>All Data</b> is not checked, this button opens a Range Properties dialog for selecting the buses/signals to be included in the export.                 |

#### See Also

- To export data to standard CSV format files (see page 207)
  - To export data to module CSV format files (see page 210)
  - To export data to module binary (ALB) format files (see page 213)
  - "Exporting Vector Sequences to CSV Format Files" (in the online help)

## **External Application Setup Dialog**

The External Application Setup dialog lets you add, edit, arrange, or remove items from the **Tools>External Applications>** menu.

| External Applicatio           | n setup                                   |      |                    |
|-------------------------------|---|------|--------------------|
| External Applications t       | o access from the Tools menu              |      |                    |
| Application Name              | Executable File Name                      |      | Add Application    |
| Notepad<br>Paint<br>My Script | notepad.exe<br>mspaint.exe<br>wscript.exe |      | Edit Application   |
|                               |   |      | Delete Application |
|                               |   |      | Move Up            |
|                               |   |      | Move Do <u>w</u> n |
| <u>o</u> k                    | Cancel                                    | Help | 1                  |

| Add Application    | Opens the Add Application dialog (see page 509) for specifying a new menu item's parameters.       |
|--------------------|--|
| Edit Application   | Opens the Edit Application dialog (see page 509) for changing the selected menu item's parameters. |
| Delete Application | Deletes the selected application from the menu item list.  |
| Move Up Move Down  | Moves the selected application up or down within the menu item list.                               |

## **External Application Add/Edit Dialog**

The Add/Edit Application dialog lets you enter or modify the parameters for an item in the **Tools>External Applications>** menu.

| Edit Application        |                          | X      |
|-------------------------|--------------------------|--------|
| Executable file         | wscript.exe              | Browse |
| Application name :      | My Script                |        |
| Command line :          | 5cripts\WSH\myScript.vbs |        |
| Application directory : | C:\WINDOWS\system32      |        |
| ОК                      | Lancel Test Run          | Help   |

| Executable file       | The name of the file to execute when the menu item is selected.             |
|-----------------------|---|
| Application name      | The name that appears on the menu item.                                     |
| Command line          | Command line options for the executable file.                               |
| Application directory | The directory that contains the executable file.                            |
| Test Run              | For quick testing, this executes the application with the given parameters. |

## **External Trigger Dialog**

There are **Trigger In** and **Trigger Out** BNC connectors located on the logic analysis system (rear panel of 16900-series, 16800-series, or 1680-series, front panel of 1690-series). These BNC connectors are used to connect the analyzer to an external instrument and either send or receive a trigger signal.

The External Trigger dialog is used for setting up triggers between the logic analyzer or logic analysis system and other, external instruments.

The 16900-series or 16800-series External Trigger dialog looks like:

| External Trigger                |                                 |                            |
|---------------------------------|---------------------------------|----------------------------|
| Frame : mtx33                   |                                 |                            |
| Threshold Level:                | TL (1.40 V)                     | V 🗐 — (+)                  |
| <ul> <li>Rising Edge</li> </ul> |                                 |                            |
| Trigger Out                     |                                 |                            |
| Output Status                   | Polarity                        | Mode                       |
| <ul> <li>Enabled</li> </ul>     | <ul> <li>Active High</li> </ul> | <ul> <li>Pulsed</li> </ul> |
| ◯ Disabled                      | O Active Low                    |                            |
|                                 | ause Trigger Out (This is the   | OR of all selected events) |
| When My 169104                  |                                 |                            |
| When My 169504                  |                                 |                            |
| When Flag 1 is se               |                                 |                            |
| When Flag 2 is se               |                                 |                            |
| When Flag 3 is se               |                                 |                            |
| When Flag 4 is se               | ł                               |                            |
| ОК                              | Cancel                          | Help                       |

The 1680/90-series External Trigger dialog looks like:

| External Trigger   |   |  |  |
|--|---|--|--|
| Trigger In<br>Threshold Level: LVTTL (1.40 V)<br>○ Falling Edge<br>ⓒ Rising Edge | Trigger Out<br>Threshold Level: LVTTL (1.40 V)<br>O Falling Edge<br>O Rising Edge |  |  |
| OK Cancel Help   |   |  |  |

**Trigger In** Lets you trigger the logic analyzer from another source. You can select whether a rising or falling edge indicates a trigger.

| Input Signal<br>Characteristic | 16900-Series               | 16800-Series          | 1680/1690-Series |
|--------------------------------|----------------------------|-----------------------|------------------|
| Input signal level:            | Selectable, ±5.5 V<br>Max. | Selectable, ±5 V Max. | TTL, 5.5 V Max.  |
| Minimum signal<br>amplitude:   | 500 mV                     | 200 mV                | 500 mV           |

Trigger Out Sends a signal to another device when the logic analyzer triggers. You can select whether the trigger will appear as a rising or falling edge.

> The trigger out signal is designed to drive a 50 Ohm load. It is recommended that for good signal quality, the trigger out signal be terminated in 50 Ohms to ground.

With a 16900-series logic analysis system frame or 16800-series logic analyzer, you can:

- Enable or disable (3-state high-impedance) the output.
- Choose the polarity of the output.
- Choose whether the output mode is **Pulsed** or **Feedthrough** (for observing flag settings).
- Select the events that will cause a trigger signal to be output.

| Output Signal<br>Characteristic | 16900-Series        | 16800-Series        | 1680/1690-Series    |
|---------------------------------|---------------------|---------------------|---------------------|
| VOH (output high<br>level):     | >2.0 V (3.3 V avg.) | >2.0 V (3.3 V avg.) | >2.0 V (3.3 V avg.) |
| VOL (output low<br>level):      | <0.5 V (0 V avg.)   | <0.5 V (0 V avg.)   | <0.5 V (0 V avg.)   |
| Pulse width:                    | Approx. 60-140 ns   | Approx. 80-160 ns   | Approx. 60-140 ns   |

See Also

• To trigger other instruments - trigger out (see page 198)

• To trigger analyzer from another instrument - trigger in (see page 199)

### **Find Dialog**

The Find dialog lets you search for patterns in captured data. You can qualify your search by specific bits, data patterns, equality, and range operators. The search result is placed at the center of the display.

## 12 Reference

| 🔆 Find  | X |
|---|---|
| Find 3 B-+ occurrences searching Forward V from Display Center  | ~ |
| Y       Bus/Signal       My Bus 1       All bits       =       03       Hex       And         Y       Bus/Signal       My Signal 1       X       Rising Edge       And       And         Y       Bus/Signal       My Signal 2       X       High       High |   |
| Store Favorite ¥ Recall Favorite ¥ Clear Options Find Close Help  |   |

| Find N occurrences | Specifies the number of occurrences to search for.  |
|--------------------|---|
| searching          | Specifies whether to search Forward or Backward.  |
| from               | Specifies the starting location (Display Center, Beginning Of Data, End Of Data, Trigger, or a marker).   |
| (pattern event)    | <ul> <li>Specifies the pattern event you wish to locate.</li> <li>In addition to the usual pattern matching operators (=, !=, &lt;, &gt;, &lt;=, &gt;=, In Range, and Not In Range), there are three additional operators you can use:</li> <li>Entering — the first sample of one or more consecutive samples that match the pattern. (By comparison, the "=" equals operator considers every sample that matches the pattern as an occurrence.)</li> <li>Exiting — the sample after one or more consecutive samples that match the pattern.</li> <li>Transitioning — entering or exiting one or more consecutive samples that match the pattern.</li> </ul>   |
| When               | A find qualifier (which further qualifies the find criteria with a time<br>duration or other operator):<br>Present<br>Not Present<br>Present> (time duration)<br>Present>= (time duration)<br>Present< (time duration)<br>Present< (time duration)<br>Present<= (time duration)<br>Present for Range (of time)<br>Not Present for Range (of time)<br>Entering<br>Exiting<br>The find qualifiers Present>, Present>=, Present<, Present<=,<br>Present for Range, and Not Present for Range let you specify a time<br>duration. This means the find event specified in the expression area will<br>be found based upon the given time and operator.<br>The other qualifiers (Present, Not Present, Entering, Exiting, and<br>Transitioning) do not allow a time duration. |
| Store Favorite     | Lets you store favorite find patterns.  |

| Recall Favorite | Lets you recall or delete favorite find patterns.                             |
|-----------------|---|
| Clear           | Clears the current find pattern.  |
| Options         | Opens the Find Options dialog that lets you specify "found" marker placement. |
| Find            | Performs the find without closing the Find dialog.                            |
| Close           | Closes the Find dialog.   |

See Also

- To quickly find bus signal patterns (see page 294)
  - To find bus/signal patterns in the captured data (see page 296)
  - To find packet patterns in the captured data (see page 298)
  - To find complex patterns in the captured data (see page 302)
  - To store, recall, or delete favorite find patterns (see page 303)
  - To specify "found" marker placement (see page 304)

## Frame/Module Information Dialog

The Frame/Module Information dialog displays detailed information about a logic analysis system *frame* (see page 789).

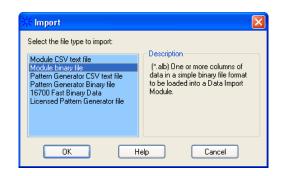
| Syste    | em Frame/Module Information 🛛 🔀                         |
|----------|---|
| System D | Details (mtx76):  |
| - 13     | Multi-Frame Set [Initialized = 3, Total = 3]            |
|          | 🕼 16902A Logic Analysis System - Master                 |
|          | 🗄 🔲 Frame Details                                       |
|          | 🗉 🚀 Module: 16760A Logic Analyzer                       |
| <u> </u> | 🕼 16900A Logic Analysis System - Slave                  |
|          | 🗈 📃 Frame Details                                       |
|          | 🗈 👷 Module: 16950A Logic Analyzer                       |
|          | 🖃 🚀 Module: 16950A Logic Analyzer                       |
|          | Number of Cards: 1                                      |
|          | Slot: D     Number of Channels: 68                      |
|          | Number of Pods: 4                                       |
|          | Max Acquisition Depth: 64 MB                            |
|          | Max Acquisition State Speed: 600 MHz                    |
|          | <ul> <li>Max Acquisition Timing Speed: 1 GHz</li> </ul> |
|          | 🖃 🔹 Upgrade Info  |
|          | 🖮 🔹 Slot D  |
|          | <ul> <li>Depth: Fully upgraded at 64 MB</li> </ul>      |
|          | <ul> <li>State Speed: Fixed at 600 MHz</li> </ul>       |
|          | <ul> <li>Timing Speed: Fixed at 1 GHz</li> </ul>        |
|          | Serial Number: US00000002                               |
|          | 🗄 🚀 Module: 16950A Logic Analyzer                       |
|          | 🕼 16900A Logic Analysis System - Slave                  |
|          | 🖶 🔲 Frame Details<br>🗉 💞 Module: 16754A Logic Analyzer  |
|          | Module: 16754A Logic Analyzer                           |
|          | Module: 10/54A Logic Analyzer                           |
|          | 🗄 💞 Module: 16754A Logic Analyzer                       |
|          | 🗄 🚀 Module: 16754A Logic Analyzer                       |
|          |   |
| 0        | K Help Set as Auto-Connect                              |

| System Details      | Displays the detailed information about the logic analysis system. This includes both information on the frame as a whole and information on each module.  |
|---------------------|--|
|                     | If the frame is participating in a multiframe set (as is the case in the example above), frame and module details on each frame is shown. In the example above, the in-use icon shows a user is currently using the multiframe set.  |
|                     | If module depth or speed is upgradeable (via hardware licensing),<br>module upgrade information is also provided.  |
|                     | Under the "Frame Details" category, you can find information about the frame's software version, host IP address, host name, whether or not the frame is password protected from remote-access, etc.   |
| Set as Auto-Connect | Selects the logic analysis system frame as the one to use when the <i>Agilent Logic Analyzer</i> application starts. The words "auto-connect" will show up next to the frame selected as an auto-connect in the Select System to Use dialog (see page 531). This button will change to "Clear Auto-Connect" if this frame is already set as an auto-connect. |
| Clear Auto-Connect  | When pressed, specifies that the logic analysis system frame not be automatically connected to when the <i>Agilent Logic Analyzer</i> application starts.  |

- **Notes:** When no auto-connect is established, the *Agilent Logic Analyzer* application attempts to go online with the local frame or starts offline if there is no local frame.
  - The auto-connect frame selection is stored on a per-user basis-so each logged on user can establish a different auto-connect frame.
  - If you are running the *Agilent Logic Analyzer* application on a standalone instrument or you are running the *Agilent Logic Analyzer* application on your PC with hosted instruments attached to your PC, the *Agilent Notification Center Icon* will be present on the taskbar (lower, right-hand corner of your desktop). This icon can be right-clicked to open an *instrument details* dialog showing the same type of information as the above dialog-but only for the local hardware.
- **See Also** To view logic analysis system details (see page 90)

### **Import Dialog**

The Import dialog lets you import certain kinds of data into the *Agilent* Logic Analyzer application.



| Module CSV text file               | Lets you import data from a CSV format text file into the logic analysis system using a <i>data import module</i> (see To create a data import module (see page 227)).                 |
|------------------------------------|--|
| Module binary file                 | Lets you import data from a module binary (ALB) format file into the logic analysis system using a <i>data import module</i> (see To create a data import module (see page 227)).      |
| Pattern Generator<br>CSV text file | Lets you import vectors of stimulus to a pattern generator module (see "<br>Importing Vector Sequences from CSV Format Files" (in the online<br>help)).                                |
| Pattern Generator<br>Binary file   | Lets you import setup information and a large number of stimulus<br>vectors to a pattern generator module (see "Importing PattGen Binary<br>(PGB) Format Files" (in the online help)). |
| 16700 Fast Binary<br>Data          | Lets you import fast binary data from the 16700-series logic analysis system (see To import 167xx fast binary data (see page 223)).  |
| Licensed Pattern<br>Generator file | Lets you import licensed pattern generator vectors.  |

### **Import Setup Dialog**

The Import Setup dialog is accessed through the menu bar's **Setup>(Data Import Module)>Bus/Signals...**.

The dialog consists of the following two tabs.

- **Buses/Signals** The Buses/Signals tab is used to edit bus and signal names in the data import module. Also, you can assign a default number base and polarity to the bus or signal. See Buses/Signals Tab (see page 516).
- File Information The File Information tab describes the contents of the file that has been imported. See File Information Tab (see page 517).

### **Buses/Signals Tab**

The Buses/Signals tab is used to edit bus and signal names in the data import module. You also use the Buses/Signal tab to set the polarity, set the default number base, and enter user comments.

| ter buses and signals ar<br>Bus/Signal Name | Chappele      | Width |    |    |    |    | N  | /ly B | us ( | 3  |    |    |    |    |          | _ |          |   |   |   |   |   |   |   | M | N |
|---|---------------|-------|----|----|----|----|----|-------|------|----|----|----|----|----|----------|---|----------|---|---|---|---|---|---|---|---|---|
|   |               |       | 21 | 20 | 19 | 18 | 17 | 16    | 15   | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 0 | 0 |
|   | My Bus 1[7:0  | 8     |    |    |    |    |    |       |      |    |    |    |    |    |          |   |          |   |   |   |   |   |   |   |   |   |
|   | My Bus 2[15:  | 16    |    |    |    |    |    |       |      |    |    |    |    |    |          |   |          |   |   |   |   |   |   |   |   |   |
| My Bus 3                                    | My Bus 3[31:  | 32    | 1  | √  | 1  | ~  | ~  | 1     | ∢    | 1  | ~  | <  | 1  | ~  | <b>√</b> | / | <b>√</b> | 1 | 1 | < | 1 | ~ | ✓ | ~ |   |   |
| My Signal 1                                 | My Signal 1[0 |       |    |    |    |    |    |       |      |    |    |    |    |    |          |   |          |   |   |   |   |   |   |   | 1 |   |
| My Signal 2                                 | My Signal 2[0 | 1     |    |    |    |    |    |       |      |    |    |    |    |    |          |   |          |   |   |   |   |   |   |   |   | 4 |
|   |               |       | <  |    |    |    |    |       |      |    |    |    |    |    |          |   |          |   |   |   |   |   |   |   |   |   |

The Buses/Signals tab is accessed through the menu bar's **Setup>(Data Import Module)>Bus/Signals...** command.

Through the **Display** button, you can select what bus/signal setup information is displayed.

The bus and signal icons in the **Bus/Signal Name** column are normally red, but they turn gray if the bus/signal is locked by an inverse assembler.

Read OnlyThe following fields are read only and cannot be edited. The display of<br/>these items can be turned on/off under the Display button.

| Width           | The Width column displays the number of assigned channels on each bus.  |
|-----------------|---|
| Activity        | <ul> <li>The Activity row displays the type of signal activity on each channel.</li> <li>Low bar = A stable low level.</li> <li>High bar = A stable high level.</li> <li>Transition arrows = An active signal transition between low and high.</li> </ul> |
| Channel Numbers | The Channel Numbers row displays pod channel numbers  |

- See Also To edit data import module bus/signal definitions (see page 229)
  - Using Data Import Modules (see page 227)

### **File Information Tab**

The File Information tab describes the contents of the file that has been imported.

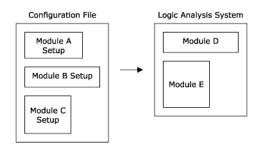
| ort Setup for My Dat   | a Import-1       |                    |  |  |
|--|------------------|--------------------|--|--|
| uses/Signals File Informati  | on               |                    |  |  |
|  | and Sattings\pu  | 5670\Mu Docume     | ents\Agilent Technologies\Logic Analyzer\Config Files\my_16910.csv                 |  |
| ile name. C. volocumenta   | and Settings (pe | Joor of any Docume |  |  |
| File   |                  |                    | Time/Trigger   |  |
| Description = Text [.csv]<br>Time file was imported = 1<br>Value separator = "."<br>Fill in value = Zeros<br>Number of rows = 104857 | 2/05/2005 03:4   |                    | Sampling period = 2 ns<br>Trigger row = 524288<br>Trigger correlation offset = 0 s |  |
| Column Name  | Width            | Туре               | Format   |  |
| Sample Number  |                  | Sample Number      | Signed Decimal   |  |
| My Bus 1   | 8                | Value              | Hex  |  |
| My Bus 2   | 16               | Value              | Hex  |  |
| My Bus 3   | 32               | Value              | Hex  |  |
| My Signal 1  | 1                | Value              | Hex  |  |
| My Signal 2  | 1                | Value              | Hex  |  |
| Time   |                  | Time Absolute      | Float Exponent=-12 Scale Factor=1.000000e+000                                      |  |
|  |                  |                    |  |  |
|  |                  |                    |  |  |

The File Information tab is accessed through the menu bar's **Setup>(Data Import Module)>File Info...** command.

- **See Also** To view data import module file information (see page 231)
  - Using Data Import Modules (see page 227)

## **Module Mapping Dialog**

The Module Mapping dialog helps you map module setup information from the configuration file you are opening to the modules in the logic analysis system you are using.



If you are opening an ALA format configuration file, modules must be compatible in order to setup a module with information from the configuration file. If you are opening an XML format configuration file, you can use setup information from any module; however, because of module differences, some settings may not transfer.

|   | _ |
|---|---|
| Module Mapping  | × |
|   |   |
| Specify how to load the specified configuration file into this        |   |
|   |   |
| C Manually specify module mapping. Specify Mapping                    |   |
| $\bigcirc$ Switch to "Offline" mode and load the configuration as-is. |   |
| Cancel Help   |   |

| Best-fit algorithm<br>(see page 518) | Automatically maps configuration file modules into the current frame.  |
|--------------------------------------|--|
| Manually map                         | The <b>Specify Mapping</b> button opens the Specify Mapping dialog (see page 540) to specify how configuration file modules should be mapped into the current frame. |
| Offline mode                         | Loads the configuration file as-is in the <i>offline mode</i> .  |

**See Also** • To transfer module setups to/from multi-module systems (see page 224)

### **Best-Fit Algorithm for Automatic Module Mapping**

The best-fit algorithms differ slightly, depending on whether you're loading XML or ALA format configuration files.

When Loading For any given module in the configuration file:

- XML Format 1 Is the module split?
  - Files: 2 Look for a module in the Overview window with the same name. If one is found, load the configuration into that module.

|                                      | <b>3</b> Look for the first module (based on the top to bottom order as shown in the Overview window) of the same <i>specific</i> type as the configuration file module. If one is found, load the configuration into that module. |
|--------------------------------------|--|
|                                      | In this case, "specific" means, for example, a 16750/1/2A/B logic analyzer vs. a 16753/4/5/6A logic analyzer.  |
|                                      | <b>4</b> Look for the first module of the same <i>general</i> type as the configuration file module.   |
|                                      | In this case, "general" means, for example, "logic analyzer" vs. "pattern generator").   |
|                                      | 5 If not found with any of the above, then:  |
|                                      | a In online (either Local or Remote) mode, don't load the module.  |
|                                      | <b>b</b> In offline mode, <i>create</i> the module.  |
| When Loading                         | For any given module in the configuration file:  |
| ALA Format<br>Configuration<br>Files | 1 Look for the first module (based on the top to bottom order as shown<br>in the Overview window) of the same <i>specific</i> type as the configuration<br>file module. If one is found, load the configuration into that module.  |
|                                      | In this case, "specific" means, for example, a 16750/1/2A/B logic analyzer vs. a 16753/4/5/6A logic analyzer.  |
|                                      | 2 If not found, skip it.   |
| NOTE                                 | In offline mode:   |
|                                      | When loading an ALA format configuration file, there is <i>always</i> a "clear" performed in the Overview window. Therefore, no matching algorithm is needed.  |
|                                      | When loading an XML format configuration file, the XML best-fit algorithm is used.   |

**See Also** • Module Mapping Dialog (see page 517)

| Module Name | Location | System Trigger | Skew Time |       |
|-------------|----------|----------------|-----------|-------|
| My 16910A-1 | A        | ۰              | 0 s       | - +   |
| My 16950A-1 | В        | C              | 0 s       | ■ - + |
| My 16750B-1 | с        | 0              | 0 s       | ■ - + |
| My 16740A-1 |          | O              | 0 s       | - +   |
|             |          |                |           |       |
|             |          |                |           |       |

# Module Skew and System Trigger Dialog

This dialog is available when there are multiple *module* (see page 790)s in a logic analyzer or logic analysis system. It lets you:

- Specify which module is the *system trigger* (that is, which module's trigger reference point is *Time=0*).
- Specify the trigger reference point skew for modules that are not the *system trigger*.

When **First module to trigger designates the System Trigger** is checked, the first module to trigger after the next run is selected as the *system trigger*. Unchecking this option and checking it again causes the module that has currently triggered first to become the selected *system trigger*.

Disabled modules are grayed out.

- See Also Setting the System Trigger and Skew Between Modules (see page 351)
  - To disable and enable modules (see page 98)

### **Netlist Import Dialog**

The Netlist Import dialog lets you set up bus/signal names and assign them to logic analyzer channels by importing netlist files. Netlist files come from the Electronic Design Automation (EDA) tools used to design the device under test, and they contain information about the signals on the connectors built into the device under test for the logic analyzer probes.

### NOTE

Before you can import bus/signal names from netlist files and assign them to logic analyzer channels, you must use the Define Probes dialog to identify the probes that are used with the logic analyzer.

| Netlist Impo  | ort     |                     |                    |    | ×      |
|---------------|---------|---------------------|--------------------|----|--------|
| Netlist File: | C:\My D | ocuments\netlist.tx | t                  |    | Browse |
| OK            | <       | Cancel              | Trim Buses/Signals | Не | lp     |

| Netlist File       | Lets you enter or browse for the name of the netlist file to import.  |
|--------------------|---|
| Trim Buses/Signals | Opens the Trim Bus/Signal Names dialog which lets you trim the bus/signal names imported from the netlist file. |

| <b>See Also</b> • To define buses and signals by importing netlist files (see page 1 | See Also | • ′ | To de | fine | buses | and | signals | by | importing | netlist | files | (see | page | 113 | ) |
|--|----------|-----|-------|------|-------|-----|---------|----|-----------|---------|-------|------|------|-----|---|
|--|----------|-----|-------|------|-------|-----|---------|----|-----------|---------|-------|------|------|-----|---|

## **Offline Startup Options Dialog**

The Offline Startup Options dialog appears when you start the *Agilent Logic Analyzer* application and it wants to start in the *offline mode* (see page 233) (if this is unexpected, see If starting in offline mode is unexpected (see page 373)). This dialog presents options for the tasks you can perform in the offline mode.

| 🔅 Offline Startup Options 🛛 🛛 🔀  |                                   |  |  |  |  |
|--|-----------------------------------|--|--|--|--|
|  |                                   |  |  |  |  |
| You have started the application in offline mode. If this is<br>"Help" for some troubleshooting ideas. | not what you expected, select     |  |  |  |  |
| There are several features available in offline mode. Sele   | ct one from the list below.       |  |  |  |  |
| <u>Go Online</u> ····> Connect to local or remote  | hardware to work online.          |  |  |  |  |
| pen File Open a configuration file to  | analyze previously acquired data. |  |  |  |  |
| Import Import data acquired from a   | an external source for analysis.  |  |  |  |  |
| Continue Offline ····> Create a new offline setup.   |                                   |  |  |  |  |
| Help   |                                   |  |  |  |  |

| Go Online        | Opens the Select System to Use dialog (see page 531) for choosing a frame to connect the <i>Agilent Logic Analyzer</i> application to. |
|------------------|--|
| Open File        | Lets you open a logic analyzer configuration file (see page 220).  |
| Import           | Opens the Import dialog (see page 514) for importing data from an external source into the logic analysis system.                      |
| Continue Offline | Opens the Create a New Configuration dialog (see page 503) for creating a new logic analyzer configuration file.                       |

**See Also** • If starting in offline mode is unexpected (see page 373)

## **Options Dialog**

To change your system options, select **Edit>Options...** from the menu bar. System options are written in the Windows registry file and persist across sessions.

- System Options (see page 522)
- Bus/Signal Naming Options (see page 523)
- Advanced Settings Options (see page 523)
- Message Dialogs/Event Logging Options (see page 524)

| Options   |  |  | ×                    |
|---|--|--|----------------------|
| System Trigger History Depth: Recent File List Entries: Repetitive Run Delay (sec):   | 10 <b>B</b> -+<br>4 <b>B</b> -+<br>0 <b>B</b> -+ | <ul> <li>Start Maximized</li> <li>Create Demo Data when offline</li> <li>Go to Trigger on Run</li> <li>Enable Numeric Grouping</li> <li>Default Folders</li> </ul> | OK<br>Cancel<br>Help |
| Bus/Signal Naming<br>Short<br>Unique  | Advanced Settings                                | d Probe Settings (APS)   |                      |
| Message Dialogs/Event Logging     Show Information Dialogs     Show Warning Dialogs     Show Error Dialogs     Event Logging Show | w Level 0  | - + and Below  |                      |

### **System Options**

| Trigger History Depth       | You can keep as many as 50 of the most recently used triggers. See To<br>store a trigger (see page 201) for more information on re-using triggers.<br>Trigger history is saved in the configuration files. The default is 10. |
|-----------------------------|---|
| Recent File List<br>Entries | This sets how many recently-loaded configuration files are shown in the <b>File</b> menu. The default is 4.   |
| Repetitive Run Delay        | Delay between repetitive measurements allows you to look at the captured data and decide whether to stop the measurement before the next run occurs.  |
| Start Maximized             | Specifies whether the <i>Agilent Logic Analyzer</i> application's main window is maximized when the application is started.   |

| Create Demo Data<br>when offline | When you run the analyzer, fake data will be created. This mode is useful<br>when learning how to use the logic analyzer software.<br><b>NOTE:</b> The logic analyzer does not trigger with fake data. You can set the<br>triggers, but will not get the same results you would with a real<br>acquisition. |
|----------------------------------|---|
| Go to Trigger on Run             | Specifies, when a logic analyzer measurement is run, whether display windows are automatically positioned around the data that triggered the analyzer.  |
| Enable Numeric<br>Grouping       | Numeric grouping adds spaces between every four hexadecimal and<br>binary digits, spaces between every three octal digits, and commas<br>between every three decimal digits (for example, FFFF FFFF, 1111 1111,<br>777 777, and 999,999).   |
| Default Folders                  | Opens the Default Folders dialog for specifying the default folder locations for configuration files, export files, and import files.   |

Bus/SignalWhen you have defined the same bus/signal name in more than oneNaming Optionmodule:

| Short  | Bus/signal names are shown without the module name even if they are<br>the same. In other words, it is possible to display two buses called<br>"ADDR" that are not the same physical bus. (You can still see the<br>module name in a tool tip by hovering over the bus/signal name.) |
|--------|--|
| Unique | Module names are pre-pended to identical bus/signal names, for example, "Module 1:ADDR" and "Module 2:ADDR".   |

| A        | dvanced |
|----------|---------|
| Settings | Options |

| Enable Advanced      | The Advanced Probe Settings are supported on U4154A and 16962 logic  |
|----------------------|--|
| Probe Settings (ASP) | analyzers and PCIe Gen3 analyzer.  |
|                      | Checking this option enables:  |
|                      | <ul> <li>the Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog. The<br/>probe setup tab is used to adjust the analyzer's equalizing snoop<br/>probe (ESP) settings. See "Adjusting the Equalizing Snoop Probe<br/>(ESP) Settings" (in the online help).</li> </ul>  |
|                      | <ul> <li>the APS button in the Buses/Signals tab of the U4154A / 16962 logic<br/>analyzer's Setup dialog. The APS button is used to change the<br/>settings for the probes used with the U4154A / 16962 logic analyzers.<br/>Probe settings include enabling peaking for the channels of these<br/>logic analyzers to compensate for the additional high frequency<br/>attenuation that some probing solutions provide on target signals.<br/>See"Changing Advanced Probe Settings for U4154A and 16962 Logic<br/>Analyzers" on page 681.</li> </ul> |

Message<br/>Dialogs/EventAs with any other program, the Agilent Logic Analyzer application<br/>generates messages about events. You can choose which messages are<br/>displayed. Check the appropriate box to indicate you wish the dialogs<br/>displayed.

| Show Information<br>Dialogs | Information dialogs offer tips such as the location of Simple Trigger, and do not indicate a failure.   |
|-----------------------------|---|
| Show Warning<br>Dialogs     | Warning dialogs occur when some setting may affect your data, such as being offline.  |
| Show Error Dialogs          | Error dialogs occur when an operation cannot be completed as specified.   |
| Event Logging               | You can choose to have all events recorded in a log file. Event logging<br>will slow down your logic analyzer. Event logs can be viewed through<br><b>Help&gt;Status Log</b> . Set the event logging level according to the directions<br>of your Agilent Technologies support person. Be sure to turn off event<br>logging when resuming normal use. |

## **Pod Assignment Dialog**

The Pod Assignment dialog lets you reserve a pod (see page 791) or pod pair (see page 791) for time tag storage. When a logic analyzer *module* (see page 790) has been split into two modules, you can also use this dialog to re-assign pods or pod pairs.

If you choose the highest acquisition memory depth (see page 135) and there is a pod pair that has no buses or signals assigned to it, that pod pair is automatically reserved for time tag storage, and there is no need to use this dialog.

| 📲 Pod Assignmen |  | ×           |
|-----------------|--|-------------|
|                 |  |             |
| Pod A1/Pod A2   | 1691D - 1                                    | Master Pods |
| Pod A3/Pod A4   | 1691D - 2                                    | Master Pods |
| Pod A5/Pod A6   | Reserved for timetag storage for 1691D - 1 💌 |             |
|                 |  |             |
|                 |  |             |
|                 |  |             |
|                 |  |             |
|                 |  |             |
|                 |  |             |
|                 | OK Cancel                                    | Help        |

| Pod/Pod Pair       | Indicates the pod or pod pair to be assigned or reserved.   |
|--------------------|---|
| (Module Selection) | For each pod or pod pair, selects the module to which it is assigned or reserves it for time tag storage. |
| Master Pods        | Indicates that the pod or pod pair is on the master card.   |

### See Also

• Split Analyzer Setup Dialog (see page 541)

- Memory Depth and Channel Count Trade-offs (see page 420)
- Pod and Channel Naming Conventions (see page 418)

## **Printing Data Dialog**

After choosing **File>Print...**, this dialog lets you print the current measurement data from a display window.

| ain          | ?   |
|--------------|---|
| Printer      |   |
| Name:        | Acrobat Distiller   Properties                    |
| Status:      | Ready Preview                                     |
| Type:        | AdobePS Acrobat Distiller                         |
| Where:       | C:\Documents and Settings\All Users\Desktop\*.pdf |
| Comment      | : 🔽 Print to file                                 |
| Print What   | t   |
| Listing - :  | 1   |
| Option       | 5   |
| Scaling      | Copies  |
| Number of    | f Pages: Number of copies: 1 👘                    |
|              |   |
|              |   |
| -Print range |   |
| -Print range |   |
| -            | · · · · · · · · · · · · · · · · · · ·             |
| C All        | from -8.692 us 1 to: 10.568 us Cancel             |

### NOTE

The first time you access the print dialog, you are asked to install a printer. Follow the directions in the printer install dialogs that appear.

| Printer    | Lets you select the printer, change its properties, and preview the print out.   |
|------------|--|
| Print What | Lets you select which display window to print from and specify printing options. |
| Scaling    | Lets you specify the number of pages to print per sheet.                         |

### 12 Reference

| Copies      | Lets you specify the number of copies to print.   |
|-------------|---|
| Print range | You can print All data, or print just a defined range between times,<br>sample numbers, or marker locations. Data is printed from the smallest<br>time/sample to the largest. |

### **See Also** • Printing Captured Data (see page 354)

- To install a printer (see page 355)
- To connect a LAN (see page 355)

## **Properties Dialog**

| Waveform Properties  |   |  |
|--|---|--|
| Window Properties Row Properties Marker Properties                     |   |  |
| Background<br>Font Size 9 1 - +<br>Overlay<br>Show Activity Indicators | Tool Tips<br>✓ Show Values<br>Transition Width<br>Markers<br>✓ Snap to Edge<br>Move Edge on Screen<br>✓ Place on Edge |  |
| OK Cance   | I Apply Help  |  |

The Properties dialog is accessed through the menu bar's **Window>Properties...** Use it to set up how the window and the displayed data appear.

- Changing Waveform Window Properties (see page 249)
- Changing Listing Window Properties (see page 263)
- To set Compare window properties (see page 307)
- Changing Source Window Properties (see page 313)
- Changing Marker Properties (see page 284)

## **Range Properties Dialog**

Data Range Tab Specifies the range of data to export.

| Range Prope      | erties                                    |              |
|------------------|---|--------------|
| Data Range       | Bus/Signal Selection                      |              |
| <u>∩ A</u> ll    |   |              |
| <u>◯ T</u> ime   | <u>f</u> rom: -873.81333 us 🔳 <u>t</u> o: | 1.2233387 ms |
| ⊙ <u>M</u> arker | from: M1 💽 to:                            | M2 💌         |
|                  |   |              |
|                  |   |              |
|                  |   |              |
|                  |   |              |
|                  | ОК  | Cancel Help  |

| Time   | Lets you specify the range of data to export by time.    |
|--------|--|
| Marker | Lets you specify the range of data to export by markers. |

**Bus/Signal** Specifies the buses/signals to export data from. **Selection Tab** 

| Range Properties                |          |                           |
|---------------------------------|----------|---------------------------|
| Data Range Bus/Signal Selection |          |                           |
| B-                              |          | Select All<br>Select None |
|                                 |          |                           |
| ,                               | OK Cance | Help                      |

| Select All  | Selects all buses/signals.    |
|-------------|-------------------------------|
| Select None | De-selects all buses/signals. |

See Also • To export data to CSV format files (see page 207)

# **Recall Trigger Dialog**

The Recall Trigger dialog lets you:

- Recall a previously-used trigger from:
  - The favorites list.

NOTE

- The recently used list.
- An XML format trigger specification file.
- Move a recently used trigger to the favorites list.
- Rename the trigger.
- Clear triggers from the favorites or recently-used list.
- View trigger details.

The favorites list is saved with the logic analyzer configuration. If you load a new configuration file, the favorites list is overwritten.

| 📽 Recall Trigger  |              | x |
|---|--------------|---|
| Stored Favorite Triggers<br>If My Bus 1 = 8F Then Trigger and fill memory | OK<br>Cancel |   |
|   | Rename       |   |
|   | Clear        |   |
| Store Selected Recent Trigger To Favorites List                           | Clear All    |   |
| Most recently used triggers (added after each run)                        | Details      |   |
| If Anything Then Trigger and fill memory                                  | Open         |   |
|   | Help         |   |
|   |              |   |

| Rename    | Lets you edit the name of the highlighted trigger.   |
|-----------|--|
| Clear     | Clears the highlighted trigger from the list.  |
| Clear All | Clears all triggers from recall lists.   |
| Details   | Shows complete definition of the highlighted trigger.  |
| Open      | Lets you recall a trigger that was previously saved to an XML format<br>trigger specification file.<br><b>NOTE:</b> When a trigger is stored to an XML format trigger specification<br>file, trigger sequence steps are converted to advanced If/Then trigger<br>functions. Therefore, the trigger may look different when you recall it<br>from an XML format file; however, it is equivalent to the trigger that was<br>saved. |

### See Also

- To store a trigger (see page 201)
- To recall a trigger (see page 202)
- To set the trigger history depth (see page 202)

# **Run Properties Dialog**

Displays the options for saving captured data after each run and stopping after a certain number of repetitive runs.

| 1 | Run Propert         | ies   | × |
|---|---------------------|---|---|
|   |                     | very acquisition e numbers between runs, starting with:   | Ĩ |
|   | Base file name:     | C:\Documents and Settings\dvutest\My Documents\Agilent  | ĺ |
|   | Save as type:       | Logic Analyzer Configuration (*.ala) 🛛 Settings   | ] |
|   | Directo<br>Data Ran | gs<br>me: LastAcquisition0001.ala<br>ory: C:\Documents and Settings\\Config Files<br>ge: All Data<br>rce: All |   |
|   | Repetitive Optio    | after 2 1 -+ acquisitions   |   |
|   |                     | OK Cancel Help  |   |

### **Save Options**

| Save after every acquisition   | Enables or disables saving captured data after every run. When enabled, you can specify additional options for naming the data files.  |  |
|--|--|--|
| Increment file<br>numbers between<br>runs, starting with   | Enables or disables saving to consecutively numbered files. When enabled, you can specify the base file name and type.   |  |
| Base file name   | Lets you enter the base file name when saving to consecutively numbered files.   |  |
| Save as type   | Lets you specify the file type to use when saving to consecutively<br>numbered files. You can choose from:<br>• Logic Analyzer Configuration (*.ala)<br>• Transferable Configuration (*.xml)<br>• Module CSV text file (*.csv)<br>• Module binary file (*.alb)<br>• Standard CSV text file (*.csv)<br>For more information on these file types, see the topics under Saving<br>Captured Data (and Logic Analyzer Setups) (see page 205). |  |
| SettingsOpens the Save As dialog (see page 206) for specifying the sindividual data files; for example, you can select the data so sample range. |  |  |
| Current Settings   | Shows the currently selected settings.   |  |

### 12 Reference

| Repetitive |                    |  |  |  |  |
|------------|--------------------|--|--|--|--|
| Options    | Stop running after | Lets you stop repetitive runs after a certain number of acquisitions.<br>When enabled, you can enter the number of acquisitions. |  |  |  |
|            |                    |  |  |  |  |

See Also • Running/Stopping Measurements (see page 203)

## **Select Symbol Dialog**

Use the Select Symbol dialog to choose a symbol to use when the numeric base (see page 267) is set to Symbols.

| Select Symbol for ADDR  |  |
|---|--|
| Symbol Name to find:  | Symbols matched = 6  |
| u   |  |
| Name 🔻 Type Value Ba:   | se File  |
| ultra_long     Variable     0000 43440000 4347     Hex       unlink     Function     FFF0 6DF0FFF0 6ELF     Hex       unsout     Function     FFF0 4FCCFFF0 538F     Hex       update_display     Function     FFF0 3184FFF0 338F     Hex       update_system     Function     FFF0 3408FFF0 3557     Hex       user_api     Section     FFF8 0000FFF8 000B     Hex | <ul> <li>indio.c (\187\lib\indio.c</li> <li>ccvprntf.c (\187\lib\ccv</li> <li>ecs2.c (\users\chrisb\c</li> <li>update_sys.c (\users\c</li> </ul> |
|   | 0000   |

The Select Symbol dialog becomes available when you use the Symbols number base in the following dialogs:

- Find (see page 296)
- "Filter/Colorize" (in the online help)
- Specifying Simple Triggers (see page 156)
- Advanced Trigger Dialog (see page 496)

In the Select Symbol dialog:

|  | Symbol Name to find | <ul> <li>Filter the list of symbols by typing characters in this field. You can also use the wildcard characters:</li> <li>* (asterisk) to represent zero or more characters.</li> <li>? (question mark) to represent a single character.</li> <li>You can sort on any column in the symbol list by clicking the column header.</li> </ul> |
|--|---------------------|--|
| NameLists the symbol names definSymbols (see page 139)). |                     | Lists the symbol names defined or loaded for the bus (see Setting Up Symbols (see page 139)).  |

| Туре             | Lists the symbol types (for example, section, variable, function, etc.).<br>When sorting on this column, the symbols associated with each type are<br>sorted by name.   |  |  |
|------------------|---|--|--|
| Value            | Lists the symbol values.  |  |  |
| Base             | Shows the number base for the symbol value.   |  |  |
| File             | Shows the high-level source file that the symbol is from. When sorting on this column, the symbols associated with each file are sorted by value.   |  |  |
| Select           | When there is a range of values associated with the selected symbol, you can choose the <b>Start Value</b> of the range, the <b>End Value</b> of the range, and if you are selecting a symbol for a range setting, the <b>Start and End Values</b> of the range.  |  |  |
| Add Offset (Hex) | Lets you add an offset to the selected symbol value, for example, in the<br>case where code is relocated.<br>Note that when you use offsets, the system stores the "real" value, not<br>the fact that it is a symbol plus an offset. This can cause the display of<br>the symbol+offset to be different than what you entered. For example,<br>for:<br>•<br>Symbol Value  |  |  |
|                  | <ul> <li>RangeSymbol1 0010</li> <li>RangeSymbol2 1120</li> <li>Symbol3 21</li> <li>Symbol4 22</li> <li>Symbol5 FF</li> <li>If you enter "Symbol3 + 1", the system interprets this as 22, which is also Symbol4. So, even though you entered "Symbol3 + 1", the system displays "Symbol4".</li> <li>If you enter "RangeSymbol2(end value) + 1", it will be displayed as "Symbol3".</li> <li>If you enter "RangeSymbol1(start value) + 12", it will be displayed as "RangeSymbol2+1".</li> <li>Symbol values can "wrap", such as "Symbol5 + 1" where the result is 00. In this case, the you enter "Symbol5 + 1" and the resulting symbol is "RangeSymbol1".</li> </ul> |  |  |

**See Also** • Setting Up Symbols (see page 139)

• Symbols Dialog (see page 545)

## **Select System to Use Dialog**

The Select System to Use dialog lets you select a logic analysis system frame (see page 789) to connect to, and it lets you manage the list of frames.

A local system is a frame connected to the machine that runs the *Agilent Logic Analyzer* application. Remote systems are frames connected to machines elsewhere on your network. The remote system list can be managed any way you wish. The list of remote systems is stored on a per-user basis (each user has their own customizable list of remote systems).

The information in the dialog can be sorted by any of the columns by clicking on the column header.

You can right-click on any row in the dialog to get quick access to a menu of system-specific actions.

| Select System to Use  |  |   |   |                        |
|---|--|---|---|------------------------|
| System Clocal)<br>Clocal (local)<br>mtx33<br>Clmtx63<br>mtx72 | Current Status<br>In use (by self)<br>Available<br>In use (SHEETS, JACK, AGILENT\dvutest<br>Available<br>Available | Analyzer Description<br>16823A Logic Analysis System<br>16900A Logic Analysis System<br>16902A Logic Analysis System<br>16903A Logic Analysis System<br>Multi-Frame: 16900A Logic Analysis System | In Use Commer<br><no comment=""><br/><not in="" use=""><br/><no comment=""><br/><not in="" use=""><br/><not in="" use=""></not></not></no></not></no> | Clo <u>s</u> e<br>Help |
| mtx96   | Host not found   | <none></none>   | <not in="" use=""></not>  |                        |
| <u>C</u> onnect<br>Set My Comments                            | Add Delete Set Local Password Set As Auto-Connect  | Refresh<br>Dețails Chaț   |   | L <u>e</u> ss <<       |

| System               | Displays the hostname or IP address of a frame in the list. A green,<br>yellow, or red indicator indicates whether you can connect to or obtain<br>information from this frame (green), the frame hardware is initializing<br>(yellow), or some other problem (red)—such as the host not having any<br>frames, the host is offline, or the software on the target machine is<br>incompatible. |
|----------------------|---|
| Current Status       | Displays whether a frame is available, offline (that is, powered down),<br>currently in use, or has an incompatible remote service (that is, its<br>software needs to be upgraded to match the version of software<br>installed on the machine displaying this dialog).   |
| Analyzer Description | Displays the type of logic analyzer frame.  |
| In Use Comment       | Displays the "system in use" comments set by the user currently using the frame.  |

| Connect             | Connects to the selected logic analysis system (either local or remote).<br>You can connect to a frame even if it is in use. You will be warned if you<br>elect to connect to a frame that is already in-use before bumping the<br>other user offline. Taking a user offline by connecting to an in-use frame<br>will result in the other user losing any unsaved acquisition data<br>(included in the warning message). For this reason, it is always<br>preferable to contact the user (perhaps using the chat feature) and ask<br>them to gracefully take themselves offline—saving any important data.<br>If the user is not reachable—this ability to claim the system remotely is<br>a powerful feature.                          |
|---------------------|---|
| Add                 | Lets you enter the hostname or IP address of a remote system to be added to the list.   |
| Delete              | Removes the selected system from the system list.   |
| Refresh             | Forces an immediate refresh of all information in this dialog. This dialog is auto-updating—so you should not need to push this button. It is provided as a fail-safe only.   |
| More >> Less <<     | Shows or hides the bottom row of buttons.   |
| Set My Comments     | Opens a dialog that lets you enter some in-use comments. If another <i>Agilent Logic Analyzer</i> application attempts to connect to the system that you are currently connected to, your "system in-use" comments will be displayed. These comments can be used to explain why you are using a particular system, give your contact information, etc. These comments can be changed before going online with a frame or while online with a frame. The changes will take effect immediately.   |
| Set Local Password  | Opens the Remote Access Password Utility dialog for establishing a<br>remote-connect password (see page 94). The icon next to a <i>remote</i><br>system will have a padlock superimposed on it if a password is required<br>to connect to that machine. A remote-access password forces remote<br>users to enter this password before connecting to any local instrument.<br>The local system icon will never have a padlock on it because a<br>remote-access password is never required for the local client. This<br>button will change to "Clear Local Password" if a remote-access<br>password is already set. Only Windows users with administrative<br>credentials will have the ability to set or clear remote-access passwords. |
| Set as Auto-Connect | Selects the logic analysis system frame as the one to use when the <i>Agilent Logic Analyzer</i> application starts. The words "auto-connect" will show up next to the frame selected as an auto-connect. This button will change to "Clear Auto-Connect" if this frame is already set as an auto-connect.  |
| Details             | Opens the Frame/Module Information dialog (see page 513) which displays detailed information about the selected logic analysis system. If the selected frame is a member of a multiframe set, frame and module information on all frames in the set is presented in this dialog.  |

### 12 Reference

|  | Opens the Chat Select Destination dialog (see page 502) for<br>communicating with someone on the selected system. You have the<br>option of opening a two-way, interactive chat with any person logged on<br>to the selected system or the user that is currently using the selected<br>frame (if different). |
|--|---|
| Close Closes the dialog without connecting to a local or remote system |   |

- **Notes:** If the systems in this dialog are slow to update, try removing any machines in the list that are unresponsive (red) or not used.
  - Slow network conditions can also slow the update rate of this dialog.
  - This dialog is auto-updating—so it is not necessary to push the refresh button to see status changes. The refresh button is provided as a fail-safe only.
- See Also Connecting to a Logic Analysis System (see page 85)

## **Software Licensing Dialog**

The Software Licensing dialog is used to manage the software licenses used by a logic analysis system. This dialog has four tabs:

- Summary Tab (see page 534)
- Activation Tab (see page 535)
- Floating License Servers Tab (see page 536)
- Borrow Tab (see page 537)
- See Also Managing Software Licenses (see page 359)

### Summary Tab

The Software Licensing dialog's Summary tab displays information about the licenses that can be used in the logic analysis system.

| oftware Licensing Summary Activation Floating License Servers Borrow   |      |
|--|------|
| Active Software Licenses           Active Software Licenses           Image: Active Software Licenses </th <th></th> |      |
| B 4607A·020, 10 available, 2 in use from dvuqa06     A 1 in use by dvutest@dvuqa01     A 1 in use by dvutest@dvuqa01     A 1 in use by pw5670@mtx33 (Borrowed - returns 11/02/05 09:59:36)     A 4vanced Switching Interface (ASI) Packet Analysis     A Advanced Switching Interface (ASI) Packet Analysis   |      |
| APM7/9 Inverse Assembler     X and APM7/9 Inverse Assembler     X indicates that the associated software which uses this license is not installed.)     Show Details     Copy to Clipboard   | ~    |
| OK Cancel Apply  | Help |

Folders in the Active Software Licenses hierarchy show the licensed software that can be used. Red check marks show floating licenses are in use. A red "X" next to a folder shows that the software is not installed.

Within a folder, the status of individual licenses is displayed.

| Show Details      | Opens a dialog that displays detailed information about the selected license. |
|-------------------|---|
| Copy to Clipboard | Copies software licensing summary information to the clip board.              |

### See Also

• To view active software license information (see page 360)

### **Activation Tab**

The Software Licensing dialog's Activation tab contains the Licensing Host ID which is needed to activate software licenses.

| Software Licensing  |
|---|
| Summary Activation Floating License Servers Borrow  |
|   |
| To purchase Entitlement Certificate(s), contact your Agilent sales representative or go to<br>http://www.agilent.com/find/contactus |
| Licensing Host ID: 473ecb54   |
|   |
|   |
|   |
| OK Cancel Apply Help  |

### 12 Reference

| Licensing Host ID This ID is used when obtaining license files for software tools. |
|--|
|--|

### **See Also** • To activate software licenses (see page 361)

## **Floating License Servers Tab**

The Software Licensing dialog's Floating License Servers tab lets you identify and order the servers that floating licenses can be obtained from.

| Software Licensing   | ×    |
|--|------|
| Summary Activation Floating License Servers Borrow                               |      |
| License Servers  |      |
| 27004@silk     Add Server     27000@dyuga06                                      |      |
| Delete Server  |      |
| Move Up  |      |
| Move Down  |      |
| Refresh  |      |
| NOTE: Servers are searched in order from top to bottom for available licenses.   |      |
| Green/Red status shows presence on network, not that a license server was found. |      |
| OK Cancel Apply  | Help |

When licenses need to be checked out, the list of **License Servers** is searched in order, and the license is checked out from the first server having an available license.

| Add Server    | Opens a dialog for entering the computer name and port number of the floating license server.<br>CAUTION Only enter names of computers (or logic analyzers) that are floating license servers. Otherwise, the license manager interface hangs up for many minutes trying to determine if the computer is really a floating license server. |
|---------------|--|
| Delete Server | Removes the selected server from the list.   |
| Move Up       | Raises the selected server in the search order.  |
| Move Down     | Lowers the selected server in the search order.  |
| Refresh       | Updates the green or red server availability indicators. This is only a check of whether the computer is on the network, not of whether the license server software is running on that computer.   |
| Apply         | License server changes must be applied before you can go to the Summary or Borrow tabs.  |

**See Also** • To access floating license servers (see page 362)

### **Borrow Tab**

The Software Licensing dialog's Borrow tab lets you borrow floating licenses from a server for a period of time, for example, if you're taking a logic analyzer (or a computer running the *Agilent Logic Analyzer* application) out of the office (or just off the network). When a borrowed license's time expires, the license is automatically returned to the server. However, you can also use the Borrow tab to return licenses early.

| Software Licensing  | × |
|---|---|
| Summary Activation Floating License Servers Borrow  |   |
| Borrow Licenses   |   |
| Click on the Borrow button to borrow additional licenses used by this configuration.  |   |
| Borrow until 11/ 9/2005 👽 09:43 AM 🛟  |   |
|   |   |
| <ul> <li>Return Borrowed Licenses</li> <li>The following licenses cannot be returned while licenses are still checked out.</li> </ul> |   |
| Advanced Customization Environment - Runtime Package (returns 11/02/05 09:56:18)  |   |
| Return  |   |
| OK Cancel Apply Help  |   |

| Borrow Licenses             | Lets you enter the amount of time you want to borrow a license for and<br>borrow the license. The default time is seven days. The minimum time is<br>ten minutes. See also Messages in the Borrow Licenses Area (see<br>page 537).                                 |
|-----------------------------|--|
| Return Borrowed<br>Licenses | Lets you return borrowed licenses early. All borrowed licenses must be<br>returned at the same time. You are not able to return borrowed licenses<br>while any licenses are checked out. See also Messages in the Return<br>Borrowed Licenses Area (see page 538). |

### **See Also** • To borrow floating licenses and return them early (see page 364)

**Messages in the Borrow Licenses Area** These messages can appear in the Software Licensing dialog's Borrow tab.

#### Borrowing is not supported while in Demo Center Mode.

Licenses cannot be borrowed while using the Demo Center feature.

### This configuration is not using any licenses. There is nothing to borrow.

No licenses are currently in use, so there is nothing to borrow.

### This configuration is not using any floating licenses. There is nothing to borrow.

If all licenses being used are node-locked, there are no licenses that can be borrowed.

### The licenses for this configuration cannot be borrowed because some are node-locked.

You cannot borrow licenses when floating licenses and node-locked licenses are in use at the same time.

### Click on the Borrow button to borrow licenses used by this configuration.

When this message is displayed, you can borrow the licenses used by the current configuration.

#### Click on the Borrow button to borrow additional licenses used by this configuration.

When this message is displayed, some licenses are already borrowed, and you can borrow the additional licenses used by the current configuration.

### All licenses needed by this configuration are already borrowed.

When this message is displayed, all licenses in use are already borrowed. To borrow additional licenses, open the feature that requires the license, and return to the Software Licensing dialog's Borrow tab.

**Messages in the Return Borrowed Licenses Area** These messages can appear in the Software Licensing dialog's Borrow tab.

#### The following licenses cannot be returned while some servers are not configured.

If a license was checked out from a server that is not currently configured, licenses cannot be returned early.

#### The following licenses cannot be returned while licenses are still checked out.

If any licenses are checked out (and not borrowed), borrowed licenses cannot be returned early.

#### The following licenses are currently borrowed for exclusive use on this system.

When this message is displayed, borrowed licenses can be returned early.

### **Source Viewer Properties Dialog**

| Source Viewer Propertie | 25                      |                   | ×  |
|-------------------------|-------------------------|-------------------|----|
| Listing Properties      | Column Properties       | Marker Properties | 1  |
| Source Properties       | Source Code Directories | Correlation Bus   | ĺ. |

- Source Properties Tab (see page 539)
- Source Code Directories Tab (see page 539)
- Correlation Bus Tab (see page 540)

The Listing Properties, Column Properties, and Marker Properties tabs are the same as in the Listing window.

**See Also** • Changing Listing Window Properties (see page 263)

• Changing Bus/Signal Column Properties (see page 265)

### **Source Properties Tab**

The Source Viewer Properties dialog's Source Properties tab lets you set the background color and font size as well as display options like the number of spaces to use for tabs and whether or not to display line numbers.

| Source Viewer Propertie                 | s   | × |
|---|---|---|
| Listing Properties<br>Source Properties | Column Properties Marker Properties<br>Source Code Directories Correlation Bus  |   |
| Background Source Text                  | Display Options<br>Tab Width 1 1 - +<br>Display Line Numbers<br>Trigger Options |   |
|   | Address Alignment 4-byte  |   |
| OK                                      | Cancel Apply Help   |   |

- **See Also** Changing Source Window Properties (see page 313)
  - Source Viewer Properties Dialog (see page 538)

### **Source Code Directories Tab**

The Source Viewer Properties dialog's Source Code Directories tab lets you specify the directories where the source code is located. This is necessary because source file paths specified in the symbol file may not be valid if you compile on one computer and debug on another. You can specify multiple directories and change their order. Directories are searched in order, and you can specify whether subdirectories are searched.

|   | es                      |                   |
|---|-------------------------|-------------------|
| Listing Properties                              | Column Properties       | Marker Properties |
| Source Properties                               | Source Code Directories | Correlation Bus   |
| dd directories where s<br>Z Search subdirectori |                         |                   |
| C:\My Documents\sou                             | irce                    | Add               |
|   |                         | Delete            |
|   |                         | Move Up           |
|   |                         | Move Down         |
|   |                         |                   |

#### See Also

- To edit the source code directory list (see page 311)
- Source Viewer Properties Dialog (see page 538)

### **Correlation Bus Tab**

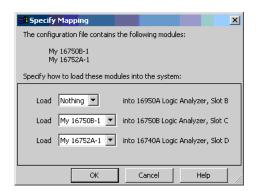
The Source Viewer Properties dialog's Correlation Bus tab lets you specify the bus whose line number symbols will be used for source correlation. Typically, you will select the "software address" bus generated by an inverse assembler tool or another address bus.

| Source Viewer Properties   |
|--|
| Listing Properties         Column Properties         Marker Properties           Source Properties         Source Code Directories         Correlation Bus           Select the bus that the viewer should correlate with         Control of the second secon |
| MPC860 Demo Board (Filter/Colorize - Motc     Motorola PowerQUICC (MPC8)()     Motorola PowerQUICC (MPC8)()     Motorola PowerQUICC (MPC8)() Inverse A     10 Software Address     10 Cycle Type-1     10 Cycle Type-2   |
| OK Cancel Apply Help   |

- **See Also** To select the correlation bus (see page 312)
  - Source Viewer Properties Dialog (see page 538)

## **Specify Mapping Dialog**

The Specify Mapping dialog lets you manually map modules from a configuration file to modules in the logic analysis system.



The top of the Specify Mapping dialog lists the module configurations in the file being loaded. The bottom part of the dialog lists modules in the logic analysis system. The **Nothing** selection says not to use any of the module configurations being loaded.

**NOTE** If you cannot load setup information from an ALA format configuration file into a particular module, the modules are not compatible, and you need to use an XML format configuration file to transfer the module setup information (see If an ALA format configuration file won't open (see page 374)).

#### **See Also** • Module Mapping Dialog (see page 517)

- To transfer module setups to/from multi-module systems (see page 224)
- ALA vs. XML, When to Use Each Format (see page 445)

#### **Split Analyzer Setup Dialog**

A logic analyzer *module* (see page 790) can be split into two logic analyzer modules, for example, to probe two buses with different clock signals.

NOTE

When you split a logic analyzer module, one of the resulting modules must be in the state sampling mode (they cannot both be in the timing sampling mode).

The Split Analyzer Setup dialog lets you specify how many channels are used in each module.

#### 12 Reference

| 🏙 Split Analyzer Setup |  | × |
|------------------------|--|---|
|                        | Advanced Pod Assignment Mode                 |   |
| Channel Assignment     | Channel Assignment Analyzer 2<br>34 channels |   |
|                        | OK Cancel Help                               |   |

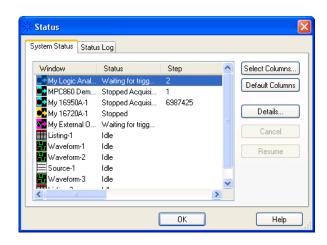
| Channel Assignment              | Drag the slider bar to split channels between the logic analyzer modules.   |  |  |  |  |
|---------------------------------|---|--|--|--|--|
| Advanced Pod<br>Assignment Mode | Select this option for finer control over which <i>pods</i> (see page 791) or <i>pod pairs</i> (see page 791) are assigned to each module or are reserved for time tag storage. |  |  |  |  |
|                                 | at Split Analyzer Setup   |  |  |  |  |
|                                 | Advanced Pod Assignment Mode  |  |  |  |  |
|                                 | Pod A1/Pod A2 Analyzer 1 Master Pods  |  |  |  |  |
|                                 | Pod A3/Pod A4 Analyzer 2  Master Pods   |  |  |  |  |
|                                 | Pod A5/Pod A6 Reserved for timetag storage for Analyzer 1   |  |  |  |  |
|                                 | OK Cancel Help  |  |  |  |  |
|                                 | Master Pods indicate that the pod or pod pair is on the master card.  |  |  |  |  |

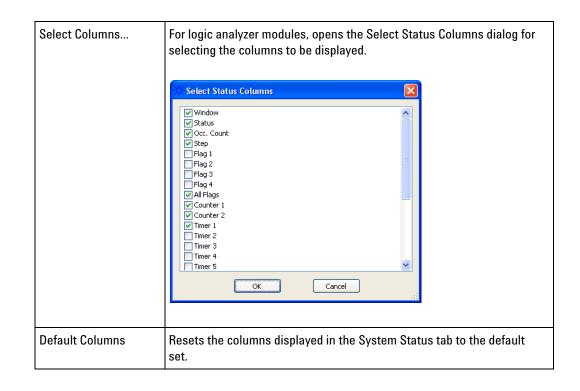
**See Also** • Configuring Logic Analyzer Modules (see page 98)

- Memory Depth and Channel Count Trade-offs (see page 420)
- Pod and Channel Naming Conventions (see page 418)

#### **Status Dialog**

System Status Displays the logic analysis system status. Tab





| Details | Displays details for the selected module, tool, or window.  |
|---------|---|
|         | Waiting for trigger in Trigger Step 2<br>For example, module details include: graphical trigger overview,<br>occurrence counter, global counter, flags, and timer status. |
| Cancel  | Cancels processing for the selected module, tool, or window.  |
| Resume  | Resumes canceled processing for the selected module, tool, or window.   |

You can copy a module, tool, or window's status to the clip board by right-clicking and choosing **Copy** from the popup menu.

**Status Log Tab** Displays the logic analysis system status log.

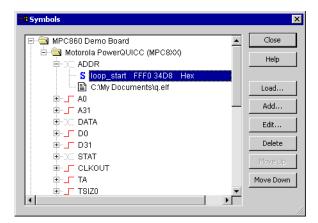
| 🗖 Status          |          |              | X   |
|-------------------|----------|--------------|---|
| System Status Sta | tus Log  |              |   |
| Show<br>Errors V  | Warnings | 💌 Informatic | Clear Log   |
| Туре              | Time     | Date         | Description   |
| Info              | 12:48:58 | 03/31/06     | The system is now operating Offline.  |
| Error             | 12:50:05 | 03/31/06     | Module: My 16950A-1<br>Slot: D<br>You must remove probe adapters from all pods to calit |
|                   |          |              | ٤   |
| ·                 |          |              | ОК Нер  |

You can select the types of log messages to display, and you can clear the log.

**See Also** • Options Dialog (see page 522)

#### **Symbols Dialog**

The Symbols dialog lets you to define, copy, and edit symbols for the entire system.



User-defined symbols are indicated by s.

Symbols files are indicated by **B**. Symbol files can be either compiler-generated object files containing symbols or general-purpose ASCII (GPA) format symbol files.

| Load              | If a bus/signal is selected, this opens the Select Symbol File dialog for<br>loading symbols from a compiler-generated object file or a<br>general-purpose ASCII (GPA) format symbol file.<br>If symbol file is selected, it is reloaded.      |
|-------------------|--|
| Add               | Adds a user-defined symbol to the selected bus/signal.   |
| Edit              | Edits the selected user-defined symbol.  |
| Delete Delete All | Removes the selected user-defined symbol or symbol file (or all symbols if a bus/signal is selected) from the list.  |
| Move Up Move Down | Moves the selected user-defined symbol or symbol file up or down<br>within the list. When the system looks for a symbol that corresponds to<br>a bus/signal value, the first match is used. (More than one symbol can<br>match a given value.) |

#### **See Also** • Setting Up Symbols (see page 139)

• Displaying Names (Symbols) for Bus/Signal Values (see page 269)

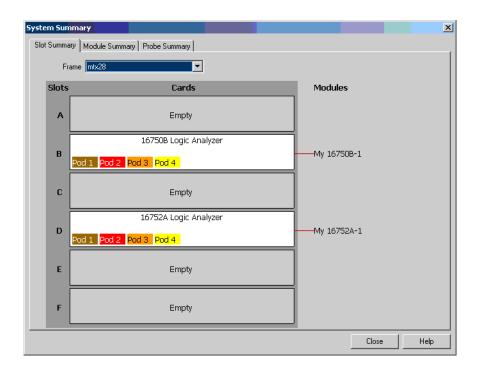
#### **System Summary Dialog**

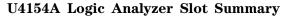
The System Summary dialog is used to see summary information about all modules in the system including a physical view of the cards in the system (Slot Summary (see page 546)), a list of all of the modules and their trigger times (Module Summary (see page 548)), and a list of how to connect all of the probes (Probe Summary (see page 548)).

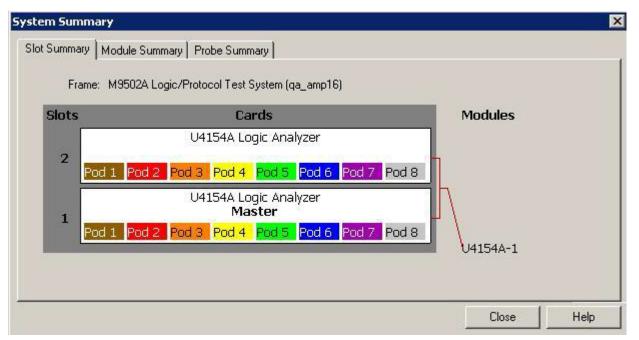
- Slot Summary Tab (see page 546)
- Module Summary Tab (see page 548)
- Probe Summary Tab (see page 548)
- **See Also** Analyzer Setup Dialog (see page 498)

#### **Slot Summary Tab**

For the selected *frame* (see page 789) (if there are multiple frames), the Slot Summary tab shows: the *slots* (see page 793), *cards* (see page 788), and *modules* (see page 790) in the logic analysis system frame, or the *cards* (see page 788) and *modules* (see page 790) in the standalone logic analyzer.







If you are using U4154A Logic Analyzer, the Slot Summary tab displays a graphical view of the slots of the AXIe chassis in which you installed the U4154A Logic Analyzer. If you are using a two-slot chassis, then the placement of the U4154A cards in these two slots is displayed. If you are

using a 5-slot chassis, then all the five slots are displayed. You can also view which U4154A card in a multi-card set is considered as the master card.

**See Also** • System Summary Dialog (see page 546)

#### Module Summary Tab

For each *module* (see page 790) in the logic analysis system, the Module Summary tab shows the *frame* (see page 789) in which the module resides, the *cards* (see page 788) that make up the module, the *slots* (see page 793) in which these cards reside, and the time that a trigger occurred.

| √lodule Name | Frame      | Slot(s) | Card(s)            | Time Of Trigger | Buses/9 |
|--------------|------------|---------|--------------------|-----------------|---------|
| 6752A - 1    | mtx59      | В       | 16752A Logic Analy |                 |         |
| 6950A - 1    | mtx59      | E       | 16950A Logic Analy |                 |         |
| 6752A - 2    | mtxspecial | A - B   | 16752A Logic Analy |                 |         |
|              |            |         |                    |                 |         |
|              |            |         |                    |                 |         |
|              |            |         |                    |                 | Þ       |
|              |            |         |                    |                 |         |

**See Also** • System Summary Dialog (see page 546)

#### **Probe Summary Tab**

The Probe Summary tab shows logic analyzer pods and channels, probe types, and the connectors or signals in the device under test to which the pods and channels should be connected.

Probe types can be defined by themselves, in XML configuration files, or while importing netlists (see page 113) (to assign bus/signal names to logic analyzer channels). If you haven't defined probe types, the flying-lead probe type is assumed.

NOTE

When connecting differential probe channel pin/pad/lead pairs to single-ended signals, make sure the negative pin/pad/lead is connected to ground and the positive pin/pad/lead is connected to the single-ended signal.

| Logic Analyzer Pod/Channel | Probe Type              | Connect To                       | <b></b> |
|----------------------------|-------------------------|----------------------------------|---------|
| Pod 1                      | E5346A - MICTOR Adapter | J1 : Odd (My Bus 1, My Signal 1) |         |
| Pod 2                      | E5346A - MICTOR Adapter | J1: Even                         |         |
| Pod 3 Channel 0            | Flying-Lead             | ADDR[0]                          |         |
| Pod 3 Channel 1            | Flying-Lead             | ADDR[1]                          |         |
| Pod 3 Channel 2            | Flying-Lead             | ADDR[2]                          |         |
| Pod 3 Channel 3            | Flying-Lead             | ADDR[3]                          |         |
| Pod 3 Channel 4            | Flying-Lead             | ADDR[4]                          |         |
| Pod 3 Channel 5            | Flying-Lead             | ADDR[5]                          |         |
| Pod 3 Channel 6            | Flying-Lead             | ADDR[6]                          |         |
| Pod 3 Channel 7            | Flying-Lead             | ADDR[7]                          |         |
| Pod 3 Channel 8            | Flying-Lead             | ADDR[8]                          |         |
| Pod 3 Channel 9            | Flying-Lead             | ADDR[9]                          |         |
| Pod 3 Channel 10           | Flying-Lead             | ADDR[10]                         |         |
| Pod 3 Channel 11           | Flying-Lead             | ADDR[11]                         |         |
| Pod 3 Channel 12           | Flying-Lead             | ADDR[12]                         |         |
| Pod 3 Channel 13           | Flying-Lead             | ADDR[13]                         |         |
| Pod 3 Channel 14           | Flying-Lead             | ADDR[14]                         |         |
| Pod 3 Channel 15           | Flying-Lead             | ADDR[15]                         |         |
| Pod 4 Channel 0            | Flying-Lead             | ADDR[16]                         |         |
| Pod 4 Channel 1            | Flying-Lead             | ADDR[17]                         |         |
| Pod 4 Channel 2            | Flying-Lead             | ADDR[18]                         |         |
| Pod 4 Channel 3            | Elving-Lead             | ADDB[19]                         | •       |

**See Also** • "To define probes" (in the online help)

- System Summary Dialog (see page 546)
- "Connecting Probes Using the Probe Summary" (in the online help)

#### **Target Control Port Dialog**

The 16900A, 16902A, 16902B, and 16903A logic analysis system *frames* (see page 789) have a *target control port*, an 8-bit, 3.3V port that can be used to send signals to a device under test. The target control port does not function like a pattern generator, but more like a remote control for switches in the device under test.

For the selected frame (if there are multiple frames), the Target Control Port dialog lets you set the output signal levels on the port.

| Target Co | ntrol P | ort           |            |                   |        | ×     |
|-----------|---------|---------------|------------|-------------------|--------|-------|
| Frame:    | cos-l   | ab-34         |            | ▼                 |        |       |
| Signal    | Enable  | Wri<br>ed Low | te<br>High | Observed<br>Value |        |       |
| 0         | •       | 0             | 1          |                   | Toggle | Pulse |
| 1         | •       | 0             | 1          |                   | Toggle | Pulse |
| 2         |         | 0             | 1          |                   | Toggle | Pulse |
| 3         |         | 0             | 1          |                   | Toggle | Pulse |
| 4         | •       | 0             | 1          |                   | Toggle | Pulse |
| 5         |         | 0             | 1          | 0                 | Toggle | Pulse |
| 6         | •       | 0             | 1          | 0                 | Toggle | Pulse |
| 7         | •       | 0             | 1          | 0                 | Toggle | Pulse |
|           |         |               |            | Close             | Help   |       |

| Signal         | Identifies the target control port signal.  |
|----------------|---|
| Enabled        | Lets you enable or disable an output signal on the target control port.<br>When disabled, the signal has a tri-state high-impedance output. When<br>enabled, the signal outputs a standard 3.3V logic level with 1 high and 0<br>low. |
| Write          | Gives you two buttons, <b>0</b> and <b>1</b> , for changing the signal output value to a standard 3.3V logic low or high, respectively.   |
| Observed Value | Displays the signal value observed on the target control port signal.   |
| Toggle         | Flips the settings of the signal and leaves them that way. For example, if your signal is set to 1 and you click <b>Toggle</b> , the setting changes to 0.  |
| Pulse          | Flips the settings for one clock cycle, which is at least 16 ms. The pulse may last longer. You cannot specify the duration of the pulse.   |

**See Also** • To control signals in the device under test (see page 83)

#### **Thresholds and Sample Positions Dialog**

The Thresholds and Sample Positions dialog lets you position the logic analyzer's setup/hold window (or sampling position) and specify the threshold voltage so that data on high-speed buses is captured accurately, in other words, so that data is sampled when it is valid.

When the device under test's data valid window is less than 2.5 ns (roughly, for clock speeds  $\geq$  200 MHz), it's easiest to use *eye finder* to locate the stable and transitioning regions of signals and to automatically adjust sampling positions.

*Eye finder* measures the location of the stable region boundaries and places the logic analyzer's sampling position in the center of the stable region. *Eye finder* also adjusts the threshold voltage setting to maximize the width of the measured stable regions.

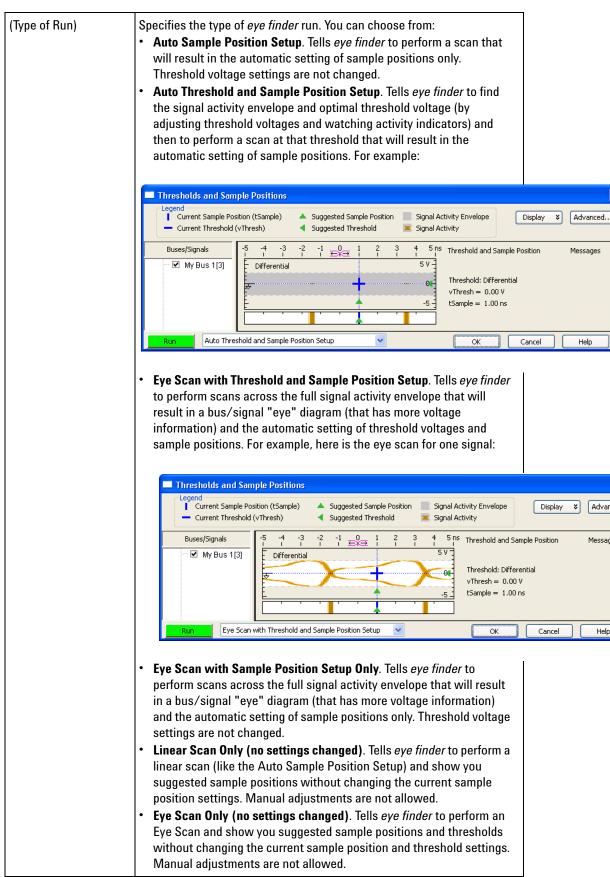
When the device under test's data valid window is greater than 2.5 ns (roughly, for clock speeds < 200 MHz), it's easiest to adjust the sampling position manually, without using the logic analyzer to locate the stable and transitioning regions of signals.

| Buses/Signals    | -5 -4 -3 |                   | 3 4        | 5 ns Sample Position  | Messages |
|------------------|----------|-------------------|------------|-----------------------|----------|
| My Bus 1         |          |                   |            | tSample = 0.28 ns avg |          |
| 🗹 My Bus 1 [0]   |          | · · · · · ·       |            | tSample = 0.38 ns     |          |
| - 🗹 My Bus 1 [1] |          | · · · · · · · · · |            | tSample = -0.36 ns    |          |
| - 🗹 My Bus 1 [2] |          | · · · · · · ·     |            | tSample = -0.28 ns    |          |
| 🗹 My Bus 1 [3]   |          |                   |            | tSample = 1.00 ns     |          |
| - 🗹 My Bus 1 [4] |          | · · · · · ·       | <b>1</b>   | tSample = 0.66 ns     |          |
| 🗹 My Bus 1 [5]   |          |                   |            | tSample = 0.27 ns     |          |
| 🗹 My Bus 1[6]    |          |                   |            | tSample = 0.27 ns     |          |
| My Bus 1[7]      |          |                   | <b>.</b> . | tSample = 0.30 ns     |          |
|                  |          |                   |            |                       |          |

| Legend        | Describes items you see in the bus/signal diagram.  |
|---------------|---|
| Display       | Lets you display or hide:<br>• Threshold and Sample Position column.<br>• Messages column.<br>• Voltage information.  |
| Advanced      | Opens the Eye Finder Advanced Options dialog (see page 555) for setting measurement duration and run mode options.  |
| Buses/Signals | Lets you choose the buses/signals to run <i>eye finder</i> on. You can expand<br>or overlay the signals in a bus, select all or select none of the signals,<br>select individual signals, or select multiple signals.<br>If a channel appears in multiple buses/signals, selecting that channel<br>will select it in each of those buses/signals.<br>After <i>eye finder</i> is run, you can right-click on a bus/signal name and<br>choose <b>Properties</b> to open the Eye Finder Properties dialog (see<br>page 557) for viewing additional information about the measurement<br>results. |

| Bus/Signal Diagram               | <ul> <li>Displays a digital "eye" diagram that represents many samples of data captured in relation to the sampling clock. The transitioning edges measured before and after the sampling clock result in a picture that is eye-shaped.</li> <li>The display area shows:</li> <li>Transitioning (dark) and stable (light) regions on the signals. Intensity shows where transitions are more prevalent (darker orange) and less prevalent (lighter).</li> <li>Suggested sampling positions (green triangles).</li> <li>The current sampling positions (vertical blue lines in stable regions, red lines in transitioning regions).</li> <li>When voltage information is displayed, the current threshold voltage settings are shown (horizontal blue lines in stable regions, red lines in transitioning regions). If you click and drag the "+" formed by the sampling position and threshold setting lines, both are adjusted; to adjust the settings individually, click and drag the appropriate dotted line. Note that adjusting threshold settings affects all channels on the same pod (and sometimes the clock input on the pod as well).</li> <li>To give you more information about the signals, the display covers +/-5 ns even though the sampling position may only be set to +/-3.25 ns.</li> </ul> |
|----------------------------------|---|
| Threshold and Sample<br>Position | Shows the numeric values of the threshold voltage and sample position<br>settings. Clicking in this column gives you entry fields for adjusting the<br>settings. You can also drag the sample position and threshold voltage<br>bars to new locations.  |
| Messages                         | <ul> <li>This column displays:</li> <li>Informational message icons. You can move the mouse pointer over<br/>the icon to cause the message to pop up.</li> <li>Time stamp information that shows when the last <i>eye finder</i><br/>measurement was run.</li> </ul>  |

| Run | Runs eye finder to automatically adjust state sampling positions and |
|-----|--|
|     | threshold voltage settings.  |



#### **See Also** • Understanding State Mode Sampling Positions (see page 424)

- How Selected/Suggested Positions Behave (see page 557)
- Eye Finder Info Messages (see page 388)
- To automatically adjust state sampling positions and threshold voltages (see page 130)
- To manually adjust state sampling positions (see page 133)

| Measurement |  |  |  |  |
|-------------|--|--|--|--|
| Duration    | Eye Finder Advanced Options  |  |  |  |
|             | Measurement Duration Run Mode  |  |  |  |
|             | Number of clock cycles measured at each offset position                    |  |  |  |
|             | Short (50 000) - requires frequent transitions                             |  |  |  |
|             | Medium (500 000) - default   |  |  |  |
|             | C Long (5 000 000) - better for infrequent transitions                     |  |  |  |
|             | Custom - 10 or more clocks   |  |  |  |
|             | # Clocks 500000  |  |  |  |
|             | Eye Scan: Complete Scan<br>(Scan all points regardless of signal activity) |  |  |  |
|             |  |  |  |  |
|             | OK Cancel Help   |  |  |  |

| Short                      | <i>Eye finder</i> looks at 50,000 clock cycles on each channel to determine the suggested sampling positions. This setting requires frequent transitions on all channels.   |
|----------------------------|---|
| Medium                     | <i>Eye finder</i> looks at 500,000 clock cycles on each channel to determine the suggested sampling positions. Use this for channels that transition at a normal rate.  |
| Long                       | <i>Eye finder</i> looks at 5 million clock cycles on each channel to determine the suggested sampling positions. Use this setting if some channels have sporadic transitions.   |
| Custom                     | Lets you specify the number of clock cycles to sample on each channel at each sampling position (each point in time).   |
| Eye Scan: Complete<br>Scan | When unchecked, eye scan measures locations where signal activity is<br>found, but does not scan the interior of the eyes where there is no signal<br>activity.<br>When checked, all locations in time and voltage are scanned, including<br>the interior of the eyes. This is useful in some situations where sporadic<br>noise (for example, once per second) is present. |

#### **Eye Finder Advanced Options Dialog**

Some things to consider when selecting among the *eye finder* advanced settings are:

- Upper address bits that don't transition as frequently as lower address bits and require more clock cycles.
- Data buses that are driven by different circuitry at different times require enough clock cycles to observe the effects of each driver on the bus.

When different channels require different settings, you can run *eye finder* on channel subsets to avoid using the Long setting on a large number of channels.

#### Run Mode

| Eye Finder Advanced Options       |  |  |  |  |  |
|-----------------------------------|--|--|--|--|--|
| Measurement Duration Run Mode     |  |  |  |  |  |
| Run Repetitively                  |  |  |  |  |  |
| Accumulate Results                |  |  |  |  |  |
| Demo Mode (no probes required)    |  |  |  |  |  |
| ✓ Enable sample position warnings |  |  |  |  |  |
| C Scan Limits                     |  |  |  |  |  |
| Min -5 ns 🔳 — +                   |  |  |  |  |  |
| Max 5 ns 🔳 — + Default            |  |  |  |  |  |
|                                   |  |  |  |  |  |
|                                   |  |  |  |  |  |
| OK Cancel Help                    |  |  |  |  |  |

| Run Repetitively                   | Runs the <i>eye finder</i> repetitively, so you can see how stable and transitioning signals vary over time.   |
|------------------------------------|--|
| Accumulate Results                 | When selected, <i>eye finder</i> data is accumulated from run-to-run. When unselected, <i>eye finder</i> data is erased before each run.   |
| Demo Mode                          | Lets you look at <i>eye finder</i> with demo data. Demo mode does not generate full eye scan data.   |
| Enable sample<br>position warnings | When checked, current sample positions in time are compared to <i>eye</i><br><i>finder</i> (or <i>eye scan</i> ) measurements, and you are warned if the sample<br>positions may no longer be in the stable region (the eye).<br>When unchecked, there are no checks for, or warnings about, possible<br>problems. This is useful for signals in some target systems with small<br>eyes, and it lets you suppress warnings that you have already seen<br>multiple times. |
| Scan Limits                        | Lets you set the range for the <i>eye finder</i> scan and display. This setting is saved in both ALA and XML format configuration files.   |

#### **Eye Finder Properties Dialog**

The Eye Finder Properties dialog displays information about the *eye finder* measurement results.

| Bus/Signal  | tPosition | vThreshold | vMin    | vMax   | Time of Measurement  | OK     |
|-------------|-----------|------------|---------|--------|----------------------|--------|
| My Bus 1[0] | 460 ps    | 0 V 0      | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[1] | -353 ps   | 0 V O      | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 | Cancel |
| My Bus 1[2] | -276 ps   | 0 V O      | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[3] | 1 ns      | 0 V        | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[4] | 657 ps    | 0 V        | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[5] | 268 ps    | 0 V        | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[6] | 345 ps    | 0 V        | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
| My Bus 1[7] | 306 ps    | 0 V        | -3.83 V | 3.83 V | Oct 10 15:39:18 2004 |        |
|             |           |            |         |        |                      |        |

| Bus/Signal          | The bus/signal name.   |  |  |
|---------------------|--|--|--|
| tPosition           | The sample position.   |  |  |
| vThreshold          | The threshold voltage.   |  |  |
| vMin                | The minimum voltage in the signal activity envelope.   |  |  |
| vMax                | The maximum voltage in the signal activity envelope.   |  |  |
| Time of Measurement | When <i>eye finder</i> was run.  |  |  |
| # Accum             | The number of accumulations that the data represents.  |  |  |
| Status              | The status information message from <i>eye finder</i> (see Eye Finder Info<br>Messages (see page 388)).        |  |  |
| Clock Spec          | Identifies the sampling clock setup.   |  |  |
| Sampling Mode       | Identifies the slot and pod that the sampling clock comes from, as well as the state sampling clock mode used. |  |  |

#### **How Selected/Suggested Positions Behave**

The *eye finder*'s selected and suggested sampling positions behave as follows:

How the Selected Position Behaves

- **1** The selected position (blue line in stable regions or red line in transitioning regions) can be dragged to the desired position without running *eye finder*.
- **2** The selected position is "snapped" to the suggested position (green triangle) each time *eye finder* is run on a channel.

| How the          | 1 | The suggested position (green triangle) is only shown in displays of a  |
|------------------|---|---|
| Suggested        |   | single channel.   |
| Position Behaves | 2 | There is only a suggested position on channels that have been measured. |

- **3** The suggested position is always in the center of the stable region closest to the selected position (blue or red line).
- **4** If the selected position is moved to a different stable region, the suggested position "hops" to the center of that region.
- **5** If a stable region is open-ended, the suggested position is placed a fixed distance from the closed end (the visible boundary); if more than one clock edge is active, the fixed distance is greater.

#### **TimingZoom Setup Dialog**

Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer.

| TimingZoom Setup   |                      |
|--|----------------------|
| Sampling Period: 250 ps<br>Trigger Position: 50% poststore | OK<br>Cancel<br>Help |

| TimingZoom Setup                | X            |
|---------------------------------|--------------|
| Sampling Period: 500 ps         | OK<br>Cancel |
| Trigger Position: 50% poststore | Help         |
| ]                               |              |
| × + ×                           |              |
| Align Trigger With: My 16742A-1 | -            |
| ,                               |              |

| Sampling Period | Displays the timing zoom sampling period. With some logic analyzers (see Logic Analyzer Notes, Timing Zoom (see page 637)), you can |
|-----------------|---|
|                 | change the sampling period to see more or less sampling resolution<br>around the trigger.   |

| Trigger Position   | Lets you position the timing zoom acquisition memory around the event that triggers the logic analyzer.  |
|--------------------|--|
| Align Trigger With | In some older logic analyzer modules, if the logic analyzer is split, this<br>lets you specify which analyzer's trigger timing zoom should be aligned<br>with. |

#### See Also • Using Timing Zoom (see page 136)

• Logic Analyzer Notes, Timing Zoom (see page 637)

### **Trigger Functions**

The trigger functions available in the Advanced Trigger dialog give you pre-configured trigger setups for common measurements. If the trigger function you need is not available, start with a trigger function that is close, convert the trigger sequence step to advanced If/Then trigger functions, and edit the If/Then trigger functions.

- Timing Mode Trigger Functions (see page 560)
- State Mode Trigger Functions (see page 573)
- See Also To show a trigger sequence step as Advanced If/Then trigger functions (see page 189)
  - To convert a trigger sequence step to Advanced If/Then trigger functions (see page 190)
  - Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)

#### **Timing Mode Trigger Functions**

The following trigger setup examples are available as Trigger Functions in the Advanced Trigger dialog when in the timing acquisition mode. To see these trigger setups in the context of an example measurement refer to Making a timing analyzer measurement (see page 72).

- Edge Edge (see page 561)
  - "N" number of edges (see page 562)
  - Edge and Pattern (see page 562)
  - Edge followed by edge (see page 563)
  - Edges too far apart (see page 563)
  - Edge followed by pattern (see page 564)
  - Pattern too late after edge (see page 564)

#### **Bus Pattern** • Pattern (see page 565)

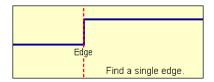
- Edge and Pattern (see page 562)
- Pattern present for > "T" time (see page 565)
- Pattern present for < "T" time (see page 566)
- Pattern absent for > "T" time (see page 566)
- Pattern absent for < "T" time (see page 567)
- Edge followed by pattern (see page 564)
- Pattern too late after edge (see page 564)
- **Other** Find anything "N" times (see page 567)

- Width violation on pattern or pulse (see page 568)
- Wait "T" seconds (see page 568)
- Run until user stop (see page 569)
- Wait for external arm (see page 569)
- Wait for arm from another module (see page 570)
- Advanced Advanced If/Then (see page 570)
  - Advanced 2-Way Branch (see page 571)
  - Advanced 3-Way Branch (see page 571)
  - Advanced 4-Way Branch (see page 572)
  - Pattern "AND" Pattern (see page 572)
  - Pattern "OR" Pattern (see page 573)
- **See Also** To replace or insert trigger functions into trigger sequence steps (see page 169)
  - State Mode Trigger Functions (see page 573)
  - To store a trigger (see page 201)
  - To recall a trigger (see page 202)

#### Edge

| Step 1 ¥ Edge                    |             |             |   |
|----------------------------------|-------------|-------------|---|
| Find 🛛 Bus/Signal 💌              | My Signal 1 | Rising Edge | • |
| Then 💐 Trigger and fill memory 💌 |             |             |   |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined edge occurs.



#### "N" number of edges

| Step 1 ¥ N number of edges                      |
|---|
| Find 🔻 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌 |
| 1 <u>1</u> - + time                             |
| Then 💐 Trigger and fill memory 💌                |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when the "Nth" occurrence of a user-defined edge occurs.

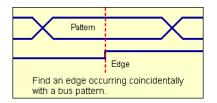
| Occurrence 1  |           | Occurrence n   |
|---------------|-----------|----------------|
|               |           |                |
| Edge          |           | Edge           |
| Find the n≞ o | occurrent | ce of an edge. |

**To edit this** • Specifying Advanced Triggers (see page 163) function

#### **Edge and Pattern**

| Step 1 × Edge and Pattern                                 |
|---|
| Find 👻 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌           |
| And 💐 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🕅 Hex 🔻 |
| Then 🔰 Trigger and fill memory                            |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when both a user-defined edge and bus pattern occur at the same time.



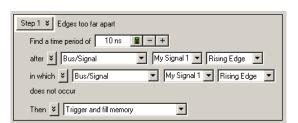
#### Edge followed by edge

| Step 1 ¥ Edge followed by edge                         |
|--|
| Find 👻 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌        |
| Followed by 💐 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌 |
| Occurring within 20 ns 📓 - +                           |
| Then 🛎 Trigger and fill memory                         |

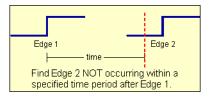
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when edge 2 occurs within a specified time period after edge 1.

| Edge 1 Edg   | je 2   |
|--|--------|
| time   |        |
| Find edge 2 occurring within a sp<br>time period after edge 1. | ecific |

#### To edit this function Edges too far apart



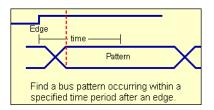
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when edge 2 does not occur within a specified time period after edge 1.



#### Edge followed by pattern

| Step 1 × Edge followed by pattern                                 |
|---|
| Find 🞽 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌                   |
| Followed by 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌 |
| Occurring within 20 ns 📕 - +                                      |
| Then 🞽 Trigger and fill memory                                    |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a bus pattern occurs within a specified time period after an edge.

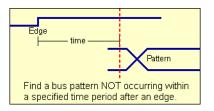


## **To edit this** • Specifying Advanced Triggers (see page 163) function

## Pattern too late after edge

| Step 1 ¥ Pattern too late after edge                           |  |  |  |
|--|--|--|--|
| Find a time period of 🛛 10 ns 📓 🗕 🛨                            |  |  |  |
| after 🞽 Bus/Signal 💌 My Signal 1 💌 Rising Edge 💌               |  |  |  |
| in which 🖇 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌 |  |  |  |
| does not occur   |  |  |  |
| Then 🗧 Trigger and fill memory                                 |  |  |  |

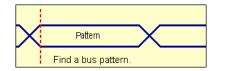
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a specified bus pattern does not occur within a specified time period after an edge.



#### Pattern

| Step 1 ¥ Pattern                 |                     |           |
|----------------------------------|---------------------|-----------|
| Find 🞽 Bus/Signal 💌 My Bus 1     | 💌 All bits 💌 Equals | 🔻 🔀 Hex 🔻 |
| Then 🗧 Trigger and fill memory 💌 |                     |           |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a designated bus pattern occurs.

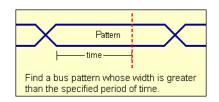


**To edit this function** • Specifying Advanced Triggers (see page 163)

#### Pattern present for > "T" time

|   | Step 1 ¥ Pattern present for >t time                       |
|---|--|
|   | Find 🞽 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌 |
| l | present for > 10 ns 🔳 - +                                  |
|   | Then 🗧 Trigger and fill memory                             |

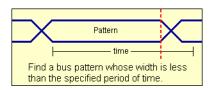
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is present greater than a specified time period.



#### Pattern present for < "T" time



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is present less than a specified time period.



## **To edit this** • Specifying Advanced Triggers (see page 163) **function**

#### Pattern absent for > "T" time

| Step 1 ¥ Pattern absent for >t time                        |  |  |
|--|--|--|
| Find 👻 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌 |  |  |
| absent for > 10 ns 🔳 - +                                   |  |  |
| Then 🔰 Trigger and fill memory                             |  |  |

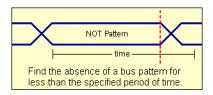
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is absent greater than a specified time period.

| $\square X$   | NOT Pattern |  |
|---|-------------|--|
|   | time        |  |
| Find the absence of a bus pattern for<br>greater than the specified period of time. |             |  |

#### Pattern absent for < "T" time

| Step 1 × Pattern absent for <t th="" time<=""></t>         |
|--|
| Find 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌 |
| absent for < 20 ns 📓 - +                                   |
| Then X Trigger and fill memory                             |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a user-defined bus pattern is absent less than a specified time period.

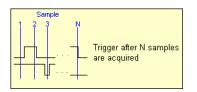


## **To edit this** • Specifying Advanced Triggers (see page 163) function

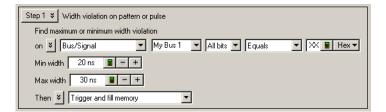
#### Find anything "N" times (timing)

| Step 1 × Find anything n times   |
|----------------------------------|
| Find Anything 1 📓 — + time       |
| Then 🞽 Trigger and fill memory 💌 |

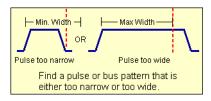
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when it sees any data (Anything) for the Nth time.



#### Width violation on pattern or pulse



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when a pulse or bus pattern is found that is either too narrow or too wide.



**To edit this** • Specifying Advanced Triggers (see page 163)

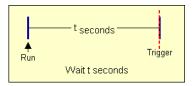
#### function

#### Wait "T" seconds



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers after the specified time period expires.

The maximum amount of time you can enter is based on the logic analyzer's sampling period. If you need to wait longer than the maximum time allowed, you can use a timer (see page 165) instead.



#### Run until user stop (timing)



This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. This trigger function sets up to never trigger. You must select the stop button to view the captured data.

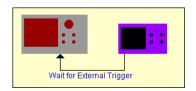


**To edit this** • Specifying Advanced Triggers (see page 163) function

#### Wait for external arm (timing)

| Step 1 🕹 | Wait for external arm |
|----------|-----------------------|
| Wait for | external arm          |

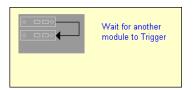
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when an external arming signal appears through the external **Trigger In** port (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)). The **Trigger In** BNC connector is located on the rear panel of the 16800-series logic analyzers, 1680-series logic analyzers, and 16900-series logic analysis systems; it is located on the front panel of the 1690-series logic analyzers.



#### Wait for arm from another module (timing)

| Step 1 🛛 Wait for arm from another module |   |
|---|---|
| × Arm in from 💌 1691D - 1                 | - |
| Then 🛛 Trigger and fill memory            | • |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when an arming signal from another module occurs (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)).



**To edit this** • Specifying Advanced Triggers (see page 163) function

#### Advanced If/Then (timing)

| Step 1 ¥ | Advanced If/Then        |                         |                  |
|----------|-------------------------|-------------------------|------------------|
| ¥ If     | ➤ Bus/Signal            | My Bus 1 💌 All bits 💌 E | iquals 💌 🔀 Hex 🔻 |
|          | occurs 💌                | 1 📓 - +                 |                  |
| Then     | Trigger and fill memory | •                       |                  |

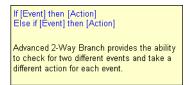
This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when the "If" clause becomes true.

| If [Event]                                     |
|--|
| Then [Action]                                  |
| Advanced If/Then is a generic function that    |
| can be modified to deal with any type of event |
| or action.                                     |
|  |

#### **Advanced 2-Way Branch (timing)**

| Step 1 🛛  | Advanced If/Then                                      |
|-----------|---|
| ¥ If      | 🗴 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 🔍 🗮 Hex 💌 |
|           | occurs 🔽 1 📓 - +                                      |
| Then      | Soto  |
| ¥ Else if | 🛿 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌 |
| Then      | 🛎 Goto 🔽 1 💌  |

This trigger function is available when the acquisition mode is set to Timing - Asynchronous. The two-way branch is evaluated true when either of two patterns (if or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.



#### To edit this • Specifying Advanced Triggers (see page 163)

## function

Advanced 3-Way Branch (timing)

| Step 1 ¥ Advanced If/Then |            |                              |             |
|---------------------------|------------|------------------------------|-------------|
| × If                      | Bus/Signal | My Bus 1 💌 All bits 💌 Equals | 🔻 🔀 🖬 Hex 🔻 |
|                           | occurs 💌   | 1 🔲 - +                      |             |
| Then                      | * Goto     | ▼ Next ▼                     |             |
| ¥ Else if                 | Bus/Signal | My Bus 1 💌 All bits 💌 Equals | 🔻 🔀 🖩 Hex 🔻 |
| Then                      | * Goto     | ▼ 1 ▼                        |             |
| ¥ Else if                 | Bus/Signal | My Bus 1 💌 All bits 💌 Equals | 🔻 🔀 🖩 Hex 🔻 |
| Then                      | ¥ Goto     |                              |             |

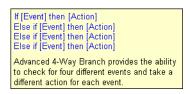
This trigger function is available when the acquisition mode is set to Timing - Asynchronous. The three-way branch is evaluated true when either of three patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.

| If [Event] then [Action<br>Else if [Event] then [A<br>Else if [Event] then [A | Action]  |
|---|--|
|   | nch provides the ability<br>erent events and take a<br>ch event. |

# To edit this function Specifying Advanced Triggers (see page 163) Advanced 4-Way Branch (timing)

#### Step 1 ¥ Advanced If/Then ¥ If 💌 My Bus 1 💌 All bits 💌 Equals Bus/Signal 🔻 🔀 🖩 Hex 🔻 occurs 1 🔳 - + • ¥ Goto ▼ Next ▼ Then ¥ Else if \* Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 🔻 🔀 🖬 Hex 🔻 \* Goto • 1 • Then ¥ Else if ➤ Bus/Signal My Bus 1 All bits 💌 Equals 💌 🔀 🖩 Hex 🕶 Then ¥ Goto • 1 • ¥ Else if \* Bus/Signal My Bus 1 💌 All bits 💌 Equals 💌 🔀 🖩 Hex 🕶 × Goto - 1 -Then

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The four-way branch is evaluated true when either of four patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.

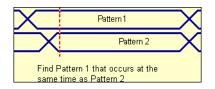


## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Pattern "AND" Pattern (timing)

| Step 1 😮 | Advanced If/Then               |                                    |           |
|----------|--------------------------------|------------------------------------|-----------|
| H 🗧      | Bus/Signal                     | 💌 My Bus 1 💌 All bits 💌 Equals 🔍 🔀 | Hex 🔻 🖌 🖛 |
|          | <ul> <li>Bus/Signal</li> </ul> | 💌 My Bus 1 💌 All bits 💌 Equals 🔍 📉 | 🖩 Hex 🔻   |
|          | occurs 💌                       | 1 📓 - +                            |           |
| Then     | Trigger and fill memory        | y 💌                                |           |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when both pattern1 "AND" pattern2 occur at the same time, and for the specified numbers of samples (occurs).



## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Pattern "OR" Pattern (timing)

| Step 1 🕹 | Advanced If/Then   |
|----------|--|
| × If     | 🖲 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌 Or 💌 |
|          | 🔻 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 🔍 🔛 Hex 💌      |
|          | occurs 🔽 1 📓 - +   |
| Then     | V Trigger and fill memory                                  |

This trigger function is available when the acquisition mode is set to **Timing - Asynchronous**. The analyzer triggers when either pattern1 "OR" pattern2 occurs for the specified numbers of samples (occurs).



## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### **State Mode Trigger Functions**

The following trigger setup examples are available as Trigger Functions in the Advanced Trigger dialog when in the state acquisition mode. To see these trigger setups in the context of an example measurement refer to Making a state analyzer measurement (see page 73).

**Patterns** • Pattern "N" times (see page 574)

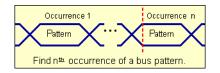
- "N" consecutive samples with Pattern1 (see page 575)
- Pattern1 followed by Pattern2 (see page 575)
- Pattern1 immediately followed by Pattern2 (see page 576)
- Pattern1 followed by Pattern2 before Pattern3 (see page 576)
- Too few states between Pattern1 and Pattern2 (see page 577)
- Too many states between Pattern1 and Pattern2 (see page 578)

|          | • Pattern2 occurring too soon after Pattern1 (see page 578)                         |
|----------|---|
|          | • Pattern2 occurring too late after Pattern1 (see page 579)                         |
|          | • Find a packet (see page 580)  |
| Other    | • Reset and start timer (see page 580)  |
|          | • Find anything "N" times (see page 581)  |
|          | • Run until user stop (see page 581)  |
|          | • Wait for external arm (see page 582)  |
|          | • Wait for arm from another module (see page 582)                                   |
|          | • Wait "N" external clock states (see page 583)                                     |
| Advanced | Advanced If/Then (see page 583)   |
|          | • Advanced 2-Way Branch (see page 584)  |
|          | Advanced 3-Way Branch (see page 585)  |
|          | Advanced 4-Way Branch (see page 585)  |
|          | Pattern "AND" Pattern (see page 586)  |
|          | Pattern "OR" Pattern (see page 587)   |
| See Also | • To replace or insert trigger functions into trigger sequence steps (see page 169) |
|          | • Timing Mode Trigger Functions (see page 560)                                      |
|          | • To specify default storage (see page 179)   |
|          | • To store a trigger (see page 201)   |
|          | • To recall a trigger (see page 202)  |
|          |   |

#### Pattern "N" times

| Default Storage (overridden by sequence level store actions):  |
|--|
| 🗴 Store 🗴 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌  |
|  |
| Step 1 × Pattern n times                                       |
| Find 1 I cocurrence of   |
| 🖲 Bus/Signal 🔽 My Bus 1 🔽 All bits 💌 Equals 💌 💥 📓 Hex 💌        |
| Then 👻 Trigger and fill memory 💌                               |
| 🗴 with 💐 Bus/Signal 🔹 My Bus 1 💌 All bits 💌 Equals 💌 💥 📓 Hex 💌 |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when it finds the nth occurrence of a bus pattern as shown below.

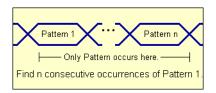


**To edit this** • Specifying Advanced Triggers (see page 163) **function** 

#### "N" consecutive samples with Pattern1

| Default Storage (overridden by sequence level store actions): |
|---|
| Step 1 ¥ N consecutive samples with Pattern1                  |
| Find 1 = + consecutive occurrence of                          |
| Sus/Signal ADDR All bits Equals Store Hext                    |
| Then 🗵 Trigger and fill memory 💌                              |
| 🗴 with 🛎 Bus/Signal 💌 ADDR 💌 All bits 💌 Equals 💌 🏷 📓 Hex 💌    |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when a bus pattern occurs a specified number times.



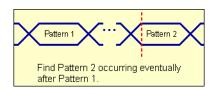
## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Pattern1 followed by Pattern2

| Default Storage (overridden by sequence level store actions):  |
|--|
| Step 1 *     Pattern1 followed by Pattern2       Find *     Bus/Signal       ADDR     All bits   Equals  |
| Followed eventually by 🕇 Bus/Signal 💌 ADDR 💌 All bits 💌 Equals 💌 XXXX 📱 Hex 💌  |
| Then     Trigger and fill memory       Image: with     Image: Bus/Signal       Image: With     Image: Bus/Signal       Image: Bus/Signal     Image: ADDR       Image: Bus/Signal     Image: ADDR |

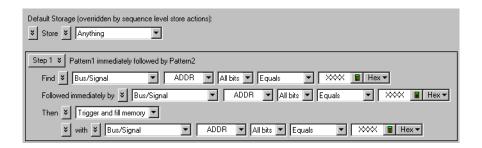
This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when pattern2 occurs eventually after pattern 1.

#### 12 Reference

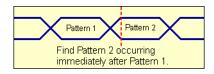


#### **To edit this function** • Specifying Advanced Triggers (see page 163)

#### Pattern1 immediately followed by Pattern2



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when pattern 2 is found immediately after exiting pattern 1.

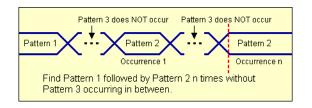


**To edit this** • Specifying Advanced Triggers (see page 163) function

#### Pattern1 followed by Pattern2 before Pattern3

| Default Storage (overridden by sequence level store actions):   |
|---|
| Step 1 × Pattern1 followed by Pattern2 before Pattern3          |
| Find 🔻 Bus/Signal 💌 ADDR 💌 All bits 💌 Equals 💌 XXXX 🗮 Hex 💌     |
| Followed by 👻 Bus/Signal 💌 ADDR 🔍 All bits 💌 Equals 💌 💥 🔛 Hex 💌 |
| Occurring 1 I - + time  |
| Before 🕏 Bus/Signal 💌 ADDR 💌 All bits 💌 Equals 🔍 XXXX 📕 Hex 💌   |
| Then 👻 Trigger and fill memory 💌                                |
| 🗴 with 🛎 Bus/Signal 💌 ADDR 💌 All bits 🔍 Equals 🔍 💥 📕 Hex 💌      |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when pattern2 occurs eventually after pattern1, for a specified number of times, without pattern3 occurring in between.



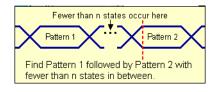
#### To edit this function

• Specifying Advanced Triggers (see page 163)

#### Too few states between Pattern1 and Pattern2

| Default Storage (overridden by sequence level store actions):<br>Store Bus/Signal My Bus 1 All bits Equals My Hex V        |
|--|
| Step 1 *     Too few states between Pattern1 and Pattern2       Find *     Bus/Signal       My Bus 1     All bits   Equals |
| Followed by 👻 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 📓 Hex 💌  |
| Then V Trigger and fill memory V<br>V with V Bus/Signal V My Bus 1 V All bits V Equals V X H Hex V                         |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when pattern1 is followed by pattern2 with fewer than "N" specified states in between.

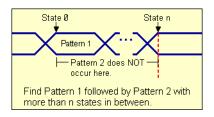


## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### **Too many states between Pattern1 and Pattern2**

| Default Storage (overridden by sequence level store actions):    |
|--|
| 🛿 Store 👻 Bus/Signal 🔍 My Bus 1 💌 All bits 💌 Equals 💌 💥 📓 Hex 💌  |
|  |
| Step 1 ¥ Too many states between Pattern1 and Pattern2           |
| Find 1 🔳 - + state   |
| After 🎽 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 📓 Hex 💌    |
| In which 👻 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 📕 Hex 💌 |
| Does not occur   |
| Then 🗧 Trigger and fill memory 💌                                 |
| 🗴 with 💐 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 📕 Hex 💌   |

This trigger function is available when the acquisition mode is set to **State** - Synchronous. It will trigger the logic analyzer when pattern1 is followed by pattern2 with more than "N" specified states in between.

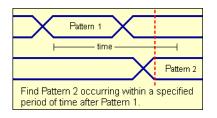


To edit this • Specifying Advanced Triggers (see page 163) function

#### Pattern2 occurring too soon after Pattern1

| Default Storage (overridden by sequence level store actions):<br>Store S Bus/Signal My Bus 1 All bits Equals My Bus 1 |
|---|
| Step 1 ¥ Pattern2 occurring too soon after Pattern1   |
| Find 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌  |
| Followed by 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌   |
| Occurring within 100 ns 🔳 - +   |
| Use timer 1 💌   |
| Then 🗧 Trigger and fill memory 💌  |
| 🗴 with 💐 Bus/Signal 🔍 My Bus 1 🔍 All bits 💌 Equals 🔍 🗮 Hex 💌  |

This trigger function is available when the acquisition mode is set to **State** - Synchronous. It will trigger the logic analyzer when pattern2 occurs within a specified time period after pattern1.

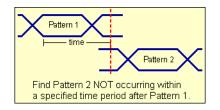


## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Pattern2 occurring too late after Pattern1

| Default Storage (overridden by sequence level store actions):   |
|---|
| 👻 Store 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 🖩 Hex 💌 |
|   |
| Step 1 ¥ Pattern2 occurring too late after Pattern1             |
| Find a time period of 100 ns 📓 - +                              |
| after 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🕅 Hex 💌     |
| in which 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔛 Hex 💌  |
| does not occur  |
| Use timer 1 💌   |
| Then 👻 Trigger and fill memory 💌                                |
| 🗴 with 💐 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌    |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when pattern2 does not occur within a specified time period after pattern1.

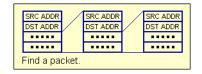


## **To edit this** • Specifying Advanced Triggers (see page 163) **function**

#### Find a packet

| Default Storage         Overridden by store actions in individual trigger steps:         Image: Store Im |
|---|
| Step 1 > Find a packet  |
| On bus Select a bus   |
| If Select a packet occurs once 💌  |
| Then 🗧 Trigger and fill memory 💌  |
| 😻 with 🛎 Default Storage 👻  |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when the selected packet and occurrence is found.



#### To edit this function

• Specifying Advanced Triggers (see page 163)

**Reset and start timer (state)** 



#### NOTE

This trigger function is not available in the 1683A/AD and 1693A/AD models because they do not have timers available.

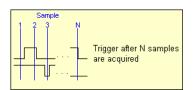
This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. This trigger function resets a timer, then starts the timer for a specified period of time. This trigger function requires that the timer value be set in either the same trigger step, or another trigger step that follows. When the timer stops, the analyzer triggers. For more information refer to "To configure a timer (see page 165)".



#### • Specifying Advanced Triggers (see page 163) function Find anything "N" times (state)



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. It will trigger the logic analyzer when any data (Anything) is seen for the Nth time. It is commonly used to create an immediate trigger, or a trigger after a user-defined delay.



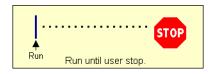
## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Run until user stop (state)



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. This trigger function sets up to never trigger. You must select the stop button to view the captured data.

#### 12 Reference

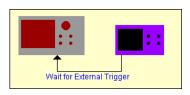


**To edit this** • Specifying Advanced Triggers (see page 163) function

#### Wait for external arm (state)



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers when an external arming signal appears through the external **Trigger In** port (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)). The **Trigger In** BNC connector is located on the rear panel of the 16800-series logic analyzers, 1680-series logic analyzers, and 16900-series logic analyzers.



To edit this<br/>function• Specifying Advanced Triggers (see page 163)Wait for arm from another module (state)

| Step 1 🛛 Wait for arm from another module |
|---|
| × Arm in from 💌 1691D - 2 💌               |
| Then 🗧 Trigger and fill memory            |
| ♥ with ♥ Default Storage ▼                |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers when an arming signal from another module occurs (see Triggering From, and Sending Triggers To, Other Modules/Instruments (see page 193)).

| Wait for another<br>module to Trigger |
|---------------------------------------|
|                                       |

## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Wait "N" external clock states



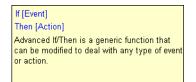
This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers on the "Nth" occurrence of the external clock signal (plus any user-defined clock qualification) from the device under test.

|   | Cloc   | k 1 Clo  |              | Cloo  |     |
|---|--------|----------|--------------|-------|-----|
| R | un     |          |              | Trig  | ger |
|   | Wait i | n exterr | hal clock st | tates |     |

# To edit this function • Specifying Advanced Triggers (see page 163) Advanced If/Then (state)

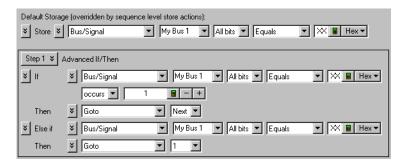
| Default Storage (ov<br>Store S Bu | verridden by sequence level store actions):<br>s/Signal V My Bus 1 V All bits V Equals V M Hex V |
|-----------------------------------|--|
|                                   | nced If/Then       Bus/Signal     My Bus 1     All bits     Equals     W     Hex                 |
|                                   |  |
|                                   | Trigger and fill memory 💌<br>with 💌 Bus/Signal 🔹 My Bus 1 💌 All bits 💌 Equals 🔍 💥 📓 Hex 💌        |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers when the "If" clause becomes true.

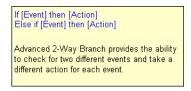


## **To edit this** • Specifying Advanced Triggers (see page 163) function

#### Advanced 2-Way Branch (state)



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The two-way branch is evaluated true when either of two patterns (if or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.

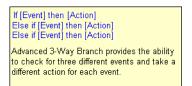


**To edit this** • Specifying Advanced Triggers (see page 163) **function** 

### Advanced 3-Way Branch (state)

| Default Stora | ge (overridden by seque | ence level store actions):                 |
|---------------|-------------------------|--|
| ¥ Store ¥     | Bus/Signal              | 💌 My Bus 1 💌 All bits 💌 Equals 💌 🔀 🖩 Hex 💌 |
|               |                         |  |
| Step 1 🛛      | Advanced If/Then        |  |
| × If          | Bus/Signal              | V My Bus 1 V All bits V Equals V Hex V     |
|               | occurs 💌                | 1 📓 - +                                    |
| Then          | ¥ Goto                  | Vext                                       |
| ➤ Else if     | ➤ Bus/Signal            | My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌     |
| Then          | × Goto                  |  |
| ▼ Else if     | ➤ Bus/Signal            | My Bus 1 V All bits V Equals V Hex V       |
| Then          | ¥ Goto                  |  |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The three-way branch is evaluated true when either of three patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.

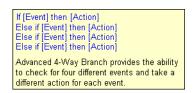


## **To edit this function** • Specifying Advanced Triggers (see page 163)

|           | ge (overridden by sequence level store actions):<br>Bus/Signal My Bus 1 All bits Equals My Bus 1 |
|-----------|--|
| Step 1 ¥  | Advanced If/Then   |
| × If      | 🗴 Bus/Signal 🔹 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌  |
|           | occurs 💌 1 📓 - +   |
| Then      | Soto Next  |
| Else if   | 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 🔍 🗮 Hex 💌  |
| Then      | Soto   |
| Else if   | 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 🔍 🗮 Hex 💌  |
| Then      | Soto I   |
| ¥ Else if | 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌  |
| Then      | Soto I I   |

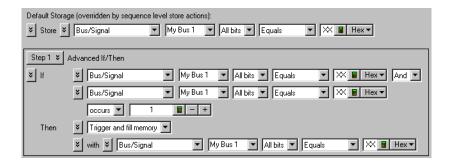
Advanced 4-Way Branch (state)

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The four-way branch is evaluated true when either of four patterns (If or Else if) are found. Depending on which pattern is found true, the appropriate "Then" action is executed.

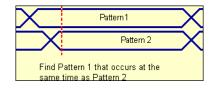


## **To edit this** • Specifying Advanced Triggers (see page 163) **function**

#### Pattern "AND" Pattern (state)



This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers when both pattern1 "AND" pattern2 occur at the same time, and for the specified numbers of samples (occurs).



## **To edit this** • Specifying Advanced Triggers (see page 163) **function**

## Pattern "OR" Pattern (state)

|          | ge (overridden by sequence level store actions):<br>Bus/Signal V My Bus 1 V All bits V Equals V Hex V |
|----------|---|
| Step 1 ¥ | Advanced If/Then  |
| × If     | Sus/Signal My Bus 1 All bits V Equals V Hex Or V  |
|          | 🗴 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 💥 🖩 Hex 💌   |
|          | occurs 💌 1 📓 - +  |
| Then     | Trigger and fill memory   |
|          | 🛎 with 🛎 Bus/Signal 💌 My Bus 1 💌 All bits 💌 Equals 💌 🗮 Hex 💌  |

This trigger function is available when the acquisition mode is set to **State** - **Synchronous**. The analyzer triggers when either pattern1 "OR" pattern2 occurs for the specified numbers of samples (occurs).



**To edit this** • Specifying Advanced Triggers (see page 163) **function** 

## **Data Formats**

| <b>Configuration File</b> • ALA Format (see page 588) |   |  |
|---|---|--|
| Formats   | • "XML Format" (in the online help)         |  |
| Data  | • Standard CSV Format (see page 588)        |  |
| Export/Import<br>Formats                              | • Module CSV Format (see page 589)          |  |
| i unnats  | • Module Binary (ALB) Format (see page 598) |  |

### **ALA Format**

The Agilent Logic Analyzer (ALA) format is the default format for saving configuration files. The ALA format is proprietary; ALA format configuration files are not intended to be read by programs other than the *Agilent Logic Analyzer* application.

ALA format configuration files contain everything that is needed to restore a session (in other words, the information necessary to reconstruct the display appearance, instrument settings, and optionally, captured data).

Configuration files are saved (see page 206) and opened (see page 220) through the File menu (see page 453).

### **Standard CSV Format**

You can export captured data to CSV (Comma-Separated Values) format files which can then be imported by other applications like Excel.

Output is standard CSV format where the first row is the headings for the columns you have chosen to export (for example, buses/signal names, sample number, or time), and each successive row contains data for those columns, in the range specified, separated by commas (or other specified separation characters). For example:

```
"Sample Number", "My Bus 1", "My Signal 1", "Time"
-10,FE,1,-13 ns
-9,FE,1,-10.5 ns
-8,FE,1,-8 ns
-7,FE,1,-5.5 ns
-6,FE,1,-3 ns
-5,FE,1,-500 ps
-4,FE,1,2 ns
-3,FE,1,4.5 ns
-2,FE,1,7 ns
-1,FE,1,9.5 ns
0,FF,1,12 ns
1,FF,1,14.5 ns
2,FF,1,17 ns
3,FF,1,19.5 ns
4,FF,1,22 ns
```

5,FF,1,24.5 ns 6,FF,1,27 ns 7,FF,1,29.5 ns 8,FF,1,32 ns 9,FF,1,34.5 ns 10,FF,1,37 ns

### **Module CSV Format**

You can export captured data to module CSV (Comma-Separated Values) format files which can then be post-processed and re-imported into the logic analysis system using a *data import module*.

#### CAUTION

Do not modify module CSV files with Microsoft Excel. When it saves the file, Excel will change the CSV format so that the data cannot be re-imported into the logic analysis system without a lot of manual text editing.

Module CSV format files contain a header section (see page 590) followed by comma separated values. For example:

```
AGILENT CSV DATA
         HEADER BEGIN
         #
         # ------
         # Created: Dec 5, 2005 15:38:38
         # By: Agilent Logic Analyzer
         # _____
         #
         VALUE SEPARATOR=","
         VALUE FILL IN=ZEROS # ZEROS, ONES, PREVIOUS, or ERROR
         TRIGGER CORRELATION OFFSET=0.00000000000000000e+000
         TRIGGER ROW=524288
         NUM ROWS=1048576
         TIME SOURCE PERIOD=2.000000000000000e-009
         COLUMN "Sample Number" SAMPLE NUMBER INTEGER
         COLUMN "My Bus 1" VALUE UNSIGNED INTEGER HEX WIDTH BITS=8
         COLUMN "My Bus 2" VALUE UNSIGNED INTEGER HEX WIDTH BITS=16
         COLUMN "My Bus 3" VALUE UNSIGNED INTEGER HEX WIDTH BITS=32
         COLUMN "My Signal 1" VALUE UNSIGNED_INTEGER HEX WIDTH_BITS=1
         COLUMN "My Signal 2" VALUE UNSIGNED INTEGER HEX WIDTH BITS=1
         COLUMN "Time" TIME FLOAT EXPONENT=-12 ABSOLUTE
         HEADER END
         -524288,53,FFF0,004103E7,1,1,-1048576000
         -524287,53,FFF0,004103E7,1,1,-1048574000
         -524286,53,FFF0,004103E7,1,1,-1048572000
         -524285,53,FFF0,004103E7,1,1,-1048570000
See Also
         • Module CSV and Module Binary File Header Format (see page 590)
```

#### Module CSV and Module Binary File Header Format

The header section comes at the beginning of the module CSV or module binary (ALB) file. The header definition is slightly different in the two cases.

AGILENT\_CSV\_DATA AGILENT\_BINARY\_DATA

*REQUIRED*: Key word tag to confirm the file type. The first is for module CSV text files. The second is for module binary (ALB) files. This tag must be the first characters 16 (or 19) characters in the file.

#

*OPTIONAL*: Comment character. All text following a # is ignored to the end of the line. Any line (except the first) may be a comment, except in module binary (ALB) files, where comments are only allowed in the header.

#### HEADER BEGIN

REQUIRED: Key word tag to delimit the beginning of the header.

TABLE BEGIN "<name>" <TableType>

A table represents data sampled at a specified timebase and sampling depth. A table can only represent a single timebase and sample depth.

*OPTIONAL*: If only one timebase and sample depth is needed, this keyword is not needed.

*REQUIRED*: If multiple timebases and sampling depths are needed, this keyword is needed to delimit the beginning of a table. The name may contain most printable characters, including embedded quote marks single or double), provided they are escaped with a backslash. For example, TABLE BEGIN "my \"perfect\" table" . . .

Generally, each analog waveform channel has its own table, and there is only one table for digital channels.

When multiple tables are used, the binary data associated with each table is concatenated after the header.

<TableType>:

- ANALOG
- DIGITAL

An identifier is needed to explicitly determine what the table contains. There are specific fields that are required depending on the type of table. Analog requires the X/Y INC/ORG/REF.

TIME\_SOURCE PERIOD = <n.nnne-nn>

TIME SOURCE FREQUENCY = <n.nnne+nn>

TIME SOURCE COLUMN = "<columnName>"

*OPTIONAL*: How to assign a time tag to each sample row. PERIOD gives the sampling period; FREQUENCY gives the sample rate. COLUMN indicates which time column contains the time tags to use (ignored if PERIOD or FREQUENCY is given).

TRIGGER ROW = <nnnn>

*OPTIONAL*: Row number containing the trigger sample, relative to the first data row in the file, which is row 0. The trigger row may be outside the range of rows in a file with a time line defined by a period or frequency, in which case it will be negative (trigger occurred before the first data row) or positive and greater than or equal to the number of data rows in the file (trigger occurred after the last data row in the file).

TRIGGER\_CORRELATION\_OFFSET = <n.nnne-nn>

*OPTIONAL*: Time offset in seconds (positive or negative) to apply to trigger (that is, to the T=0 reference) when correlating with data from other modules. If not given, 0.0 is assumed. The offset is rounded to the nearest picosecond.

NUM\_ROWS = <nnn>

*REQUIRED*: If TABLE\_BEGIN is present. Indicates the total number of data rows that will be read in from the file.

*OPTIONAL*: The expected number of data rows in the file. A warning is given if the number given does not match the actual number of rows in the file. This is provided as an optional sanity check to detect file truncation.

X\_INC = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

X ORG = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

X REF = <nnn>

OPTIONAL: Used for oscilloscope data processing.

Y INC = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

Y ORG = <nnn.nnn>

OPTIONAL: Used for oscilloscope data processing.

 $Y REF = \langle nnn \rangle$ 

OPTIONAL: Used for oscilloscope data processing.

Y\_MIN = <nnn.nnn>

*OPTIONAL*: Used for oscilloscope data processing--the minimum voltage value represented in the data.

Y\_MAX = <nnn.nnn>

*OPTIONAL*: Used for oscilloscope data processing--the maximum voltage value represented in the data.

VALUE SEPARATOR = "<ccc>"

*OPTIONAL, Module CSV only*: One or more characters to be used as the separation character(s) between values in each row. If not given, the comma character is used. If the value for a column is missing (for example, two consecutive commas), its value is determined by the VALUE\_FILL\_IN property. The separation string may contain any printable character, and/or the blank and tab characters, except the following ambiguous characters:

- '#' the comment character.
- '-', '+' sign characters (signed decimal, also known as two's complement, and floats).
- '.' the period, used in floating point.
- a-f, A-F hex.
- 0-9 digits.

VALUE\_FILL\_IN = PREVIOUS | ZEROS | ONES | ERROR

*OPTIONAL, Module CSV only*: The value to be used for a skipped cell in a row. This attribute is optional. The default is ZEROS. PREVIOUS is consistent with the VCD file format and means "use the value from the

cell above". ERROR indicates that any missing value should be treated as an error. This setting applies to all columns except TIME. Any missing time tag is an error.

BYTE ORDER = LITTLE ENDIAN | BIG ENDIAN

*OPTIONAL, Module binary (ALB) only*: The order of bytes in a multi-byte value. An Intel-compatible system uses little endian as its internal format. This applies to both integer and floating point values. The default is LITTLE ENDIAN.

```
LABEL "<name>" CHANNELS = "<ChannelDescription>" [HEX |
DECIMAL | OCTAL | BINARY | SYMBOL]
```

*OPTIONAL*: As described below, a COLUMN represents a pod. If there are no LABELs defined, a LABEL is created by default which has the same characteristics as the COLUMN. If a LABEL is defined, it represents a subset of the data defined by the COLUMN. Another way to look at it is that a COLUMN defines the physical data that was exported and a LABEL is an interpretation of the data. The "<name>" may contain most printable characters, including embedded quote marks (single or double), provided they are escaped with a backslash. For example, LABEL "my \"perfect\" label". It is required that LABEL names be unique. If a duplicated name is found, only the first instance of the LABEL definition will be processed. There is an optional base which, if specified, will be the default label base. The default is HEX.

<ChannelDescription>

A channel description consists of the following format: <COLUMN\_NAME>[bit position] with multiple channel descriptions separated by a comma. A <COLUMN\_NAME> corresponds to the COLUMN name attribute. If there are multiple COLUMNs by the same name, the first one will be used. The bit position list is enclosed in [] and is order dependent. The MSB is on the left-hand side and the LSB is on the right-hand side For example, [7:0] represents bits 0-7 and [7,4,3,1] represents individual bits. 1, 3, 4, and 7. Bit patterns that are not monotonically increasing from right to left are considered reordered. For example, [1,3,4,7] represents bits 7 as the LSB and bit 1 as the MSB.

```
SYMBOL "<name>" LABEL = "<label or column name>" VALUE =
    "<value> | <value..value>" [HEX | DECIMAL | OCTAL |
    BINARY]
```

TABLE END

REQUIRED: If TABLE BEGIN is used.

HEADER\_END

*REQUIRED*: The explicit end of the header. Information obtained from the header is evaluated at this point to determine if the file makes sense (for example, that a time base and one or more columns were defined).

Each line of a module CSV file (including sample rows following the header) are processed by first stripping the comment character and all characters following it, and then removing all leading whitespace (except blanks or tabs if a blank or tab is part of the delimiter string). If the resulting line is then empty, it is silently skipped. Otherwise, each data row is parsed using the definitions provided by the COLUMN definitions in the header, defined below.

**COLUMN Syntax** One or more COLUMN definitions are required. The order of definitions in the header corresponds to the order of the columns in the data section. At least one of these must define a VALUE column. COLUMN syntax is more complicated than the other statements, so it is given in pieces:

COLUMN "<name>" <CSVcolumnType> | <ALBcolumnType>

These are the major parts of a COLUMN definition. The details are different for module CSV versus module binary (ALB) files. The name may contain most printable characters, including embedded quote marks (single or double), provided they are escaped with a backslash. For example, COLUMN "my \"perfect\" data" . . .

<CSVcolumnType>:

- VALUE <CSVformat> WIDTH BITS = <nnn>
- TIME <CSVformat> <timeUnit> ABSOLUTE | RELATIVE
- LINE NUMBER <CSVformat>
- SAMPLE\_NUMBER <CSVformat>
- IGNORE

The column type gives the purpose of the values in the column.

Line numbers begin at 0 on the first row and increase by 1 for each subsequent row.

Sample numbers begin at 0 on the trigger row, decreasing by one for each row above the trigger row and increasing by one for each row after it. Time columns give the time position for the sample. Absolute time positions are referenced to T=0 on the trigger row. Relative time positions give the amount of time elapsed from the arrival of the previous sample to the arrival of the sample on the row with the time tag.

Value columns contain data samples to be displayed in viewers in the application. The width in bits of a value is the width assigned to the pod which represents this column in the Bus/Signal setup page. Values are truncated (or expanded) to fit the width. Signed values are sign extended. Floating point values are converted to integers of the appropriate size (after applying the scale factor, if given).

<ALBcolumnType>:

- VALUE NBYTES = <nnn> <ALBformat> WIDTH BITS = <nnn>
- TIME NBYTES = <nnn> <ALBformat> <timeUnit> ABSOLUTE | RELATIVE
- LINE NUMBER NBYTES = <nnn> <ALBformat>
- SAMPLE NUMBER NBYTES = <nnn> <ALBformat>
- IGNORE NBYTES = <nnn>

This is the same as <CSVcolumnType>, with the addition of an NBYTES attribute that gives the number of bytes in the binary data that are assigned to the column.

<CSVformat>:

- INTEGER [HEX | DECIMAL | OCTAL | BINARY]
- UNSIGNED INTEGER [HEX | DECIMAL | OCTAL | BINARY]
- FLOAT [SCALE = <nnn.nnn>]

The column format describes the way the value is represented in the file. The base is optional, and defaults to hex if not given. SCALE is also optional, and defaults to 1.0; it allows the values in the column to be scaled before loading into the data import module. The final value loaded is the value in the column, multiplied by the scale factor, rounded to the nearest integer (except for time values, which are rounded to the nearest  $10^{-24}$  sec). All values are checked for overflow with respect to the field's WIDTH\_BITS. Line numbers and sample numbers are treated as 32-bit quantities.

<ALBformat>:

- INTEGER
- UNSIGNED INTEGER
- FLOAT [SCALE = <nnn.nnn>]

The same as <CSVformat>, except there is no numeric base. Floating point values must be in IEEE Standard 754, and so must be either four bytes or eight bytes wide.

<timeUnit>:

EXPONENT = <nnn>
EXPONENT = -<nnn>

The unit to apply to time tag values (in addition to the scale factor, if used with floating point values). For example, EXPONENT = -12 is equivalent to picosecond time ticks.

| Header Example | AGILENT CSV DATA  |
|----------------|---|
| -              | #   |
|                | # #   |
|                | # Created: 2008 Sep 21 21:18 #                              |
|                | # By: Agilent Logic Analyzer #                              |
|                | # #   |
|                | #   |
|                | HEADER BEGIN  |
|                | TIME COLUMN="tSample"                                       |
|                | TRIGGER_ROW=100   |
|                | TRIGGER_CORRELATION_OFFSET=1.24e-9                          |
|                | COLUMN "Sample" SAMPLE_NUMBER INTEGER DECIMAL               |
|                | COLUMN "Address" VALUE INTEGER HEX WIDTH_BITS=24            |
|                | COLUMN "Data" VALUE INTEGER HEX WIDTH_BITS=16               |
|                | COLUMN "Status" VALUE INTEGER BIN WIDTH_BITS=8              |
|                | COLUMN "DigRF" VALUE FLOAT SCALE=16.0e+3 WIDTH_BITS=16      |
|                | COLUMN "tSample" TIME INTEGER DECIMAL EXPONENT=-12 RELATIVE |
|                | VALUE_SEPARATOR ","   |
|                | VALUE_FILL_IN PREVIOUS                                      |
|                | HEADER END  |
|                | # Start data  |
|                | Oafc38,ff98,01000110,0.114,5000                             |
|                | 0afc3c,055a,,,2500  |
|                | # embedded comment  |
|                | Oafc38,ff98,01010001,0.116,2500                             |
|                |   |

#### **Module CSV Format File Characteristics**

The file must define a time line so that each sample can be associated with a time tag. To do this, a periodic rate, or a time column with absolute or relative time tags, is required (see the TIME\_SOURCE property in the file header). Time tags in the file are verified to be monotonically increasing. The specification of a periodic rate overrides the presence of time tag columns, if any.

The file must have one or more data value columns. Data value columns have the data to load. Other columns, such as line numbers, sample numbers, and time tags, annotate that data, but are not loaded as data.

Data rows in the file are indexed beginning with row 0 first, then 1, and so on. Row numbers are file-centric. They are not the same as the sample numbers in the module's listing. Sample numbers are always relative to the location of the trigger row, not the first row in the file.

The file header has a property, TRIGGER\_ROW, giving the row number, in the file, associated with logic analyzer trigger. The trigger row is defined as the time origin, and contains T=0.

In a multi-module logic analyzer, only one module's trigger is at T=0. All the others are offset by hardware delays associated with the propagation of the trigger signal from the originating module to the receiving modules. The time delay is indicated by the TRIGGER\_CORRELATION\_OFFSET property. This is the amount of time that must be added to the time of each sample in the file to correctly position each sample on a time line with samples from another module in the system. By including this property, a file containing data exported from a module can be imported into the same system and will be positioned (correlated) correctly with data from the other modules.

An interesting case arises if the trigger sample is not included in the export range. This can legitimately occur if the time source is periodic. In this case, the TRIGGER\_ROW value will indicate a row not in the file. For example, if the first data row in the file is the first sample after the trigger in the module, then TRIGGER\_ROW=-1. Conversely, if the trigger was the first sample after the last row in the exported data, TRIGGER\_ROW is equal to the number of rows in the file. If the trigger was two samples after the last row, TRIGGER\_ROW is the number of rows in the file plus one, and so on. With these adjustments, the export file can now be imported and positioned correctly relative to the original master trigger without misrepresenting the location of the trigger sample (which was not in the file). Sample numbers are handled in a similar manner, with sample 0 on the trigger row. If the trigger row is not in the file, sample 0 is not in the file either.

These statements about the contents of a module CSV file will always be true:

- The first data row in the file is row 0. The next is 1, then 2, and so on.
- The TRIGGER\_ROW is always relative to the first row in the file (row 0). The trigger row may or may not be in the file.
- The time associated with the TRIGGER\_ROW is always 0. The TRIGGER\_CORRELATION\_OFFSET property allows correct correlation to other data sets.

- The sample number on the TRIGGER\_ROW (if a sample number column is present) is always 0. Sample numbers increase by one for each row after the trigger row; they decrease by one for each row before the trigger. Sample numbers are not the same as row numbers.
- Line numbers, if exported to the file, always begin at 0 on row 0, then increase by one for each row thereafter: lineNumber = rowNumber.

Inconsistencies between a T=0 time tag, sample numbers and the TRIGGER ROW property are resolved in this order:

- 1 The data row containing an absolute time tag of 0 is the trigger row and sample numbers are re-aligned if necessary to begin at zero on that row.
- **2** If the time line is defined by a period or frequency, and a sample number column is given, then the data row with sample number 0 is the trigger row. (This may or may not be within the span of the file itself).
- **3** Finally, the TRIGGER\_ROW property is used. If time tags (relative or absolute) are used, the trigger row will be moved if it is not within the file.
- See Also Module CSV and Module Binary File Header Format (see page 590)

#### Module Binary (ALB) Format

You can export captured data to module binary files or import module binary files into the logic analysis system using a *data import module*.

Module binary format files contain a header section (see page 590) followed by binary data. For example:

```
AGILENT BINARY DATA
HEADER BEGIN
#
# Created: Dec 5, 2005 16:14:36
# By: Agilent Logic Analyzer
#
BYTE ORDER=LITTLE ENDIAN
TRIGGER CORRELATION OFFSET=0.0000000000000000e+000
TRIGGER ROW=524288
NUM ROWS=1048576
TIME SOURCE PERIOD=2.000000000000000000000
COLUMN "Sample Number" SAMPLE NUMBER NBYTES=4 INTEGER
COLUMN "My Bus 1" VALUE NBYTES=1 UNSIGNED INTEGER WIDTH BITS=8
COLUMN "My Bus 2" VALUE NBYTES=2 UNSIGNED INTEGER WIDTH BITS=16
COLUMN "My Bus 3" VALUE NBYTES=4 UNSIGNED INTEGER WIDTH BITS=32
COLUMN "My Signal 1" VALUE NBYTES=1 UNSIGNED INTEGER WIDTH BITS=1
COLUMN "My Signal 2" VALUE NBYTES=1 UNSIGNED INTEGER WIDTH BITS=1
COLUMN "Time" TIME NBYTES=8 FLOAT EXPONENT=-12 ABSOLUTE
```

HEADER\_END <binary data>

The binary data section of the file contains only binary data. Binary data is organized by rows, where there are a fixed number of columns within a row (the number of COLUMN definitions in the header) and a fixed number of bytes per column (1, 2, 4, 8, or 16 as specified by NBYTES in the COLUMN definition). This simplifies reading the data, because these sizes match the native C language sizes of char, short, long, and long long (\_\_int64). Values of 16 bytes contain 128 bits which is the widest bus supported in the logic analysis system. By restricting exported sizes to these values, an ALB file with no header and only one bus/signal becomes a simple dump of an array of integers.

**See Also** • Module CSV and Module Binary File Header Format (see page 590)

## **Object File Formats Supported by the Symbol Reader**

The logic analysis system can read symbol files in the following formats:

- OMF96
- OMFx86
- IEEE-695
- ELF/DWARF
- ELF/stabs
- TI COFF

For ELF/DWARF1, ELF/stabs, and ELF/stabs/Mdebug files, C++ symbols are demangled so that they can be displayed in the original C++ notation. To improve performance for these ELF symbol files, type information is not associated with variables. Hence, some variables (typically a few local static variables) may not have the proper size associated with them. They may show a size of 1 byte and not the correct size of 4 bytes or even more. All other information function ranges, line numbers, global variables and filenames will be accurate. These behaviors may be changed by editing the readers.ini (see page 143) file.

- **See Also** To load symbols from a file (see page 141)
  - To change symbol reader options (see page 143)
  - To create an ASCII symbol file (see page 143)

## General-Purpose ASCII (GPA) Symbol File Format

General-purpose ASCII (GPA) format files are loaded into a logic analyzer just like other object files.

If your compiler does not produce object files in a supported format, or if you want to define symbols that are not included in the object file, you can create an ASCII format symbol file.

Typically, ASCII format symbol files are created using text processing tools that convert the symbol table information from a compiler or linker map output file.

Different types of symbols are defined in different records in the GPA file. Record headers are enclosed in square brackets, for example, [USER]. For a summary of GPA file records and associated symbol definition syntax, refer to the General-Purpose ASCII (GPA) Record Format Summary (see page 602).

Each entry in the symbol file must consist of a symbol name followed by an address or address range.

The address or address range must be a hexadecimal number. It must appear on the same line as the symbol name, and it must be separated from the symbol name by one or more blank spaces or tabs. Address ranges must be in the following format:

beginning address..ending address

The following example defines two symbols that correspond to address ranges and one symbol that corresponds to a single address.

main 00001000..00001009
test 00001010..0000101F
var1 00001E22 #this is a variable

For more detailed descriptions of GPA file records and associated symbol definition syntax, refer to the following topics:

- SECTIONS (see page 603)
- FUNCTIONS (see page 604)
- USER (see page 604)
- VARIABLES (see page 605)
- SOURCE LINES (see page 606)
- START ADDRESS (see page 606)
- Comments (see page 606)

## **General-Purpose ASCII (GPA) Record Format Summary**

Format [SECTIONS (see page 603)] section\_name start..end attribute [FUNCTIONS (see page 604)] func name start..end [USER (see page 604)] sym\_name value base sym\_name start\_value [size] base sym\_name start\_value..end\_value base [VARIABLES (see page 605)] var\_name start [size] var\_name start..end [SOURCE LINES (see page 606)] File: file name line# address [START ADDRESS (see page 606)] address #comment text (see page 606)

> Lines without a preceding header are assumed to be symbol definitions in one of the [USER] formats.

**Example** This is an example GPA file that contains several different kinds of records.

| [SECTION | 5]         |                |                                 |   |
|----------|------------|----------------|---------------------------------|---|
| proq     | 0000100000 | 00101F         |                                 |   |
| data     | 4000200040 | 009FFF         |                                 |   |
| common   | FFFF0000FF | 'FF1000        |                                 |   |
| [FUNCTIO | NS]        |                |                                 |   |
| main     | 0000100000 | 001009         |                                 |   |
| test     | 0000101000 | 00101F         |                                 |   |
| [USER]   |            |                |                                 |   |
| bdontcar | e 00x1     | binary         |                                 |   |
| hvalue   | OOEF       | hex            |                                 |   |
| drange   | 099        | decimal        |                                 |   |
| srange   | -23 20     | signed decimal | # The 20 is a decimal value for | s |
| ize.     |            |                |                                 |   |
| [VARIABL | ES]        |                |                                 |   |
| total    | 40002000 4 |                |                                 |   |
| value    | 40008000 4 |                |                                 |   |
| [SOURCE  | LINES]     |                |                                 |   |
| File: ma | in.c       |                |                                 |   |
| 10       | 00001000   |                |                                 |   |
| 11       | 00001002   |                |                                 |   |

14 0000100A 22 0000101E File: test.c 5 00001010 7 00001012 11 0000101A

## SECTIONS

Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

NOTE

To enable section relocation, section definitions must appear before any other definitions in the file.

#### NOTE

If you use section definitions in a GPA symbol file, any subsequent function or variable definitions must be within the address ranges of one of the defined sections. Functions and variables that are not within the range are ignored.

#### Format [SECTIONS]

section\_name start..end attribute

| section_name | A symbol representing the name of the section.  |  |
|--------------|---|--|
| start        | The first address of the section, in hexadecimal.   |  |
| end          | The last address of the section, in hexadecimal.  |  |
| attribute    | <ul> <li>(optional) Attribute may be one of the following:</li> <li>NORMAL (default) - The section is a normal, relocatable section, such as code or data.</li> <li>NONRELOC - The section contains variables or code that cannot be relocated. In other words, this is an absolute segment.</li> <li>AddReloc reloc_offset - Lets you specify an offset value (up to 32-bit) for a relocated section.</li> <li>SetReloc reloc_value - Lets you specify a new base value (up to 32-bit) for a relocated section.</li> </ul> |  |

Example [SECTIONS]

| prog       | 0000100000001FFF |          |          |
|------------|------------------|----------|----------|
| data       | 0000200000003FFF |          |          |
| display_io | 000080000000801F | NONRELOC |          |
| sect3      | 0000300000003FFF | AddReloc | 1000     |
| sect4      | 0000500000005FFF | SetReloc | 0000F000 |
|            |                  |          |          |

## **FUNCTIONS**

Use FUNCTIONS to define symbols for program functions, procedures or subroutines.

Format [FUNCTIONS]

func\_name start..end

| func_name | A symbol representing the function name.           |
|-----------|--|
| start     | The first address of the function, in hexadecimal. |
| end       | The last address of the function, in hexadecimal.  |

```
Example [FUNCTIONS]
main 00001000..00001009
test 00001010..0000101F
```

## USER

Under the [USER] record header, you can create symbols with don't care values, and you can use value number bases other than hex.

USER is the default record type; this means symbols defined without any record header ([USER], [VARIABLE], etc.) are assumed to be USER symbols.

USER symbol definitions can have 128-bit values; symbol definitions in all other record types are limited to 32-bit values.

#### Format [USER]

sym\_namevaluebasesym\_namestart\_value[size]basesym\_namestart\_value..end\_valuebase

\* use quotes(") around names or values with spaces.

| sym_name    | A symbol name.   |
|-------------|--|
| value       | The value of the symbol.   |
| base        | The number base of the value(s); can be:<br>• binary<br>• octal<br>• hex (or hexadecimal or blank)<br>• decimal<br>• signed decimal (two's complement) |
| start_value | The low value of the range.  |

| end_value   |         | The high v | alue of the ra | nge.                                |
|-------------|---------|------------|----------------|-------------------------------------|
| size        |         | The size o | f the range of | values, in decimal.                 |
|             |         |            |                |                                     |
| [USER]      |         |            |                |                                     |
| bdontcare   | 00x1    |            | binary         |                                     |
| bvalue      | 0011    |            | binary         |                                     |
| brange      | 0000.   | .0011      | binary         |                                     |
| brange2     | 0011    | 9          | binary         | # The 9 is a decimal value for size |
|             |         |            | _              |                                     |
| odontcare   | 00x7    |            | octal          |                                     |
| ovalue      | 0077    |            | octal          |                                     |
| orange      | 0000.   | .0077      | octal          |                                     |
| orange2     | 0000    | 99         | octal          | # The 99 is a decimal value for siz |
| е.          |         |            |                |                                     |
| hdontcare   | 00xF    |            | hex            |                                     |
| hvalue      | OOEF    |            | hex            |                                     |
| hrange      | 0000.   | .00FF      | hex            |                                     |
| hrange3     | 0000    | 99         | hex            | # The 99 is a decimal value for siz |
| e.          |         |            |                |                                     |
| dvalue      | 1090    |            | decimal        |                                     |
| drange      | 099     |            | decimal        |                                     |
| drange2     | 0 1     | 00         | decimal        | # The 100 is a decimal value for    |
| size.       |         |            |                |                                     |
| svalue      | -23     |            | signed d       | lecimal                             |
| srange      | -23     | 5          | signed d       | lecimal                             |
| srange      | -23 2   | 0          | signed d       | lecimal # The 20 is a decimal value |
| for size.   |         |            |                |                                     |
| "hvalue wit | h space | " "01XX    | FFFF" hex      |                                     |
| "hrange wit | h space | " "0100    | FFFF""04       | 00 FFFF" hex # Applies to other bas |
| es also.    |         |            |                |                                     |

## VARIABLES

**Example** 

You can specify symbols for variables using:

- The address of the variable.
- The address and the size of the variable.
- The range of addresses occupied by the variable.

If you specify only the address of a variable, the size is assumed to be 1 byte.

```
Format [VARIABLES]
```

var\_name start [size]
var\_name start..end

| var_name | A symbol representing the variable name.           |
|----------|--|
| start    | The first address of the variable, in hexadecimal. |

#### 12 Reference

| end  | The last address of the variable, in hexadecimal.          |
|------|--|
| size | (optional) The size of the variable, in bytes, in decimal. |

**Example** [VARIABLES]

| subtotal    | 40002000  | 4         |
|-------------|-----------|-----------|
| total       | 40002004  | 4         |
| data_array  | 40003000. | .4000302F |
| status_char | 40002345  |           |

## **SOURCE LINES**

Use SOURCE LINES to associate addresses with lines in your source files.

Format [SOURCE LINES]

File: file\_name line# address

| file_name | The name of a file.                             |
|-----------|---|
| line#     | The number of a line in the file, in decimal.   |
| address   | The address of the source line, in hexadecimal. |

| Example | [SOURCE LINES] |          |
|---------|----------------|----------|
|         | File: ma       | ain.c    |
|         | 10             | 00001000 |
|         | 11             | 00001002 |
|         | 14             | 0000100A |
|         | 22             | 0000101E |

**See Also** • Viewing Source Code Associated with Captured Data (see page 308)

### **START ADDRESS**

Format [START ADDRESS] address

| address | The address of the program entry point, in hexadecimal. |
|---------|---|
|---------|---|

Example [START ADDRESS] 00001000

### Comments

Use the # character to include comments in a file. Any text following the # character is ignored. You can put comments on a line alone or on the same line following a symbol entry.

Format #comment text

**Example** #This is a comment

#### 12 Reference

## **Product Overviews**

- 1680/1690-Series Logic Analyzer Product Overview (see page 608)
- 16800-Series Logic Analyzer Product Overview (see page 614)
- 16900-Series Logic Analysis System Product Overview (see page 617)
- U4154A Logic Analyzer Product Overview (see page 626)
- 16850-Series Logic Analyzer Product Overview (see page 628)
- Agilent Logic and Protocol Analyzer Application Product Overview (see page 631)
- See Also Tutorial Getting to know your logic analyzer (see page 60)

### 1680/1690-Series Logic Analyzer Product Overview

The Agilent Technologies 1680/1690-series logic analyzers provide a variety of channel widths, memory depths, and state and timing acquisition speeds (see tables below).

• The 1680A/AD-series comes with a large integrated 12.1-inch color flat panel display which can show up to 22 waveforms on screen simultaneously.



• The 1690A/AD-series is a PC-hosted model which connects to a personal computer via an IEEE 1394 interface; this lets you carry out measurement and debug work in your own PC environment. (One 1690-series logic analyzer per PC is supported.)



Both model series have the familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 408).

- 1680-Series Front Panel Operation (see page 609)
- 1680-Series Display Brightness (see page 614)

Supplied1680A/AD-series logic analyzers:AccessoriesPS/2 mouse.

- PS/2 mini keyboard.
  - Front panel cover.
  - Accessory pouch.

1690A/AD-series logic analyzers:

- IEEE 1394 PCI card and cable.
- Laptop IEEE 1394 cable.
- Accessory pouch.

**Optional** • Rack Mount Kit - Option 1CM.

- Accessories Additional IEEE 1394 PCI card and cable.
  - See Also
- Tutorial Getting to know your logic analyzer (see page 60)
  - 1680/1690-Series Logic Analyzer Characteristics (see page 715)
  - 1680/1690-Series Logic Analyzer Specifications (see page 715)

#### **1680-Series Front Panel Operation**

The front panel interface consists of knobs and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

# **NOTE** When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 610)
- Open/Save/Default Setup Buttons (see page 610)
- General Purpose Knob (see page 611)
- Alphanumeric Keypad (see page 611)
- Shortcut Buttons (see page 611)
- Vertical Knobs (see page 612)
- Horizontal Knobs (see page 613)
- Marker Knob/Button (see page 613)

#### Run/Stop Buttons



| ltem                  | Description  |
|-----------------------|--|
| Run Single            | Runs a single acquisition (see page 203). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.                    |
| Run Rep. (Repetitive) | Runs a repetitive acquisition (see page 203). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out. |
| Stop                  | Stops (see page 203) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.   |

Open/save/Defa ult Setup Buttons



| ltem          | Description  |
|---------------|--|
| Open Setup    | Accesses the Open Configuration (see page 220) dialog. |
| Save Setup    | Accesses the Save Configuration (see page 206) dialog. |
| Default Setup | Resets setup to the default power up configuration.    |

General Purpose Knob



Ent

The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

Alphanumeric Keypad

| ter | Tab Esc | Don't<br>Care |
|-----|---------|---------------|
|     | DEF     | Meg           |
|     | A B C   | kilo          |
|     | 7 8 9   | milli         |

In OK/Cancel dialogs, the escape key acts as a cancel operation and exits the dialog.

| ltem                      | Description   |
|---------------------------|---|
| Enter                     | Accepts value or configuration change and exits dialog.       |
| Tab                       | Scrolls configuration fields left-to-right and top-to-bottom. |
| Backspace (left<br>arrow) | Backspaces cursor in an alphanumeric assignment field.        |
| Esc                       |   |
| Keypad                    | Used for alphanumeric entry.                                  |
| Units                     | Sets unit of measure.   |

**Shortcut Buttons** 

| - Shor   | tcuts    |
|----------|----------|
| Setup    | Trigger  |
| Waveform | File Mgr |
| Listing  | Print    |
| Find     | Help     |

| ltem     | Description   |
|----------|---|
| Setup    | Accesses the Buses/Signals (see page 499) tab in the Analyzer Setup dialog.                                   |
| Waveform | Accesses Waveform display (see page 476) window. When the Waveform display is active, the button turns green. |
| Listing  | Accesses Listing display (see page 482) window. When the Listing display is active, the button turns green.   |
| Find     | Accesses advanced search (see page 294) dialog.   |
| Trigger  | Accesses advanced trigger (see page 496) dialog.  |
| File Mgr | Accesses the Explore file manager dialog.   |
| Print    | Accesses the Printing Data dialog (see page 525).   |
| Help     | Accesses the online help system's main window. Same as F1 key.  |

#### **Vertical Knobs**



| ltem   | Description   |
|--------|---|
| Size   | Adjusts height of all waveform rows. The selection lights up green<br>indicating it's part of the waveform group, and that the waveform group<br>is currently active. |
| Page   | Scrolls a page at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.    |
| Scroll | Scrolls row at a time of Waveform data. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.    |
| Line   | Scrolls a line at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.    |

#### **Horizontal Knobs**



| ltem     | Description  |
|----------|--|
| Time/Div | Changes time/division (see page 240) scale of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active. |
| Bus/Sig  | Scrolls first column to last column in Listing Display. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.           |
| Delay    | Changes delay (see page 242) of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.               |
| Column   | Scrolls a column at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.                       |

# Marker/Knob Button



| ltem                 | Description   |
|----------------------|---|
| Move marker knob     | Moves selected marker in the display.   |
| Choose marker button | Selects marker for "Move" operation. Press button to scroll through available markers. If no markers are defined, pressing Choose will create an M1 marker. |

For more marker information, refer to Marking, and Measuring Between, Data Points (see page 271).

# **1680-Series Display Brightness**

Included with the 1680-series logic analyzers is a *display brightness* control.

You can double-click the  $\ge$  icon in the Windows taskbar to toggle between high and low brightness settings.

# 16800-Series Logic Analyzer Product Overview

The Agilent Technologies 16800-series logic analyzers are standalone benchtop logic analyzers that range from 34 to 204 logic acquisition channels and 48 pattern generator channels, depending on the model.

| Model      |
|------------|
| Comporioon |

Comparison

| Agilent<br>model<br>number<br>:           | 16801A | 16802A | 16803A | 16804A | 16806A | 16821A | 16822A | 16823A |
|---|--------|--------|--------|--------|--------|--------|--------|--------|
| Logic<br>acquisit<br>ion<br>channel<br>s: | 34     | 68     | 102    | 136    | 204    | 34     | 68     | 102    |
| Pattern<br>generat<br>or<br>channel<br>s: | 0      | 0      | 0      | 0      | 0      | 48     | 48     | 48     |

Features, Logic Acquisition

- 1 M to 32 M memory depth per channel (depending on memory option), software upgradeable.
- 250 MHz or 500 Mb/s maximum state data rate (depending on state speed option), software upgradeable. The 500 Mb/s maximum state data rate option is available on the 68-, 120-, 136-, and 204-channel logic analyzer models.
- 1 GHz, 64 M deep timing analysis on half channels.
- Automated threshold and sample position setup.
- 4 GHz timing zoom with 64 K memory depth.

Features, Mainframe

- Built-in 15 inch TFT color LCD display, 1,024 x 768 (XGA) resolution. Touch screen with Option 103. See Tips for Using the Touch Screen (see page 618).
  - Front panel knob and buttons. See 16800 Series Front Panel Operation (see page 616).
  - 80 GB hard disk drive (or external hard drive Option 109).

- 10/100 Base-T LAN port.
- USB 2.0 ports (six total, two on front, four on back).
- One PCI expansion slot.
- One PCI Express x1 expansion slot.
- Windows<sup>®</sup> XP Professional operating system. With the 05.20.0000 release of the Agilent Logic Analyzer application, 16800-series logic analyzers having serial number MY51420101 are shipped from the factory with Windows 7 operating system.
- *Agilent Logic Analyzer* application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 408).

# **CAUTION** When powering off the 16800-series logic analyzer, wait until the fans stop turning (about 15 seconds) before turning the logic analyzer back on. This ensures that internal circuitry restarts in a known state. (For more information on powering off the logic analyzer, see the "16800-Series Logic Analyzer Installation/Quick Start Guide".)

| Features, Pattern       | • 24 channels at 300 MHz clock; 48 channels at 180 MHz clock.   |
|-------------------------|---|
| Generator               | • Memory Depth: 16,777,216 vectors.   |
|                         | • Logic Level (data pods): TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL/PECL/LVPECL terminated, ECL unterminated, and differential ECL (without pod). |
|                         | • Data Inputs: 3-bit pattern level sensing (clock pod).   |
|                         | • Clock Output: Synchronized to output data, delay of 7 ns in 14 steps (clock pod).   |
|                         | • Clock Input: DC to 300 MHz (clock pod).   |
|                         | • Internal Clock Period: Programmable from 1 MHz to 300 MHz in 1 MHz steps.   |
|                         | • External Clock Period: DC to 300 MHz.   |
|                         | • External Clock Duty Cycle: 1.3 ns minimum high time.  |
| Supplied                | • PS/2 mouse.   |
| Accessories             | • PS/2 mini keyboard.   |
|                         | • Accessory pouch.  |
|                         | • Power cord.   |
| Optional<br>Accessories | • Probes.   |
| See Also                | • Tutorial - Getting to know your logic analyzer (see page 60)  |

• 16800-Series Logic Analyzer Specifications and Characteristics (see page 742)

# **16800-Series Front Panel Operation**

The front panel interface consists of a knob and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

# **NOTE** When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 616)
- General Purpose Knob (see page 616)
- Touch Off Button (see page 617)

# Run/Stop Buttons



| ltem                  | Description  |
|-----------------------|--|
| Run Single            | Runs a single acquisition (see page 203). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.                    |
| Run Rep. (Repetitive) | Runs a repetitive acquisition (see page 203). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out. |
| Stop                  | Stops (see page 203) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.   |

#### General Purpose Knob



The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

#### **Touch Off Button**



| ltem      | Description  |
|-----------|--|
| Touch Off | Turns off the touch screen so that accidental touches don't affect the instrument. |

**See Also** • Tips for Using the Touch Screen (see page 618)

# **16900-Series Logic Analysis System Product Overview**

The Agilent Technologies 16900-series logic analysis systems are modular systems with slots for logic analyzer and other types of measurement instrument cards.

| Agilent model<br>number | Numb<br>er of<br>slots | Multifr<br>ame<br>Pro | Display and resolution   | PCI expansion slots              |  |  |
|-------------------------|------------------------|-----------------------|--|----------------------------------|--|--|
| 16900A                  | 6                      | Yes                   | Uses external monitor. Supports up<br>to four external monitors at up to<br>1600 x 1200 (with PCI video card)  | 2 full profile, 1<br>low profile |  |  |
| 16901A                  | 2                      | Yes                   | Built-in color touch screen display,<br>15 inch at 1024 x 768, supports<br>external monitor (without additional<br>PCI video card)                     | 1 full profile                   |  |  |
| 16902A                  | 6                      | Yes                   | Built-in color touch screen display,<br>12.1 inch at 800 x 600, supports up to<br>four external monitors at up to 1600 x<br>1200 (with PCI video card) | 2 full profile, 1<br>low profile |  |  |
| 16902B                  | 6                      | Yes                   | Built-in color touch screen display,<br>15 inch at 1024 x 768, supports<br>external monitor (without additional<br>PCI video card)                     | 1 full profile                   |  |  |
| 16903A                  | 3                      | No                    | Built-in color touch screen display,<br>12.1 inch at 800 x 600, supports up to<br>four external monitors at up to 1600 x<br>1200 (with PCI video card) | 1 full profile, 1<br>low profile |  |  |

|             | <ul><li>All models have the familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 408).</li><li>Tips for Using the Touch Screen (see page 618)</li></ul>  |
|-------------|--|
|             | • 16901A/16902B Front Panel Operation (see page 620)   |
|             | • 16902A/16903A Front Panel Operation (see page 622)   |
| CAUTION     | When powering off the 16900-series logic analysis system, wait until the fans stop turning (about 15 seconds) before turning the logic analysis system back on. This ensures that internal circuitry restarts in a known state. (For more information on powering off the logic analysis system, see the<br><i>Logic System Installation Guide</i> ".) |
| Supplied    | • PS/2 mouse.  |
| Accessories | • PS/2 mini keyboard.  |
|             | Accessory pouch.   |
|             | • Power cord.  |
|             | • Ten-conductor flying-lead cable for the <i>target control port</i> (see page 83) (on 16900A, 16902A, 16902B, and 16903A models).   |
| Optional    | • Multiframe cable (E5861A).   |
| Accessories | <ul> <li>1 Gbit low-profile LAN card (option 014 or E5860A for 16900A,<br/>16902A, and 16903A models).</li> </ul>  |
|             | • Probes.  |
| See Also    | • Tutorial - Getting to know your logic analyzer (see page 60)   |
|             | <ul> <li>16900-Series Logic Analysis System Frame Characteristics (see<br/>page 774)</li> </ul>  |
|             | Tips for Using the Touch Screen  |
|             | The 16901A, 16902A, 16902B, and 16903A logic analysis system frames<br>and 16850-series and 16800-series logic analyzer frames with Option 103<br>have a touch screen. Here are some tips for using the touch screen:  |
|             | • Use firm, even pressure on the touch screen.   |
|             | • You may prefer to use a stylus.  |
|             | • Use the front panel marker knobs to place markers. Placing markers is  |

- Use the front panel marker knobs to place markers. Placing markers is hard to do accurately using the touch screen. (Any marker can be selected using the Marker **Choose** button.)
- For trees, the touchable area around the +/- buttons is expanded.
- For option selections, both the option and the caption are active.

To open a Inside the Agilent Logic Analyzer application:

keyboard dialog

• Press the I keyboard button in any edit field. This opens a dialog for entering field values.

| New Bus/Signal Name   |
|---|
| My Bus 2  |
| $\begin{array}{c c} & \ddots & 1 & @ & \# & \$ & \$ & \$ & \$ & \$ & \$ & \$ & \$ & \$$                         |
| $\begin{array}{c} \text{Shift} \\ z \\ x \\ c \\ v \\ b \\ n \\ m \\ , \\ , \\ , \\ , \\ , \\ , \\ \end{array}$ |
| Space <>  |
| OK Cancel   |

Outside the Agilent Logic Analyzer application:

• Press the front panel Keyboard button. This opens the Microsoft On-Screen Keyboard and the touch screen Event Selector.

| 0 🔤          | n-S      | Sci | reer | n Ke | eyb        | oar   | ď   |            |    |   |   |    |    |     |     |    |    |     |        |     |     |     |     |   |   | X   |
|--------------|----------|-----|------|------|------------|-------|-----|------------|----|---|---|----|----|-----|-----|----|----|-----|--------|-----|-----|-----|-----|---|---|-----|
| <u>F</u> ile | K        | ey  | boa  | rd   | <u>S</u> e | ettir | ngs | <u>H</u> e | lp |   |   |    |    |     |     |    |    |     |        |     |     |     |     |   |   |     |
| esc          |          |     | F1   | F2   | 2          | F3    | F4  |            | F5 | F | 6 | F7 |    | F8  |     | F9 | F1 | 0 F | 11 F12 | psc | slk | brk |     |   |   |     |
| •            | 1        | Ι   | 2    | 3    |            | 4     | 5   | 6          |    | 7 | 8 |    | 9  | 0   |     | -  | =  | Γ   | bksp   | ins | hm  | pup | nik | 1 | • | -   |
| tab          |          | q   |      | w    | е          | Г     | r I | t          | у  | Ī | 1 | i  | Γ  | 0   | Р   | Т  | 1  | 1   | ×      | del | end | pdn | 7   | 8 | 9 |     |
| loc          | <b>k</b> |     | а    | s    | I          | d     | f   | g          |    | h | j |    | k  | Т   | Τ   | :  | •  | Γ   | ent    |     |     |     | 4   | 5 | 6 | +   |
| s            | hft      |     | Z    | :    | x          | c     | ;   | v          | Ь  | n |   | m  | Ι. | . [ |     | 1  | ·  |     | hft    |     | 1   |     | 1   | 2 | 3 |     |
| ctrl         | I        | 2   | 7    | alt  |            |       |     |            |    |   |   |    |    |     | alt |    | 9  |     | ctrl   | +   | Ŧ   | →   | - ( | ) |   | ent |

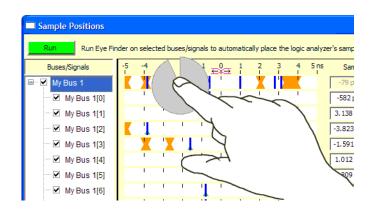
(You can also choose Start>All **Programs>Accessories>Accessibility>On-Screen Keyboard**.)

To access right Inside the Agilent Logic Analyzer application, most right mouse button mouse button behavior is accessible just by touching the screen.

Outside the Agilent Logic Analyzer application:

• Press down on the touch screen until a full circle is drawn around your finger; then, a right-click occurs.

behavior



• Or, you can choose **Start>All Programs>Agilent Logic Analyzer>Utilities>Touch Screen>Event Selector** to open the window:



Touching inside this window causes your next touch to act as a right-click.

To recalibrate the<br/>touch screen• If the touch screen needs to be recalibrated, choose Start>All<br/>Programs>Agilent Logic Analyzer>Utilities>Touch Screen>Calibrate.

- See Also
- 16800-Series Panel Operation (see page 616)
  - 16901A/16902B Front Panel Operation (see page 620)
- 16902A/16903A Front Panel Operation (see page 622)

### 16901A/16902B Front Panel Operation

The front panel interface consists of a knob and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

**NOTE** When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 621)
- General Purpose Knob (see page 621)

• Touch Off Button (see page 621)

Run/Stop Buttons



| ltem                  | Description  |
|-----------------------|--|
| Run Single            | Runs a single acquisition (see page 203). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.                    |
| Run Rep. (Repetitive) | Runs a repetitive acquisition (see page 203). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out. |
| Stop                  | Stops (see page 203) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.   |

#### General Purpose Knob



The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

# Touch Off Button



| ltem      | Description  |
|-----------|--|
| Touch Off | Turns off the touch screen so that accidental touches don't affect the instrument. |

See Also

• Tips for Using the Touch Screen (see page 618)

### 16902A/16903A Front Panel Operation

The front panel interface consists of a touch screen, knobs, and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used windows/dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

# NOTE

When multiple instances of the *Agilent Logic Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware. Likewise, in a multiframe configuration, the front panel knobs and buttons only work for the application running on the *master frame*.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons (see page 622)
- Open/Save/New File Buttons (see page 623)
- General Purpose Knob and Enter Button (see page 623)
- Shortcut Buttons (see page 623)
- Vertical Knobs (see page 624)
- Horizontal Knobs (see page 625)
- Marker Knob/Button (see page 625)
- Touch Off Button (see page 626)

#### Run/Stop Buttons



| ltem                  | Description  |
|-----------------------|--|
| Run Single            | Runs a single acquisition (see page 203). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.                    |
| Run Rep. (Repetitive) | Runs a repetitive acquisition (see page 203). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out. |
| Stop                  | Stops (see page 203) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.   |

# Open/Save/New File Buttons



| ltem      | Description  |
|-----------|--|
| Open File | Accesses the Open Configuration (see page 220) dialog. |
| Save File | Accesses the Save Configuration (see page 206) dialog. |
| New File  | Resets setup to the default power up configuration.    |

# General Purpose Knob and Enter Button



| ltem                 | Description   |
|----------------------|---|
| General purpose knob | The general purpose knob acts on the field that has the current focus.<br>Fields that have the current focus have the blue background. The general<br>purpose knob is typically used to increase/decrease numeric values<br>such as waveform scale and delay. |
| Enter button         | Accepts value or configuration change and exits dialog.   |

# **Shortcut Buttons**

| - Short        | cuts -   |
|----------------|----------|
| Waveform       | Setup    |
| Listing        | Trigger  |
| Scope          | Find     |
| Mixed          | Keyboard |
| Full<br>Screen | Help     |

| ltem     | Description   |
|----------|---|
| Waveform | Accesses Waveform display (see page 476) window. When the Waveform display is active, the button turns green. |

# 12 Reference

| Listing     | Accesses Listing display (see page 482) window. When the Listing display is active, the button turns green.   |
|-------------|---|
| Scope       | Runs the " <i>Add External Oscilloscope</i> wizard" (in the online help) for connecting an external Infiniium oscilloscope to the logic analyzer using the E5850A time correlation fixture. |
| Mixed       | Enables full screen display and tiles windows horizontally or disables the mixed window setup.  |
| Full Screen | Enables or disables full screen display.  |
| Setup       | Accesses the Buses/Signals (see page 499) tab in the Analyzer Setup dialog.   |
| Trigger     | Accesses advanced trigger (see page 496) dialog.  |
| Find        | Accesses advanced search (see page 294) dialog.   |
| Keyboard    | Opens a keyboard dialog for entering information.   |
| Help        | Accesses the online help system's main window. Same as F1 key.  |

# Vertical Knobs



| ltem   | Description   |
|--------|---|
| Size   | Adjusts height of all waveform rows. The selection lights up green<br>indicating it's part of the waveform group, and that the waveform group<br>is currently active. |
| Page   | Scrolls a page at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.    |
| Scroll | Scrolls row at a time of Waveform data. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.    |
| Line   | Scrolls a line at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.    |

#### **Horizontal Knobs**



| ltem     | Description  |
|----------|--|
| Time/Div | Changes time/division (see page 240) scale of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active. |
| Bus/Sig  | Scrolls first column to last column in Listing Display. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.           |
| Delay    | Changes delay (see page 242) of Waveform display. The selection lights up green indicating it's part of the waveform group, and that the waveform group is currently active.               |
| Column   | Scrolls a column at a time of Listing data. The selection lights up green indicating it's part of the listing group, and that the listing group is currently active.                       |

Marker Knob/Button



| ltem                 | Description   |
|----------------------|---|
| Move marker knob     | Moves selected marker in the display.   |
| Choose marker button | Selects marker for "Move" operation. Press button to scroll through available markers. If no markers are defined, pressing Choose will create an M1 marker. |

For more marker information, refer to Marking, and Measuring Between, Data Points (see page 271).

### 12 Reference

#### **Touch Off Button**



| ltem      | Description  |
|-----------|--|
| Touch Off | Turns off the touch screen so that accidental touches don't affect the instrument. |

#### **See Also** • Tips for Using the Touch Screen (see page 618)

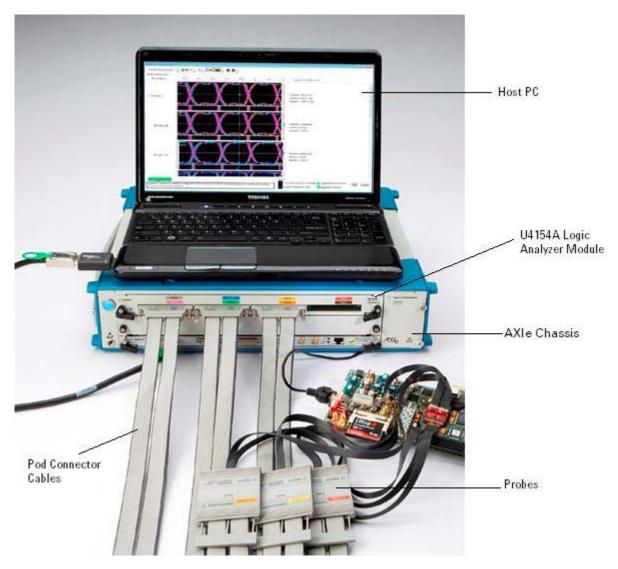
# **U4154A Logic Analyzer Product Overview**

The Agilent U4154A logic analyzer is a 136 channel AXIe based high speed state and timing logic analyzer. It provides reliable data capture with powerful analysis and validation tools for high data rate memory based products. It helps you to perform functional validation and characterization of your memory based products.

U4154A comes as an instrument module that you can install in one of the slots of the Agilent AXIe chassis. The Agilent AXIe chassis is a modular instrument chassis that supports complex and high density testing. The chassis provides slots for installing multiple instrument modules such as the U4154A Logic Analyzer module.

You can configure, control, and use the U4154A Logic Analyzer module through the Agilent Logic Analyzer application (version 5.0 and above). You can install this application on a host PC (a laptop or a desktop with a PCIe interface or the Agilent M9536A Embedded Controller Module). The laptop or desktop host PC connects to the U4154A module through the PCIe x8 interface of the AXIe chassis.

The following figure displays a sample setup of the U4154A Logic Analyzer module in one of the slots of the Agilent AXIe chassis.



You can install a single U4154A module or multiple U4154A modules in slots of an AXIe chassis to increase the channel count. You can connect two U4154A modules in an AXIe chassis to form a two-card set with 272 channels.

# CAUTION

You must power down the AXIe chassis before inserting, replacing, or removing the U4154A Logic Analyzer module. The enclosure surface of the U4154A module may become hot during use. If you need to remove the module, first power down the AXIe chassis, wait for at least five minutes to allow the module to cool, and then pull the module out of the chassis.

To know more about the hardware components of the U4154A Logic Analyzer module and how to set up this module in AXIe chassis, refer to the  $\checkmark$  AXIe Based Logic Analysis and Protocol Test Modules Installation Guide.

| Supplied<br>Accessories | • Flex cables for connecting multiple U4154A modules in different slots of an AXIe chassis |
|-------------------------|--|
|                         | Accessory pouch  |
|                         | • Pod connector cables for connecting Logic Analyzer pods to probes.                       |
| Optional<br>Accessories | • Probes.  |
| See Also                | • Tutorial - Getting to know your logic analyzer (see page 60)                             |
|                         | • U4154A Logic Analyzer Specifications and Characteristics (see page 775)                  |

# **16850-Series Logic Analyzer Product Overview**

The Agilent Technologies 16850-series logic analyzers are standalone benchtop logic analyzers that range from 34 to 136 logic acquisition channels, depending on the model.

Model Comparison

| Agilent<br>model<br>number<br>:           | 16851A | 16852A | 16853A | 16854A |
|---|--------|--------|--------|--------|
| Logic<br>acquisit<br>ion<br>channel<br>s: | 34     | 68     | 102    | 136    |

- **Features, Logic** 2 M to 128 M memory depth per channel (depending on memory option), software upgradeable.
  - 350 MHz or 700 MHz maximum state data rate (depending on state speed option), software upgradeable.
  - Full Channel Timing Mode at 2.5 GHz sampling with 12.5 GHz Timing Zoom.
  - Half Channel Timing Mode at 5.0 GHz sampling with 12.5 GHz Timing Zoom.
  - Automated threshold and sample position setup.
  - 12.5 GHz timing zoom with 256 K samples.

# Features, Built- in 15 inch TFT color LCD display, 1,024 x 768 (XGA) resolution. Mainframe Touch screen with Option 103. See Tips for Using the Touch Screen (see page 618).

- Front panel knob and buttons. See 16850 Series Front Panel Operation (see page 629).
- 500 GB hard disk drive (or external hard drive option).
- 10Base-T, 100Base-T, 1000Base-T LAN port.
- USB 2.0 ports (six total, two on front, four on back).
- One PCI expansion slot.
- One PCI Express x1 expansion slot.
- Windows 7 operating system.
- *Agilent Logic and Protocol Analyzer* application which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 408).

## CAUTION

When powering off the 16850-series logic analyzer, wait until the fans stop turning (about 15 seconds) before turning the logic analyzer back on. This ensures that internal circuitry restarts in a known state. (For more information on powering off the logic analyzer, see the  $\nearrow$  "16850-Series Logic Analyzer Installation/Quick Start Guide".)

| Supplied<br>Accessories | <ul> <li>PS/2 mouse</li> <li>PS/2 mini keyboard</li> <li>Accessory pouch</li> <li>Power cord</li> </ul> |
|-------------------------|---|
| Optional<br>Accessories | • Probes  |
| See Also                | • Tutorial - Getting to know your logic analyzer (see page 60)  |
|                         | • 16850-Series Logic Analyzer Specifications and Characteristics (see page 779)                         |

#### **16850-Series Front Panel Operation**

The front panel interface consists of a knob and buttons that you use to set up and run measurements. There are also shortcut buttons that quickly access commonly used dialogs in the interface. When a front panel action is not valid, an audible "beep" will sound.

# **NOTE** When multiple instances of the *Agilent Logic and Protocol Analyzer* application are running on the logic analyzer, the front panel knobs and buttons only work for the application that is connected to the *local* acquisition hardware.

All functions available with the front panel knobs and buttons can also be performed in the graphical user interface (GUI).

- Run/Stop Buttons
- General Purpose Knob
- Touch Off Button

Run/Stop Buttons



| ltem                  | Description  |
|-----------------------|--|
| Run Single            | Runs a single acquisition (see page 203). The Run Single button turns green indicating when a Run action is valid. While the analyzer is running, the light goes out.                    |
| Run Rep. (Repetitive) | Runs a repetitive acquisition (see page 203). The Run Repetitive button turns green indicating when a Run Repetitive action is valid. While the analyzer is running, the light goes out. |
| Stop                  | Stops (see page 203) the current acquisition. The Stop button turns red during a Run cycle indicating when the Stop action is valid.   |

#### General Purpose Knob



The general purpose knob acts on the field that has the current focus. Fields that have the current focus have the blue background. The general purpose knob is typically used to increase/decrease numeric values such as waveform scale and delay.

# **Touch Off Button**



| Item      | Description  |
|-----------|--|
| Touch Off | Turns off the touch screen so that accidental touches don't affect the instrument. |

**See Also** • Tips for Using the Touch Screen (see page 618)

# **Agilent Logic and Protocol Analyzer Application Product Overview**

The *Agilent Logic Analyzer* application is a familiar Windows-based user interface which takes the complexity out of making logic analyzer measurements. You can perform all operations directly from one window. See Intrinsic Support (see page 408).

Agilent's Simple, Quick and Advanced Trigger functions take the complexity out of triggering. Use Simple Trigger's pull down menus to define events in terms of edges and patterns. With Quick Trigger you can see if a suspect event ever reoccurs by just drawing a box around the event in the display. Quick trigger will do the rest! Use Advanced Trigger's drag and drop graphical icons with sentence-like structures to customize complex trigger scenarios.

• Keyboard Commands (see page 631)

#### **Keyboard Commands**

- Access Menus (see page 631)
- File Operations (see page 632)
- Edit Operations (see page 632)
- Search Operations (see page 632)
- View operations (see page 633)
- Run/Stop Operations (see page 633)
- Compare Operations (see page 633)
- Listing Operations (see page 633)
- Waveform Operations (see page 633)
- Window Operations (see page 633)
- Help Operations (see page 634)
- Miscellaneous (see page 634)

### **Access Menus**

| Alt+F | Access to File menu |
|-------|---------------------|
| Alt+E | Access to Edit menu |

# 12 Reference

| Alt+V | Access to View menu     |
|-------|-------------------------|
| Alt+S | Access to Setup menu    |
| Alt+T | Access to Tools menu    |
| Alt+M | Access to Markers menu  |
| Alt+R | Access to Run/Stop menu |
| Alt+W | Access to Window menu   |
| Alt+H | Access to Help menu     |

File Operations The following operations are located under File in the menu bar.

| Ctrl+N  | File - New    |
|---------|---------------|
| Ctrl+0  | File - Open   |
| Ctrl+F4 | File - Close  |
| Ctrl+S  | File - Save   |
| Ctrl+I  | File - Import |
| Shift+E | File - Export |
| Ctrl+P  | File - Print  |

Edit Operations The following operations are located under Edit in the menu bar.

| Ctrl+Z | Edit - Undo                          |
|--------|--------------------------------------|
| Ctrl+X | Edit - Cut                           |
| Ctrl+C | Edit - Copy                          |
| Ctrl+V | Edit - Paste                         |
| Alt+I  | Edit - Insert Bus/Signal into Window |
| Alt+P  | Edit - Current Window Properties     |

**Search** The following operations are located under **Edit** in the menu bar. **Operations** 

| Ctrl+F   | Edit - Find            |
|----------|------------------------|
| Shift+F3 | Edit - Find Previous   |
| F3       | Edit - Find Next       |
| Ctrl+B   | Edit - Go To Beginning |
| Ctrl+T   | Edit - Go To Trigger   |

| Ctrl+E | Edit - Go To End |
|--------|------------------|
| Ctrl+G | Edit - Go To     |

#### View Operations The following operations are located under View in the menu bar.

| Shift+F | View - Zoom Out Full         |
|---------|------------------------------|
| Shift+0 | View - Zoom Out              |
| Shift+I | View - Zoom In               |
| F9      | View - Full Screen           |
| F11     | View - Toggle Tabbed Windows |
| F12     | View - Toggle Status Bar     |

# **Run/Stop** The following operations are located under **Run/Stop** in the menu bar. **Operations**

| F5            | Run/Stop - Run            |
|---------------|---------------------------|
| Ctrl+F5       | Run/Stop - Run Repetitive |
| F8            | Run/Stop - Stop           |
| Shift+F8      | Run/Stop - Cancel         |
| Shift+Ctrl+F8 | Run/Stop - Resume         |

| Compare    | The f | following | operations | are | located | under | Compare | in | the | menu | bar. |
|------------|-------|-----------|------------|-----|---------|-------|---------|----|-----|------|------|
| Operations |       |           |            |     |         |       |         |    |     |      |      |

| Alt+P | <b>Compare - Properties</b> |
|-------|-----------------------------|
|-------|-----------------------------|

**Listing** The following operations are located under **Listing** in the menu bar.

Operations

| Alt+P Listing - Properties |  |
|----------------------------|--|
|----------------------------|--|

**Waveform** The following operations are located under **Waveform** in the menu bar. **Operations** 

| Alt+P | Waveform - Properties |  |
|-------|-----------------------|--|
|-------|-----------------------|--|

Window The following operations are located under Window in the menu bar. **Operations** 

# 12 Reference

|                 | F6  | Window - Toggle to Next     |  |  |
|-----------------|---|-----------------------------|--|--|
|                 | Shift+F6  | Window - Toggle to Previous |  |  |
| Help Operations | The following operations are located under <b>Help</b> in the menu bar.             |                             |  |  |
|                 | F1 Help - Help Topics   |                             |  |  |
| Miscellaneous   | <b>Miscellaneous</b> The following operations are located throughout the interface. |                             |  |  |
|                 | Ctrl+esc  | Shows Windows Start bar     |  |  |

# **Logic Analyzer Notes**

|   | Channels and Memory Depth (see page 635)   |
|---|--|
|   | • Timing Mode Sampling Options (see page 635)  |
|   | • State Mode Sampling Options (see page 636)   |
|   | • Timing Zoom (see page 637)   |
| Channels and<br>Memory Depth              | <ul> <li>1680/1690-Series Logic Analyzer Notes, Channels and Memory Depth<br/>(see page 637)</li> </ul>  |
|   | <ul> <li>16740/41/42 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 639)</li> </ul>   |
|   | <ul> <li>16750/51/52 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 640)</li> </ul>   |
|   | <ul> <li>16753/54/55/56 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 643)</li> </ul>  |
|   | <ul> <li>16760 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 645)</li> </ul>   |
|   | <ul> <li>16800-Series Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 651)</li> </ul>  |
|   | <ul> <li>16910/11 Logic Analyzer Notes, Channels and Memory Depth (see page 654)</li> </ul>  |
|   | <ul> <li>16950/51 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 656)</li> </ul>  |
|   | <ul> <li>16960 Logic Analyzer Notes, Channels and Memory Depth (see page 658)</li> </ul>   |
|   | <ul> <li>16962 Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 669)</li> </ul>   |
|   | <ul> <li>U4154A Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 678)</li> </ul>  |
|   | <ul> <li>16850-Series Logic Analyzer Notes, Channels and Memory Depth (see<br/>page 711)</li> </ul>  |
| Timing Mode<br>Sampling<br>Options/Period | The timing mode sampling options let you choose between <i>Full Channel Timing Mode</i> (default), <i>Half Channel Timing Mode</i> (faster sampling), or <i>Transitional / Store Qualified Timing Mode</i> (greater measurement length). For notes on these modes in a particular logic analyzer, see: |
|   | <ul> <li>1680/1690-Series Logic Analyzer Notes, Timing Mode Sampling<br/>Options/Period (see page 637)</li> </ul>  |
|   |  |

• 16740/41/42 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 639)

- 16750/51/52 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 640)
- 16753/54/55/56 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 643)
- 16760 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 645)
- 16800-Series Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 652)
- 16910/11 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 654)
- 16950/51 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 656)
- 16960 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 659)
- 16962 Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 669)
- U4154A Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 678)
- 16850-Series Logic Analyzer Notes, Timing Mode Sampling Options/Period (see page 711)

State ModeThe state mode sampling options let you choose between General StateSampling OptionsMode (default) or Turbo State Mode (faster sampling). For notes on these<br/>modes in a particular logic analyzer, see:

- 1680/1690-Series Logic Analyzer Notes, State Mode (see page 638)
- 16740/41/42 Logic Analyzer Notes, State Mode (see page 640)
- 16750/51/52 Logic Analyzer Notes, State Mode Sampling Options (see page 642)
- 16753/54/55/56 Logic Analyzer Notes, State Mode Sampling Options (see page 644)
- 16760 Logic Analyzer Notes, State Mode Sampling Options (see page 646)
- 16800-Series Logic Analyzer Notes, State Mode Sampling Options (see page 653)
- 16910/11 Logic Analyzer Notes, State Mode Sampling Options (see page 655)
- 16950/51 Logic Analyzer Notes, State Mode Sampling Options (see page 657)
- 16960 Logic Analyzer Notes, State Mode Sampling Options (see page 659)

- 16962 Logic Analyzer Notes, State Mode Sampling Options (see page 670)
- U4154A Logic Analyzer Notes, State Mode Sampling Options (see page 679)
- 16850-Series Logic Analyzer Notes, State Mode Sampling Options (see page 711)

#### **Timing Zoom** • 1680/1690-Series Logic Analyzers don't have the timing zoom feature.

- 16740/41/42 Logic Analyzer Notes, Timing Zoom (see page 640)
- 16750/51/52 Logic Analyzer Notes, Timing Zoom (see page 642)
- 16753/54/55/56 Logic Analyzer Notes, Timing Zoom (see page 644)
- 16760 Logic Analyzers don't have the timing zoom feature.
- 16800-Series Logic Analyzer Notes, Timing Zoom (see page 654)
- 16910/11 Logic Analyzer Notes, Timing Zoom (see page 656)
- 16950/51 Logic Analyzer Notes, Timing Zoom (see page 657)
- 16960 Logic Analyzers don't have the timing zoom feature.
- 16962 Logic Analyzers don't have the timing zoom feature.
- U4154A Logic Analyzer Notes, Timing Zoom (see page 679)
- 16850-Series Logic Analyzer Notes, Timing Zoom (see page 654)

# 1680/1690-Series Logic Analyzer Notes

- Channels and Memory Depth (see page 637)
- Timing Mode Sampling Options/Period (see page 637)
- State Mode (see page 638)

#### Channels and Memory Depth

|                  | 1680A<br>1690A | 1680AD<br>1690AD | 1681A<br>1691A | 1681AD<br>1691AD | 1682A<br>1692A | 1682AD<br>1692AD | 1683A<br>1693A | 1683AD<br>1693AD |
|------------------|----------------|------------------|----------------|------------------|----------------|------------------|----------------|------------------|
| Memor<br>y depth | 512 K          | 2 M              |
| Channe<br>Is     | 136            | 136              | 102            | 102              | 68             | 68               | 34             | 34               |

Timing Mode Sampling Options/Period • Full channel (see page 637), 400 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 637) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go slower with the Sample Period control.

• Half channel (see page 637), 800 MHz = Half Channel Timing Mode

| With this sampling option, only one pod of each pod pair is available, |  |  |  |  |
|--|--|--|--|--|
| and the memory depth (see page 637) is doubled. Channels assigned to   |  |  |  |  |
| unavailable pods are ignored. You can specify which pod to use in the  |  |  |  |  |
| Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod     |  |  |  |  |
| button and selecting the desired pod.                                  |  |  |  |  |

Data is sampled and stored every 1.25 ns; this rate cannot be changed.

• Transitional / Store qualified, Full channel 400 MHz = Transitional / Store Qualified Timing Mode

At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 637) by using 1/2 (or less) of a module's acquisition memory depth (see page 637) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 422).

**NOTE** When you select the timing sampling mode's 400 MHz option (800 MHz option), the trigger marker in captured data may be off by 1 sample (3 samples). This occurs because the logic analyzer hardware uses 2 pipelines (4 pipelines). When triggering on a pattern, the actual sample that causes the trigger may be 1 sample before (within 3 samples before) the trigger marker. When triggering on an edge, the actual sample that causes the trigger may be within +/-1 sample (+/-2 samples) of the trigger marker.

#### State Mode • 200 Mb/s maximum clock rate = General State Mode

In the state (synchronous sampling) mode, you can have full channels (see page 637) and half memory depth (see page 637), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 200 MHz.

#### **See Also** • 1680/1690-Series Logic Analyzer Specifications (see page 715)

• 1680/1690-Series Logic Analyzer Characteristics (see page 715)

# 16740/41/42 Logic Analyzer Notes

- Channels and Memory Depth (see page 639)
- Timing Mode Sampling Options/Period (see page 639)

- State Mode (see page 640)
- Timing Zoom (see page 640)

#### Channels and Memory Depth

|              | 16740A                                       | 16741A | 16742A |  |
|--------------|--|--------|--------|--|
| Memory depth | 1 M  | 4 M    | 16 M   |  |
| Channels     | 68 channels/card * number of cards in module |        |        |  |

Timing Mode Sampling
Full channel (see page 639), 400 MHz = Full Channel Timing Mode
With this sampling option, you can use the full memory depth (see page 639) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go

slower with the Sample Period control.

### NOTE

When the Sample Period is 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

• Half channel (see page 639), 800 MHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 639) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 1.25 ns; this rate cannot be changed.

NOTE

When the Sample Period is 1.25 ns, data is acquired at four times the trigger sequencer rate. This, along with other half-channel mode characteristics, means that data must be present for at least five samples before the trigger sequencer can reliably detect it. The trigger sequencer cannot detect data present for less than two sample periods, and could miss data present for less than five sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by up to three samples.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

• Transitional / Store qualified, Full channel 400 MHz = Transitional / Store Qualified Timing Mode

At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 639) by using 1/2 (or less) of a module's acquisition memory depth (see page 639) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 422).

State Mode • 200 Mb/s maximum clock rate = General State Mode

In the state (synchronous sampling) mode, you can have full channels (see page 639) and half memory depth (see page 639), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 200 MHz.

**Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 16K-sample, 2 GHz timing analyzer to sample data as closely as every 500 ps on all channels.

**See Also** • 16740/41/42 Logic Analyzer Specifications (see page 717)

• 16740/41/42 Logic Analyzer Characteristics (see page 718)

# 16750/51/52 Logic Analyzer Notes

- Channels and Memory Depth (see page 640)
- Timing Mode Sampling Options/Period (see page 640)
- State Mode Sampling Options (see page 642)
- Timing Zoom (see page 642)

| Channels and<br>Memory Depth |              | 16750A/B                                     | 16751A/B | 16752A/B |
|------------------------------|--------------|--|----------|----------|
|                              | Memory depth | 4 M  | 16 M     | 32 M     |
|                              | Channels     | 68 channels/card * number of cards in module |          |          |

Timing Mode Sampling Options/Period • Full channel (see page 640), 400 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 640) of your logic analyzer card, with data being sampled and stored as often as every 2.5 ns. You can set the sample rate to go slower with the Sample Period control.

#### NOTE

When the Sample Period is 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

#### • Half channel (see page 640), 800 MHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 640) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 1.25 ns; this rate cannot be changed.

### NOTE

When the Sample Period is 1.25 ns, data is acquired at four times the trigger sequencer rate. This, along with other half-channel mode characteristics, means that data must be present for at least five samples before the trigger sequencer can reliably detect it. The trigger sequencer cannot detect data present for less than two sample periods, and could miss data present for less than five sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by up to three samples.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

• Transitional / Store qualified, Full channel 400 MHz = Transitional / Store Qualified Timing Mode

At the 400 MHz sample rate (2.5 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 640) by using 1/2 (or less) of a module's acquisition memory depth (see page 640) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. See transitional timing (see page 422).

State Mode Sampling Options

# • 200 MHz = General State Mode

With this sampling option, you can have full channels (see page 640) and half memory depth (see page 640), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 200 MHz.

• 400 MHz = Turbo State Mode

With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 640). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

State sampling speed matches your device under test's clock rate, up to 400 MHz.

**NOTE** When Store Qualification is performed in the 400 MHz State mode, there may be the case where data occupying memory is further disqualified. As a result, you may see a non-contiguous listing of states as well as a reduction of usable memory.

**Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 16K-sample, 2 GHz timing analyzer to sample data as closely as every 500 ps on all channels.

# **NOTE** When in the Turbo State Mode, the start of timing zoom data may occur after the actual trigger point. The reason for this data mis-alignment is due to how the trigger sequencer functions when in this mode.

The analyzer sequencer works on *pairs* of samples. It will not evaluate the first sample of the pair until the second sample has entered the sequencer. If, for example, the trigger point is determined to be on the first sample, the analyzer displays the timing zoom data relative to the evaluation of the second sample. Whatever time difference is seen between the two samples (of the pair) is reflected in the data display between the trigger point and the start of the timing zoom data.

This time difference can be noticeable if your measurement is using bursted clocks and the first sample (actual trigger point) is clocked on the last clock signal of a burst, and the second sample (of the pair) is clocked with the first clock of the next burst. The time difference between the clock bursts is reflected as a mis-alignment between the trigger point and the start of the timing zoom data.

The best thing to do to help mitigate this situation is to set the timing zoom to "0% poststore" to capture as much data near the first sample as possible.

- **See Also** 16750/51/52 Logic Analyzer Specifications (see page 722)
  - 16750/51/52 Logic Analyzer Characteristics (see page 723)

# 16753/54/55/56 Logic Analyzer Notes

- Channels and Memory Depth (see page 643)
- Timing Mode Sampling Options/Period (see page 643)
- State Mode Sampling Options (see page 644)
- Timing Zoom (see page 644)

# Channels and Memory Depth

|              | 16753A                                       | 16754A | 16755A | 16756A |  |
|--------------|--|--------|--------|--------|--|
| Memory depth | 1 M  | 4 M    | 16 M   | 64 M   |  |
| Channels     | 68 channels/card * number of cards in module |        |        |        |  |

**Timing Mode** • Full channel (see page 643), 600 MHz = Full Channel Timing Mode Sampling

**Options/Period** With this sampling option, you can use the full memory depth (see page 643) of your logic analyzer card, with data being sampled and stored as often as every 1.67 ns. You can set the sample rate to go slower with the Sample Period control.

• Half channel (see page 643), 1.2 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 643) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 833 ps; this rate cannot be changed.

• Transitional / Store qualified, Full channel 600 MHz = Transitional / Store Qualified Timing Mode

At the 600 MHz sample rate (1.667 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 643) by using 1/2 (or less) of a module's acquisition memory depth (see page 643) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 1.667 ns to 500 us. See transitional timing (see page 422).

State Mode Sampling Options • 300 MHz = General State Mode

With this sampling option, you can have full channels (see page 643) and half memory depth (see page 643), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 300 MHz.

• 600 MHz = Turbo State Mode

With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 643). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

State sampling speed matches your device under test's clock rate, up to 600 MHz.

- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.
  - **See Also** Eye Scan in Logic Analyzers that Support Differential Signals (see page 428)
    - 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 727)

# **16760 Logic Analyzer Notes**

- Differences from Other Logic Analyzers (see page 645)
- Channels and Memory Depth (see page 645)
- Timing Mode Sampling Options/Period (see page 645)
- State Mode Sampling Options (see page 646)

Differences from<br/>Other LogicCompared to most other logic analyzers supported in the 16900-series<br/>logic analysis system, the 16760 logic analyzer differs in the following<br/>ways:

- There are three additional state mode sampling options beyond the normal *General State Mode* and *Turbo State Mode* options.
- In state mode, the clock input is always from pod 1 (on the master card in multi-card modules). You cannot qualify the sampling clock input with signals from the other pods clock inputs.
- You cannot split a 16760 logic analyzer module.
- Pods are assigned individually instead of in *pod pairs* (and you can only assign a pod to the module or reserve it for time tag storage).
- There is no Half Channel Timing Mode.
- There is no timing zoom feature.

# Channels and Memory Depth

Sampling

**Options/Period** 

|              | 16760A                                       |
|--------------|--|
| Memory depth | 64 M   |
| Channels     | 34 channels/card * number of cards in module |

**Timing Mode** • Full channel (see page 645), 800 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 645) of your logic analyzer card, with data being sampled and stored every 1.25 ns.

NOTE

With the Sample Period at 1.25 ns, data is acquired at four times the trigger sequencer rate. This means that data must be present for at least four samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than four sample periods.

The trigger sequencer treats the data as a group of four samples for each sequencer clock. This means that the trigger point indication could be off by three samples and bus/signal occurrence counts could be off by up to a factor of four.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

# • Transitional / Store qualified, Full channel 400 MHz = Transitional / Store Qualified Timing Mode

At the 400 MHz sample rate (2.5 ns sampling period), one *pod* (17 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 645) by using 1/2 (or less) of a module's acquisition memory depth (see page 645) (for more information, see 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 648)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.5 ns to 1 ms. You can set the sample rate to go slower with the Sample Period control. See transitional timing (see page 422).

# NOTE

With the Sample Period at 2.5 ns, data is acquired at two times the trigger sequencer rate. This means that data must be present for at least two samples before the trigger sequencer can reliably detect it. The trigger sequencer could miss data present for less than two sample periods.

The trigger sequencer treats the data as a group of two samples for each sequencer clock. This means that the trigger point indication could be off by one sample and bus/signal occurrence counts could be off by up to a factor of two.

Although the trigger sequencer cannot detect all data, the analyzer will correctly capture all data present for at least one sample period.

State ModeFor all state mode sampling options, clocking is restricted to the J clockSampling Optionson Pod 1 of the master card of the module.

• 200 Mb/s = General State Mode

With this sampling option:

- You can have full channels (see page 645) and quarter memory depth (see page 645), or you can get half memory depth by reserving one pod (17 channels) for time tag storage (for more information, see 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 648)).
- You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
- You have full trigger resources (16 patterns, 15 ranges, timers, global counters, occurrence counters) and full trigger actions.
- State sampling speed matches your device under test's clock rate, up to 200 MHz.
- 400 Mb/s = Turbo State Mode

With this sampling option:

- One pod (17 channels) is reserved for time tag storage.
- You have half memory depth (see page 645).
- You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
- Trigger resources are limited to 8 patterns, 4 ranges, and 2 occurrence counters. Trigger actions are limited to: goto and trigger and fill memory.
- State sampling speed matches your device under test's clock rate, up to 400 MHz.
- 800 Mb/s = 800 Mb/s State Mode

With this sampling option:

- One pod (17 channels) is reserved for time tag storage.
- You have full memory depth (see page 645).
- You must specify whether the input clock signal is periodic or aperiodic. You can have clocks where the rising edge, the falling edge, or both edges indicate valid data.
- Trigger resources are limited to 4 patterns or 2 ranges on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 4 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 800 MHz.
- 1250 Mb/s Half Channel = 1250 Mb/s State Mode

With this sampling option:

- One pod (17 channels) is reserved for time tag storage. Data is only acquired from the even-numbered channels (0, 2, 4, etc.).
- You have double memory depth (see page 645).
- The input clock signal must be periodic, and both edges indicate valid data. Clock inputs on *expander cards* of a multi-card *module* cannot be used as extra data channels.
- Trigger resources are limited to 3 patterns or 1 range on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 2 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 1250 MHz.
- 1500 Mb/s Half Channel = 1500 Mb/s State Mode

With this sampling option:

- One pod (17 channels) is reserved for time tag storage. Data is only acquired from the even-numbered channels (0, 2, 4, etc.).
- You have double memory depth (see page 645).

- The input clock signal must be periodic, and both edges indicate valid data. Clock inputs on *expander cards* of a multi-card *module* cannot be used as extra data channels.
- Trigger resources are limited to 3 patterns or 1 range on each pod. Trigger actions are limited to trigger and fill memory. You can have a maximum of 2 sequence steps.
- State sampling speed matches your device under test's clock rate, up to 1500 MHz.

Typically, in the 1250 Mb/s and 1500 Mb/s state modes, the E5386A adapter is used to reduce the number of probes and connectors required.

| See Also   | • 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs (see page 648)   |
|--|---|
|  | • Eye Finder Operation in the 16760 Logic Analyzer (see page 649)   |
|  | • Eye Scan in Logic Analyzers that Support Differential Signals (see page 428)  |
|  | • 16760 Logic Analyzer Specifications and Characteristics (see page 734)  |
|  | 16760 Logic Analyzer Memory Depth and Channel Count Trade-offs  |
|  | This topic describes the interaction between channel count, memory depth, and triggering in the 16760 logic analyzer's:   |
|  | State Sampling Mode (see page 648)  |
|  | • Transitional Timing Sampling Mode (see page 649)  |
| 200 Mb/s<br>General State<br>Sampling Mode                         | (With all other state mode sampling options, one pod (17 channels) is reserved for time tag storage.)   |
| Time Tag Storage<br>Requires 1 Pod or<br>16M Acquisition<br>Memory | • In the <i>Agilent Logic Analyzer</i> application, all modules are time-correlated; you cannot turn off <i>time tag storage</i> (as you could with previous Agilent logic analysis systems). |
|  | • To use 32M of a module's acquisition memory, one <i>pod</i> must be <i>reserved for time tag storage</i> . To use all pods, you must use 16M (or less) of a module's acquisition memory.    |
|  | <ul> <li>In the 16760 logic analyzer's 200 Mb/s State Mode, the number of timers available = 2 x (number of cards) - 1.</li> </ul>  |
| Default Settings   | • Time tag storage is always on (and cannot be turned off).   |
|  | • Memory depth is set at 16M.   |
|  | • All pods are available for capturing data.  |
|  | • If 32M memory is selected, the default pod to be used for time tag  |

• If 32M memory is selected, the default pod to be used for time tag storage is the leftmost, but any pod without buses or signals assigned can be used.

| Selecting 32M<br>Memory Depth<br>when No<br>Channels<br>Assigned to a Pod | • The pod is automatically reserved for time tag storage.   |
|---|---|
| Selecting 32M<br>Memory Depth<br>when Channels<br>Assigned to All<br>Pods | <ul><li>A dialog appears to caution you that:</li><li>Bus/signals will lose assigned channels.</li><li>Trigger specifications that use timer resources may be affected.</li></ul>   |
| Going from 32M<br>Memory Depth to<br>16M Memory<br>Depth                  | • The pod reserved for time tag storage is automatically freed (assigned to the logic analyzer) so it can be used to capture data.  |
| Transitional<br>Timing Sampling<br>Mode                                   |   |
| Time Tag Storage<br>Requires 1 Pod or<br>16M Acquisition<br>Memory        | <ul> <li>The transitional timing sampling mode also requires <i>time tag storage</i>.</li> <li>When the smallest sampling period (2.5 ns) is chosen, one <i>pod</i> must be <i>reserved for time tag storage</i>. In this case, you cannot use 16M (or less) of a module's acquisition memory to gain back the <i>pod</i>.</li> <li>With other sampling periods, the memory depth and channel count trade-offs are the same as in the state sampling mode. That is, to use 32M of a module's acquisition memory, one <i>pod</i> must be <i>reserved for time tag storage</i>. To use all pods, you must use 16M (or less) of a</li> </ul> |
|   | <ul> <li>module's acquisition memory.</li> <li>In the 16760 logic analyzer's timing modes, the number of timers available = 2 x (number of cards) - 1.</li> </ul>   |
| Default Settings  | <ul><li>Time tag storage is required.</li><li>If full memory is selected, the default pod to be used for time tag storage is the leftmost, but any pod without buses or signals assigned can be used.</li></ul>   |
| See Also  | <ul> <li>16760 Logic Analyzer Notes (see page 645)</li> <li>Configuring Logic Analyzer Modules (see page 98)</li> <li>To set acquisition memory depth (see page 135)</li> <li>Choosing the Sampling Mode (see page 119)</li> </ul>  |
|   | Eye Finder Operation in the 16760 Logic Analyzer  |
|   | For a general description of <i>eye finder</i> see Eye Finder Overview (see   |

page 425).

| In the 16760 Logic | Eye finder operation in the 16760 logic analyzer can be confusing because |
|--------------------|---|
| Analyzer           | there are five state mode sampling options:                               |

| State Sampling Option                                   | Sampling Clock Edges                        | Edges-To-Edge Timing  |
|---|---|-----------------------|
| <b>200 Mb/s</b> = General State<br>Mode                 | Rising edge, Falling edge, or<br>Both edges | Aperiodic or Periodic |
| <b>400 Mb/s</b> = Turbo State Mode                      | Rising edge, Falling edge, or<br>Both edges | Aperiodic or Periodic |
| <b>800 Mb/s</b> = <i>800 Mb/s State</i><br><i>Mode</i>  | Rising edge, Falling edge, or<br>Both edges | Aperiodic or Periodic |
| <b>1250 Mb/s Half Channel</b> =<br>1250 Mb/s State Mode | Both edges                                  | Periodic              |
| <b>1500 Mb/s Half Channel =</b><br>1500 Mb/s State Mode | Both edges                                  | Periodic              |

The 200 and 400 Mb/s modes support single clock edge sampling (either rising or falling) as well as sampling on both edges. There is no restriction on variability in edge-to-edge timing.

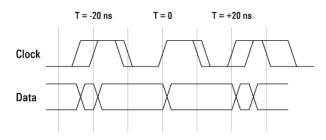
The 800 Mb/s mode also supports single and dual edge clocking. An option appears to let you indicate whether the clock is periodic (time between active edges is constant) or aperiodic (time between active edges can vary). This option does not affect the sampling operation. It tells the software how to process time tags.

The 1250 and 1500 Mb/s modes require a periodic clock and only support sampling on both clock edges.

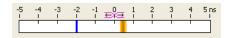
16760 Logic Analyzer Eye Finder Example
For example, if the device under test operates with an aperiodic clock that alternates between a 20 ns and a 25 ns period, then the 200, 400, or 800 Mb/s modes can be used. The 1250 and 1500 Mb/s modes cannot be used because they require a periodic clock.

What you'll see in *eye finder* is bounded by the *eye finder* scan range. In the 200 or 400 Mb/s mode, the *eye finder* scan range is +/- 5 ns around the clock edge (T=0). Because the minimum clock period is 20 ns, the *eye finder* scan will not see the data transitions for the previous and next clock cycles.

Consider a rising edge active flip flop clocked by with a dual mode 20/25 ns clock. If you look at the clock and data with an oscilloscope in infinite persistence mode at 10 ns/div, you might see:



In *eye finder*, in the 200 or 400 Mb/s mode, you'd see the transitions related to the active clock edge at T=0 because the *eye finder* scan range is +/-5 ns.



If you set the sample position (blue bar in the *eye finder* display) at about T=-2 ns, you will sample good data before the clock edge in this example. To sample data after the clock, place the blue bar at T=+2 ns.

The signals in your device under test may have a different delay from the clock, which will shift the location of the detected transitions in the sample *eye finder* display above. If the delay exceeds 5 ns, *eye finder* won't show you the transition at all. In this case, sampling at T=0 is as good as any other position.

**See Also** • Eye Scan in Logic Analyzers that Support Differential Signals (see page 428)

#### 16800-Series Logic Analyzer Notes

- Channels and Memory Depth (see page 651)
- Maximum State Sampling Speed (see page 652)
- Timing Mode Sampling Options/Period (see page 652)
- State Mode Sampling Options (see page 653)
- Timing Zoom (see page 654)

| Channels and |              |            |                         |                         |                         |
|--------------|--------------|------------|-------------------------|-------------------------|-------------------------|
| Memory Depth |              | Option 001 | Option 004 <sup>*</sup> | Option 016 <sup>*</sup> | Option 032 <sup>*</sup> |
|              | Memory depth | 1 M        | 4 M                     | 16 M                    | 32 M                    |

| Channels   | 16801A, 16821A: 34 channels 16802A, 16822A: 68 channels 16803A, 16823A:<br>102 channels 16804A: 136 channels 16806A: 204 channels |  |  |  |
|--|---|--|--|--|
| - For 16801A or 16<br>- For 16802A or 16<br>- For 16803A or 16<br>- For 16803A, use<br>- For 16806A, use |   |  |  |  |

See also Memory Depth and Channel Count Trade-offs (see page 420).

#### Maximum State Sampling Speed

|  | Option 250 | Option 500 <sup>*</sup> |  |
|--|------------|-------------------------|--|
| Max. state clock rate  | 250 MHz    | 450 MHz                 |  |
| Max. state data rate   | 250 Mb/s   | 500 Mb/s                |  |
| *Upgrades for the 16800 Series logic analyzers can be ordered using these model numbers:<br>- For 16802A or 16822A, use E5877A.<br>- For 16803A or 16823A, use E5878A.<br>- For 16804A, use E5879A.<br>- For 16806A, use E5880A.<br>(See also Installing Licensed Hardware Upgrades (see page 147).) |            |                         |  |

Timing Mode Sampling Options/Period

• Full channel (see page 652), 500 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 652) of your logic analyzer card, with data being sampled and stored as often as every 2.0 ns. You can set the sample rate to go slower with the Sample Period control.

• Half channel (see page 652), 1 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 652) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 1 ns; this rate cannot be changed.

This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

• Transitional / Store qualified, Full channel 500 MHz = Transitional / Store Qualified Timing Mode At the 500 MHz sample rate (2.0 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 652) by using 1/2 (or less) of a module's acquisition memory depth (see page 652) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.0 ns to 500 us. See transitional timing (see page 422).

The maximum sample rate with this option for the 16801A and 16821A 34-channel logic analyzer models is 250 MHz, and you must use 1/2 (or less) of the module's acquisition memory.

State Mode Sampling Options • 250 MHz = General State Mode

With this sampling option, you can have full channels (see page 652) and half memory depth (see page 652), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 250 MHz.

In the 16801A and 16821A 34-channel logic analyzer models, you are limited to half memory depth.

• 450 MHz = Turbo State Mode

With this sampling option (available with Option 500), one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 652). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

State sampling speed matches your device under test's clock rate, up to 450 MHz.

This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

• 500 MHz = Turbo State Mode (requires sampling on both clock edges)

This sampling option is similar to the 450 MHz Turbo State Mode, except that the logic analyzer can only sample on both edges of the input clock.

State sampling speed matches your device under test's clock rate, up to 500 MHz.

This option is not available with the 16801A and 16821A 34-channel logic analyzer models.

- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.
  - See Also • 16800 Series Logic Analyzer Specifications and Characteristics (see page 742)

### 16910/11 Logic Analyzer Notes

- Channels and Memory Depth (see page 654)
- Maximum State Sampling Speed (see page 654)
- Timing Mode Sampling Options/Period (see page 654)
- State Mode Sampling Options (see page 655)
- Timing Zoom (see page 656)

| Channels and |                 |            |                                     |                                   |                         |    |
|--------------|-----------------|------------|-------------------------------------|-----------------------------------|-------------------------|----|
| Memory Depth |                 | Option 256 | Option 001 <sup>*</sup>             | Option 004 <sup>*</sup>           | Option 016 <sup>*</sup> | Op |
|              | Memory<br>depth | 256 K      | 1 M                                 | 4 M                               | 16 M                    | 32 |
|              | Channels        |            | annels/card * n<br>* number of card | umber of cards in<br>Is in module | module 16911A:          | 68 |

Upgrades for the 16910A and 16911A logic analyzers can be ordered using model numbers E5865A and E5866A, respectively.

Option 032<sup>\*</sup>

32 M

(See also Installing Licensed Hardware Upgrades (see page 147).)

See also Memory Depth and Channel Count Trade-offs (see page 420).

## **Maximum State**

#### **Sampling Speed**

|   | Option 250 | Option 500 <sup>*</sup> |  |  |
|---|------------|-------------------------|--|--|
| Max. state clock rate   | 250 MHz    | 450 MHz                 |  |  |
| Max. state data rate  | 250 Mb/s   | 500 Mb/s                |  |  |
| <sup>*</sup> Upgrades for the 16910A and 16911A logic analyzers can be ordered using model numbers E5865A and E5866A, respectively.<br>(See also Installing Licensed Hardware Upgrades (see page 147).) |            |                         |  |  |

**Timing Mode** Sampling **Options/Period**  • Full channel (see page 654), 500 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 654) of your logic analyzer card, with data being sampled and stored as often as every 2.0 ns. You can set the sample rate to go slower with the Sample Period control.

• Half channel (see page 654), 1 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 654) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 1 ns; this rate cannot be changed.

• Transitional / Store qualified, Full channel 500 MHz = Transitional / Store Qualified Timing Mode

At the 500 MHz sample rate (2.0 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 654) by using 1/2 (or less) of a module's acquisition memory depth (see page 654) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 2.0 ns to 500 us. See transitional timing (see page 422).

State Mode Sampling Options

• 250 MHz = General State Mode

With this sampling option, you can have full channels (see page 654) and half memory depth (see page 654), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 250 MHz.

• 450 MHz = Turbo State Mode

With this sampling option (available with Option 500), one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 654). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

State sampling speed matches your device under test's clock rate, up to 450 MHz.

• 500 MHz = *Turbo State Mode* (requires sampling on both clock edges)

This sampling option is similar to the 450 MHz Turbo State Mode, except that the logic analyzer can only sample on both edges of the input clock.

State sampling speed matches your device under test's clock rate, up to 500 MHz.

- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.
  - See Also 16910/11 Logic Analyzer Specifications and Characteristics (see page 749)

### 16950/51 Logic Analyzer Notes

- Channels and Memory Depth (see page 656)
- Timing Mode Sampling Options/Period (see page 656)
- State Mode Sampling Options (see page 657)
- Timing Zoom (see page 657)

#### **Channels and Memory Depth** 16950A/B Option Option Option Option Option Option Memory 256\*\* 001 004 032 064 016 depth 256 K 1 M 4 M 16 M 32 M 64 M 16951B 256 M (no memory depth options) Memory depth 68 channels/card \* number of cards in module Channels <sup>\*</sup>Upgrades for the 16950 logic analyzer can be ordered using model number E5875A. (See also Installing Licensed Hardware Upgrades (see page 147).) <sup>\*</sup>Available on the 16950A logic analyzer only.

Timing Mode Sampling Options/Period

• Full channel (see page 656), 600 MHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth (see page 656) of your logic analyzer card, with data being sampled and stored as often as every 1.67 ns. You can set the sample rate to go slower with the Sample Period control.

• Half channel (see page 656), 1.2 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 656) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod. Data is sampled and stored every 833 ps; this rate cannot be changed.

• Transitional / Store qualified, Full channel 600 MHz = Transitional / Store Qualified Timing Mode

At the 600 MHz sample rate (1.667 ns sampling period), one *pod pair* (34 channels) must be *reserved for time tag storage*. At slower sample rates, you can get full channels (see page 656) by using 1/2 (or less) of a module's acquisition memory depth (see page 656) (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 1.667 ns to 500 us. See transitional timing (see page 422).

State Mode Sampling Options • 300 MHz = General State Mode

Sampling Options

With this sampling option, you can have full channels (see page 656) and half memory depth (see page 656), or you can get full memory depth by reserving one pod pair (34 channels) for time tag storage (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

State sampling speed matches your device under test's clock rate, up to 300 MHz.

• 600 MHz (16950A) or 667 MHz (16950B, 16951B) = Turbo State Mode

With this sampling option, one pod pair (34 channels) is reserved for time tag storage, and you have full memory depth (see page 656). Clocking is restricted to the J clock on Pod 1 of the *master card* of the *module*, and triggering is restricted to two trigger functions.

State sampling speed matches your device under test's clock rate, up to 600 MHz (16950A) or 667 MHz (16950B, 16951B).

NOTE

In *Turbo State Mode* when using a single-edge clock, if the clock channel is assigned to a bus/signal name, the logic analyzer displays the clock signal at half of the actual clock rate. This is because the clock signal is divided by 2 in the comparator, and the output of the comparator is what is displayed. This division is not done in *General State Mode* with any clock selection or in *Turbo State Mode* when clocking on both edges of the clock.

- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 64K-sample, 4 GHz timing analyzer to sample data every 250 ps on all channels.
  - **See Also** Eye Scan in Logic Analyzers that Support Differential Signals (see page 428)

• 16950/51 Logic Analyzer Specifications and Characteristics (see page 757)

### **16960 Logic Analyzer Notes**

- Differences from Other Logic Analyzers (see page 658)
- Channels and Memory Depth (see page 658)
- Timing Mode Sampling Options/Period (see page 659)
- State Mode Sampling (see page 659)

Differences from<br/>Other LogicCompared to most other logic analyzers supported in the 16900-series<br/>logic analysis system, the 16960 logic analyzer differs in the following<br/>ways:

- There is one synchronous sampling (state) analysis mode that is set up differently than most other logic analyzers (see State Mode Sampling (see page 659) below and Setting Up the State Sampling Clock in the 16960 Logic Analyzer (see page 659)).
- Full memory depth is available on all channels. There are no trade-offs between memory depth and channel count. However, using storage qualifiers in the triggering setup can reduce the number samples that are stored.
- You cannot split a 16960 logic analyzer module. (Because of this, and with no memory depth and channel count trade-offs, there is no need for pod assignment.)
- When multiple cards are connected in a multi-card module, there is no notion of master and slave cards. Pods are indexed from the bottom card up.
- Trigger set up resources are different. For more information, see Specifying Advanced Triggers in the 16960 Logic Analyzer (see page 660).
- In *state* sampling mode, the behavior when stopping a running acquisition is different from most other logic analyzers (see Stop Behavior in the 16960/16962 Logic Analyzers (see page 676)).

| Channels and |                  |                                     |                         |                               | 1                       |                         |
|--------------|------------------|-------------------------------------|-------------------------|-------------------------------|-------------------------|-------------------------|
| Memory Depth | 16960A<br>Memory | Option 004 <sup>*</sup>             | Option 016 <sup>*</sup> | Option 032 <sup>*</sup>       | Option 064 <sup>*</sup> | Option 100 <sup>*</sup> |
|              | depth            | 4 M                                 | 16 M                    | 32 M                          | 64 M                    | 100 M                   |
|              | Channels         | 68 channels/c                       | ard * number of         | cards in module               |                         |                         |
|              |                  | the 16960A logic<br>nsed Hardware U |                         | ordered using mo<br>ge 147).) | odel number E58         | 86A. (See also          |

## Agilent Logic and Protocol Analyzer Online Help

Timing Mode Sampling
Options/Period
Full channel (see page 658), 2.0 GHz = Full Channel Timing Mode With this sampling option, you can use the full memory depth (see page 658) of your logic analyzer card, with data being sampled and stored every 500 ps; this rate cannot be changed.

• 1.6 Gb/s = General State Mode

• Transitional / Store qualified, Full channel 2.0 GHz = Transitional / Store Qualified Timing Mode

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period is 500 ps and cannot be changed. See transitional timing (see page 422).

State Mode Sampling

The sampling speed matches your device under test's clock rate, from 100 Mb/s up to 1.6 Gb/s.

Sampling occurs on both edges of the input clock signal which must be continuous.

Clock inputs on odd pods can be used for the sampling clock. Clock inputs on even pods can be used as a clock ready (a signal whose level indicates when the sampling clock signal is stable).

Frequency-related sampling clocks can be selected for each pod pair. (Only one clock ready input can be used for all pod pairs.)

In a multi-card module, sampling clock signals can come from any module.

- **See Also** Setting Up the State Sampling Clock in the 16960 Logic Analyzer (see page 659)
  - Specifying Advanced Triggers in the 16960 Logic Analyzer (see page 660)
  - Eye Scan in Logic Analyzers that Support Differential Signals (see page 428)
  - 16960 Logic Analyzer Specifications and Characteristics (see page 764)

#### Setting up the State Sampling Clock in the 16960 Logic Analyzers

The sampling speed matches your device under test's clock rate, from 100 Mb/s up to 1.6 Gb/s.

Sampling occurs on both edges of the input clock signal which must be continuous.

| CState Clock Option | ns           |   |   |
|---------------------|--------------|---|---|
| State Clock 1:      | Pod B1 Clock | ~ | Both edges V  |
| State Clock 2:      | Pod A1 Clock | ~ | State Clock 1 and 2 must be the same exact frequency. Phase can be different. |
| Clock Ready:        | Pod B2 Clock | ~ | Latched High 🗸 Refer to Clock Ready on-line documentation for usage details.  |

Clock inputs on odd pods can be used for the sampling clock.

Clock inputs on even pods can be used as a clock ready (a signal whose level indicates when the sampling clock signal is stable).

Frequency-related sampling clocks can be selected for each pod pair. (Only one clock ready input can be used for all pod pairs.)

In a multi-card module, sampling clock signals can come from any module.

See Also • Specifying Advanced Triggers in the 16960/16962 Logic Analyzers (see page 660)

- 16960 Logic Analyzer Notes (see page 658)
- 16960 Logic Analyzer Specifications and Characteristics (see page 764)

#### Specifying Advanced Triggers in the 16960/16962 Logic Analyzers

When setting up advanced triggers, the 16960/16962 logic analyzers have some differences from other logic analyzers:

- The "Find a packet" trigger function is currently unavailable. All the other typical state and timing trigger functions are available.
- Up to four trigger sequence steps are available.
- Events and storage specifications in the trigger sequence steps let you choose the new **Burst** pattern event type. For more information, see:
  - "To specify burst patterns (16960/16962 logic analyzers)" on page 661
  - "Burst Patterns in Default Storage (16960/16962 logic analyzers)" on page 663
  - "Burst Patterns in "If" Clauses (16960/16962 logic analyzers)" on page 664
  - "Burst Patterns in "Else If" Clauses (16960/16962 logic analyzers)" on page 667
  - "Trigger Errors (16960/16962 logic analyzers)" on page 668
- There are no global counters.
- There is one timer in the timing sampling mode and there are no timers in the state sampling mode.
- Occurrence counters (one is available in each sequence step) count eventual occurrences. You can achieve a consecutive occurrence counter by using "Else if" clauses with the "Reset occurrence counter" action.

- There are the additional storage control actions: "Store sample and Turn on default storage" and "Don't store sample and Turn off default storing".
- See Also "Setting up the State Sampling Clock in the 16960 Logic Analyzers" on page 659
  - "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674
  - "16960 Logic Analyzer Notes" on page 658
  - "16962 Logic Analyzer Notes" on page 668
  - "16960 Logic Analyzer Specifications and Characteristics" on page 764
  - "16962 Logic Analyzer Specifications and Characteristics" on page 769

#### To specify burst patterns (16960/16962 logic analyzers)

When using burst patterns in non-"Advanced" trigger functions, be sure to view the trigger function as Advanced If/Then steps (see "To show a trigger sequence step as Advanced If/Then trigger functions" on page 189) to verify the actual steps, occurrence counts, etc.

For example, when non-"Advanced" trigger functions that specify a number of states are used with burst patterns, the actual number of states can be multiplied by the burst depth in a way that is unexpected when reading the original trigger function.

1 In the Advanced Trigger dialog, select the **Burst** event type.

| Step 1 × Advanced If/Then |   |                                   |              |  |  |
|---------------------------|---|-----------------------------------|--------------|--|--|
| 💙 If                      | ۲ | Anything 🛛 🗸                      |              |  |  |
|                           |   | Burst<br>Bus/Signal<br>Acceltaine | 1 🔳 — +      |  |  |
| Then                      | ۲ | Anything<br>Nothing               | emory 🔽      |  |  |
|                           | * | Flag<br>Arm in from               | lt Storage 🔽 |  |  |

2 Select the number of samples in the burst pattern.

| Step 1 🛛 | Advanced If/Then |          |                           |
|----------|------------------|----------|---------------------------|
| 💙 If     | 💙 Burst          | × 4 ×    | My Bus 1 🛛 🗸 🛠            |
|          |                  | 2<br>3   | XXXX XXXX XXXX XXXX Hex V |
|          |                  | 4<br>.Z: | XXXX XXXX XXXX II Hex V   |
|          |                  | .3:      | XXXX XXXX XXXX II Hex V   |
|          |                  | .4:      | XXXX XXXX XXXX XXXX Hex ¥ |

You can have up to eight 2-sample burst patterns or four 3- or 4-sample burst patterns.

**3** Select the bus or signal.

NOTE

TIP

| Step 1 | X Advanced If/Then |       |             |            |
|--------|--------------------|-------|-------------|------------|
| 💙 If   | 💙 Burst            | 4 🖌 ( | My Bus 1    | ×          |
|        |                    | .1:   | My Signal 1 | XX 🔳 Hex 💙 |
|        |                    | .2:   | More        | XX 🔳 Hex 💙 |
|        |                    | .3:   | Add         | XX 🔳 Hex 💙 |
|        |                    | .4: , | Delete      | XX 📕 Hex 🕏 |

Clicking 💌 lets you:

- Select from recently used bus/signal names.
- Select from other bus/signal names (More...).
- Add another bus/signal to the burst pattern.

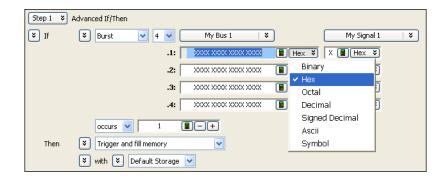
Additional buses/signals are AND'ed in the burst pattern. You can add as many buses/signals as you like, without consuming additional trigger resources.

Add buses/signals to the burst pattern instead of inserting AND'ed events. AND'ed events consume trigger resources.

• **Delete** the bus/signal from the burst pattern.

Clicking elsewhere on a bus/signal name button opens a Select dialog for selecting a different name.

- **4** Specify the burst pattern values:
  - a Select the number base (Binary, Hex, Octal, Decimal, Signed Decimal, also known as two's complement, Ascii, or Symbol).



**b** Enter the burst pattern value(s).

When the **Symbol** number base is selected, you use the Select Symbol dialog (see page 530) to specify the pattern values.

662

| Step 1 > Advanced If/Then |   |   |
|---------------------------|---|---|
| 🛛 If 💙 Burst              | ▼ 4 ▼ My Bus 1 × My Signal 1              | * |
|                           | .1: FFFF EEEE DDDD CCCC H Hex 🕇 1 Hex 🕇   |   |
|                           | .2: BBBB AAAA 9999 8888 🔳 Hex 💐 0 🗐 Hex 💐 |   |
|                           | .3: 7777 6666 5555 4444 🔳 Hex 😵 1 🗐 Hex 😵 |   |
|                           | .4: 3333 2222 1111 0000 🔳 Hex 💐 0 📓 Hex 💐 |   |

5 You can insert events AND'ed or OR'ed with the burst pattern.

| Step 1 ¥ | Advanced If/Then             |
|----------|------------------------------|
| 💙 If     | 💙 Burst 💌 4 💌 My Bus 1       |
|          | Insert Event After (AND/OR)  |
|          | Insert Event Before (AND/OR) |
|          | Delete Event                 |
|          | .3: 7777 6666 5              |

As previously mentioned, instead of inserting AND'ed events, add buses/signals to the burst pattern whenever possible to conserve trigger resources.

You can OR burst patterns to effectively increase the sample depth of a pattern (for example, find 3 occurrences of burstA OR burstB OR burstC) provided that the device under test does not send the bursts out of order (or you don't care if it does).

- See Also "To insert or delete events" on page 180
  - "Burst Patterns in Default Storage (16960/16962 logic analyzers)" on page 663
  - "Burst Patterns in "If" Clauses (16960/16962 logic analyzers)" on page 664
  - "Burst Patterns in "Else If" Clauses (16960/16962 logic analyzers)" on page 667
  - "Trigger Errors (16960/16962 logic analyzers)" on page 668
  - Burst Patterns in Default Storage (16960/16962 logic analyzers)  $\bullet$  When a single burst pattern event is specified as default storage, all burst samples are stored.



• When a burst pattern is OR'ed with other events, the union of burst samples and other event samples are stored.

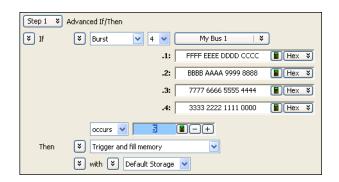
| Default Storage<br>Overridden by store actions in individual trigger steps: |
|---|
| 💐 Store 💐 Burst 💌 4 💌 My Bus 1 🛛 💐  |
| .1: FFFF EEEE DDDD CCCC   |
| .2: BBBB AAAA 9999 8888 🔳 Hex 💙   |
| .3: 7777 6666 5555 4444 🔳 Hex 🎽   |
| .4: 3333 2222 1111 0000 🔳 Hex 💙 🔽   |
| Bus/Signal     My Bus 2     All bits     =     AAAA 5555     Hex V          |

• When a burst pattern is AND'ed with other events, the intersection of burst samples and other event samples are stored.

| Default Storage         Overridden by store actions in individual trigger steps:         Image: Store Im |
|---|
|   |
| .1:   FFFF EEEE DDDD CCCC        Hex ≥  |
| .2: BBBB AAAA 9999 8888   |
| .3: 7777 6666 5555 4444 🔳 Hex 🐳   |
| .4: 3333 2222 1111 0000 🔳 Hex 😻 And 👽   |
| 😻 Bus/Signal 🔽 My Bus 2 😻 All bits 💌 = 🔍 AAAA 5555 📗 Hex 👻  |

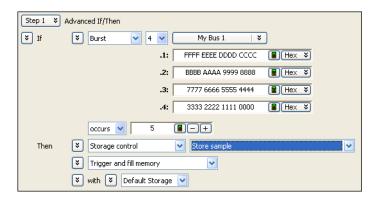
- See Also "To specify default storage" on page 179
  - "To insert or delete events" on page 180
  - "Trigger Errors (16960/16962 logic analyzers)" on page 668

**Burst Patterns in "If" Clauses (16960/16962 logic analyzers)** The occurrence counter associated with the "If" clause in a trigger sequence step takes action on complete burst patterns. For example, you can look for the fifth eventual occurrence of a 4-sample burst:



In the previous example, the logic analyzer counts 20 samples internally – the occurrence count times the burst depth (5 \* 4). The maximum occurrence count of a burst is the maximum single sample occurrence count (as described in the logic analyzer characteristics) divided by the burst depth. In the above example, this is 2E+24 / 4.

The "If" clause action occurs after the last sample of the last burst. If you add a storage control action to "Store sample", it will store the last sample of the last burst.



AND'ed events consider complete burst patterns. In the following example, the action occurs after:

• 5 bursts during which the the flag is set.

| Step 1 🛛                                   | Advanced If/Then                      |  |  |  |  |  |  |  |  |  |
|--|---------------------------------------|--|--|--|--|--|--|--|--|--|
| 😻 If                                       | 💙 Burst 💙 4 💙 My Bus 1 🛛 🛠            |  |  |  |  |  |  |  |  |  |
|  | .1: FFFF EEEE DDDD CCCC II Hex 💐      |  |  |  |  |  |  |  |  |  |
|  | .2: BBBB AAAA 9999 8888 📓 (Hex 💐      |  |  |  |  |  |  |  |  |  |
|  | .3: 7777 6666 5555 4444 📓 Hex 🍣       |  |  |  |  |  |  |  |  |  |
|  | .4: 3333 2222 1111 0000 📓 Hex 💐 And 🗸 |  |  |  |  |  |  |  |  |  |
| Flag  I    I  Is    Set      occurs      5 |                                       |  |  |  |  |  |  |  |  |  |
| Then                                       | Trigger and fill memory               |  |  |  |  |  |  |  |  |  |
|  | 💙 with 🗳 Default Storage 💌            |  |  |  |  |  |  |  |  |  |

OR'ed events consider the maximum number of samples potentially required. In the following example, to potentially capture 10 occurrences of a 4-sample burst event, 40 samples are required. Therefore, it takes 40 samples of matching events for the action to occur. These 40 samples could actually be made up of:

- 10 occurrences of the 4-sample burst event. (This would also be the case if the events were overlapping, that is, if the bus/signal pattern occurred during the burst pattern.)
- 8 occurrences of the 4-sample burst event plus 8 occurrences of the 1-sample bus/signal event ((8 \* 4) + (8 \* 1) = 40 samples).
- 40 occurrences of the 1-sample bus/signal event.
- Any combination of burst events and bus/signal events that add up to 40 samples.

| Step 1 💙 | Advanced If/Then                                      |
|----------|---|
| If       | 🗧 Burst 🔽 4 💌 My Bus 1 🛛 🗧                            |
|          | .1: 0000 Hex V  |
|          | .2: 0101 Hex V  |
|          | .3: 0202 Hex V  |
|          | .4: 0303 📳 Hex 🔻 Or 💌                                 |
|          | 🗧 Bus/Signal 💌 My Bus 2 💙 All bits 💙 = 🔍 FCFC 📳 Hex 💙 |
|          | occurs 🗸 10 📓 — +                                     |
| Then     | Trigger and fill memory                               |
|          | 😻 with 😻 Anything 💌                                   |

#### See Also

- "To specify burst patterns (16960/16962 logic analyzers)" on page 661
  - "Burst Patterns in Default Storage (16960/16962 logic analyzers)" on page 663
  - "Burst Patterns in "Else If" Clauses (16960/16962 logic analyzers)" on page 667
  - "Trigger Errors (16960/16962 logic analyzers)" on page 668

- "To insert or delete events" on page 180
- "To show a trigger sequence step as Advanced If/Then trigger functions" on page 189
- "To convert a trigger sequence step to Advanced If/Then trigger functions" on page 190

**Burst Patterns in "Else If" Clauses (16960/16962 logic analyzers)** Because there is no occurrence counter associated with "Else if" clauses, these clauses act on individual samples, not an entire burst. Therefore, burst patterns within "Else if" clauses are useful for checking whether a sample is in a burst or is not in a burst.

For example, here the "Else if" action occurs if a sample is in the burst pattern:



And, here the "Else if" action occurs if a sample is not in the burst pattern:

| 🗧 Else if not 🗧 Burst 💽 4 💌 | My Bus 1 🛛 🕹 💙              |
|-----------------------------|-----------------------------|
| .1:                         | FFFF EEEE DDDD CCCC         |
| .2:                         | BBBB AAAA 9999 8888 📓 Hex 💐 |
| .3:                         | 7777 6666 5555 4444 🔳 Hex 😻 |
| .4:                         | 3333 2222 1111 0000 🔳 Hex 💙 |
| Then 🛛 Goto                 | ✓ 1 ✓                       |

Negated "Else if" clauses can be used to count consecutive occurrences of a burst pattern by inserting a "Reset occurrence counter" action.

See Also

- "To specify burst patterns (16960/16962 logic analyzers)" on page 661
  - "Burst Patterns in Default Storage (16960/16962 logic analyzers)" on page 663
  - "Burst Patterns in "If" Clauses (16960/16962 logic analyzers)" on page 664
  - "Trigger Errors (16960/16962 logic analyzers)" on page 668
  - "To show a trigger sequence step as Advanced If/Then trigger functions" on page 189

• "To convert a trigger sequence step to Advanced If/Then trigger functions" on page 190

**Trigger Errors (16960/16962 logic analyzers)** These errors can occur when setting up 16960/16962 logic analyzer triggers.

#### No more Burst Recognizer resources available.

This message occurs when the trigger specification requires more burst recognizer resources than are available. You can have up to eight 2-sample burst patterns or four 3- or 4-sample burst patterns.

#### No more Transitional Storage control resources available.

In the 16960 or 16962 logic analyzer's *Transitional / Store Qualified Timing Mode* (see page 659), this message occurs when the trigger specification requires more storage control resources than are available.

#### Trigger Specification is too complex.

In the 16960 or 16962 logic analyzer, this message can occur when the event list expression is too complex. Remember, instead of inserting AND'ed events, add buses/signals to the burst pattern whenever possible to conserve trigger resources (see "To specify burst patterns (16960/16962 logic analyzers)" on page 661).

#### Cannot use <, <=, >, >=, or range on a bus with clock bits that span cards.

In the 16960 or 16962 logic analyzer, a bus that contains clock bits from multiple cards cannot use the <, <=, >, >=, or range operators.

#### Cannot use <, <=, >, >=, or range on a bus that spans cards.

In the 16960 or 16962 logic analyzer, a bus that contains channels from multiple cards cannot use the <, <=, >, >=, or range operators.

#### Multiple Goto actions for same event list (also Branch <number>).

In the 16960 or 16962 logic analyzer, only one Goto action is allowed per "If" or "Else if" clause.

**See Also** • "Trigger Errors" on page 384

#### 16962 Logic Analyzer Notes

- Differences from Other Logic Analyzers (see page 669)
- Channels and Memory Depth (see page 669)
- Timing Mode Sampling Options/Period (see page 669)

• State Mode Sampling (see page 670)

Differences from<br/>Other Logic<br/>AnalyzersCompared to most other logic analyzers supported in the 16900-series<br/>logic analysis system, the 16962 logic analyzer differs in the following<br/>ways:

- You can set threshold voltages on a per channel basis. (Most other logic analyzers let you set threshold voltages on a per pod basis.) For more information, see Setting Threshold Voltages in the 16962 Logic Analyzer (see page 671).
- There is one synchronous sampling (state) analysis mode that is set up differently than most other logic analyzers (see State Mode Sampling (see page 670) below and Setting Up the State Sampling Clock in the 16962 Logic Analyzer (see page 674)).
- Full memory depth is available on all channels. There are no trade-offs between memory depth and channel count. However, using storage qualifiers in the triggering setup can reduce the number samples that are stored.
- You cannot split a 16962 logic analyzer module. (Because of this, and with no memory depth and channel count trade-offs, there is no need for pod assignment.)
- When multiple cards are connected in a multi-card module, there is no notion of master and slave cards. Pods are indexed from the bottom card up.
- Trigger set up resources are different. For more information, see Specifying Advanced Triggers in the 16960/16962 Logic Analyzers (see page 660).
- In *state* sampling mode, the behavior when stopping a running acquisition is different from most other logic analyzers (see Stop Behavior in the 16960/16962 Logic Analyzers (see page 676)).
- You can logically separate analyzer cards that are physically connected into a single module; contact your Agilent Representative for more information.

#### Channels and Memory Depth

| 16962A<br>Memory | Option 004 <sup>*</sup>                      | Option 016 <sup>*</sup> | Option 032 <sup>*</sup> | Option 064 <sup>*</sup> | Option 100 <sup>*</sup> |  |  |  |  |  |
|------------------|--|-------------------------|-------------------------|-------------------------|-------------------------|--|--|--|--|--|
| depth            | 4 M  | 16 M                    | 32 M                    | 64 M                    | 100 M                   |  |  |  |  |  |
| Channels         | 68 channels/card * number of cards in module |                         |                         |                         |                         |  |  |  |  |  |
| 10               | ne 16962A logic a<br>sed Hardware Up         | ,                       | 0                       | lel number E5887        | A. (See also            |  |  |  |  |  |

Timing Mode<br/>Sampling• Full channel (see page 669), 2.0 GHz = Full Channel Timing Mode<br/>SamplingOptions/Period

With this sampling option, you can use the full memory depth (see page 669) of your logic analyzer card, with data being sampled and stored every 500 ps; this rate cannot be changed.

• Half channel (see page 669), 4 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth (see page 669) is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

| els<br>ned Widt |       | to : | sele | ect F | )od | B4) | - |    |      |     |    |    | Slo | it B | Pod | 1 (0 | Click | c to | sel |
|-----------------|-------|------|------|-------|-----|-----|---|----|------|-----|----|----|-----|------|-----|------|-------|------|-----|
|                 | Width | old: |      |       |     |     | Y |    |      | Po  |    |    |     |      |     |      |       | old: | _   |
|                 |       |      |      |       |     |     |   | SI | ot B | Poo | 14 | n  |     |      |     |      |       |      |     |
|                 |       | 7    | 6    | 5     | 4   | 3   | Z | Т  | U    | 15  | 14 | 13 | 12  | 11   | 10  | 9    | 8     | 7    | 6   |
| 7:0]            | 8     |      |      |       |     |     |   |    |      |     |    |    |     |      |     |      |       | 1    | 1   |

Data is sampled and stored every 250 ps; this rate cannot be changed.

• Quarter channel (see page 669), 8 GHz = Quarter Channel Timing Mode

With this sampling option, only one pod of each pod pair and only even-numbered channels on that pod are available, and the memory depth (see page 669) is quadrupled. Channels assigned to unavailable pods/channels are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data is sampled and stored every 125 ps; this rate cannot be changed.

Typically, in quarter channel timing mode, the E5386A adapter is used to reduce the number of probes and connectors required.

• Transitional / Store qualified, (Full, Half, Quarter channel modes) = Transitional / Store Qualified Timing Mode

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period is 500 ps, 250 ps, or 125 ps for the Full, Half, and Quarter channel modes, respectively, and cannot be changed. See transitional timing (see page 422).

State Mode
Sampling
2 Gb/s = General State Mode
The sampling speed matches your device under test's clock rate, from 100 Mb/s up to 2 Gb/s. See Setting Up the State Sampling Clock in the 16962 Logic Analyzers (see page 674).

#### See Also • "Setting Threshold Voltages in the 16962 Logic Analyzer" on page 671

- "Setting up the State Sampling Clock in the 16962 Logic Analyzer" on page 674
- "Stop Behavior in the 16960/16962 Logic Analyzers" on page 676
- "Specifying Advanced Triggers in the 16960/16962 Logic Analyzers" on page 660
- "Eye Scan in Logic Analyzers that Support Differential Signals" on page 428
- "16962 Logic Analyzer Specifications and Characteristics" on page 769

#### Setting Threshold Voltages in the 16962 Logic Analyzer

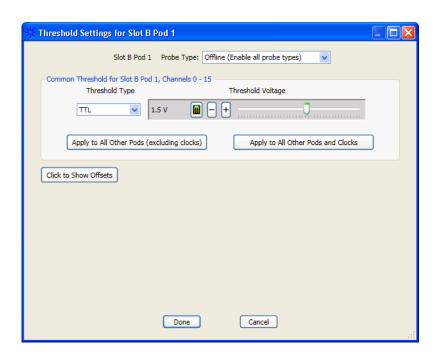
The 16962 logic analyzer lets you set threshold voltages on a per channel basis.

It is important to specify a threshold voltage that matches your device under test. Incorrectly specified threshold voltages result in incorrect data.

- 1 From the menu bar, select Setup>(Logic Analyzer Module)>Bus/Signal....
- 2 In the Buses/Signals Setup dialog, click any **Threshold** button. The Threshold buttons are located under the Pod or Clocks label.

| Display 💙 🔍 🗨  |    |    |    |    |    |    |   |  |   |   |   |   |     |   |   |   |
|----------------|----|----|----|----|----|----|---|--|---|---|---|---|-----|---|---|---|
| Slot B Pod 1   |    |    |    |    |    |    |   |  |   |   |   |   |     |   |   |   |
| Threshold: TTL |    |    |    |    |    |    |   |  |   |   |   |   |     |   |   |   |
|                |    |    |    |    |    |    |   |  |   |   |   | _ | nv. |   |   |   |
| ו              | 15 | 14 | 13 | 12 | 11 | 10 | 9 |  | 7 |   |   | ٤ |     | 2 |   | ٥ |
| - 1            |    |    |    |    |    |    |   |  | 1 | 1 | 1 | 4 | 1   | 1 | 1 | 1 |

**3** In the Threshold Settings dialog:



**a** If offline, select the **Probe Type**; this may affect other settings that can be selected.

When online, the currently connected probe type (if any) is shown in a read-only field.

- **b** Select the **Common Threshold**; you can do this using the **Threshold Type** drop-down or by dragging the slider to the desired setting. You can enter a value from -3.00 to 5.00 V.
  - Click **Apply to All Other Pods (excluding clocks)** if you want the common settings to apply to all pods (excluding clock inputs); otherwise, the settings apply only to the selected pod.
  - Click **Apply to All Other Pods and Clocks** if you want the common settings to apply to all pods and clock inputs.
- 4 If you want to specify individual channel offsets, click **Click to Show Offsets**, and enter the offsets or drag the sliders.

| Threshold Setting                | s for Slot B Pod 1  |                     |  |  |  |  |  |  |  |  |  |
|----------------------------------|---|---------------------|--|--|--|--|--|--|--|--|--|
|                                  | Slot B Pod 1 Probe Type: Offline (Enable all probe types)                     |                     |  |  |  |  |  |  |  |  |  |
|                                  | Common Threshold for Slot B Pod 1, Channels 0 - 15                            |                     |  |  |  |  |  |  |  |  |  |
| Threshold Type Threshold Voltage |   |                     |  |  |  |  |  |  |  |  |  |
| ΠL V H - +                       |   |                     |  |  |  |  |  |  |  |  |  |
| Apply to Al                      | Apply to All Other Pods (excluding clocks) Apply to All Other Pods and Clocks |                     |  |  |  |  |  |  |  |  |  |
| Click to Hide Offset             | ]   |                     |  |  |  |  |  |  |  |  |  |
|                                  | Clear   | All Offsets to Zero |  |  |  |  |  |  |  |  |  |
| Channel                          | Threshold Offset Effe   | ective Threshold    |  |  |  |  |  |  |  |  |  |
| [0] 1.5V +                       | ov 🗑 - +  | = 1.5 V             |  |  |  |  |  |  |  |  |  |
| [1] 1.5V +                       | ov 🗑 - +  | = 1.5 V             |  |  |  |  |  |  |  |  |  |
| [2] 1.5V +                       | ov 🗑 - +  | = 1.5 V             |  |  |  |  |  |  |  |  |  |
| [3] 1.5V +                       | ov 🗑 - +  | = 1.5 V             |  |  |  |  |  |  |  |  |  |
|                                  | Done Cancel   | .:                  |  |  |  |  |  |  |  |  |  |

**5** The 16962 logic analyzer lets you specify threshold voltages for clock channels individually. This may be useful in situations, for example, where the clock channels are probing differential signals while the data channels are probing single-ended signals.

|       |    |    | (  | Clo | ck | s   |     |    |    |    |
|-------|----|----|----|-----|----|-----|-----|----|----|----|
| Width | C  | lo | ck | Th  | re | sha | old | s  |    |    |
| muur  |    |    |    |     |    |     |     | Ч  | ŝ  |    |
|       | A¢ | A3 | A2 | A1  | 84 | 83  | 82  | 81 | 15 | 14 |
| 8     |    |    |    |     |    |     |     |    |    |    |
|       | 1  | 1  |    |     |    |     |     |    |    | 1  |

In the Threshold Settings for Clock Channels dialog:

| K Threshold Setting     | for Clock Channels             |                           |
|-------------------------|--------------------------------|---------------------------|
| Apply the first channel | settings to all clock channels | Clear All Offsets to Zero |
| Slot B Pod 1 Clock      |                                |                           |
| πι 💌                    | 1.5 V 📓 – +                    | ┚────                     |
| + Offset                | ov 📓 – 🕂 🚃 🗍                   | = 1.5 V                   |
| Slot B Pod 2 Clock      |                                |                           |
| ΠL 💌                    | 1.5 V 📓 - +                    |                           |
| + Offset                | ov 📓 – 🕂 🗾 🥄                   | = 1.5 V                   |
| Slot B Pod 3 Clock      |                                |                           |
| TTL 🗸                   | 1.5 V 📓 - +                    | <b>D</b>                  |
| + Offset                | ov 🔋 – + 🗾 🥄                   | = 1.5 V                   |
| Slot B Pod 4 Clock      |                                |                           |
|                         | 15V 🔲 🗌 🕂                      | •                         |
|                         | Done Cancel                    | ]                         |

- **a** Select the first clock channel's threshold using the threshold type drop-down or by dragging the slider to the desired setting. You can enter a value from -3.00 to 5.00 V.
- **b** If you want to specify individual clock channel threshold offsets, enter the offsets or drag the sliders. (To reset all clock channel offets, click **Clear All Offsets to Zero**.)
- **c** Set up thresholds and offsets for the remaining clock channels, or click **Apply the first channel's settings to all clock channels**.
- **NOTE** In the state sampling mode, threshold voltages can be adjusted automatically (along with sample positions). See "To automatically adjust state sampling positions and threshold voltages" on page 130.

#### See Also • "Pod and Channel Naming Conventions" on page 418

#### Setting up the State Sampling Clock in the 16962 Logic Analyzer

The sampling speed matches your device under test's clock rate, from 100 Mb/s up to 2 Gb/s.

| -State Clock Optic |              |   |  |
|--------------------|--------------|---|--|
| Clock Mode:        | Master       | ~ | Thresholds and Sample Positions  |
| State Clock 1:     | Pod B1 Clock | ~ | Both edges 🛛 👻   |
| State Clock 2:     | Pod A1 Clock | * | State Clock 1 and 2 must be the same frequency. Phase can be different.      |
| Clock Ready:       | Pod B2 Clock | ~ | Latched High 🗸 Refer to Clock Ready on-line documentation for usage details. |

The **Clock Mode** lets you select between **Master** and **Dual Sample** modes. These clock modes work the same as in other logic analyzers (see "Selecting the State Sampling Clock Mode" on page 123). After you enable the dual sample clock mode, you actually set it up in the Buses/Signals tab of the Analyzer Setup dialog (see "To set up the dual sample sampling clock mode" on page 127).

The **State Clock** selections let you select the sampling clock inputs. Clock inputs on odd pods can be used for the sampling clock.

Sampling can occur on rising, falling, or both edges of the input clock signal. The input clock signal must be continuous.

Clock inputs on even pods can be used as a **Clock Ready** (a signal whose level indicates when the sampling clock signal is stable). The Clock Ready can be a High or Low level, either Latched or Enabled:

- Latched does not take effect immediately (there will be a few clock stages of delay). This signal is meant to go true sometime after the clock becomes stable, not necessarily exactly on the first stable clock edge. Therefore, this signal cannot be used to gate the clock on and off in a clock qualification mode.
- Enabled takes effect immediately. Therefore, this signal can be used to effectively gate the clock on and off for clock qualification (the logic analyzer will not sample data when the clock is disabled by this signal). However, to achieve this, the clock ready signal must come from the same pod pair as the clock.

Frequency-related sampling clocks can be selected for each pod pair. (Only one clock ready input can be used for all pod pairs.)

In a multi-card module, sampling clock signals should come from a middle card for best performance. In 4- and 5-card modules, you are only allowed to choose a clock from the bottom 3 cards. You have more available delay for sampling position adjustment when the clock comes from a middle card.

16962 Logic Analyzer State Sampling Clock Restrictions

- State Clock 1 and State Clock 2 must always use the same edge qualification.
- If Clock Ready is "Off", then there are no restrictions on State Clock 1 or State Clock 2.

- If Clock Ready is "Latched", then State Clock 1 MUST clock on both edges and State Clock 2 can be on any appropriate Clock or Off.
- If Clock Ready is "Enabled", then State Clock 2 is not available and State Clock 1 and Clock Ready MUST be a Clk1/Clk2 or Clk3/Clk4 pair of the same card.
- See Also "Specifying Advanced Triggers in the 16960/16962 Logic Analyzers" on page 660
  - "16962 Logic Analyzer Notes" on page 668
  - "16962 Logic Analyzer Specifications and Characteristics" on page 769

#### Stop Behavior in the 16960/16962 Logic Analyzers

In the *state* sampling mode, the stop behavior in the 16960/16962 logic analyzers is different from most other logic analyzers.

In situations where a storage qualifier prevents acquision memory from being filled after a Stop (either before or after the trigger is found), the storage qualifier will switch to "all samples" so that acquisition memory can be filled. This lets you see the activity that did not match the storage qualifier. You will be able to identify the point where all samples started being stored by its large time gap.

It is still possible that acquisition memory cannot be filled after a Stop because of a missing clock signal. In this case, there may be some incorrect data in acquisition memory at the end of the trace (as many as the last 13 samples). Remember, the 16960/16962 logic analyzers require a continuous input clock signal.

- See Also "Running/Stopping Measurements" on page 203
  - "16962 Logic Analyzer Notes" on page 668
  - "16962 Logic Analyzer Specifications and Characteristics" on page 769

#### U4154A Logic Analyzer Notes

- Differences from Other Logic Analyzers (see page 676)
- Channels and Memory Depth (see page 678)
- Timing Mode Sampling Options/Period (see page 678)
- State Mode Sampling (see page 679)
- Timing Zoom (see page 679)

Differences from<br/>Other LogicCompared to other Agilent logic analyzers supported in earlier releases,<br/>the U4154A logic analyzer differs in the following ways:AnalyzersThe second sec

• There is no quarter channel timing mode.

- U4154A supports two license based state speeds. A "01G" license sets the maximum state speed of U4154A to 1.4Gbs. A "02G license sets it to 2.5Gbs. These license options do not however control and set the timing speed of the U4154A module.
- There is a single state sampling clock with four qualifiers. The clock qualifiers allow you to sample only when qualifying signal is active so that you can view more system activity. The state sampling clock input is always from Pod1 on the master card in a multi-card set. (The master card is the lower-middle card of a multi-card set). You cannot use the signals from the other pods clock inputs as the sampling clock inputs. For more information, refer to the topic "Setting up the State Sampling Options in U4154A Logic Analyzer" on page 686.
- Advanced probe settings are enabled for U4154A and 16962 logic analyzers. You can enable or disable the peaking at the channel/pod/module level for the probing system used for these logic analyzers. For more information, refer to "Changing Advanced Probe Settings for U4154A and 16962 Logic Analyzers" on page 681.
- Memory depth controls and licensing is different in U4154A Logic Analyzer compared to previous Agilent logic analyzers. Unlike previous logic analyzers, the density of data samples stored in U4154A memory varies with the acquisition mode. The amount of U4154A memory available is fixed based on the memory license that you have purchased. However, there is a variation in the maximum number of samples that you can store in the fixed memory based on the selected acquisition mode.
- You cannot logically split a U4154A logic analyzer module.
- The U4154A module is installed in one of the slots of the Agilent AXIe chassis. It connects to the host PC through the PCIe interface of the AXIe chassis. You can connect two U4154A modules to form a two-card set in an AXIe chassis.
- Colorized Eyescan on all signals is supported to quickly set accurate sample positions and threshold voltages as per the optimal values suggested by the eye scan run. You can also export the eyescan data to a specified .csv file. For more information, refer to "Setting up and Running Eyescans in U4154A Logic Analyzer" on page 690.
- Trigger expansions with more levels and deeper bursts. Burst levels increased from 4 to 8. Faster trigger sequencer rate (with triggers on sequential events upto 2.5 Gb/s). New event counter added for specifying the trigger action. For more information, refer to "Specifying Advanced Triggers in the U4154A Logic Analyzer" on page 688.

• The DDR Setup Assistant tool has been enhanced to support the set up of the U4154A Logic Analyzer module using this tool. The automated setup steps now also include automatically determining and setting the optimal acquisition sample position at the center of the eye on individual channels of U4154A. You can now use this tool to automatically set the sampling positions for command, address, read and write data signals separately while setting up DDR measurement setup with U4154A logic analyzer. The eye scan feature of the U4154A Logic Analyzer is used to accomplish this. To learn more, refer to the DDR Setup Assistant online help integrated with this help.

| Channels and<br>Memory Depth | U4154A<br>Memory | Option<br>002                                | Option<br>004                                    | Option<br>008 | Option<br>016 | Option<br>032 | Option<br>064 | Option<br>128 | Option<br>200 |
|------------------------------|------------------|--|--|---------------|---------------|---------------|---------------|---------------|---------------|
|                              | depth            | 2 M  | 4 M  | 8 M           | 16 M          | 32 M          | 64 M          | 128 M         | 200 M         |
|                              | Channels         | channels<br>In a mult<br>136 chan<br>chassis | inels per U4<br>;)<br>i-card set:<br>inels * num | ber of U41    | 54A module    | es installed  | l in slots o  | f an Agilen   | t AXIe        |

Timing Mode Sampling Options/Period • Full channel 2.5 GHz = Full Channel Timing Mode

With this timing mode sampling option, you can use the full memory depth of your U4154A logic analyzer module, with data sampling period ranging from 400 ps to 10 ns. You can set the sample period using the Sample Period field.

• Half channel 5.0 GHz = Half Channel Timing Mode

With this timing mode sampling option, only one pod of each pod pair is available, and the memory depth is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

|    |    | 15 |    |    |    |   | ick<br>she |   |   |   |   |   |   |   | ×    | <ul> <li>SI</li> </ul> |    | -   |    |    |    | e | sh | old | : Т | TL |   |   |  |
|----|----|----|----|----|----|---|------------|---|---|---|---|---|---|---|------|------------------------|----|-----|----|----|----|---|----|-----|-----|----|---|---|--|
| _  | _  | _  | -  | _  | _  | _ | _          | _ | _ | _ | _ | - | - | _ | 1.00 | S                      | ot | 1 P | od | 4  |    |   | _  | _   |     | _  | - | - |  |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0    | 15                     | 14 | 13  | 12 | 11 | 10 | 9 | 8  | 7   | 6   | 5  | 4 | 3 |  |

Data is sampled and stored every 200 ps; this rate cannot be changed.

• The Quarter channel timing mode is not supported.

#### • Transitional / Store Qualified Timing Mode

This timing mode sampling option provides maximum duration of acquisition because data is only stored when a change from the last value is detected. See transitional timing on page 422. Two sampling options are available in this mode:

- **Transitional / Store qualified, (Full channel mode), 2.5 GHz** With this sampling option, you can use the full memory depth of your U4154A logic analyzer module, with data being sampled at regular intervals but stored only when there is a signal transition across the threshold voltage level. You can set the sampling period from 400 ps to 10 ns for this mode.
- **Transitional / Store qualified, (Half channel mode), 5.0 GHz** -With this sampling option, only one pod of each pod pair is available, and the memory depth is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod. Data is sampled at regular intervals but stored only when there is a signal transition across the threshold voltage level. The sampling period is 200 ps for this mode and cannot be changed.
- State Mode Sampling
   U4154A has two license based state speeds. A "01G" license sets the maximum state speed of U4154A to 1.4Gbs. A "02G license sets it to 2.5Gbs. Based on the license option that you have purchased for U4154A, the maximum available state speed of U4154A is automatically set. If the licensed speed is 1.4Gbs (01G option) and while acquiring data, the clock frequency is found to exceed the maximum state speed available as per the 01G license, an error message is displayed and the data is discarded.
  - There is a single state sampling clock with four qualifiers. In a multi-card set, the sampling clock signals can come only from Pod 1 of the master card in the set. The qualifiers can take clock signal inputs only from the pods 2 to 5 on the master card in the set. The clock can be used as a rising, falling, or both edge clock.
  - U4154A supports Full channel (Master) and Dual sample clock modes. In both these modes, the sampling option is as per the state speed license acquired for U4154A.
- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 256K-depth, 12.5 GHz timing analyzer to sample data every 80 ps on all channels. Timing zoom is available for all acquisition modes.
  - See Also Setting up the State Sampling Options in U4154A Logic Analyzer
    - Changing Advanced Probe Settings for U4154A and 16962 Logic Analyzers

- Specifying Advanced Triggers in the U4154A Logic Analyzer
- Setting up and Running Eyescans in U4154A Logic Analyzer
- U4154A Logic Analyzer Specifications and Characteristics
- Pod and Channel Naming Conventions in U4154A Logic Analyzer

#### Pod and Channel Naming Conventions in U4154A Logic Analyzer

In U4154A Logic Analyzer module:

- Slots are named "1" through "5" in the Agilent AXIe chassis starting with the bottom slot.
- A U4154A module installed in a slot has eight pods. These pods are named "1" to "8".
- A U4154A pod is represented as <Slot\_number\_of\_module><Pod\_number>. For instance, Slot 1 Pod 2 represents the Pod 2 of the U4154A module that you installed in slot 1 of chassis. This pod is also referred to as Pod 1.2 in Logic Analyzer GUI.
- Each pod has 16 data channels named "0" through "15". Pod 2.8[11] represents the channel 11 of the Pod 8 of the module installed in slot 2.

|                     |               |           |     |    |    |    | _  |     |   | SI | ot 1 | I P  | od  | 2  |     |        | _   |   |   |    | Ţ  |    |    |    | 1  | Slo | t 1 | Po | d 1    |      |        |    |
|---------------------|---------------|-----------|-----|----|----|----|----|-----|---|----|------|------|-----|----|-----|--------|-----|---|---|----|----|----|----|----|----|-----|-----|----|--------|------|--------|----|
|                     | Channels      |           |     | _  |    |    | T  | nre | - |    |      |      |     |    | off | se     | t   |   |   | -  |    |    | Th | re | -  |     | _   |    |        | - 01 | ffs    | e  |
| Bus/Signal Name     | Assigned      | Width     |     | -  |    |    |    |     |   | Ma | ste  | er ( | Clo | ck |     |        |     |   |   | -  |    |    |    |    | N  | las |     |    | loc    |      |        | _  |
|                     |               |           | 1   | Ŧ  | Ţ  | I. | 1  | 11  | 1 |    | Ţ    | 1    | 6   | 5  | 4   | 1<br>3 | 1 2 | 1 | - | Ŧ  | Ŧ  |    |    | Ŧ  | 10 | Ŧ   | \$  | 1  | 1<br>6 | -    | ‡<br>4 | \$ |
| CS1#                | Pod 1.1[11]   | 1         | , v | 10 | 14 | 10 | 14 |     |   |    | 0    | 3    | +   |    | -   | *      | -   |   |   | 10 | 14 | 10 | 14 | 1  | 10 | 2   | •   | 1  | 0      | -    | +      | 4  |
| <mark>)⊂</mark> CS# | Pod 1.1[11,8] | 2         | 1   | t- |    | t  |    | 1   |   |    | t    | t    | 1   |    | T   | t      | t   | t | T |    |    |    |    | 1  |    |     | 1   |    |        | Ť    | 1      | -  |
| DATA_R              | Pod 1.3M[5:4  |           |     | F  |    | T  | T  | t   | t |    | 1    | t    | T   |    |     | t      | 1   | 1 | T | 1  |    |    |    |    |    |     |     | -  |        | 1    | 1      | -  |
|                     | Pod 1.3S[5:4, | 25        | 22  |    |    | Γ  | 1  | T   | T |    | 1    | T    |     |    | T   | t      | T   | 1 | T | İ- |    |    |    |    |    |     |     | -  |        | T    | 1      |    |
|                     | Pod 1.3M[1],  | 3         |     |    |    |    |    |     | 1 |    |      | T    |     |    |     |        |     |   |   |    |    |    |    |    |    |     |     |    |        |      | 1      |    |
| 🗩 DQS_W             | Pod 1.3S[1],  | 3         |     | 1  |    |    |    |     | 1 |    |      |      |     |    |     |        |     |   | 1 |    |    |    |    |    |    |     |     |    |        |      |        | _  |
| )_ STAT             | Clks[C2], Pod | 12        |     |    |    |    |    |     |   |    |      |      |     |    |     | 3      |     | 1 |   | 6  |    | 10 | 9  | 8  |    |     | 7   |    |        | 5    |        |    |
| CKE                 | Clks[C2]      | 1         |     | Γ  |    |    |    | T   |   |    |      | Τ    |     |    |     | Γ      |     |   |   |    |    |    |    |    |    |     |     |    |        |      |        |    |
| СК0                 | Clks[C1]      | 1         |     |    |    |    |    |     |   | 1  |      | T    |     |    |     |        |     |   | 1 |    |    |    |    |    |    |     |     |    |        |      | T      |    |
|                     |               | <u>82</u> | 4   | 1  |    |    |    |     |   |    |      | 1    |     |    |     |        | •   |   |   |    |    |    |    |    |    |     |     |    |        |      |        |    |

• Each pod has one clock channel making it a total of eight clock channels for a U4154A module. These clock channels are named C1 through C8. If you have installed multiple U4154A module in an AXIe chassis, then the clock channels of the next U4154A module are named C9 through C16 and so on for the rest of the modules in the set. The following is an example of the clock channels naming convention in U4154A.

| er buses and signals ar | nd the channels the | ev corresi | Done | d to:   |    |    |    |    |      |      |     |      |    |    |    |    |    |   |
|-------------------------|---------------------|------------|------|---------|----|----|----|----|------|------|-----|------|----|----|----|----|----|---|
|                         | 1                   |            |      | 11.2625 |    | _  | _  | _  |      | Clo  | cks |      | _  | _  | _  | _  |    | _ |
| Bus/Signal Name         | Channels            | Width      |      |         |    |    |    | С  | lock | c Th | res | hold | ls |    |    |    |    |   |
| Dus/Signal Name         | Assigned            | Muth       | -    | -       | -  | -  | -  | -  | -    | -    | -   | -    | -  | -  | -  | -  | -  |   |
|                         |                     |            | 28   | 27      | 26 | 25 | 24 | 23 | 22   | 21   | 18  | 17   | 16 | 15 | 14 | 13 | 12 | ł |
| T My Bus 1              | Clks[C9:C8,C1]      | 3          |      |         |    |    |    |    |      | 1    | 1   |      |    |    |    |    |    |   |

The clock channel of Pod 8 of the U4154A module installed in slot 1 is represented as:

- 18
- Clk8
- C8

Similarly, the clock channel of Pod 4 of the U4154A module installed in slot 2 is represented as:

- 24
- Clk12
- C12

The input from the clock channel of Pod 1 is used as the state sampling clock input. If you have installed multiple U4154A cards in chassis, then the clock of Pod 1 of the master card in the set is used as the state sampling clock. For instance, if there are five cards in the set, then the third card from the bottom is the master card. The clock of Pod 1 of this card is the state sampling clock.

#### **Changing Advanced Probe Settings for U4154A and 16962 Logic Analyzers**

You can change the settings for the probes used with the U4154A / 16962 logic analyzers. You can enable peaking for channels of these logic analyzers to compensate for the additional high frequency attenuation that some probing solutions provide on target signals. Enabling the peaking can improve the capture window of the input signals by peaking the edges of the input signals. This is particularly useful in situations when the additional attenuation on target signals becomes significant at high frequencies and DDR3 edge rates.

When you enable peaking with the DDR3 Eyefinder tool, it can increase the capture window for the data signals therefore providing increased accuracy for capturing the data. (The DDR3 Eyefinder tool helps you set the appropriate sampling positions for read and write data signals to capture DDR data. it is specifically designed to find DDR3 data signal eyes.)

It is recommended that you run the DDR3 Eyefinder tool on the high-speed target systems with the peaking enabled and then disabled to determine the setting that best suits the target system.

#### CAUTION

Changing the peaking settings can improve or reduce the performance of the probing system. For instance, if the DDR BGA Interposer probe is used at speeds of DDR3-1600 or higher, enabling the peaking results in improving the capture window.

#### NOTE

The advanced probe settings feature is only supported for U4154A and 16962 logic analyzers.

To change probe settings, you must first enable the probe settings and then adjust these settings. These procedures are described below.

# To enable Advanced Probe Settings (APS) for the Logic Analyzer Module

- 1 From the menu bar, select **Edit** > **Options**.
- 2 In the **Options** dialog, select the **Enable Advanced Probe Settings** (APS) checkbox.
- 3 Click OK.

| Options  |     |  |                      |
|--|-----|--|----------------------|
| System<br>Trigger <u>H</u> istory Depth:<br>Recent <u>F</u> ile List Entries:<br>Repetitive Run <u>D</u> elay (see |     | <ul> <li>Start Maximized</li> <li>Create Demo Data when offline</li> <li>Go to Trigger on Run</li> <li>Enable Numeric Grouping</li> <li>Default Folders</li> </ul> | OK<br>Cancel<br>Help |
| Bus/Signal Naming  |     | (Applies to supported module only) —<br>ed Probe Settings (APS)  |                      |
| Message Dialogs/Event Lo  Show Information Dial  Show Warning Dialogs  Show Error Dialogs Event Logging            | ogs | - + and Below  |                      |

On enabling the advanced probe settings in the Options dialog, the **APS** button is added to the **Buses/Signals** tab of the **Analyzer Setup** dialog of the logic analyzer module. You can use this button to view and change the advanced probe settings.

| ses/Signals<br>nter buses a | Sampling<br>nd signals an | d the channels | they corr | resp | on | d to | ): ( |    |    |    |         |   | _          | PS |     | _       | ispl | ay   | ×   | 0 | Q | 0  | 2     |
|-----------------------------|---------------------------|----------------|-----------|------|----|------|------|----|----|----|---------|---|------------|----|-----|---------|------|------|-----|---|---|----|-------|
| Ruo Cim                     | nal Name                  | Channels       | Width     |      |    |      |      |    |    |    | s<br>Th | - | t A<br>she |    |     | -       |      |      | 900 |   |   |    |       |
| bus/sigi                    | iai name                  | Assigned       | widdi     | 1    | 0  | 15   | 14   | 13 | 12 | 11 | 10      | 9 | 8          | 7  | 6   | 5       | 4    | 3    | 2   | 1 | 0 | 15 | 14    |
|                             | 9us 1                     | Pod A1[7:0]    | 8         |      | -  |      |      |    | 17 |    |         |   |            |    |     |         |      |      | 170 |   |   |    |       |
|                             |                           |                |           |      |    |      |      |    |    |    |         |   |            |    |     |         |      |      |     |   |   |    |       |
| )                           | elete                     | Delete Al      |           |      |    |      |      |    |    |    |         |   |            | r  | 1.0 | t verte |      | etli |     |   | r |    | iyste |

To change the Advanced Probe Settings for the Logic Analyzer Module

- 1 From the menu bar, select **Setup > Bus/Signal**.
- 2 In the **Buses/Signals** tab of the Analyzer Setup dialog, click the **APS** button.

The **Advanced Probe Settings** dialog is displayed. All the logic analyzer cards that you installed in different slots of the chassis to make up the logical module are displayed. On expanding a slot, the pods available for that logic analyzer card are displayed. Each pod further expands to the supported channels per pod. The following screen displays the advanced probe settings dialog for the U4154A logic analyzer. In this screen, the logical module comprises of two U4154A modules installed in slot A and B of the AXIe chassis. For each U4154A, there are eight pods available. Each of these pods expands to 16 data channels and 1 clock channel.

| Advanced Probe Settings   |   |
|---|---|
| For trained operators only!   |   |
| The Advanced Probe Settings dialog allows changing low lev<br>system for this module. The effect of a change may not be o<br>as well as improve, the performance of the probing system i<br>settings are provided for use by probing solution d | vious, and could reduce,<br>your application. These |
| Click Cancel now to continue using the current  | settings.   |
| Click checkboxes to enable (checked) or disable (unchecked) P   | aking for that group or                             |
| channel.  |   |
| 🗉 🗌 Module  | <u>^</u>  |
| Slot A  |   |
|   |   |
|   |   |
|   |   |
|   |   |
| B Pod 6   |   |
|   |   |
|   |   |
| 🖃 🔲 Slot B  |   |
| 🖃 📃 Pod 1   |   |
| Pod 1[0]  |   |
| Pod 1[1]  | ~   |
| Default OK  | Cancel  |

- **3** You can choose to enable the peaking at the channel/pod/slot/logical module level by selecting the checkbox displayed with these options. By default, peaking is disabled at all these levels.
- 4 Click OK.

| ses/Signals Si                                     | ampling                   |                          |                 |                 |                       |   |  |
|--|---------------------------|--------------------------|-----------------|-----------------|-----------------------|---|--|
| Acquisition<br>C Timing - As<br>C State - Syr      | 6                         |                          | 2<br>2          |                 |                       |   | Trigger Position<br>50 <u>■ - +</u> % Poststore              |
| Timing Options<br>Sampling Optic<br>Sampling Peric | ons: Half Ch              |                          | GHz<br>+        |                 |                       | T | Force Prestore   |
| State Options                                      | Specify wł                | nen the log              | c analyzer      | should acc      | quire samp            |   |  |
| -State Options -<br>Clock Mode:                    | Specify wh                |                          | c analyzer      | should acc      | quire samp            |   | Eye Scan: Sample Positions and Threshol                      |
|  |                           |                          | c analyzer      | should acc      | quire samp<br>Pod 1.1 |   |  |
| Clock Mode:  | Dual S                    | ample                    | •               | [               |                       |   | Eye Scan: Sample Positions and Threshol                      |
| Clock Mode:<br>Pod:                                | Dual S<br>Pod 1.5<br>Clk5 | ample Pod 1.4 Clk4       | Pod 1.3<br>Clk3 | Pod 1.2         | Pod 1.1<br>Clk1       |   | Eye Scan: Sample Positions and Threshol<br>Clock Description |
| Clock Mode:<br>Pod:<br>Clock:                      | Dual S<br>Pod 1.5<br>Clk5 | ample<br>Pod 1.4<br>Clk4 | Pod 1.3<br>Clk3 | Pod 1.2<br>Clk2 | Pod 1.1<br>Clk1       |   | Eye Scan: Sample Positions and Threshol<br>Clock Description |

# Setting up the State Sampling Options in U4154A Logic Analyzer

The U4154A state sampling speed matches your device under test's clock rate, from 100 Mb/s up to 2.5 Gb/s.

The state sampling clock inputs let signals from the device under test specify when data should be captured.

U4154A provides the following two license options for state mode speeds (2.5Gb/s and 1.4Gb/s) at which the state sampling clock matches input clock edges from the device under test.

- **2.5 Gb/s speed** If you have the 02G license for U4154A module, then the maximum available state speed of U4154A is automatically set to 2.5Gb/s.
- **1.4 Gb/s speed** If you have the 01G license for U4154A module, then the maximum available state speed of U4154A is automatically set to 1.4Gb/s. If, while acquiring data, the clock frequency is found to exceed the maximum state speed available as per the 01G license, an error message is displayed and the data is discarded.

## State Sampling Clock Mode

The state sampling clock mode specifies how the clock inputs are used for sampling. There are two state sampling clock modes to choose from:

- Master all pods sampled on one master clock.
- **Dual Sample** one pod in the pod pair sampled on one master clock but with different delays. When you enable this clock mode, the next step is to set up the pod pairs that you want to be dual sampled in the Busses/Signals tab of the Analyzer Setup dialog box (see "To set up the dual sample sampling clock mode" on page 127). Data on the active pod in a dual sampled pod pair is sampled twice (as master sample and second sample).

| Buses/Signals | Sampling     | 1             |            |      |     |     |      |     |    |                 |     |     |     |     |    |    |       |   |   |   |    |    |    |    |     |    |     |     |     |      |     |   |
|---------------|--------------|---------------|------------|------|-----|-----|------|-----|----|-----------------|-----|-----|-----|-----|----|----|-------|---|---|---|----|----|----|----|-----|----|-----|-----|-----|------|-----|---|
| Enter buses a | nd signals a | and the chann | els they a | corr | esp | ond | d to | );  |    |                 |     |     |     |     |    |    |       |   |   |   |    |    |    |    |     |    |     |     | Dis | play | y : | ¥ |
|               |              |               |            |      |     |     | S    | lot | 21 | <sup>0</sup> 00 | 12  | (M  | as  | ter | S  | am | ple   | ) |   |   |    |    | SI | ot | 2 F | 00 | 2   | (Se | eco | nd   | Sa  | T |
| and the       |              | Channels      |            | 1    |     |     |      |     | Ne | o p             | rol | be  | att | ac  | he | d  | ane e |   |   |   |    |    |    | -  |     |    | - 3 | -   |     |      |     |   |
| Bus/Sig       | nal Name     | Assigned      | Width      |      |     |     |      | _   | _  | ۵               | lua | I S | ап  | ple | e  | _  | _     |   |   |   | 1  |    |    |    |     |    |     |     |     |      |     |   |
|               |              |               |            | -    | -   | -   | -    | -   | -  | -               | -   | -   | -   | -   | -  | -  | -     | - | - | _ | -  | -  | -  | -  | -   | -  | -   | -   | -   |      | -   | - |
|               |              |               |            | 0    | 15  | 14  | 13   | 12  | 11 | 10              | 9   | 8   | 7   | 6   | 5  | 4  | 3     | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11  | 10 | 9   | 8   | 7   | 6    | 5   | 4 |

The pods for which you select the dual sample mode have their associated clock bit also dual sampled. The active clock bit of the pods in a dual sampled pod pair is the clock bit of the selected active pod in that pod pair. notice that in the following screen, the clock channels of the dual sample pod pair (pod 1.3 and pod 1.4) are also dual sampled. These dual sampled clocks are represented as 13 M or C3M and 13 S or C3S (C3 Master Sample and C3 Second Sample).

|    |    |    |    |    |    |      | Clo  | cks | 3    |    |    |       |     |    |   |
|----|----|----|----|----|----|------|------|-----|------|----|----|-------|-----|----|---|
| _  |    |    |    |    | С  | lock | t Th | res | hold | ls |    |       |     |    |   |
|    | 1  |    | Ţ  |    | -  |      | -    |     | -    |    | -  |       | -   | -  |   |
| 28 | 27 | 26 | 25 | 24 | 23 | 22   | 21   | 18  | 17   | 16 | 15 | 13.00 | 135 | 12 | 1 |

For instructions on setting up these state sampling clock modes, see:

- "To set up the master only sampling clock mode" on page 125
- "To set up the dual sample sampling clock mode" on page 127

## State Sampling Clock and Qualifiers

In U4154A, only one state sampling clock is provided. The state sampling clock is the clock of Pod 1 of the master card (the lower middle level card in the set). To know which card is the master card in the set, click **System Summary** button in the Busses/Signals tab of the Analyzer Setup dialog box.

You can choose the sampling to occur on rising, falling, or both edges of the input clock signal.

There are four qualifiers available for the state clock. The clock inputs of pods 2 to 5 are used as the state clock qualifiers. In a multi card set, the clock inputs of pods 2 to 5 of the master card in the set are used as the state clock qualifiers.

You cannot use the signals from the other pods clock inputs as the sampling clock inputs or its qualifiers.

In the following screen, the clock channel (Clk1) of pod 1 of the master card (first card from bottom in the set of two cards) is used as the sampling clock. Clk2, Clk3, Clk4, and Clk5 are the state clock qualifiers.

| Clock Mode: | Dual S  | ample   |         | l       |                    | C AND 💿 OR Clock Qualifiers            |
|-------------|---------|---------|---------|---------|--------------------|--|
| Pod:        | Pod 1.5 | Pod 1.4 | Pod 1.3 | Pod 1.2 | Pod 1.1            | Clock Description                      |
| Clock:      | Clk5    | Clk4    | Clk3    | Clk2    | Clk1               |  |
| Activity:   |         |         |         |         |                    |  |
| Master:     | X ×     | 1 ×     | 0 \$    | 1 ×     | <u></u> <b>₹</b> ≈ | Clk1↑ AND (Clk2=1 OR Clk3=0 OR Clk4=1) |

You can use the "AND"/ "OR" conditional operators with the state clock qualifiers to add conditions and completely describe the clock as a combination of edges and highs or lows.

## **Determining Optimal Sample Positions and Thresholds**

In the state sampling acquisition mode, you need to adjust the sampling positions on each U4154A channel relative to the sampling clock to make sure data is sampled when it is valid.

You can use the eye scan feature of the U4154A Logic Analyzer to automatically determine and set the optimal sample positions and thresholds for the individual signals. Clicking the **Eye scan: Sample Positions and Threshold** button in the **Sampling** tab displays the Eye Scan - Sample Positions and Threshold Settings dialog box where you can set up and run the eye scan measurement for U4154A channels. Refer to the topic Setting up and Running Eyescans in U4154A Logic Analyzer to learn more.

## Specifying Advanced Triggers in the U4154A Logic Analyzer

When setting up advanced triggers, the U4154A logic analyzer has some differences from previous logic analyzers. This topic highlights these differences:

- Up to eight trigger sequence steps are available.
- 2.5 GHz trigger sequencer enables reliable trigger and capture of DDR3 signals at speed.
- There is one timer available in the timing sampling mode as well as the state sampling mode.

• An Occurrence counter is available in each sequence step to count eventual occurrences. You can achieve a consecutive occurrence counter by using "Else if" clauses with the "Reset occurrence counter" action.

#### **Event counter**

In a U4154A trigger sequence step, you can add an "Event counter" as the trigger action. You can Increment or Reset this event counter in the trigger sequence.

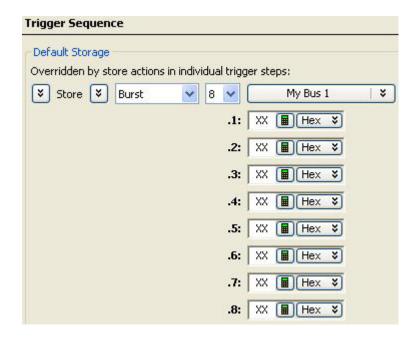
| Trigger Sequ | ence                    |
|--------------|-------------------------|
| Step 1 🛛 🕹   | Advanced If/Then        |
| 💙 If         | X Anything              |
|              | occurs 🔽 1 🔳 — +        |
| Then         | Event Counter           |
|              | Trigger and fill memory |

## **Specifying Burst Patterns**

You can specify the Burst pattern event type in a trigger sequence step. The burst level has been increased to 8 in U4154A Logic Analyzer allowing you to specify a maximum of eight samples in the burst pattern event.

| Step 1 ¥ | Advanc | ed If/Then |     |     |            |   |
|----------|--------|------------|-----|-----|------------|---|
| ¥ If     | *      | Burst      | ٤ 🖌 | 8 🗸 | My Bus 1   | * |
|          |        |            |     | .1: | XX Hex V   |   |
|          |        |            |     | .2: | XX Hex ¥   |   |
|          |        |            |     | .3: | XX Hex V   |   |
|          |        |            |     | .4: | XX Hex ¥   |   |
|          |        |            |     | .5: | XX Hex V   |   |
|          |        |            |     | .6: | XX Hex V   |   |
|          |        |            |     | .7: | XX 🔳 Hex 😻 |   |
|          |        |            |     | .8: | XX Hex 🕏   |   |
|          |        | occurs 🗸   | 1   | 1   |            |   |

In the **Default Storage** of a trigger, you can specify a maximum of eight burst patterns to store burst samples as the default storage.



## Setting up and Running Eyescans in U4154A Logic Analyzer

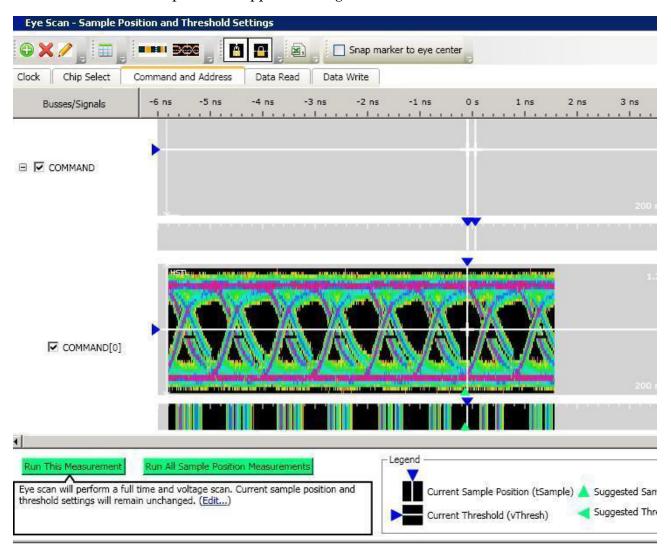
The U4154A logic analyzer allows you to set up and run eyescans for automatically adjusting the state mode sampling positions and threshold voltages of address and control signals so that data is sampled when it is valid. This topic describes how you can set up and run the eyescan measurements when using the U4154A Logic Analyzer.

For U4154A, you can set the sampling positions and threshold voltages for signals in an eyescan measurement and then run the measurement to allow U4154A logic analyzer to find out and suggest optimal sample positions and threshold voltages for these signals. You can then choose to set the sampling position and threshold voltages suggested in the eyescan run or manually adjust these settings based on the suggested values.

When you run an eyescan measurement, logic analyzer determines the threshold voltage that results in the widest possible data valid window by examining the signals from the DUT. Then logic analyzer determines the location of the data valid window in relation to the sampling clock, and suggests the ideal threshold voltage and sampling position.

Eyescan sets the sample position on individual channels of U4154A and therefore, is an easy way to get the smallest possible logic analyzer setup/hold window to accurately capture data.

You use the **Eye Scan - Sample Position and Threshold Settings** dialog box to set up and run eyescan measurements for U4154A channels. The following screen displays this dialog box with five predefined eyescan measurements - Clock, Chip Select, Command and Address, Data Read, and Data Write. The eyescan results of the Command and Address eye scan measurement is shown. The eyescan diagram is displayed for channel 1 of pod 1.1 mapped to a signal named COMMAND.



#### Creating an eyescan measurement

In an eyescan measurement, you:

- select buses/signals on which you want to run the eyescan measurement. For these buses/signals, you can select either all or specific U4154A channels mapped to these buses/signals.
- set the sample positions and thresholds for the selected signals.
- select the eyescan parameters including the type of eyescan run.

#### Before creating an eyescan measurement

Ensure that you have:

- **1** Connected the U4154A logic analyzer channels to the appropriate signals on the DUT to probe the DUT.
- **2** Assigned bus/signal names and mapped the names to the U4154A channels that you used in step1. You use the Buses/Signals tab of the Analyzer setup dialog box to do this.
- **3** If you already set the threshold voltages for channels in the Buses/Signals tab, then these settings will be displayed as the current threshold settings in the eyescan setup.
- 4 Selected the state (synchronous sampling) mode.
- 5 Set the state sampling clock options. (see Setting State Sampling Options in U4154A)

#### To create an eyescan measurement

1 Click the **Eye Scan: Sample Positions and Thresholds** button in the **Sampling** tab of the **Analyzer setup** dialog box.

The Eye Scan - Sample Position and Threshold Settings dialog box is displayed.

- 2 A Default Measurement is displayed with the currently mapped buses/signals and channels. For each channel, the current threshold voltage and sample position is displayed. You can either rename this measurement by right-clicking this measurement and selecting Rename. Or you can create a new measurement by clicking the Add New Measurement toolbar button.
- 3 Click the tab of the new measurement that you created.
- **4** Assign signals/buses to this measurement so that eyescan is run on the assigned signals only. To do this:
  - a Click 🗐 Assign Buses / Signals to Measurements toolbar button.
  - b All the buses/signals that you created in the Analyzer setup dialog box are displayed. You can expand these to display the mapped U41554A channels.
  - **c** Select the checkbox displayed with a bus/signal on which you want to run the eyescan. This selects all the channels that are a part of the bus/signal. Alternatively, you can select individual channels from the different buses/signal names by selecting the checkbox displayed with a channel.
  - d Click OK.
- **5** All the signals that you selected are now displayed in the measurement tab. The current threshold type, threshold voltage, and sample position settings are also displayed for each of these signals. These settings are editable. If needed, you can edit these settings.



- 6 Click Edit to customize the eyescan run options.
- 7 Select the appropriate scan options and click OK.

After you have created an eyescan measurement, you can edit the measurement to customize how you want the U4154A Logic Analyzer to run the eyescan measurement. You do this by clicking **Edit Current Measurement** button in the Eye Scan - Sample Position and Threshold Settings dialog box. Refer to the topic *Customizing an Eyescan Measurement* to know more.

## Creating multiple eyescan measurements

You can also create multiple eyescan measurements to use different eye scan parameters for different signals. For instance, you can create a measurement for control signals to perform a simple time scan and another one for data read and write signals to do a full time and voltage scan.

## NOTE

If you need to create multiple eye scan measurements, you can include a signal in only one of these measurements for setting the signal's sample position. This ensures that you get the eye scan results for a signal in only that measurement. If you assign a signal that already exists in a measurement to another measurement, then the signal is automatically removed from the earlier assigned measurement.

| Assign Busses/Sign                         | als to Sample P | osition Measurem   | ents 🔳                   |       |
|--|-----------------|--------------------|--------------------------|-------|
| Busses/Signals                             | Clock Chip Sel  | ect Command and Ad | dress Data Read Data Wri | te 🔼  |
| CK0  |                 |                    |                          |       |
| CK1  |                 |                    |                          |       |
|  |                 |                    |                          |       |
| CS#  |                 |                    |                          |       |
| RAS#                                       |                 | $\checkmark$       |                          |       |
| CAS#                                       |                 |                    |                          |       |
| WE#  |                 |                    |                          |       |
| ACT#                                       |                 | <b>V</b>           |                          |       |
| COMMAND                                    |                 |                    |                          |       |
| RESET#                                     |                 |                    |                          |       |
| ALERT#                                     |                 |                    |                          |       |
| CHIPID                                     |                 |                    |                          |       |
| ⊞ BA                                       |                 |                    |                          |       |
| ⊞ BG                                       |                 |                    |                          |       |
| ADDR     ROWADDR                           |                 |                    |                          |       |
| E COLADDR                                  |                 |                    |                          |       |
| E ODT                                      |                 |                    |                          | _     |
| E STAT                                     |                 |                    |                          |       |
| DATAR                                      | 88              | H                  |                          |       |
| ■ DATAR_7-0                                |                 | H                  |                          |       |
| ■ DATA <u>R</u> 15-8                       |                 | H                  |                          |       |
| ■ DATA <u>R</u> 13-6 ■ DATA <u>R</u> 23-16 |                 | H                  |                          |       |
| ⊡ DATA <u>N</u><br>∃ DATA <u>W</u>         |                 | E C                |                          |       |
| ■ DATAW<br>■ DATAW_7-0                     |                 | E C                |                          |       |
|  |                 | E C                |                          |       |
| ■ DATA <u>W</u> 13-0 ■ DATA <u>W</u> 23-16 |                 |                    |                          | ~     |
|  |                 |                    | ОК                       | ancel |
|  |                 |                    |                          | ancer |

## **Customizing an Eyescan Measurement**

Once you have created an eyescan measurement, you can configure various settings in the **Eye Scan - Sample Position and Threshold Settings** dialog box to customize how you want the U4154A Logic Analyzer to run the eyescan measurement. For instance, you can set eyescan parameters such as the type of eyescan run or the eyescan resolution.

To customize an eyescan measurement, you edit the measurement by clicking **Edit Current Measurement** toolbar button in the Eye Scan - Sample Position and Threshold Settings dialog box. On clicking this button, the following dialog box is displayed with various configurable eyescan options organized in different tabs.

| Edit  | Measurem                                     | ent   |                   |                      |                       |   |
|-------|--|---|-------------------|----------------------|-----------------------|---|
| Scan  | Display                                      | Scan Qualification  | Advanced          |                      |                       |   |
| 00    | Dimensions<br>)o time scan<br>)o full time/v |   |                   |                      |                       |   |
| ٧L    | .ock sample p                                | Position and Threshold<br>positions. (Sample posit<br>ds. (Thresholds are not | ions are not char |                      |                       | not be changed manually.)<br>red manually.) |
| The s | ettings above                                | e will have the following   | result when the   | measurement is ru    | n:                    |   |
| Eye   | scan will per                                | form a full time and vol  | tage scan. Curre  | nt sample position a | and threshold setting | s will remain unchanged.                    |
|       |  |   |                   |                      |                       |   |

Based on the combination of edit options that you select to customize the eye scan, an explanation of the expected eyescan results is displayed in the **Eye Scan - Sample Position and Threshold Settings** dialog box as follows.

| Run This Measurement | Run All Sample Position Measurements  |
|----------------------|---|
|                      | e the middle threshold. Then, it will perform a time-only scan at the current and middle thresholds. At t<br>ideal sample position will be automatically set. Threshold settings will remain unchanged. ( <u>Edit</u> ) |

This topic describes some of the configurable options for eyescan.

## Types of eyescans:

- **Time scan only** This eyescan option performs a full time scan at the middle threshold voltage and suggests the optimal sample position. It sets the threshold voltage and sample positions based on the optimal values depending on whether or not you selected to lock the current threshold and sample position settings.
- **Time and voltage scan** This eyescan option finds the signal activity envelop and adjusts the threshold voltage to determine the optimal threshold voltage. Then it performs a full time scan at that threshold to suggest the optimal sample position. It sets the threshold voltage and sample positions based on the optimal values depending on whether or not you selected to lock the current threshold and sample position settings.

Locking the current settings

At times, you may want to run the eyescan to view the suggested optimal settings but do not want logic analyzer to automatically adjust your current settings based on the eyescan results. In such a situation, you can lock your current threshold and sample position settings to ensure that the eyescan run suggestions do not automatically alter your current settings. By locking the settings, you lock these for manual adjustments as well. If you do not lock these settings, then eye scan run automatically adjusts the current settings as per the suggested optimal settings. You can later choose to retain these adjusted settings or modify manually. The following screen displays these lock settings that are available in Edit Measurement dialog box.

Automatic Sample Position and Threshold Modification

Lock sample positions? (Sample positions are not changed when a scan is completed and cannot be changed manually.

Lock thresholds? (Thresholds are not changed when a scan is completed and cannot be changed manually.)

#### Setting eyescan resolution

You can select the eyescan resolution that you want for the resulting scans. If you have the 02G license option for U4154A module, then you can select either Normal or High resolution for the scans. However, if you have the 01G license option for the U4154A module, then only the Normal resolution option is available. The High resolution option is disabled for 01G license.

If you select the Normal option, you get a time resolution of 20 ps in scans. With the High resolution option, you get a time resolution of 4.8 ps in scans.

The following screen displays these two resolution options.

| Scan Display Scan Qualification Advanced  |   |
|---|---|
| Number of clock cycles measured at each offset position         Short (50,000) - Requires frequent transitions         Medium (500,000) - Default         Long (5,000,000) - Better for infrequent transitions         Custom -         500000         Clocks   | Run Mode         Demo Mode (no probes required)         Enable sample position warnings         Scan Limits         Min       Image ns         Max       Image ns |
| <ul> <li>Complete eye scan - scan all points regardless of signal activity</li> <li>Scan Resolution         <ul> <li>Normal - Faster scan adequate for setting sample positions on most systems.</li> <li>High - Detailed scan for high-speed systems with smaller eyes or for optimal bus-level signal integrity insight.</li> </ul> </li> </ul> | Default Scan Limits Unit Interval Control Use this control to adjust left or right the "windo scan will be performed.   |

## Configuring Unit Interval (UI) settings

There may be a situation when the eyes in which you want to set the sampling positions are outside of the adjustment range in the eyescan. In such a situation, you can configure the unit interval settings to move the signals left or right (in relation to the zero time) by Unit Interval (clock cycle) amounts. You can use the left and right arrow keys displayed in the **Unit Interface Controls** section to adjust the window on which the eyescan will be performed. The currently applicable scan window is represented by the green shaded area. Each mark to the left represents a whole clock cycle. Moving the slider to the left results in the data eyes moving left in the display after rerunning a scan.

After configuring the unit interval settings, you must rescan and then set the sampling positions again.

## 12 Reference

| Edit Measurement  |   |
|---|---|
| Scan Display Scan Qualification Advanced  |   |
| Measurement Duration  | Run Mode  |
| Number of clock cycles measured at each offset position         Short (50,000) - Requires frequent transitions         Medium (500,000) - Default         Long (5,000,000) - Better for infrequent transitions         Custom -         500000         Clocks   | Demo Mode (no probes required) Enable sample position warnings Scan Limits Min Signs Max Signs Max Cigns Ci |
| <ul> <li>Complete eye scan - scan all points regardless of signal activity</li> <li>Scan Resolution         <ul> <li>Normal - Faster scan adequate for setting sample positions on most systems.</li> <li>High - Detailed scan for high-speed systems with smaller eyes or for optimal bus-level signal integrity insight.</li> </ul> </li> </ul> | Default Scan Limits Unit Interval Control Use this control to adjust left or right the "window" over scan will be performed.  |

## **Running an Eyescan**

After you have created an eyescan measurement and customized it to suit your specific requirements, you can run the eyescan measurement. This allows U4154A logic analyzer to determine and suggest optimal values for sample positions and thresholds.

If you created multiple eyescan measurements, you can either run these measurements separately or as a sequential batch. In a sequential batch, the measurements are run in the same order in which these are displayed in the tabbed list.

#### To run an eyescan measurement

- 1 Click the tab of the eyescan measurement that you want to run in the **Eye Scan Sample Position and Threshold Settings** dialog box.
- 2 Click Run this measurement.

To run multiple eyescan measurements

1 Click **Run All Sample Position Measurements** in the **Eye Scan** - **Sample Position and Threshold Settings** dialog box.

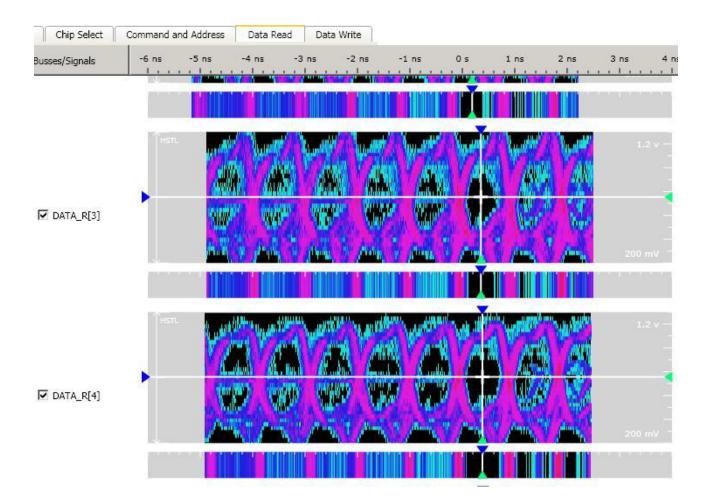
Interpreting the eyescan results and eye diagrams

By performing full time and voltage scans, U4154A is able to give you a map of transitions detected in small windows of time and voltage. These scans are called eyescans.

The eyescan results show:

- Suggested sampling positions and threshold voltages (green triangles).
- The current sampling positions (vertical blue lines in stable regions, red lines in transitioning regions) and threshold voltages (horizontal blue lines in stable regions, red lines in transitioning regions).
- A digital "eye" diagram that represents many samples of data captured in relation to the sampling clock. The transitioning edges measured before and after the sampling clock result in a picture that is eye-shaped. Eye diagrams are used to display the measurement data.

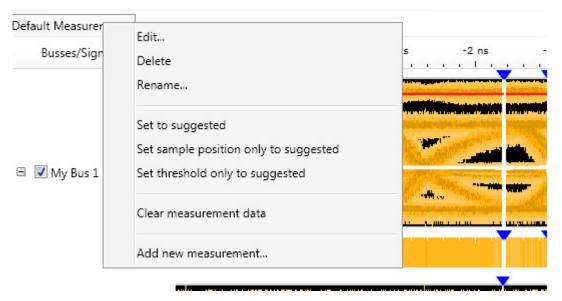
The following screen displays the results of a time and voltage eye scan run on the data read signals. The current settings have been automtaically adjusted by the eye scan based on the optimal settings determined during the eye scan.



## Adjusting sample positions and thresholds

## Setting sample positions for all signals to their suggested positions

You can set the sample positions for all the signals included in a measurement to their suggested sample positions displayed in the eyescan results in a single click. To accomplish this, right-click the measurement and select the **Set sample position only to suggested** option.



You can also set the thresholds to their suggested threshold values by clicking the Set threshold only to suggested option. The Set to suggested option sets both the sample positions and thresholds to their suggested values.

## Adjusting/moving the sample positions manually

After viewing the eyescan results, if needed, you can mark the ideal sample position for each signal by manually moving the sample position markers in the eyescan. You do this:

- either by dragging and dropping the sample position markers to the required positions.
- or by clicking on the required position. This automatically moves the marker to the clicked position. For this, you need to select the **Click to move markers** checkbox. By default, this checkbox is deselected.

While adjusting the sample positions, you may want to deselect the **Snap marker to eye center** checkbox to get greater control over the sample position placements. On deselecting this checkbox, the sample position markers are set exactly at the same position at which you dropped the

marker or clicked. When this checkbox is selected, the sample position marker is set at the center of the eye irrespective of where you clicked or dropped the marker while moving it.



If the eyes in which you want to set the sampling positions are outside of the adjustment range in the eyescan, you can configure the unit interval settings to move the signals left or right (in relation to the zero time) by Unit Interval (clock cycle) amounts. You can use the left and right arrow keys displayed in the Unit Interface Controls section to adjust the window on which the eyescan will be performed. The currently applicable scan window is represented by the green shaded area. Each mark to the left represents a whole clock cycle. Moving the slider to the left results in the data eyes moving left in the display after rerunning a scan.

After configuring the unit interval settings, you must rescan and then set the sampling positions again.

| Edit Measurement  |  |
|---|--|
| can Display Scan Qualification Advanced   |  |
| feasurement Duration  | Run Mode   |
| Number of clock cycles measured at each offset position O Short (50,000) - Requires frequent transitions  | Demo Mode (no probes required)     Enable sample position warnings   |
| 💿 Medium (500,000) - Default  | C Scan Limits  |
| <ul> <li>Long (5,000,000) - Better for infrequent transitions</li> <li>Custom - 500000 Clocks</li> </ul>  | Min s s - +<br>Max s ns s - +<br>Default Scan Limits   |
| <ul> <li>Complete eye scan - scan all points regardless of signal activity</li> <li>Scan Resolution</li> <li>Normal - Faster scan adequate for setting sample positions on most systems.</li> <li>High - Detailed scan for high-speed systems with smaller eyes or for optimal bus-level signal integrity insight.</li> </ul> | Unit Interval Control<br>Use this control to adjust left or right the "window" ov<br>scan will be performed. |

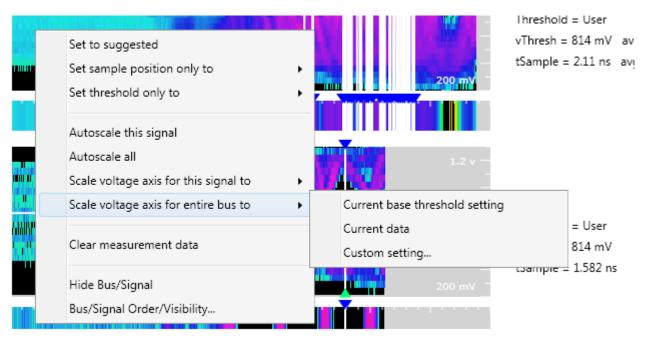
#### Scaling voltage axis for a signal or an entire bus

After you have run the eyescan measurement and acquired the eyescan data, you can scale the voltage axis for individual signals or an entire bus in that eyescan. When you scale the voltage axis for a bus, each child signal in that bus is scaled to the same value that you select.

Note: The scaling options are available only on a full time/voltage eyescan diagram. On a Time Only eyescan diagram, these options are not displayed as the eyescan data is time-only. Further, if you generated a full time/voltage eyescan diagram from a time-only scan, the scaling options will be displayed for use but not meaningful as the data is still time-only. Scaling provides meaningful results on a full time/voltage eyescan diagram that has been acquired by running a full time and voltage scan.

#### To scale the voltage axis

- 1 In the displayed eyescan diagram, navigate to the signal or the bus for which you want to scale the voltage axis.
- 2 Right-click the signal or the bus. A context menu is displayed.



- **3** To scale an entire bus, select the **Scale voltage axis for entire bus to** option. To scale an individual signal, select the **Scale voltage axis for this signal to** option.
- **4** A submenu is displayed with three scaling options that represent the value to be used to scale the signal(s). Select a menu option that suits your scaling requirement. You can select from:

- **Current base threshold setting** Selecting this option scales the signal(s) using the base threshold voltage setting with which you run the eyescan measurement. This threshold setting is displayed in the Threshold column on the right of the diagram.
- **Current data** Selecting this option scales the signal(s) using the voltage setting currently displayed in the acquired eyescan data.
- **Custom setting** Selecting this option scales the signal(s) using the minimum and maximum voltage values that you specify when you select this menu option.

The selected signal or the signals in the entire bus are then scaled to the selected value.

#### Exporting eyescan data to a .CSV file

After you have run the eyescan measurement, you can export the displayed eyescan data to a specified .csv file.

## To export eyescan data to a .csv file

1 Click the Export Measurement Data to CSV File toolbar button in the Eye Scan - Sample Position and Threshold Settings dialog box.

The Save As dialog box is displayed.

2 Specify the name and location of the .csv file to which you want to export the displayed eyescan data and then click **Save**.

#### Contents of the .csv file

In the CSV file, the eyescan data is exported for each signal that you included in the eyescan measurement. The following screen displays a sample .csv file in Excel with eyescan data for the MyBus1[0] signal.

## 12 Reference

| A                          | В           | С        | D        | E        | F        | G        | Н        | 1        |   |  |
|----------------------------|-------------|----------|----------|----------|----------|----------|----------|----------|---|--|
| Eye scan data output file. |             |          |          |          |          |          |          |          |   |  |
| Signal_info                | My Bus 1[0] | My Bus 1 | 0        | Pod 2.1  | 0        |          |          |          | ٦ |  |
| Scan_start_date            | 8/24/2011   |          |          |          |          |          |          |          |   |  |
| Scan_start_time            | 2:03:33 PM  |          |          |          |          |          |          |          |   |  |
| Threshold_scan             | True        |          |          |          |          |          |          |          |   |  |
| tMin                       | -5.76E-09   |          |          |          |          |          |          |          |   |  |
| tMax                       | 1.61E-09    |          |          |          |          |          |          |          |   | General information  |
| tRes                       | 4.80E-12    |          |          |          |          |          |          |          |   | on signals and scan  |
| vMin                       | 0.125976    |          |          |          |          |          |          |          |   |  |
| vMax                       | 1.35424785  |          |          |          |          |          |          |          |   |  |
| vRes                       | 0.03149415  |          |          |          |          |          |          |          |   |  |
| nCols                      | 1537        |          |          |          |          |          |          |          |   |  |
| nRows                      | 40          |          |          |          |          |          |          |          |   |  |
| eye_scan_data              |             |          |          |          |          |          |          |          |   |  |
| 0                          | 0           | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 1 |  |
| 2.40E-05                   | 2.40E-05    | 1.80E-05 | 1.80E-05 | 8.00E-06 | 8.00E-06 | 1.20E-05 | 1.40E-05 | 8.00E-06 |   | PRODUCTION OF A DESCRIPTION OF A DESCRIP |
| 4.80E-05                   | 6.80E-05    | 6.80E-05 | 6.20E-05 | 5.20E-05 | 8.60E-05 | 8.00E-05 | 8.60E-05 | 9.60E-05 | 1 | _ Eyescan data   |
| 0.000759991                | 0.000611993 | 0.000682 | 0.000848 | 0.000548 | 0.000492 | 0.00058  | 0.000946 | 0.00076  |   |  |
| 0.001461982                | 0.002027976 | 0.001462 | 0.00281  | 0.00281  | 0.00226  | 0.00163  | 0.00252  | 0.001462 |   | 0  |

As displayed in the above screen, the .csv file contains information in the following two sections for each of the mapped bus/signal and channel that you included in the eyescan measurement.

- General information on signal and scan This section displays:
  - **Signal\_Info** The name of the signal and mapped channel followed by the name of the parent bus name, the numerical index of the signal within the bus, the U4154A pod which contains the signal, and the bit index within that pod.
  - Scan\_start\_date The date at which the eye scan was started.
  - Scan\_start\_time The time at which the eye scan was started.
  - **Threshold\_scan** Displays True if a full time/voltage scan was performed and False if only a time scan was performed.
  - tMin, tMax, and tRes Represent the minimum time, maximum time, and time resolution (step size).
  - vMin, vMax, and vRes Represent the minimum voltage, maximum voltage, and voltage resolution.
  - **nCols and nRows** The number of columns and rows of eyescan data displayed in the .csv file for the signal.
- Eyescan data (eye\_scan\_data) In this section, the eyescan data for the signal is displayed for various voltage/time points. Rows in this section represent voltage points and columns represent time points in the scan. The first row in this section shows the scan data for the minimum voltage in the scan. The last row shows the scan data for the maximum voltage in the scan. The first cell in each of these rows is the earliest time in the scan.

Each cell in the eyescan data section has a value that represents a hit probability (signal activity) for the time/voltage point that the row and column combination of the cell represents. The cells can have the following values:

- 0 This value indicates that there was no signal activity at that voltage and time combination.
- -1 This value indicates that no scan data was taken at that voltage and therefore all other values displayed in that row should be ignored. In the .csv file generated for a full eye scan, none of the rows in the eyescan data section start with -1 because all voltage values have been measured.
- 1 This value indicates that there was a hit (signal activity) at every clock (a rare situation).

You can determine the voltage of a row in the eyescan data section by using the following formula:

vRow = vMin + (rowNum \* vRes)

where rowNum is the 0-based index of the row.

You can determine the time for a column in the eyescan data section by using the following formula:

tCol = tMin + (colNum \* tRes)

#### **Modifying General or Target-specific Scan Qualification**

You use the **Scan Qualification** tab in the **Edit Measurement** dialog box invoked from the Eye Scan - Sample Positions and Threshold Settings dialog box to modify the scan qualification for general as well as target-specific scans such as DDR scans. This tab displays different fields based on whether you are modifying scan qualification for a general or a target-specific scan. This topic describes how to use this tab to modify general or target-specific scan qualification.

#### **General Scan Qualification**

For generating general trigger specifications when using the U4154 module, the Scan Qualification tab displays only the **Scan Qualification...** button as displayed below.

| 🗱 Edit Measurement   |
|--|
| Scan Display Scan Qualification Advanced   |
| Scan Qualification Interface: General 🔻  |
| Use the Logic Analyzer trigger and storage qualification interface to specify the scan qualification |
| Scan Qualification   |
|  |
|  |
|  |
|  |
| When you click the Scan Qualification button the Evescan Trigger dialog                              |

When you click the **Scan Qualification** button, the **Eyescan Trigger** dialog box is displayed. Using this dialog box, you can specify a sequence of trigger conditions for a generalized eyescan measurement. These trigger conditions allow you to control when U4154A logic analyzer takes samples that are used in that eyescan for determining the optimal threshold and sample positions.

| = E            | yescan Trigger                               |   |
|----------------|--|---|
| Т              | rigger Functions                             | Trigger Sequence  |
| er Patterns    | Pattern n<br>times                           | Default Storage         Overridden by store actions in individual trigger steps:         Image: Store Im |
| Advanced Other | N<br>consecutive<br>samples with<br>Pattern1 | Step 1 * Advanced If/Then   * If   occurs   Image: Then   * Goto   1  |
|                | Pattern1<br>followed by<br>Pattern2          |   |
|                | Store Re                                     | call Clear OK Cancel Help   |

The eyescan trigger feature in U4154A is similar to the general trigger function of logic analyzer (for specifying when to capture data from DUT). However, an eyescan trigger has only one type of action (Goto <trigger step>) when the trigger condition is met.

## DDR/LPDDR-specific Scan Qualification

Once you have created an initial DDR/LPDDR setup and set the initial sample positions using the DDR Setup Assistant tool, there may be situations when you want to modify the DDR/LPDDR-specific scan qualification parameters before running subsequent eyescans for DDR/LPDDR signals. In such situations, you use the **Scan Qualification** tab of the **Edit Measurement** dialog box invoked from the Eye Scan - Sample Positions and Threshold Settings dialog box.

In a general eyescan usage scenario, the **Scan Qualification** tab displays a single button to modify a general trigger condition for scan qualification. However, when you load a DDR/LPDDR specific configuration file or an already saved DDR setup .ala file in the Logic Analyzer GUI, this tab displays DDR/LPDDR-specific scan qualification fields. By default, these fields display the values that you set while creating the initial DDR setup using the DDR Setup Assistant tool. You can modify these default values using this tab.

When you confirm and save the DDR-specific scan qualification settings, these settings are used to create a DDR trigger specification. The eyescan feature of the U4154A module then uses this trigger specification while performing subsequent eyescan runs to find DDR data signal eyes and set sample positions for DDR signals.

## NOTE

The Scan Qualification tab is used to set/modify the scan qualification only when you are using the U4154A module for capturing DDR data. This tab cannot be used with 16960/62 series of Logic Analyzers. For these logic analyzers, you use the Agilent DDR3 Eyefinder tool to modify the scan parameters that were initially set using the DDR Setup Assistant tool.

## To modify the DDR-specific scan qualification

**NOTE** Ensure that you have installed the *Agilent DDR3 Eyefinder* software package from the Agilent web site www.agilent.com/find/la-sw-download. Without installing this package, the DDR/LPDDR-specific scan qualification fields are not available in the Scan Qualification tab.

1 In the Agilent Logic Analyzer GUI, load the required DDR/LPDDR-specific configuration file for U4154A. (The default

DDR/LPDDR configuration files are available if you have installed the DDR packages, *Agilent Bus Decoder for DDR2 and DDR3* and *Agilent Bus Decoder for LPDDR and LPDDR2*. Also, you should have the appropriate software license to use these software packages.)

OR

Open the Logic Analyzer configuration (.ala) file in which you saved the DDR setup (probes, module, tools, and windows) that you created using the DDR Setup Assistant tool.

2 Click the **Sampling Setup** link of the module displayed in the DDR setup.

The **Sampling** tab is displayed.

- 3 Ensure that the **State Synchronous sampling** option is selected in the **Sampling** tab.
- 4 Click the Eye Scan: Sample Positions and Thresholds... button.
- 5 In the Eye Scan Sample Position and Threshold Settings dialog box, select the tab for Chip Select, Command and Address, Data Read or Data Write to modify the scan qualification for the appropriate signals.

| 🔆 Eye Scan - Sample Position and Threshold Settings |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|
| - <b>X</b>  | 🧷 📰 🚽 🎫 🜌 📲 📳 🔹 🗔 Snap markers to eye center         |  |  |  |  |  |  |
| Clock   | Chip Select Command and Address Data Read Data Write |  |  |  |  |  |  |

- 6 Click the Edit Current Measurement toolbar button.
- 7 Click the Scan Qualification tab.
- 8 Based on the signals tab you selected in step 5, the options are displayed in the Scan qualification interface listbox. Select one of the following options from this listbox:
  - DDR/LPDDR Chip Select option to modify the scan qualification for chip select signals.
  - DDR/LPDDR Command and Address option to modify the scan qualification for command and address signals.
  - DDR Data Read option to modify the scan qualification for data read signals.
  - DDR Data Write option to modify the scan qualification for data write signals.

On selecting the **DDR/LPDDR Chip Select** option in the previous step, the following fields are displayed for chip select scan qualification:

| Edit Measurement              |                         |           |
|-------------------------------|-------------------------|-----------|
| Scan Display Scan Qualif      | ication Advanced        |           |
| Scan Qualification Interface: | DDR/LPDDR Chip Select 🔻 |           |
| Memory Configuration          |                         |           |
| Select all active clock enab  | le signals.             |           |
| Clock Enable 0                | *                       |           |
| Clock Enable 1                |                         |           |
|                               |                         |           |
|                               |                         |           |
|                               |                         |           |
|                               |                         | OK Cancel |

**9** For the DDR/LPDDR Chip Select signals, make the appropriate selections based on the active clock enable signals.

On selecting the **DDR/LPDDR Command and Address** option in the step 8, the following fields are displayed for scan qualification:

| 👯 Edit Measurement   |
|--|
| Scan Display Scan Qualification Advanced   |
| Scan Qualification Interface: DDR/LPDDR Command/Address 🔻  |
| Memory Configuration   |
| Check and select the appropriate clock enable setting for ALL active chip selects. Additionally, select the subset of include in the scan. |
| ✓ Chip Select 0 None ▼ In Scan: ▼  |
| Chip Select 1 None T In Scan:  |
|  |
|  |

**10** For the DDR/LPDDR Command and Address signals, make the appropriate Memory Configuration selections based on the chip selects used in the DUT.

On selecting the **DDR/LPDDR Data Read** or **Data Write** interface in step 8, the following fields are displayed for scan qualification:

## 12 Reference

| Edit Measurement  |   |
|---|---|
| Scan Display Scan Qualification Advanced  |   |
| Scan Qualification Interface: DDR Data Write 💌  |   |
| Total Write Latency: 7.0<br>Memory Configuration<br>Check and select the appropriate clock enable setting for ALL<br>active chip selects. Additionally, select the subset of chip<br>selects you wish to include in the scan. | Overlay vs. Signal Trace<br>© Eye Overlay Mode (for finding ideal sample po<br>© Signal Trace Mode (for viewing signal swing vs<br>Signal Trace Options<br>View Beginning  v of data burst. |
| Chip Select 0 None  In Scan: Chip Select 1 None In Scan:  | Capture All vs. No Back To Back<br>© Capture and store all memory bursts  |

11 For DDR Data Read or Write signals:

**a** The DUT's **Total Read / Write Latency** value that you set up in the initial DDR setup is displayed. If needed, modify this value. To find an appropriate value of Total Read/Write Latency, you can set up the Mode Register Settings (MRS) trigger, take a trace, and scan it for latency values. Refer to the DDR Setup Assistant online help to know more on how to find latency values.

The latency values specified here represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.

- b In the Memory Configuration section, choose the appropriate Chip Select(s) for the memory path being traced.
- **c** In the **Burst Length** field, specify the number of words read or written for each read/write command. To find appropriate value of Burst Length for the DUT, you can set up the Mode Register Settings (MRS) trigger, take a trace, and scan it for burst length. Refer to the DDR Setup Assistant online help to know how to find burst length.
- d Select the appropriate scan mode:

## NOTE

- **Eye Overlay Mode** Use this mode when setting sample positions for DDR data signals. In this mode, the eyescan feature of U4154A overlays the eyes for each bit in a burst in order to show a composite eye, without tri-state or noise, that helps you locate the best sample position.
- **Signal Trace Mode** Use this mode for viewing signal swing vs. time. Although sample positions can be checked and modified in this mode, it is generally not recommended. In this mode, the eyescan feature of U4154A overlays complete bursts in order to provide additional qualitative insight into the signal integrity on the DDR system at the logic analyzer probe location. In this mode, you can view how the bits in a complete burst compare to one another. When you select the Signal Trace Mode, the following three options are provided to you to select the data burst area to view:
  - Beginning Scans are made at the beginning of a data burst.
  - Middle Scans are made at the middle of a data burst.
  - End Scans are made at the end of a data burst.
- 12 Select the Capture and store all memory bursts radio button to capture and store back to back memory bursts.
- **13** Select the **Do not store back-to-back memory bursts** radio button to eliminate the "double eye" effect in scan results.
- 14 Click OK to confirm the settings.

You can save the modified scan qualification settings in the Logic Analyzer .ala or .xml configuration file.

## **16850-Series Logic Analyzer Notes**

- Channels and Memory Depth
- Maximum State Sampling Speed
- Timing Mode Sampling Options/Period
- State Mode Sampling Options
- Timing Zoom

Channels and Memory Depth

| nory Depth Default | Option | Option | Option | Option | Option | Option |
|--------------------|--------|--------|--------|--------|--------|--------|
|                    | 004    | 008    | 016    | 032    | 064    | 128    |

## 12 Reference

| Memory depth  | 2 M                                    | 4 M                                   | 8 M                       | 16 M                  | 32 M | 64 M | 128 M |
|---|--|---------------------------------------|---------------------------|-----------------------|------|------|-------|
| *Memory depth u<br>appending the rel<br>16851AU, 16852A<br>For instance, 168<br>(See also Installin | levant mem<br>AU, 16853A<br>51AU-008 t | iory option<br>U, 16854A<br>o upgrade | number t<br>U<br>to 8M sa | o the follo<br>mples. |      |      |       |

|          | 16851A | 16852A | 16853A | 16854A |
|----------|--------|--------|--------|--------|
| Channels | 34     | 68     | 102    | 136    |

See also Memory Depth and Channel Count Trade-offs (see page 420).

#### Maximum State Sampling Speed

| Samp | ling | Speed |  |
|------|------|-------|--|
|      |      |       |  |

|  | Default  | Option 700 <sup>*</sup> |
|--|----------|-------------------------|
| Max. state clock rate  | 350 MHz  | 700 MHz                 |
| Max. state data rate   | 700 Mb/s | 1400 Mb/s               |
| *State sampling speed upgrade for the 16850 Series logic analyzers can be ordered by appending<br>the -700 option number to the following upgrade model numbers:<br>16851AU, 16852AU, 16853AU, 16854AU<br>(See also Installing Licensed Hardware Upgrades (see page 147).) |          |                         |

## Timing Mode Sampling Options/Period

• Full channel, 2.5 GHz = Full Channel Timing Mode

With this sampling option, you can use the full memory depth of your logic analyzer, with data sampling period on all channels as 400 ps to 10 ns. You can set the sample rate to go slower with the Sample Period field.

• Half channel, 5 GHz = Half Channel Timing Mode

With this sampling option, only one pod of each pod pair is available, and the memory depth is doubled. Channels assigned to unavailable pods are ignored. You can specify which pod to use in the Buses/Signals tab of the Analyzer Setup dialog by clicking the Pod button and selecting the desired pod.

Data sampling period is 200 ps and is fixed.

 Transitional / Store qualified, Full channel 2.5 GHz / Half channel 5.0 GHz = Transitional / Store Qualified Timing Modes

At the 2.5 GHz sample rate, one pod pair (34 channels) must be reserved for time tag storage. At slower sample rates, you can get full channels by using 1/2 (or less) of a module's acquisition memory depth (for more information, see Memory Depth and Channel Count Trade-offs (see page 420)).

Transitional / Store Qualified Timing mode provides maximum duration of acquisition because data is only stored when a change from the last value is detected. The sampling period ranges from 10 ns to 400 ps for full channel mode and is fixed at 200 ps for half channel mode. (see page 422).

- **Timing Zoom** Timing zoom collects additional high-speed timing data around the trigger of the logic analyzer. It uses a 256 K-sample, 12.5 GHz timing analysis sample rate to sample data at a sampling period of 80 ps.
  - **See Also** 16850 Series Logic Analyzer Specifications and Characteristics (see page 779)

# **Specifications and Characteristics**

Describes the specifications, characteristics, and requirements of supported logic analyzers and logic analysis systems.

- 1680/1690-Series Logic Analyzer Specifications and Characteristics (see page 714)
- 16740/41/42 Logic Analyzer Specifications and Characteristics (see page 717)
- 16750/51/52 Logic Analyzer Specifications and Characteristics (see page 722)
- 16753/54/55/56 Logic Analyzer Specifications and Characteristics (see page 727)
- 16760 Logic Analyzer Specifications and Characteristics (see page 734)
- 16800-Series Logic Analyzer Specifications and Characteristics (see page 742)
- 16910/11 Logic Analyzer Specifications and Characteristics (see page 749)
- 16950/51 Logic Analyzer Specifications and Characteristics (see page 757)
- 16960 Logic Analyzer Specifications and Characteristics (see page 764)
- 16962 Logic Analyzer Specifications and Characteristics (see page 769)
- 16900-Series Logic Analysis System Frame Characteristics (see page 774)
- U4154A Logic Analyzer Specifications and Characteristics (see page 775)
- 16850-Series Logic Analyzer Specifications and Characteristics (see page 779)

#### **See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

## 1680/1690-Series Logic Analyzer Specifications and Characteristics

Describes the specifications, characteristics, and requirements of the 1680A/AD-series and 1690A/AD-series logic analyzers.

- 1680/1690-Series Logic Analyzer Specifications (see page 715)
- 1680/1690-Series Logic Analyzer Characteristics (see page 715)

#### **See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

# 1680/1690-Series Logic Analyzer Specifications

| Threshold Accuracy                                    | ±(65 mV +1.5 % of setting)  |
|---|---|
| Minimum<br>Master-to-Master<br>Clock Time             | 5.0 ns  |
| Setup/Hold Time<br>(Single Clock, Single<br>Edge)     | 2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel |
| Setup/Hold Time<br>(Multiple Clock,<br>Multiple Edge) | 3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel |

# 1680/1690-Series Logic Analyzer Characteristics

- General Information (see page 715)
- State Analysis (see page 715)
- Timing Analysis (see page 716)
- Triggering (see page 716)
- Operating Environment Characteristics (see page 717)

## General Information

| State/timing<br>channels: | 1680A/AD, 1690A/AD: 136<br>1681A/AD, 1691A/AD: 102<br>1682A/AD, 1692A/AD: 68<br>1683A/AD, 1693A/AD: 34  |  |
|---------------------------|---|--|
| User interface:           | Windows® XP Professional  |  |
| Printers:                 | Can print to any local or network printer supported by Windows® XP Professional.  |  |
| Dimensions:               | 1680 - 257 mm height (10.14 in), 443 mm width (17.45 in), 385 mm depth<br>(15.15 in)<br>1690 - 153 mm height (6.05 in), 438 mm width (17.23 in), 335 mm depth<br>(13.16 in) |  |
| Weight:                   | 1680 - 13.2 kg (29.1 lbs)<br>1690 - 7.5 kg (16.5 lbs)   |  |

## **State Analysis**

| Maximum state<br>speed: | 200 MHz  |
|-------------------------|--|
| State memory depth:     | 1680/1690A-series: 256K<br>1680/1690AD-series: 1 M |

| Minimum state clock<br>pulse width:   | 1.2 ns                              |  |
|---------------------------------------|-------------------------------------|--|
| Time tag resolution:                  | 4ns or ±0.1% (whichever is greater) |  |
| Maximum time count<br>between states: | 17 seconds                          |  |
| State clock/qualifiers                | 4 (2 on 34 channel models)          |  |
| Minimum<br>master-to-master<br>clock: | 5.0 ns                              |  |
| Minimum<br>master-to-slave clock:     | 2.0 ns                              |  |
| Minimum<br>slave-to-slave clock:      | 5.0 ns                              |  |

# **Timing Analysis**

| Maximum timing sample rate:      | Half channel: 800 MHz<br>Full channel: 400 MHz   |  |
|----------------------------------|--|--|
| Timing memory depth:             | 1680/1690A-series, half channel: 1 M<br>1680/1690A-series, full channel: 512 K<br>1680/1690AD-series, half channel: 4 M<br>1680/1690AD-series, full channel: 2 M |  |
| Sample period, full channels:    | 2.5 ns to 1 ms   |  |
| Sample period, half<br>channels: | 1.25 ns  |  |
| Sample period<br>accuracy:       | $\pm 0.01\%$ of sample period $\pm 100$ ps   |  |
| Channel-to-channel<br>skew:      | <1.5 ns typical  |  |
| Time interval<br>accuracy:       | ±(sample period + channel-to-channel skew + 0.01% of time interval reading)  |  |

# Triggering

| Sequencer speed:                | 200 MHz                |  |
|---------------------------------|------------------------|--|
| Maximum occurrence count value: | 16,777,215             |  |
| Range width:                    | 32 bits                |  |
| Timer value range:              | 100 ns to 5497 seconds |  |
| Timer resolution:               | 5 ns                   |  |

| Timer accuracy:                    | ±10 ns + 0.01%   |  |
|------------------------------------|--|--|
| Trigger resources:                 | 16 patterns 15 patterns  |  |
| Timers:                            | 1680A/AD, 1690A/AD: 3<br>1681A/AD, 1691A/AD: 2<br>1682A/AD, 1692A/AD: 1<br>1683A/AD, 1693A/AD: 0 |  |
| Occurrence counters:               | 1 per sequence step  |  |
| Trigger sequence<br>steps:         | 16   |  |
| Minimum detectable<br>glitch:      | 1.5 ns   |  |
| Trigger in arms logic<br>analyzer: | 15 ns, typical delay   |  |
| Trigger to trigger out:            | 150 ns, typical delay  |  |

## Operating Environment Characteristics

| Temperature: | Instrument: 5°C to 50°C<br>Disk media: 10°C to 40°C<br>Probe lead sets and cables: 0°C to 65°C            |
|--------------|---|
| Humidity:    | Instrument: Up to 95% relative humidity at 40°C<br>Disk media and hard drive: 8% to 85% relative humidity |
| Altitude:    | 4,572 m (15,000 ft) operating<br>15,300 m (50,000 ft) non-operating                                       |

# 16740/41/42 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16740/41/42 logic analyzers.

- 16740/41/42 Logic Analyzer Specifications (see page 717)
- 16740/41/42 Logic Analyzer Characteristics (see page 718)

## See Also

- What is a Specification (see page 785)
- What is a Characteristic (see page 786)

## 16740/41/42 Logic Analyzer Specifications

| Maximum State Clock<br>Speed | 200 MHz                              |
|------------------------------|--------------------------------------|
| Threshold Accuracy           | ±(65 mV + 1.5% of threshold setting) |

| Minimum<br>Master-to-Master<br>Clock Time  | 5.0 ns at 200 MHz   |
|--|---|
| Setup/Hold Time<br>(Single Clock, Single<br>Edge) <sup>1</sup> (see<br>page 718)   | 2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel |
| Setup/Hold Time<br>(Multiple Clock,3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps<br>increments per channelMultiple Edge) 1 (see<br>page 718)1 (see<br>(see base of the sec of th |   |
| <sup>1</sup> Specified for an input s  | tignal VH = -0.9 V, VL = -1.7 V, threshold = -1.3 V, slew rate = 1 V/ns.                  |

# 16740/41/42 Logic Analyzer Characteristics

- General Information (see page 718)
- State Analysis (see page 718)
- Timing Analysis (see page 719)
- Triggering (see page 720)
- Power Requirements (see page 721)
- Operating Environment Characteristics (see page 721)
- Storage (see page 722)

## General

| Channel counts: | 1-card module = 64 data, 4 clock  |
|-----------------|-----------------------------------|
|                 | 2-card module = 132 data, 4 clock |
|                 | 3-card module = 200 data, 4 clock |
|                 | 4-card module = 268 data, 4 clock |
|                 | 5-card module = 336 data, 4 clock |
|                 |                                   |

## **State Analysis**

| Maximum state clock<br>speed:                            | 200 MHz   |
|--|---|
| Maximum memory<br>depth:                                 | 16740A = 1 M<br>16741A = 4 M<br>16742A = 16 M   |
| Minimum setup/hold<br>time <sup>1</sup> (see page 719) : | 2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100–ps increments per channel |
| Minimum state clock<br>pulse width:                      | 1.2 ns  |

| Minimum<br>master-to-master<br>clock:                       | 5.0 ns at 200 MHz             |
|---|-------------------------------|
| Minimum<br>master-to-slave clock:                           | 2 ns                          |
| Minimum<br>slave-to-slave clock:                            | 5.0 ns at 200 MHz             |
| State clocks:   | 4                             |
| State clock qualifiers:                                     | 4                             |
| Time tag resolution <sup>2</sup><br>(see page 719) :        | 4 ns                          |
| Maximum time count<br>between states:                       | 17 seconds                    |
| Maximum state tag<br>count <sup>2</sup> (see<br>page 719) : | 2e32                          |
| Store qualification:  | Default and per sequence step |

# Timing Analysis

• Timing Zoom (see page 719)

- Conventional Timing (see page 720)
- Transitional Timing (see page 720)

# Timing Zoom

| Sample rates:               | 2 GHz, 1 GHz, 500 MHz, 250 MHz  |
|-----------------------------|---|
| Sample period<br>accuracy:  | ±50 ps  |
| Channel-to-channel<br>skew: | <1.0 ns   |
| Timing interval accuracy:   | ±(sample period + channel-to-channel skew + 0.01% of time interval reading) |
| Trigger position:           | Start, center, end, or user-defined   |
| Memory depth:               | 16 K  |

## Conventional Timing

| Maximum sample<br>rate:      | Half channel = 800 MHz Full channel = 400 MHz  |
|------------------------------|--|
| Memory depth:                | 16740A, half channel = 2 M samples per channel<br>16740A, full channel = 1 M samples per channel<br>16741A, half channel = 8 M samples per channel<br>16741A, full channel = 4 M samples per channel<br>16742A, half channel = 32 M samples per channel<br>16742A, full channel = 16 M samples per channel |
| Sample period<br>accuracy:   | ±(250 ps + 0.01% of sample period)   |
| Channel-to-channel<br>skew:  | <1.5 ns, typical   |
| Timing interval<br>accuracy: | ±(sample period + channel-to-channel skew + 0.01% of time interval reading)  |
| Minimum data pulse<br>width: | 1.5 ns for data capture 5.0 ns for trigger sequencing  |

# Transitional Timing

| Maximum timing<br>analysis sample rate: | 400 MHz   |
|---|---|
| Minimum data pulse<br>width:            | 3.8 ns for data capture 5.1 ns for trigger sequencing   |
| Number of channels:                     | For sample rates < 400 MHz: 68 x (number of cards)<br>For sample rates = 400 MHz: 68 x (number of cards) - 34 |
| Global counters:                        | 1   |
| Glitch/edge<br>recognizers:             | 1 per pod pair  |

# Triggering

| Maximum trigger sequencer speed: | 200 MHz                        |
|----------------------------------|--------------------------------|
| State sequence steps:            | 16                             |
| Timing sequence steps:           | 16                             |
| Sequence step<br>branching:      | Arbitrary 4-way "If/then/else" |
| Maximum occurrence count value:  | 16,777,215                     |
| Pattern recognizers:             | 16                             |

| Range recognizers:            | 15  |
|-------------------------------|---|
| Range width:                  | 32  |
| Occurrence counters:          | 1 per sequence step   |
| Global counters:              | 2   |
| Flags:                        | 4, shared across all connected logic analysis system frames             |
| Flag set/reset to evaluation: | 110 ns, typical   |
| Timers:                       | 200 MHz state: 2 x number of cards<br>timing: (2 x number of cards) - 1 |
| Timer value range:            | 100 ns to 5497 seconds  |
| Timer resolution:             | 5 ns  |
| Timer accuracy:               | ±10 ns + 0.01%  |
| Timer reset latency:          | 70 ns   |
| Glitch/edge<br>recognizers:   | 2 per pod pair (timing only)  |
| Minimum detectable<br>glitch: | 1.5 ns  |
| Greater than duration:        | 6 ns to 100 ms in 6–ns increments                                       |
| Less than duration:           | 12 ns to 100 ms in 6–ns increments                                      |
| Data in to trigger out:       | 150 ns, typical   |

**Power** All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

## Operating Environment Characteristics

| Indoor use only. |  |  |
|------------------|--|--|
| Temperature:     | Instrument (except disk and media): 0°C to 50°C (+32°F to 122°F)<br>Probe lead sets and cables: 0°C to 65°C (+32°F to 149°F)   |  |
| Humidity:        | Instrument, probe lead sets, and cables: Up to 80% relative humidity at 40°C (+104°F)  |  |
| Altitude:        | Operating: 4,600 m (15,000 ft)<br>Non-operating: 15,300 m (50,000 ft)  |  |
| Vibration:       | Operating: Random vibration 5-500 Hz, 10 minutes per axis,<br>approximately 0.2 g rms<br>Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis,<br>approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz,<br>0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |  |

Reliability is enhanced when operating within the following ranges:

| Temperature: | +20°C to 35°C (+68°F to 95°F) |
|--------------|-------------------------------|
| Humidity:    | 20% to 80% non-condensing     |

Storage Store or ship the logic analyzer in environments with the following limits:

| Temperature: | -40°C to +75°C                      |  |
|--------------|-------------------------------------|--|
| Humidity:    | Up to 90% relative humidity at 65°C |  |
| Altitude:    | Up to 15,300 m (50,000 ft)          |  |

Protect the module from temperature extremes which cause condensation on the instrument.

# 16750/51/52 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16750/51/52 logic analyzers.

- 16750/51/52 Logic Analyzer Specifications (see page 722)
- 16750/51/52 Logic Analyzer Characteristics (see page 723)
- See Also
- What is a Specification (see page 785)
- What is a Characteristic (see page 786)

## 16750/51/52 Logic Analyzer Specifications

| Maximum State Clock<br>Speed   | 400 MHz   |
|--|---|
| Threshold Accuracy   | ±(65 mV + 1.5% of threshold setting)  |
| Minimum<br>Master-to-Master<br>Clock Time  | 5.0 ns at 200 MHz 2.5 ns at 400 MHz   |
| Setup/Hold Time<br>(Single Clock, Single<br>Edge) <sup>1</sup> (see<br>page 723) | 2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel |

|   | 3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel |
|---|---|
| <sup>1</sup> Specified for an input signal VH = -0.9 V, VL = -1.7 V, threshold = -1.3 V, slew rate = $1 \text{ V/ns}$ . |   |

## 16750/51/52 Logic Analyzer Characteristics

- General Information (see page 723)
- State Analysis (see page 723)
- Timing Analysis (see page 724)
- Triggering (see page 725)
- Power Requirements (see page 726)
- Operating Environment Characteristics (see page 726)
- Storage (see page 726)

#### General Information

| aviiviui |                 |                                   |
|----------|-----------------|-----------------------------------|
| ormation | Channel counts: | 1-card module = 64 data, 4 clock  |
|          |                 | 2-card module = 132 data, 4 clock |
|          |                 | 3-card module = 200 data, 4 clock |
|          |                 | 4-card module = 268 data, 4 clock |
|          |                 | 5-card module = 336 data, 4 clock |

#### **State Analysis**

| Maximum state clock speed:                               | 400 MHz   |
|--|---|
| Maximum memory<br>depth:                                 | 16750A/B = 4 M<br>16751A/B = 16 M<br>16752A/B = 32 M                                      |
| Minimum setup/hold<br>time <sup>1</sup> (see page 724) : | 2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100–ps increments per channel |
| Minimum state clock<br>pulse width:                      | 1.2 ns  |
| Minimum<br>master-to-master<br>clock:                    | 5.0 ns at 200 MHz<br>2.5 ns at 400 MHz  |
| Minimum<br>master-to-slave clock:                        | 2 ns  |
| Minimum<br>slave-to-slave clock:                         | 5.0 ns at 200 MHz<br>2.5 ns at 400 MHz  |
| State clocks:  | 4   |

|                 | State clock qualifiers:                                     | 4  |
|-----------------|---|--|
|                 | Time tag resolution <sup>2</sup> (see page 724) :           | 4 ns   |
|                 | Maximum time count between states:                          | 17 seconds   |
|                 | Maximum state tag<br>count <sup>2</sup> (see<br>page 724) : | 2e32   |
|                 | Store qualification:  | Default and per sequence step  |
|                 |   | ge, single-clock acquisition. Multi-edge setup/hold window is 3.0 ns.<br>ng used, time or state tags halve the memory depth.   |
| Timing Analysis | <ul><li>Timing Zoom (s</li><li>Conventional Ti</li></ul>    | ee page 724)<br>ming (see page 724)  |
|                 |   | ning (see page 725)  |
| Timing Zoom     |   |  |
|                 | Sample rates:   | 2 GHz, 1 GHz, 500 MHz, 250 MHz   |
|                 | Sample period<br>accuracy:                                  | ±50 ps   |
|                 | Channel-to-channel<br>skew:                                 | <1.0 ns  |
|                 | Timing interval accuracy:                                   | ±(sample period + channel-to-channel skew + 0.01% of time interval reading)  |
|                 | Memory depth:   | 16 К   |
| Conventional    | <b></b>   |  |
| Timing          | Maximum sample<br>rate:                                     | Half channel = 800 MHz Full channel = 400 MHz  |
|                 | Memory depth:   | 16750A/B, half channel = 8 M samples per channel<br>16750A/B, full channel = 4 M samples per channel<br>16751A/B, half channel = 32 M samples per channel<br>16751A/B, full channel = 16 M samples per channel<br>16752A/B, half channel = 64 M samples per channel<br>16752A/B, full channel = 32 M samples per channel |
|                 | Sample period<br>accuracy:                                  | ±(250 ps + 0.01% of sample period)   |
|                 | Channel-to-channel<br>skew:                                 | <1.5 ns, typical   |

| Timing interval accuracy:    | ±(sample period + channel-to-channel skew + 0.01% of time interval reading) |
|------------------------------|---|
| Minimum data pulse<br>width: | 1.5 ns for data capture 5.0 ns for trigger sequencing                       |

## Transitional Timing

| Maximum timing<br>analysis sample rate: | 400 MHz   |
|---|---|
| Minimum data pulse<br>width:            | 3.7 ns for data capture<br>5.0 ns for trigger sequencing  |
| Number of channels:                     | For sample rates < 400 MHz: 68 x (number of cards)<br>For sample rates = 400 MHz: 68 x (number of cards) - 34 |
| Global counters:                        | 1   |
| Glitch/edge<br>recognizers:             | 1 per pod pair  |

# Triggering

| Maximum trigger sequencer speed: | 200 MHz   |
|----------------------------------|---|
| State sequence steps:            | 16  |
| Timing sequence<br>steps:        | 16  |
| Sequence step<br>branching:      | Arbitrary 4-way "If/then/else"  |
| Maximum occurrence count value:  | 16,777,215  |
| Pattern recognizers:             | 16  |
| Range recognizers:               | 15  |
| Range width:                     | 32  |
| Occurrence counters:             | 1 per sequence step   |
| Global counters:                 | 2   |
| Flags:                           | 4, shared across all connected logic analysis system frames             |
| Flag set/reset to evaluation:    | 110 ns, typical   |
| Timers:                          | 200 MHz state: 2 x number of cards<br>timing: (2 x number of cards) - 1 |
| Timer value range:               | 100 ns to 4397 seconds  |
| Timer resolution:                | 4 ns  |

| Timer accuracy:               | ±10 ns + 0.01%                     |
|-------------------------------|------------------------------------|
| Timer reset latency:          | 60 ns                              |
| Glitch/edge<br>recognizers:   | 2 per pod pair (timing only)       |
| Minimum detectable<br>glitch: | 1.5 ns                             |
| Greater than duration:        | 6 ns to 100 ms in 6–ns increments  |
| Less than duration:           | 12 ns to 100 ms in 6–ns increments |
| Data in to trigger out:       | 150 ns, typical                    |

All necessary power is supplied by the backplane connector of the logic

Power Requirements

analysis system mainframe.

Operating Environment Characteristics

| Indoor use only. |  |
|------------------|--|
| Temperature:     | Instrument (except disk and media): 0°C to 50°C (+32°F to 122°F)<br>Probe lead sets and cables: 0°C to 65°C (+32°F to 149°F)   |
| Humidity:        | Instrument, probe lead sets, and cables: Up to 80% relative humidity at 40°C (+104°F)  |
| Altitude:        | Operating: 4,600 m (15,000 ft)<br>Non-operating: 15,300 m (50,000 ft)  |
| Vibration:       | Operating: Random vibration 5-500 Hz, 10 minutes per axis,<br>approximately 0.2 g rms<br>Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis,<br>approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz,<br>0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

Reliability is enhanced when operating within the following ranges:

| Temperature: | +20°C to 35°C (+68°F to 95°F) |
|--------------|-------------------------------|
| Humidity:    | 20% to 80% non-condensing     |

Storage Store or ship the logic analyzer in environments with the following limits:

| Temperature: | -40°C to +75°C                      |
|--------------|-------------------------------------|
| Humidity:    | Up to 90% relative humidity at 65°C |
| Altitude:    | Up to 15,300 m (50,000 ft)          |

Protect the module from temperature extremes which cause condensation on the instrument.

## 16753/54/55/56 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16753/54/55/56 logic analyzers.

#### NOTE

Items marked with an asterisk (\*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 727)
- Probes (see page 727)
- Timing Zoom (see page 727)
- State (Synchronous) Analysis Mode (see page 728)
- Timing (Asynchronous) Analysis Mode (see page 731)
- Power Requirements (see page 733)
- Environmental Characteristics (see page 733)

# Module Channel

|                | State Analysis      | Timing Analysis |
|----------------|---------------------|-----------------|
| 1-card module: | 64 data + 4 clocks  | 68              |
| 2-card module: | 132 data + 4 clocks | 136             |
| 3-card module: | 200 data + 4 clocks | 204             |
| 4-card module: | 268 data + 4 clocks | 272             |
| 5-card module: | 336 data + 4 clocks | 340             |

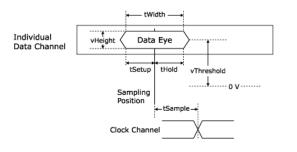
**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

#### **Timing Zoom**

| Timing analysis sample rate: | 4 GHz  |
|------------------------------|--|
| Timing interval accuracy:    | Within a pod pair: ±(750 ps + 0.01% of time interval reading)<br>Between pod pairs: ±(1.5 ns + 0.01% of time interval reading) |
| Memory depth:                | 64 K   |

| Trigger position:            | Start, center, end, or user-defined |
|------------------------------|-------------------------------------|
| Minimum data pulse<br>width: | 750 ps                              |

## State (Synchronous) Analysis Mode



|  | 300 Mb/s State Mode  | 600 Mb/s State Mode  |
|--|--|--|
| tWidth <sup>*</sup> (see page 731), 1 (see<br>page 731), 2 (see page 731) <sub>.</sub>             | 1 ns <sup>* (see page 731)</sup> , 600 ps<br>typical                                       | 1 ns <sup>* (see page 731)</sup> , 600 ps<br>typical                                       |
| tSetup:  | 0.5 tWidth   | 0.5 tWidth   |
| tHold:   | 0.5 tWidth   | 0.5 tWidth   |
| tSample range <sup>3 (see page 731)</sup> :  | -4 ns to +4 ns   | -4 ns to +4 ns   |
| tSample adjustment<br>resolution:  | 80 ps typical  | 80 ps typical  |
| tSample accuracy, manual<br>adjustment:  | ±300 ps  | ±300 ps <sup>4 (see page 731)</sup>  |
| Maximum state data rate on<br>each channel:  | 300 Mb/s   | 800 Mb/s   |
| Maximum channels on a<br>single time base and trigger: <sup>5</sup><br>(see page 731) <sub>:</sub> | 340 - (number of clocks)   | 306 - (1 clock)  |
| Memory depth <sup>5</sup> (see page 731) <sub>:</sub>  | 16753A: 1 M samples<br>16754A: 4 M samples<br>16755A: 16 M samples<br>16756A: 64 M samples | 16753A: 1 M samples<br>16754A: 4 M samples<br>16755A: 16 M samples<br>16756A: 64 M samples |
| Number of independent<br>analyzers <sup>6 (see page 731)</sup> :                                   | 2  | 1  |
| Number of clocks <sup>7 (see</sup><br>page 731) :  | 4  | 1  |

| Number of clock qualifiers <sup>7</sup> (see page 731) .                                | 4  | N/A   |
|---|--|---|
| Minimum time between active clock edges <sup>*</sup> (see page 731), 8 (see page 731) : | 3.33 ns  | 1.67 ns   |
| Minimum master-to-slave<br>clock time:  | 1 ns   | N/A   |
| Minimum slave-to-master clock time:   | 1 ns   | N/A   |
| Minimum slave-to-slave clock<br>time:   | 3.33 ns  | N/A   |
| Minimum state clock pulse width:  | Single edge: 1.0 ns<br>Multiple edge: 1.0 ns   | Single edge: 500 ps<br>Multiple edge: 1.67 ns   |
| Clock qualifier setup time:   | 500 ps   | N/A   |
| Clock qualifier hold time:  | 0  | N/A   |
| Time tag resolution <sup>5 (see</sup> page 731) :                                       | 2 ns   | 1.5 ns  |
| Maximum time count between stored states:   | 32 days  | 32 days   |
| Maximum trigger sequence<br>speed:  | 300 MHz  | 600 MHz   |
| Maximum trigger sequence<br>steps:  | 16   | 16  |
| Trigger sequence step<br>branching:   | Arbitrary 4-way if/then/else   | 2-way if/then/else  |
| Trigger position:   | Start, center, end, or<br>user-defined   | Start, center, end, or<br>user-defined  |
| Trigger resources:  | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>2 timers per card</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>14 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>7 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:  | Arbitrary Boolean<br>combinations  | Arbitrary Boolean<br>combinations   |

| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger and fill memory</li> </ul> |
|--------------------------------|---|--|
| Store qualification:           | Default (global) and per sequence step  | Default (global)   |
| Maximum global counter:        | 2E+24   | N/A  |
| Maximum occurrence<br>counter: | 2E+24   | 2E+24  |
| Maximum pattern width:         | 128 bits  | 128 bits   |
| Maximum range width:           | 32 bits   | 32 bits  |
| Timer value range:             | 40 ns to 2199 seconds   | N/A  |
| Timer resolution:              | 2 ns  | N/A  |
| Timer accuracy:                | ±(5 ns + 0.01%)   | N/A  |

| Fimer reset latency:   | 40 ns   | N/A  |
|--|---|--|
|  | (*) are specifications. All others an value of the parameter based on                                       |  |
| Minimum eye width in system  | under test.   |  |
| Your choice of probe can limit s<br>naintain system bandwidth.   | ystem bandwidth. Choose a probe   | rated at 600 Mb/s or greater to                                |
| position causes the input to be s<br>edge. A positive sample position<br>after each active clock edge. A s<br>sampled coincident with each c | •   | nount before each active clock<br>busly sampled by that amount |
| Use of eye finder is recommend   | led in 600 Mb/s state mode.   |  |
| lepth. With one pod pair (34 cha   | all pods assigned, memory depth i<br>annels) unassigned, the memory d<br>ned for time tags in 600 Mb/s stat | epth is full One pod pair (34                                  |
| Independent analyzers may be only one analyzer may be used.  | either state or timing. When the 60   | 00 Mb/s state mode is selected                                 |
| In the 300 Mb/s state mode, th'<br>nputs must be on the master m   | e total number of clocks and qual<br>odules.  | fiers is 4. All clock and qualifier                            |
| Tootod with input signal $Vh = 0$  | .9 V, VI = -1.7 V, slew rate = 1 V/n  | s, threshold = -1.3 V.   |
| iesteu with input signal vii – u   |   |  |

|  | Conventional Timing      | Transitional Timing <sup>9 (see</sup><br>page 731)  |
|--|--------------------------|---|
| Sample rate on all channels:                                     | 600 MHz                  | 600 MHz   |
| Sample rate in half channel mode:                                | 1200 MHz                 | N/A   |
| Number of channels:  | 68 x (number of cards)   | For sample rates <600 MHz:<br>68 x (number of cards).<br>For 600 MHz sample rate: 68 x<br>(number of cards) - 34. |
| Maximum channels on a single time base and trigger:              | 340                      | 340   |
| Number of independent<br>analyzers <sup>6 (see page 731)</sup> : | 2                        | 2   |
| Sample period (half channel):                                    | 833 ps                   | N/A   |
| Sample period (full channel):                                    | 1.67 ns                  | 1.67 ns   |
| Minimum data pulse width:  | 1 sample period + 500 ps | 1 sample period + 500 ps  |

## Timing (Asynchronous) Analysis Mode

| Time interval accuracy:               | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  |
|---------------------------------------|---|---|
| Memory depth in full channel mode:    | 16753A: 1 M<br>16754A: 4 M<br>16755A: 16 M<br>16756A: 64 M  | 16753A: 1 M<br>16754A: 4 M<br>16755A: 16 M<br>16756A: 64 M  |
| Memory depth in half channel<br>mode: | 16753A: 2 M<br>16754A: 8 M<br>16755A: 32 M<br>16755A: 128 M   | N/A   |
| Maximum trigger sequence<br>speed:    | 300 MHz   | 300 MHz   |
| Maximum trigger sequence<br>steps:    | 16  | 16  |
| Trigger sequence step<br>branching:   | Arbitrary 4-way if/then/else  | Arbitrary 4-way if/then/else  |
| Trigger position:                     | Start, center, end, or<br>user-defined  | Start, center, end, or<br>user-defined  |
| Trigger resources:                    | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>2 edge/glitch</li> <li>2 timers per card</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>2 timers per card</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:          | Arbitrary Boolean<br>combinations   | Arbitrary Boolean<br>combinations   |
| Trigger actions:                      | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                     | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                     |
| Maximum global counter:               | 2E+24   | 2E+24   |

| Maximum occurrence counter: | 2E+24                                    | 2E+24                                    |
|-----------------------------|--|--|
| Maximum range width:        | 32 bits                                  | 32 bits                                  |
| Maximum pattern width:      | 128 bits                                 | 128 bits                                 |
| Timer value range:          | 40 ns to 2199 seconds                    | 40 ns to 2199 seconds                    |
| Timer resolution:           | 2 ns                                     | 2 ns                                     |
| Timer accuracy:             | ±(5 ns + 0.01%)                          | ±(5 ns + 0.01%)                          |
| Greater than duration:      | 3.33 ns to 55 ms in 3.3 ns<br>increments | 3.33 ns to 55 ms in 3.3 ns<br>increments |
| Less than duration:         | 6.67 ns to 55 ms in 3.3 ns<br>increments | 6.67 ns to 55 ms in 3.3 ns<br>increments |
| Timer reset latency:        | 40 ns                                    | 40 ns                                    |

PowerAll necessary power is supplied by the backplane connector of the logicRequirementsanalysis system mainframe.

**Environmental** Indoor use only. Characteristics

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 733)
- Non-operating Environment (see page 733)

| Operating<br>Environment | Temperature: | 0°C to 50°C (+32°F to 122°F). Reliability is enhanced when operating within the following range +20°C to 35°C (+68°F to 95°F).  |
|--------------------------|--------------|---|
|                          | Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing. |
|                          | Altitude:    | 0 to 3,000 m (10,000 ft)  |
|                          | Vibration:   | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms   |

#### Non-operating Environment

| Temperature:                    | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|---------------------------------|--|
| Humidity:                       | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                       | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

| See Also | • What is a Specification (see page 785)  |
|----------|---|
|          | • What is a Characteristic (see page 786) |

## **16760 Logic Analyzer Specifications and Characteristics**

Describes the specifications and characteristics of the 16760 logic analyzer.

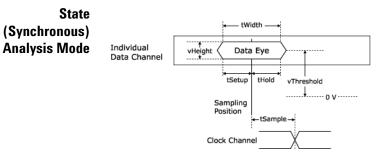
| NOTE Items r | marked with an asterisk (* | ) are specifications. | All others are characteristics. |
|--------------|----------------------------|-----------------------|---------------------------------|
|--------------|----------------------------|-----------------------|---------------------------------|

- Module Channel Counts (see page 734)
- Probes (see page 734)
- State (Synchronous) Analysis Mode (see page 734)
- Timing (Asynchronous) Analysis Mode (see page 740)
- Power Requirements (see page 742)
- Environmental Characteristics (see page 742)

#### Module Channel Counts

|                | State Analysis      | Timing Analysis |
|----------------|---------------------|-----------------|
| 1-card module: | 32 data + 2 clocks  | 34              |
| 2-card module: | 66 data + 2 clocks  | 68              |
| 3-card module: | 100 data + 2 clocks | 102             |
| 4-card module: | 134 data + 2 clocks | 136             |
| 5-card module: | 168 data + 2 clocks | 170             |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".



## Specifications for Each Input

|  | 800, 1250, 1500 Mb/s<br>Modes | 200, 400 Mb/s<br>Modes | Description/Notes  |
|--|-------------------------------|------------------------|--|
| Minimum tWidth<br>(data to clock):   | 500 ps                        | 1.25 ns                | Eye width in system<br>under test. <sup>2 (see</sup><br>page 735)  |
| Minimum tSetup<br>(data to clock):   | 250 ps                        | 625 ps                 | Data setup time<br>required before<br>tSample.   |
| Minimum tHold (data<br>to clock):  | 250 ps                        | 625 ps                 | Data hold time<br>required after<br>tSample.   |
| Minimum vHeight <sup>1</sup><br><sup>(see page 735)</sup> (all<br>inputs): | 100 mV                        | 100 mV                 | E5379A 100-pin<br>differential probe. <sup>3</sup><br>(see page 735)   |
|  | 250 mV                        | 250 mV                 | E5378A 100-pin<br>single-ended probe <sup>4</sup><br>(see page 735), E5382A<br>single-ended<br>flying-lead probe set |
|  | 300 mV                        | 300 mV                 | E5380A 38-pin<br>single-ended probe  |

<sup>\*</sup>All specifications noted by an asterisk are the performance standards against which the product is tested.

<sup>1</sup>The analyzer can be configured to sample on the rising edge, the falling edge, or both edges of the clock. If both edges are used with a single-ended clock input, take care to set the clock threshold accurately to avoid phase error.

<sup>2</sup>Eye width and height are specified at the probe tip. Eye width as measured by eye finder in the analyzer may be less, and still sample reliably.

pSignal vHeight vHeigh

<sup>3</sup>For each side of a differential signal:

<sup>4</sup>The

clock inputs in the E5378A probe and the E5382A probe set may be connected differentially or single ended. Use the E5379A probe vHeight specification for clock channel(s) connected differentially.

User Adjustable Settings for Each Input

| Adjustment Range        |                         |                        |  |                        |
|-------------------------|-------------------------|------------------------|--|------------------------|
| 1500 Mb/s<br>State Mode | 1250 Mb/s<br>State Mode | 800 Mb/s<br>State Mode |  | 200 Mb/s<br>State Mode |

| tSample <sup>5 (see</sup><br><sup>page 736)</sup> (data<br>to clock): | 0 ns to +4 ns,<br>10 ps<br>resolution | -2.5 ns to<br>+2.5 ns, 10 ps<br>resolution | -2.5 ns to<br>+2.5 ns, 10 ps<br>resolution | -3.2 ns to<br>+3.2 ns,<br>100 ps<br>resolution | -3.5 ns to<br>+3 ns, 100 ps<br>resolution |
|---|---------------------------------------|--|--|--|---|
| vThreshold <sup>6</sup>   | -3 V to +5 V,                         | -3 V to +5 V,                              | -3 V to +5 V,                              | -3 V to +5 V,                                  | -3 V to +5 V,                             |
| (see page 736)  | 10 mV                                 | 10 mV                                      | 10 mV                                      | 10 mV  | 10 mV                                     |
| (all inputs):   | resolution                            | resolution                                 | resolution                                 | resolution                                     | resolution                                |

<sup>5</sup>Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes synchronous sampling coincident with each active clock edge.

<sup>6</sup>Threshold applies to single-ended input signals. Thresholds are independently adjustable for the clock input of each pod and for each set of 16 data inputs for each pod. Threshold limits apply to both the internal reference and to the external reference input on the E5378A probe.

#### Synchronous State Analysis

|  | 1500 Mb/s<br>State Mode   | 1250 Mb/s<br>State Mode   | 800 Mb/s<br>State Mode   | 400 Mb/s<br>State Mode   | 200 Mb/s<br>State Mode   |
|--|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|
| Maximum<br>data rate on<br>each channel<br>9 (see page 740).   | 1.5 Gb/s                  | 1.25 Gb/s                 | 800 Mb/s                 | 400 Mb/s                 | 200 Mb/s                 |
| Minimum<br>clock interval,<br>active edge<br>to active<br>edge <sup>*</sup> (see<br>page 740), 9 (see<br>page 740).  | 667 ps                    | 800 ps                    | 1.25 ns                  | 2.5 ns                   | 5 ns                     |
| Minimum<br>state clock<br>pulse width<br>with clock<br>polarity rising<br>or falling <sup>9</sup><br>(see page 740). | N/A                       | N/A                       | 600 ps                   | 1.5 ns                   | 1.5 ns                   |
| Clock<br>periodicity:  | Clock must<br>be periodic | Clock must<br>be periodic | Periodic or<br>aperiodic | Periodic or<br>aperiodic | Periodic or<br>aperiodic |
| Number of<br>clocks:   | 1                         | 1                         | 1                        | 1                        | 1                        |

| Clock<br>polarity:  | Both edges                          | Both edges                          | Rising,<br>falling, or<br>both   | Rising,<br>falling, or<br>both      | Rising,<br>falling, or<br>both |
|---|-------------------------------------|-------------------------------------|--|-------------------------------------|--------------------------------|
| Minimum<br>data pulse<br>width <sup>* (see</sup><br>page 740).  | 600 ps                              | 750 ps                              | E5378A,<br>E5379A,<br>E5382A<br>probes:<br>750 ps<br>E5380A<br>probe: 1.5 ns | 1.5 ns                              | 1.5 ns                         |
| Number of<br>channels <sup>7</sup><br>(see page 740).           | 16 x (number<br>of cards) - 8       | 16 x (number<br>of cards) - 8       | 34 x (number<br>of cards) - 16   | 34 x (number<br>of cards) - 16      | 34 x (number<br>of cards)      |
| Maximum<br>channels on a<br>single time<br>base and<br>trigger: | 72 (5 cards)                        | 72 (5 cards)                        | 154 (5 cards)  | 154 (5 cards)                       | 170 (5 cards)                  |
| Maximum<br>memory<br>depth:                                     | 128 M<br>samples                    | 128 M<br>samples                    | 64 M<br>samples  | 32 M<br>samples                     | 32 M<br>samples                |
| Time tag<br>resolution:   | 4 ns <sup>8 (see</sup><br>page 740) | 4 ns <sup>8 (see</sup><br>page 740) | 4 ns <sup>8 (see</sup><br>page 740)  | 4 ns <sup>8 (see</sup><br>page 740) | 4 ns                           |
| Maximum<br>time count<br>between<br>states:                     | 17 seconds                          | 17 seconds                          | 17 seconds   | 17 seconds                          | 17 seconds                     |

| Trigger<br>resources: | <ul> <li>3 patterns<br/>evaluated<br/>as =, ≠, &gt;,<br/>&gt;=, &lt;, &lt;=<br/>on one<br/>pod; or<br/>evaluated<br/>as =, ≠<br/>across<br/>multiple<br/>pods; or 1<br/>ranges on<br/>each pod</li> <li>4 flags</li> <li>Arm in</li> </ul> | <ul> <li>3 patterns<br/>evaluated<br/>as =, ≠, &gt;,<br/>&gt;=, &lt;, &lt;=<br/>on one<br/>pod; or<br/>evaluated<br/>as =, ≠<br/>across<br/>multiple<br/>pods; or 1<br/>ranges on<br/>each pod</li> <li>4 flags</li> <li>Arm in</li> </ul> | <ul> <li>4 patterns<br/>evaluated<br/>as =, ≠, &gt;,<br/>&gt;=, &lt;, &lt;=<br/>on one<br/>pod; or<br/>evaluated<br/>as =, ≠<br/>across<br/>multiple<br/>pods; or 2<br/>ranges on<br/>each pod</li> <li>4 flags</li> <li>Arm in</li> </ul> | <ul> <li>8 patterns<br/>evaluated<br/>as =, ≠, &gt;,<br/>&gt;=, &lt;, &lt;=</li> <li>4 ranges<br/>evaluated<br/>as in<br/>range, not<br/>in range</li> <li>2<br/>occurrenc<br/>e counters</li> <li>4 flags</li> <li>Arm in</li> </ul> | <ul> <li>16<br/>patterns<br/>evaluated<br/>as =, ≠, &gt;,<br/>&gt;=, &lt;, &lt;=</li> <li>15 ranges<br/>evaluated<br/>as in<br/>range, not<br/>in range</li> <li>2 timers<br/>per card - 1</li> <li>2 global<br/>counters</li> <li>1<br/>occurrenc<br/>e counter<br/>per<br/>sequence<br/>step</li> <li>4 flags</li> <li>Arm in</li> </ul>  |
|-----------------------|--|--|--|---|---|
| Trigger<br>actions:   | • Trigger and fill memory  | • Trigger and fill memory  | • Trigger and fill memory  | <ul> <li>Go To</li> <li>Trigger and<br/>fill memory</li> </ul>  | <ul> <li>Go To</li> <li>Trigger,<br/>send<br/>email, and<br/>fill memory</li> <li>Trigger and<br/>Go To</li> <li>Store/don't<br/>store<br/>sample</li> <li>Turn<br/>on/off<br/>default<br/>storing</li> <li>Timer<br/>start/stop<br/>/pause/re<br/>sume</li> <li>Global<br/>counter<br/>increment<br/>/reset</li> <li>Occurrence<br/>counter<br/>reset</li> <li>Flag<br/>set/clear</li> </ul> |

| Maximum<br>trigger<br>sequence<br>steps:     | 2                                    | 2                                    | 4                                    | 16                                   | 16                                   |
|--|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| Maximum<br>trigger<br>sequence<br>speed:     | 1.5 Gb/s                             | 1.25 Gb/s                            | 800 MHz                              | 400 MHz                              | 200 MHz                              |
| Store<br>qualification:                      | Default                              | Default                              | Default                              | Default                              | Default and<br>per sequence<br>step  |
| Maximum<br>global<br>counter:                | N/A                                  | N/A                                  | N/A                                  | N/A                                  | 16,777,215                           |
| Maximum<br>occurrence<br>counter:            | N/A                                  | N/A                                  | N/A                                  | N/A                                  | 16,777,215                           |
| Maximum<br>pattern/rang<br>e term width:     | 32 bits <sup>10 (see</sup> page 740) |
| Timer value<br>range:                        | N/A                                  | N/A                                  | N/A                                  | N/A                                  | 100 ns to<br>4397 seconds            |
| Timer<br>resolution:                         | N/A                                  | N/A                                  | N/A                                  | N/A                                  | 4 ns                                 |
| Timer<br>accuracy:                           | N/A                                  | N/A                                  | N/A                                  | N/A                                  | ±(10 ns +<br>0.01%)                  |
| Timer reset<br>latency:                      | N/A                                  | N/A                                  | N/A                                  | N/A                                  | 65 ns                                |
| Data in to<br>BNC port out<br>delay latency: | 150 ns                               |

| Flag                    | N/A | N/A | N/A | N/A | 110 ns |
|-------------------------|-----|-----|-----|-----|--------|
| set/reset to evaluation |     |     |     |     |        |
| latency:                |     |     |     |     |        |

<sup>\*</sup>All specifications noted by an asterisk are the performance standards against which the product is tested.

<sup>7</sup>In 1.25 Gb/s and 1.5 Gb/s modes, only the even numbered channels (0, 2, 4, etc.) are acquired.

<sup>8</sup>The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.

<sup>9</sup>The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

 $^{10}\mbox{Maximum bus/signal width is 32 bits. Wider patterns can be created by "Anding" multiple bus/signals together.$ 

## Timing (Asynchronous) Analysis Mode

|   | Conventional Timing   | Transitional Timing  |
|---|---|--|
| Maximum timing analysis sample rate:                | 800 MHz   | 400 MHz  |
| Number of channels:                                 | 34 x (number of cards)  | For sample rates <400 MHz:<br>34 x (number of cards).<br>For sample rates =400 MHz:<br>34 x (number of cards) - 17 <sup>11</sup><br>(see page 742) |
| Maximum channels on a single time base and trigger: | 170 (5 cards)   | 170 (5 cards)  |
| Sample period:                                      | 1.25 ns   | 2.5 ns to 1 ms <sup>11 (see page 742)</sup>  |
| Memory depth:                                       | 64 M samples  | 32 M samples <sup>11 (see page 742)</sup>  |
| Sample period accuracy:                             | ±(250 ps + 0.01% of sample<br>period)   | ±(250 ps + 0.01% of sample<br>period)  |
| Channel-to-channel skew:                            | <1.5 ns   | <1.5 ns  |
| Time interval accuracy:                             | ±[sample period +<br>(channel-to-channel skew) +<br>(0.01% of time interval)] | ±[sample period +<br>(channel-to-channel skew) +<br>(0.01% of time interval)]  |
| Minimum data pulse width:                           | 1.5 ns for data capture 5.1 ns<br>for trigger sequencing                      | 3.8 ns for data capture 5.1 ns for trigger sequencing  |
| Maximum trigger sequence<br>speed:                  | 200 MHz   | 200 MHz  |

| Trigger resources:                        | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>15 ranges evaluated as in<br/>range, not in range</li> <li>2 edge/glitch</li> <li>(2 timers per card) - 1</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags, arm in</li> </ul> | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>15 ranges evaluated as in<br/>range, not in range</li> <li>2 edge/glitch</li> <li>(2 timers per card) - 1</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags, arm in</li> </ul> |
|---|--|--|
| Trigger resource conditions:              | Arbitrary Boolean<br>combinations  | Arbitrary Boolean<br>combinations  |
| Trigger actions:                          | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                |
| Maximum global counter:                   | 16,777,215   | 16,777,215   |
| Maximum occurrence<br>counter:            | 16,777,215   | 16,777,215   |
| Timer value range:                        | 100 ns to 4397 seconds   | 100 ns to 4397 seconds   |
| Timer resolution:                         | 4 ns   | 4 ns   |
| Timer accuracy:                           | ±(10 ns + 0.01%)   | ±(10 ns + 0.01%)   |
| Greater than duration:                    | 5 ns to 83 ms in 5 ns<br>increments  | 5 ns to 83 ms in 5 ns<br>increments  |
| Less than duration:                       | 10 ns to 83 ms in 5 ns<br>increments   | 10 ns to 83 ms in 5 ns<br>increments   |
| Timer reset latency:                      | 60 ns  | 60 ns  |
| Data in to BNC port out delay<br>latency: | 150 ns   | 150 ns   |
| Flag set/reset to evaluation latency:     | 110 ns   | 110 ns   |
| -   | <br>sitional/store qualified timing, mir<br>A samples.   | <br>nimum sample period is 5 ns and  |

| Power<br>Requirements | All necessary power is supplied by the backplane connector of the logic analysis system mainframe. |   |  |  |  |
|-----------------------|--|---|--|--|--|
| Environmental         |  |   |  |  |  |
| Characteristics       | See individual prol<br>environmental char  | be Specifications and Characteristics for probe racteristics. |  |  |  |
| Operating             | Operating  |   |  |  |  |
| Environment           | Temperature:         0°C to 45°C (+32°F to 113°F).   |   |  |  |  |
|                       |  |   |  |  |  |

- **See Also** What is a Specification (see page 785)
  - What is a Characteristic (see page 786)

# **16800-Series Logic Analyzer Specifications and Characteristics**

Describes the specifications and characteristics of the 16800-series logic analyzers.

**NOTE** Items marked with an asterisk (\*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Channel Count per Measurement Mode (see page 742)
- Probes (see page 743)
- Timing Zoom (see page 743)
- Other (see page 743)
- State (Synchronous) Analysis Mode (see page 743)
- Timing (Asynchronous) Analysis Mode (see page 746)
- General Information (see page 748)
- Environmental Characteristics (see page 749)

#### Channel Count per Measurement Mode

|  | 16801A/<br>16821A     | 16802A/<br>16822A     | 16803A/<br>16823A     | 16804A                 | 16806A                 |
|--|-----------------------|-----------------------|-----------------------|------------------------|------------------------|
| State<br>analysis <sup>11</sup><br>(see page 743). | 32 data + 2<br>clocks | 64 data + 4<br>clocks | 98 data + 4<br>clocks | 132 data + 4<br>clocks | 200 data + 4<br>clocks |
| Conventional<br>timing:                            | 34                    | 68                    | 102                   | 136                    | 204                    |

| Transitional<br>timing for<br>sample rates<br>< 500 MHz: | 34  | 68 | 102 | 136 | 204 |
|--|---|----|-----|-----|-----|
| Transitional<br>timing for<br>500 MHz<br>sample rate:    |   | 34 | 68  | 102 | 170 |
| <sup>11</sup> Unused clock                               | <sup>11</sup> Unused clock channels can be used as data channels. |    |     |     |     |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

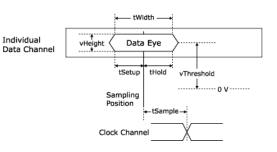
#### **Timing Zoom**

| Timing analysis sample rate: | 4 GHz (250 ps sample period)  |
|------------------------------|---|
| Timing interval<br>accuracy: | Within a pod pair: $\pm(1 \text{ ns} + 0.01\% \text{ of time interval reading})$<br>Between pod pairs: $\pm(1.75 \text{ ns} + 0.01\% \text{ of time interval reading})$ |
| Memory depth:                | 64 K  |
| Trigger position:            | Start, center, end, or user-defined   |
| Minimum data pulse<br>width: | 1 ns  |

#### Other

| Voltage threshold:  | -5 V to 5 V (10 mV increments)       |
|---------------------|--------------------------------------|
| Threshold accuracy: | $\pm 50 \text{ mV} + 1\%$ of setting |

State (Synchronous) Analysis Mode



|   | Option 250   | Option 500 <sup>10 (see page 746)</sup>  |
|---|--|--|
| tWidth <sup>*</sup> (see page 746), 1 (see<br>page 746) <u>.</u>                              | 1.5 ns <sup>* (see page 746)</sup> (@"latest<br>data sheet")   | 1.5 ns <sup>* (see page 746)</sup> (@"latest<br>data sheet")   |
| tSetup:   | 0.5 tWidth   | 0.5 tWidth   |
| tHold:  | 0.5 tWidth   | 0.5 tWidth   |
| tSample range <sup>2 (see page 746)</sup> :   | -3.2 ns to +3.2 ns   | -3.2 ns to +3.2 ns   |
| tSample adjustment<br>resolution:   | 80 ps typical  | 80 ps typical  |
| Maximum state data rate on<br>each channel:   | 250 Mb/s   | 500 Mb/s   |
| Memory depth <sup>4</sup> (see page 746) .  | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples |
| Number of independent<br>analyzers <sup>5 (see page 746)</sup> :                              | 2 (1 for 16801A or 16821A)   | 1  |
| Number of clocks <sup>6 (see</sup><br>page 746) <sub>:</sub>                                  | 4 (2 for 16801A or 16821A)   | 1  |
| Number of clock qualifiers <sup>6</sup><br>(see page 746)                                     | 4 (2 for 16801A or 16821A)   | N/A  |
| Minimum time between active<br>clock edges <sup>*</sup> (see page 746), 7 (see<br>page 746) : | 4.0 ns   | 2.0 ns   |
| Minimum master-to-slave<br>clock time:  | 1 ns   | N/A  |
| Minimum slave-to-master<br>clock time:  | 1 ns   | N/A  |
| Minimum slave-to-slave clock<br>time:   | 4.0 ns   | N/A  |
| Minimum state clock pulse<br>width:   | Single edge: 1.0 ns<br>Multiple edge: 1.0 ns   | Single edge: 1.0 ns<br>Multiple edge: 2.0 ns   |
| Clock qualifier setup time:   | 500 ps   | N/A  |
| Clock qualifier hold time:  | 0  | N/A  |
| Time tag resolution:  | 2 ns   | 1.5 ns   |
| Maximum time count between stored states:   | 32 days  | 32 days  |

| Maximum trigger sequence speed:     | 250 MHz   | 500 MHz   |
|-------------------------------------|---|---|
| Maximum trigger sequence<br>steps:  | 16  | 16  |
| Trigger sequence step<br>branching: | Arbitrary 4-way if/then/else  | 2-way if/then/else  |
| Trigger position:                   | Start, center, end, or user-defined   | Start, center, end, or<br>user-defined  |
| Trigger resources:                  | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul>                      | <ul> <li>14 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>7 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:        | Arbitrary Boolean combinations  | Arbitrary Boolean<br>combinations   |
| Trigger actions:                    | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger and fill memory</li> </ul>  |
| Store qualification:                | Default (global) and per sequence step  | Default (global)  |
| Maximum global counter:             | 2E+24   | N/A   |
| Maximum occurrence<br>counter:      | 2E+24   | 2E+24   |
| Maximum pattern width:              | Smaller of 128 bits or maximum number of channels   | Smaller of 128 bits or<br>maximum number of channels  |
| Maximum range width:                | Smaller of 64 bits or maximum number of channels  | Smaller of 64 bits or maximum number of channels  |

| Timer value range:   | 60 ns to 2199 seconds | N/A |
|----------------------|-----------------------|-----|
| Timer resolution:    | 2 ns                  | N/A |
| Timer accuracy:      | ±(5 ns + 0.01%)       | N/A |
| Timer reset latency: | 60 ns                 | N/A |

<sup>\*</sup>Items marked with an asterisk (\*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

<sup>1</sup>Minimum eye width in system under test.

<sup>2</sup>Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

<sup>3</sup>Use of eye finder is recommended in 500 Mb/s state mode.

<sup>4</sup>In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.

<sup>5</sup>Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.

<sup>6</sup>In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

<sup>7</sup>Tested with input signal Vh = 1.25 V, Vl = 0.75 V, threshold = 1.0 V, tr/tf = 180 ps ±30 ps (10%, 90%).

<sup>8</sup>Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

<sup>9</sup>For sample rates <500 MHz. For 500 MHz sample, subtract 34 channels.

<sup>10</sup>This option is not available for the 16801A and 16821A 34-channel logic analyzer models.

|  | Conventional Timing        | Transitional Timing <sup>8 (see</sup><br>page 746) |
|--|----------------------------|--|
| Sample rate on all channels:                                     | 500 MHz                    | 500 MHz  |
| Sample rate in half channel mode:                                | 1 GHz                      | N/A  |
| Number of independent<br>analyzers <sup>5 (see page 746)</sup> : | 2 (1 for 16801A or 16821A) | 2 (1 for 16801A or 16821A)                         |
| Sample period (half channel):                                    | 1.0 ns                     | N/A  |
| Sample period (full channel):                                    | 2.0 ns                     | 2.0 ns   |
| Minimum data pulse width:  | 1 sample period + 1.0 ns   | 1 sample period + 1.0 ns                           |

#### Timing (Asynchronous) Analysis Mode

| Time interval accuracy:               | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  |
|---------------------------------------|---|---|
| Memory depth in full channel<br>mode: | Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M  | Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M  |
| Memory depth in half channel<br>mode: | Option 000: 512 K<br>Option 001: 2 M<br>Option 004: 8 M<br>Option 016: 32 M<br>Option 032: 64 M   | N/A   |
| Maximum trigger sequence speed:       | 250 MHz   | 250 MHz   |
| Maximum trigger sequence<br>steps:    | 16  | 16  |
| Trigger sequence step<br>branching:   | Arbitrary 4-way if/then/else  | Arbitrary 4-way if/then/else  |
| Trigger position:                     | Start, center, end, or<br>user-defined  | Start, center, end, or<br>user-defined  |
| Trigger resources:                    | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>15 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:          | Arbitrary Boolean<br>combinations   | Arbitrary Boolean<br>combinations   |

| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> |
|--------------------------------|---|---|
| Maximum global counter:        | 2E+24   | 2E+24   |
| Maximum occurrence<br>counter: | 2E+24   | 2E+24   |
| Maximum range width:           | 32 bits   | 32 bits   |
| Maximum pattern width:         | Smaller of 128 bits or maximum number of channels   | Smaller of 128 bits or<br>maximum number of channels  |
| Timer value range:             | 60 ns to 2199 seconds   | 60 ns to 2199 seconds   |
| Timer resolution:              | 2 ns  | 2 ns  |
| Timer accuracy:                | ±(5 ns + 0.01%)   | ±(5 ns + 0.01%)   |
| Greater than duration:         | 4.0 ns to 67 ms in 4.0 ns<br>increments   | 4.0 ns to 67 ms in 4.0 ns<br>increments   |
| Less than duration:            | 8.0 ns to 67 ms in 4.0 ns<br>increments   | 8.0 ns to 67 ms in 4.0 ns<br>increments   |
| Timer reset latency:           | 60 ns   | 60 ns   |

## **General** Power:

#### Information

16801A, 16802A, 16803A: 115/230 V, 48 to 66 Hz, 615 W max. 16804A, 16806A, 16821A, 16822A, 16823A: 115/230 V, 48 to 66 Hz, 775 W max.

#### **Dimensions:**

288.22 mm height (11.347 in), 443.23 mm width (17.450 in), 330.32 mm depth (13.005 in)

#### Weight:

|         | Max Net            | Max Shipping       |
|---------|--------------------|--------------------|
| 16801A: | 12.9 kg (28.5 lbs) | 19.7 kg (43.5 lbs) |

| 16802A: | 13.2 kg (28.9 lbs) | 19.9 kg (43.9 lbs) |
|---------|--------------------|--------------------|
| 16803A: | 13.7 kg (30.3 lbs) | 20.5 kg (45.3 lbs) |
| 16804A: | 14.2 kg (31.3 lbs) | 21.0 kg (46.3 lbs) |
| 16806A: | 14.6 kg (32.1 lbs) | 21.4 kg (47.1 lbs) |
| 16821A: | 14.2 kg (31.2 lbs) | 20.9 kg (46.2 lbs) |
| 16822A: | 14.2 kg (31.6 lbs) | 21.1 kg (46.6 lbs) |
| 16823A: | 14.5 kg (32.0 lbs) | 21.3 kg (47.0 lbs) |

User interface:

Windows® XP Professional

Windows 7 (With the 05.20.0000 release of the Agilent Logic Analyzer application, 16800-series logic analyzers having serial number MY51420101 or higher are shipped from the factory with Windows 7 operating system.)

#### Printers:

Can print to any local or network printer supported by the installed operating system (Windows<sup>®</sup> XP Professional or Windows 7).

# **Environmental** Indoor use only. Characteristics

See individual probe Specifications and Characteristics for probe environmental characteristics.

• Operating Environment (see page 749)

#### Operating Environment

| nvironment | Temperature: | 0°C to 50°C (+32°F to 122°F).                |
|------------|--------------|--|
|            | Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). |
|            | Altitude:    | 0 to 3,000 m (10,000 ft)                     |

**See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

## 16910/11 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16910/11 logic analyzer.

NOTE

Items marked with an asterisk (\*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 750)
- Probes (see page 750)
- Timing Zoom (see page 750)
- State (Synchronous) Analysis Mode (see page 751)
- Timing (Asynchronous) Analysis Mode (see page 754)
- Power Requirements (see page 756)
- Environmental Characteristics (see page 756)

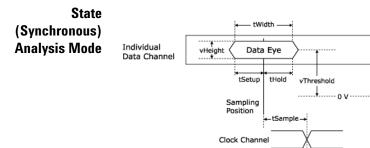
#### Module Channel Counts

|                | State Analysis<br>16910A | State Analysis<br>16911A | Timing Analysis<br>16910A | Timing Analysis<br>16911A |
|----------------|--------------------------|--------------------------|---------------------------|---------------------------|
| 1-card module: | 98 data + 4<br>clocks    | 64 data + 4<br>clocks    | 102                       | 68                        |
| 2-card module: | 200 data + 4<br>clocks   | 132 data + 4<br>clocks   | 204                       | 136                       |
| 3-card module: | 302 data + 4<br>clocks   | 200 data + 4<br>clocks   | 306                       | 204                       |
| 4-card module: | 404 data + 4<br>clocks   | 268 data + 4<br>clocks   | 408                       | 272                       |
| 5-card module: | 506 data + 4<br>clocks   | 336 data + 4<br>clocks   | 510                       | 340                       |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

#### **Timing Zoom**

| Timing analysis sample rate: | 4 GHz   |
|------------------------------|---|
| Timing interval<br>accuracy: | Within a pod pair: ±(1 ns + 0.01% of time interval reading)<br>Between pod pairs: ±(1.75 ns + 0.01% of time interval reading) |
| Memory depth:                | 64 K  |
| Trigger position:            | Start, center, end, or user-defined   |
| Minimum data pulse<br>width: | 1 ns  |



|   | Option 250  | Option 500  |
|---|---|---|
| tWidth <sup>*</sup> (see page 754), 1 (see<br>page 754) <u>:</u>                              | 1.5 ns <sup>* (see page 754)</sup> (@"latest<br>data sheet")  | 1.5 ns <sup>* (see page 754)</sup> (@"latest<br>data sheet")  |
| tSetup:   | 0.5 tWidth  | 0.5 tWidth  |
| tHold:  | 0.5 tWidth  | 0.5 tWidth  |
| tSample range <sup>2 (see page 754)</sup> :   | -3.2 ns to +3.2 ns  | -3.2 ns to +3.2 ns  |
| tSample adjustment resolution:  | 80 ps typical   | 80 ps typical   |
| Maximum state data rate on each channel:  | 250 Mb/s  | 500 Mb/s  |
| Number of channels on a single time base and trigger <sup>4</sup> (see page 754) :            | 16910A: 510 - (number of<br>clocks)<br>16911A: 340 - (number of<br>clocks)  | 16910A: 510 - (number of<br>clocks)<br>16911A: 340 - (number of<br>clocks)  |
| Memory depth <sup>4</sup> (see page 754) :  | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples |
| Number of independent<br>analyzers <sup>5 (see page 754)</sup> :                              | 2   | 1   |
| Number of clocks <sup>6 (see</sup> page 754) :  | 4   | 1   |
| Number of clock qualifiers <sup>6</sup><br>(see page <sup>754</sup> ) :                       | 4   | N/A   |
| Minimum time between active<br>clock edges <sup>*</sup> (see page 754), 7 (see<br>page 754) : | 4.0 ns  | 2.0 ns  |
| Minimum master-to-slave<br>clock time:  | 1 ns  | N/A   |

| Minimum slave-to-master clock time:       | 1 ns   | N/A   |
|---|--|---|
| Minimum slave-to-slave clock<br>time:     | 4.0 ns   | N/A   |
| Minimum state clock pulse width:          | Single edge: 1.0 ns<br>Multiple edge: 1.0 ns   | Single edge: 1.0 ns<br>Multiple edge: 2.0 ns  |
| Clock qualifier setup time:               | 500 ps   | N/A   |
| Clock qualifier hold time:                | 0  | N/A   |
| Time tag resolution:                      | 2 ns   | 1.5 ns  |
| Maximum time count between stored states: | 32 days  | 32 days   |
| Maximum trigger sequence speed:           | 250 MHz  | 500 MHz   |
| Maximum trigger sequence<br>steps:        | 16   | 16  |
| Trigger sequence step<br>branching:       | Arbitrary 4-way if/then/else   | 2-way if/then/else  |
| Trigger position:                         | Start, center, end, or<br>user-defined   | Start, center, end, or<br>user-defined  |
| Trigger resources:                        | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>14 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>7 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:              | Arbitrary Boolean<br>combinations  | Arbitrary Boolean<br>combinations   |

| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger and fill memory</li> </ul> |
|--------------------------------|---|--|
| Store qualification:           | Default (global) and per sequence step  | Default (global)   |
| Maximum global counter:        | 2E+24   | N/A  |
| Maximum occurrence<br>counter: | 2E+24   | 2E+24  |
| Maximum pattern width:         | 128 bits  | 128 bits   |
| Maximum range width:           | 64 bits   | 64 bits  |
| Timer value range:             | 60 ns to 2199 seconds   | N/A  |
| Timer resolution:              | 2 ns  | N/A  |
| Timer accuracy:                | ±(5 ns + 0.01%)   | N/A  |

| Timer reset latency:  | 60 ns   | N/A  |
|---|---|--|
| <sup>*</sup> Items marked with an asterisk (<br>represents the average or media<br>significant number of units.   | , ,   |  |
| <sup>1</sup> Minimum eye width in system u  | inder test.   |  |
| <sup>2</sup> Sample positions are independed<br>position causes the input to be side. A positive sample position<br>after each active clock edge. A sister sampled coincident with each clock | ynchronously sampled by that ar<br>causes the input to be synchron<br>ampling position of zero causes t | nount before each active clock<br>ously sampled by that amount |
| <sup>3</sup> Use of eye finder is recommend   | ed in 500 Mb/s state mode.  |  |
| <sup>4</sup> In 250 Mb/s state mode, with a depth. With one pod pair (34 cha channels) must remain unassign   | nnels) unassigned, the memory (   | depth is full One pod pair (34                                 |
| <sup>5</sup> Independent analyzers may be e only one analyzer may be used.  | ither state or timing. When the 5   | 00 Mb/s state mode is selected,                                |
| <sup>6</sup> In the 250 Mb/s state mode, the inputs must be on the master mo  |   | ifiers is 4. All clock and qualifier                           |
| <sup>7</sup> Tested with input signal Vh = 1.1 tr/tf = 180 ps $\pm$ 30 ps (10%, 90%)  |   | V.   |
| 0   | emory depth are halved unless a   | spare pod pair (34 channels) is                                |

|  | Conventional Timing             | Transitional Timing <sup>8 (see</sup><br>page 754)   |
|--|---------------------------------|--|
| Sample rate on all channels:                                     | 500 MHz                         | 500 MHz  |
| Sample rate in half channel mode:                                | 1000 MHz                        | N/A  |
| Number of channels:  | 16910A: 102 x (number of cards) | 16910A: For sample rates<br><500 MHz: 102 x (number of<br>cards).<br>For 500 MHz sample rate: 102<br>x (number of cards) - 34. |
|  | 16911A: 68 x (number of cards)  | 16911A: For sample rates<br><500 MHz: 68 x (number of<br>cards).<br>For 500 MHz sample rate: 68 x<br>(number of cards) - 34.   |
| Maximum channels on a single time base and trigger:              | 16910A: 510<br>16911A: 340      | 16910A: 510<br>16911A: 340   |
| Number of independent<br>analyzers <sup>5 (see page 754)</sup> : | 2                               | 2  |

## Timing (Asynchronous) Analysis Mode

| Sample period (half channel):         | 1.0 ns  | N/A   |
|---------------------------------------|---|---|
| Sample period (full channel):         | 2.0 ns  | 2.0 ns  |
| Minimum data pulse width:             | 1 sample period + 1.0 ns  | 1 sample period + 1.0 ns  |
| Time interval accuracy:               | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  |
| Memory depth in full channel<br>mode: | Option 256: 256 K<br>Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M   | Option 256: 256 K<br>Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M   |
| Memory depth in half channel<br>mode: | Option 000: 512 K<br>Option 001: 2 M<br>Option 004: 8 M<br>Option 016: 32 M<br>Option 032: 64 M   | N/A   |
| Maximum trigger sequence speed:       | 250 MHz   | 250 MHz   |
| Maximum trigger sequence steps:       | 16  | 16  |
| Trigger sequence step<br>branching:   | Arbitrary 4-way if/then/else  | Arbitrary 4-way if/then/else  |
| Trigger position:                     | Start, center, end, or<br>user-defined  | Start, center, end, or<br>user-defined  |
| Trigger resources:                    | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>15 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:          | Arbitrary Boolean<br>combinations   | Arbitrary Boolean<br>combinations   |

| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> |
|--------------------------------|---|---|
| Maximum global counter:        | 2E+24   | 2E+24   |
| Maximum occurrence<br>counter: | 2E+24   | 2E+24   |
| Maximum range width:           | 32 bits   | 32 bits   |
| Maximum pattern width:         | 128 bits  | 128 bits  |
| Timer value range:             | 60 ns to 2199 seconds   | 60 ns to 2199 seconds   |
| Timer resolution:              | 2 ns  | 2 ns  |
| Timer accuracy:                | ±(5 ns + 0.01%)   | ±(5 ns + 0.01%)   |
| Greater than duration:         | 4.0 ns to 67 ms in 4.0 ns<br>increments   | 4.0 ns to 67 ms in 4.0 ns<br>increments   |
| Less than duration:            | 8.0 ns to 67 ms in 4.0 ns<br>increments   | 8.0 ns to 67 ms in 4.0 ns<br>increments   |
| Timer reset latency:           | 60 ns   | 60 ns   |

PowerAll necessary power is supplied by the backplane connector of the logicRequirementsanalysis system mainframe.

**Environmental** Indoor use only. Characteristics

See individual probe Specifications and Characteristics for probe environmental characteristics.

- Operating Environment (see page 756)
- Non-operating Environment (see page 757)

#### Operating Environment

| Temperature: | 0°C to 40°C (+32°F to 104°F) when operating in a 16900A or 16902A/B mainframe. 0°C to 50°C (+32°F to 122°F) when operating in a 16901A or 16903A mainframe. |
|--------------|---|
| Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.                             |

| Altitude:  | 0 to 3,000 m (10,000 ft)  |
|------------|---|
| Vibration: | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms |

#### Non-operating

| E | nvi | ron | m | ent |
|---|-----|-----|---|-----|

| Temperature:                       | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|------------------------------------|--|
| Humidity:                          | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                          | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping<br>carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately<br>2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak),<br>5-minute resonant dwell at 4 resonances per axis. |

- **See Also** What is a Specification (see page 785)
  - What is a Characteristic (see page 786)

### 16950/51 Logic Analyzer Specifications and Characteristics

Describes the specifications and characteristics of the 16950/51 logic analyzer.

#### NOTE

Items marked with an asterisk (\*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 757)
- Probes (see page 758)
- Timing Zoom (see page 758)
- State (Synchronous) Analysis Mode (see page 758)
- Timing (Asynchronous) Analysis Mode (see page 761)
- Power Requirements (see page 763)
- Environmental Characteristics (see page 764)

#### Module Channel Counts

|                | State Analysis      | Timing Analysis |
|----------------|---------------------|-----------------|
| 1-card module: | 64 data + 4 clocks  | 68              |
| 2-card module: | 132 data + 4 clocks | 136             |
| 3-card module: | 200 data + 4 clocks | 204             |

#### 12 Reference

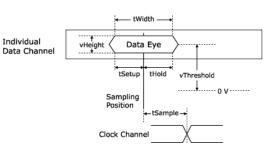
| 4-card module: | 268 data + 4 clocks | 272 |
|----------------|---------------------|-----|
| 5-card module: | 336 data + 4 clocks | 340 |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

#### **Timing Zoom**

| Timing analysis sample rate: | 4 GHz  |
|------------------------------|--|
| Timing interval accuracy:    | Within a pod pair: ±(750 ps + 0.01% of time interval reading)<br>Between pod pairs: ±(1.5 ns + 0.01% of time interval reading) |
| Memory depth:                | 64 K   |
| Trigger position:            | Start, center, end, or user-defined  |
| Minimum data pulse<br>width: | 750 ps   |





|  | 300 Mb/s State Mode  | 600 Mb/s State Mode<br>(16950A)<br>667 Mb/s State Mode<br>(16950B, 16951B)   |
|--|--|--|
| tWidth <sup>*</sup> (see page 761), 1 (see<br>page 761), 2 (see page 761) <u>.</u> | 16950A: 1 ns <sup>* (see page 761)</sup> ,<br>600 ps typical<br>16950B: 850 ps <sup>* (see page 761)</sup> ,<br>550 ps typical<br>16951B: 850 ps <sup>* (see page 761)</sup> ,<br>550 ps typical | 16950A: 1 ns <sup>* (see page 761)</sup> ,<br>600 ps typical<br>16950B: 850 ps <sup>* (see page 761)</sup> ,<br>550 ps typical<br>16951B: 850 ps <sup>* (see page 761)</sup> ,<br>550 ps typical |
| tSetup:  | 0.5 tWidth   | 0.5 tWidth   |
| tHold:   | 0.5 tWidth   | 0.5 tWidth   |
| tSample range <sup>3 (see page 761)</sup> :  | -4 ns to +4 ns   | -4 ns to +4 ns   |

| tSample adjustment resolution:  | 80 ps typical  | 80 ps typical  |
|---|--|--|
| tSample accuracy, manual adjustment:  | ±300 ps  | ±300 ps <sup>4</sup> (see page 761)  |
| Maximum state data rate on each channel:  | 300 Mb/s   | 16950A: 800 Mb/s<br>16950B: 1066 Mb/s<br>16951B: 1066 Mb/s   |
| Maximum channels on a single time base and trigger: <sup>5</sup> (see page 761) .           | 340 - (number of clocks)   | 306 - (1 clock)  |
| Memory depth <sup>5 (see page 761)</sup> :  | Option 256: 256 K samples <sup>10</sup><br>(see page 761)<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples<br>16951B: 256 M samples | Option 256: 256 K samples <sup>10</sup><br>(see page 761)<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples<br>16951B: 256 M samples |
| Number of independent<br>analyzers <sup>6 (see page 761)</sup> :                            | 2  | 1  |
| Number of clocks <sup>7 (see</sup> page 761) .  | 4  | 1  |
| Number of clock qualifiers <sup>7</sup> (see page 761)                                      | 4  | N/A  |
| Minimum time between active<br>clock edges <sup>*</sup> (see page 761), 8 (see<br>page 761) | 3.33 ns  | 16950A: 1.67 ns<br>16950B: 1.50 ns<br>16951B: 1.50 ns  |
| Minimum master-to-slave<br>clock time:  | 1 ns   | N/A  |
| Minimum slave-to-master clock time:   | 1 ns   | N/A  |
| Minimum slave-to-slave clock<br>time:   | 3.33 ns  | N/A  |
| Minimum state clock pulse<br>width:   | Single edge: 1.0 ns<br>Multiple edge: 1.0 ns   | Single edge: 500 ps<br>Multiple edge, 16950A: 1.67 ns<br>Multiple edge, 16950B: 1.50 ns<br>Multiple edge, 16951B: 1.50 ns  |
| Clock qualifier setup time:   | 500 ps   | N/A  |
| Clock qualifier hold time:  | 0  | N/A  |

### 12 Reference

| Time tag resolution <sup>5</sup> (see page 761) : | 2 ns  | 1.5 ns  |
|---|---|---|
| Maximum time count between stored states:         | 32 days   | 32 days   |
| Maximum trigger sequence<br>speed:                | 300 MHz   | 16950A: 600 MHz<br>16950B: 667 MHz<br>16951B: 667 MHz   |
| Maximum trigger sequence<br>steps:                | 16  | 16  |
| Trigger sequence step<br>branching:               | Arbitrary 4-way if/then/else  | 2-way if/then/else  |
| Trigger position:                                 | Start, center, end, or<br>user-defined  | Start, center, end, or<br>user-defined  |
| Trigger resources:                                | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul>                      | <ul> <li>14 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>7 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
| Trigger resource conditions:                      | Arbitrary Boolean<br>combinations   | Arbitrary Boolean<br>combinations   |
| Trigger actions:                                  | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> | <ul> <li>Go To</li> <li>Trigger and fill memory</li> </ul>  |
| Store qualification:                              | Default (global) and per<br>sequence step   | Default (global)  |
| Maximum global counter:                           | 2E+24   | N/A   |

| Maximum occurrence<br>counter: | 2E+24                 | 2E+24    |
|--------------------------------|-----------------------|----------|
| Maximum pattern width:         | 128 bits              | 128 bits |
| Maximum range width:           | 128 bits              | 128 bits |
| Timer value range:             | 50 ns to 2199 seconds | N/A      |
| Timer resolution:              | 2 ns                  | N/A      |
| Timer accuracy:                | ±(5 ns + 0.01%)       | N/A      |
| Timer reset latency:           | 50 ns                 | N/A      |

<sup>\*</sup>Items marked with an asterisk (\*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

<sup>1</sup>Minimum eye width in system under test.

<sup>2</sup>Your choice of probe can limit system bandwidth. Choose a probe rated at 600 Mb/s or greater to maintain system bandwidth.

<sup>3</sup>Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

 $^{4}$  Use of eye finder is recommended in 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode.

<sup>5</sup>In 300 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full One pod pair (34 channels) must remain unassigned for time tags in 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode.

<sup>6</sup>Independent analyzers may be either state or timing. When the 600 Mb/s (16950A) or 667 Mb/s (16950B, 16951B) state mode is selected, only one analyzer may be used.

<sup>7</sup>In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

<sup>8</sup>Tested with input signal Vh = 1.125 V, VI = 0.875 V, threshold = 1.0 V, tr/tf = 180 ps  $\pm 30$  ps (10%, 90%).

<sup>9</sup>Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

<sup>10</sup>Available on 16950A only.

| Timing         |
|----------------|
| (Asynchronous) |
| Analysis Mode  |

|                                   | Conventional Timing | Transitional Timing <sup>9 (see</sup><br>page 761) |
|-----------------------------------|---------------------|--|
| Sample rate on all channels:      | 600 MHz             | 600 MHz  |
| Sample rate in half channel mode: | 1200 MHz            | N/A  |

| Number of channels:  | 68 x (number of cards)   | For sample rates <600 MHz:<br>68 x (number of cards).<br>For 600 MHz sample rate: 68 x<br>(number of cards) - 34.   |
|--|--|---|
| Maximum channels on a single time base and trigger:              | 340  | 340   |
| Number of independent<br>analyzers <sup>6 (see page 761)</sup> : | 2  | 2   |
| Sample period (half channel):                                    | 833 ps   | N/A   |
| Sample period (full channel):                                    | 1.67 ns  | 1.67 ns   |
| Minimum data pulse width:  | 1 sample period + 500 ps   | 1 sample period + 500 ps  |
| Time interval accuracy:  | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)   | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)  |
| Memory depth in full channel<br>mode:                            | Option 256: 256 K <sup>10 (see<br/>page 761)</sup><br>Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M<br>Option 064: 64 M<br>16951B: 256 M  | Option 256: 256 K <sup>10 (see<br/>page 761)</sup><br>Option 001: 1 M<br>Option 004: 4 M<br>Option 016: 16 M<br>Option 032: 32 M<br>Option 064: 64 M<br>16951B: 256 M |
| Memory depth in half channel<br>mode:                            | Option 000: 512 K <sup>10 (see<br/>page 761)</sup><br>Option 001: 2 M<br>Option 004: 8 M<br>Option 016: 32 M<br>Option 032: 64 M<br>Option 064: 128 M<br>16951B: 512 M | N/A   |
| Maximum trigger sequence<br>speed:                               | 300 MHz  | 300 MHz   |
| Maximum trigger sequence steps:                                  | 16   | 16  |
| Trigger sequence step<br>branching:                              | Arbitrary 4-way if/then/else   | Arbitrary 4-way if/then/else  |
| Trigger position:  | Start, center, end, or<br>user-defined   | Start, center, end, or<br>user-defined  |

| Trigger resources:             | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>15 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>14 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>3 edge/glitch</li> <li>1 timer for every 34<br/>channels</li> <li>2 global counters</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> |
|--------------------------------|---|---|
| Trigger resource conditions:   | Arbitrary Boolean<br>combinations   | Arbitrary Boolean<br>combinations   |
| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                                     | <ul> <li>Go To</li> <li>Trigger, send email, and fill memory</li> <li>Trigger and Go To</li> <li>Turn on/off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Global counter increment/decrement/res et</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                                     |
| Maximum global counter:        | 2E+24   | 2E+24   |
| Maximum occurrence<br>counter: | 2E+24   | 2E+24   |
| Maximum range width:           | 128 bits  | 128 bits  |
| Maximum pattern width:         | 128 bits  | 128 bits  |
| Timer value range:             | 50 ns to 2199 seconds   | 50 ns to 2199 seconds   |
| Timer resolution:              | 2 ns  | 2 ns  |
| Timer accuracy:                | ±(5 ns + 0.01%)   | ±(5 ns + 0.01%)   |
| Greater than duration:         | 3.33 ns to 55 ms in 3.3 ns<br>increments  | 3.33 ns to 55 ms in 3.3 ns<br>increments  |
| Less than duration:            | 6.67 ns to 55 ms in 3.3 ns increments   | 6.67 ns to 55 ms in 3.3 ns<br>increments  |
| Timer reset latency:           | 50 ns   | 50 ns   |

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

#### 12 Reference

| Environmental   | Indoor use only.  |
|-----------------|---|
| Characteristics | See individual probe Specifications and Characteristics for probe<br>environmental characteristics. |

- Operating Environment (see page 764)
- Non-operating Environment (see page 764)

#### Operating Environment

| Temperature: | 0°C to 40°C (+32°F to 104°F) when operating in a 16900A or 16902A/B mainframe. 0°C to 50°C (+32°F to 122°F) when operating in a 16901A or 16903A mainframe. |
|--------------|---|
| Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.                             |
| Altitude:    | 0 to 3,000 m (10,000 ft)  |
| Vibration:   | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms   |

#### Non-operating Environment

| Temperature:                    | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|---------------------------------|--|
| Humidity:                       | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                       | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

**See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

### **16960 Logic Analyzer Specifications and Characteristics**

Describes the specifications and characteristics of the 16960 logic analyzer.

NOTE

Items marked with an asterisk (\*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 765)
- Probes (see page 765)
- State (Synchronous) Analysis Mode (see page 765)
- Timing (Asynchronous) Analysis Mode (see page 767)

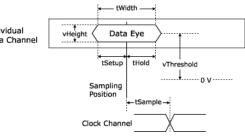
- Power Requirements (see page 769)
- Environmental Characteristics (see page 769)

#### Module Channel Counts

|                | State Analysis   |
|----------------|--|
| 1-card module: | 68 data channels (includes 2 clock/data channels and 2 clock ready/data channels)  |
| 2-card module: | 136 data channels (includes 4 clock/data channels and 4 clock ready/data channels) |
| 3-card module: | 204 data channels (includes 6 clock/data channels and 6 clock ready/data channels) |
| 4-card module: | 272 data channels (includes 6 clock/data channels and 6 clock ready/data channels) |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

## State (Synchronous) Analysis Mode Individual Data Channel



|   | 1.6 Gb/s State Mode                           |
|---|---|
| tWidth <sup>*</sup> (see page 767), 1 (see page 767), 2 (see page 767) <u>;</u> | 500 ps $^{*}$ (see page 767) , 400 ps typical |
| tSetup:   | 0.5 tWidth                                    |
| tHold:  | 0.5 tWidth                                    |
| tSample range <sup>3 (see page 767)</sup> :                                     | 5 ns  |
| tSample adjustment resolution:  | 11 ps typical                                 |
| Maximum state data rate on each channel <sup>* (see page 767)</sup> :           | 1.6 Gb/s                                      |
| Minimum state data rate on each channel:  | 100 Mb/s                                      |

| Maximum channels on a single time base and trigger:           | 272 - (1 clock)   |
|---|---|
| Memory depth:   | Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples<br>Option 100: 100 M samples  |
| Number of independent analyzers:                              | 1   |
| Number of clocks:   | 2 per card (on odd pods), 2 can be selected   |
| Number of clock ready inputs:                                 | 2 inputs per card (on even pods), 1 can be selected   |
| Minimum state clock pulse width <sup>4 (see</sup> page 767) : | 600 ps  |
| Time tag resolution:  | 25 ps   |
| Maximum time count between stored states:                     | 83.4 days   |
| Maximum trigger sequence speed:                               | 1.6 GHz   |
| Maximum trigger sequence steps:                               | 4   |
| Trigger sequence step branching:                              | Arbitrary 4-way if/then/else  |
| Trigger position:   | Start, center, end, or user-defined   |
| Trigger resources:  | <ul> <li>16 patterns evaluated as =, ≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>8 double-bounded ranges evaluated as in range, not in range</li> <li>1 occurrence counter per sequence step</li> <li>4 flags</li> </ul>   |
| Maximum burst events:   | 4 x 4 deep or 8 x 2 deep  |
| Maximum burst depth:  | 16 patterns (using 4 events x 4 deep)   |
| Maximum burst state speed:                                    | 1.6 GHz   |
| Trigger resource conditions:                                  | Arbitrary Boolean combinations  |
| Trigger actions:  | <ul> <li>Go To</li> <li>Trigger and Go To</li> <li>Trigger and fill memory</li> <li>Trigger, send email, and fill memory</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Store sample and Turn on default storing</li> <li>Don't store sample and Turn off default storing</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> |

| Store qualification:        | Default (global) and per sequence step |
|-----------------------------|--|
| Maximum occurrence counter: | 2E+24                                  |
| Maximum pattern width:      | 128 bits per bus                       |
| Maximum range width:        | 68 bits                                |

<sup>\*</sup> Items marked with an asterisk (\*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

<sup>1</sup> Minimum eye width in system under test.

 $^2$  Your choice of probe can limit system bandwidth. Choose a probe rated at 1.6 Mb/s or greater to maintain system bandwidth.

<sup>3</sup> Use of eye finder is recommended.

<sup>4</sup> Tested with input signal Vh = 1.125 V, Vl = 0.875 V, threshold = 1.0 V, tr/tf = 180 ps  $\pm 30$  ps (10%, 90%).

### Timing (Asynchronous) Analysis Mode

|   | Conventional Timing  | Transitional Timing  |
|---|--|--|
| Sample rate on all channels:                        | 2.0 GHz  | 2.0 GHz  |
| Number of channels:                                 | 68 x (number of cards)   | 68 x (number of cards)   |
| Maximum channels on a single time base and trigger: | 272  | 272  |
| Number of independent analyzers:                    | 1  | 1  |
| Sample period (full channel):                       | 500 ps   | 500 ps   |
| Minimum data pulse width:                           | 1 sample period + 500 ps   | 1 sample period + 500 ps   |
| Time interval accuracy:                             | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)   | ±(1 sample period + 1.25 ns +<br>0.01% of time interval reading)   |
| Memory depth in full channel<br>mode:               | Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples<br>Option 100: 100 M samples | Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples<br>Option 100: 100 M samples |
| Maximum trigger sequence<br>speed:                  | 2 GHz  | 2 GHz  |
| Maximum trigger sequence<br>steps:                  | 4  | 4  |
| Trigger sequence step<br>branching:                 | Arbitrary 4-way if/then/else   | Arbitrary 4-way if/then/else   |
| Trigger position:                                   | Start, center, end, or<br>user-defined   | Start, center, end, or<br>user-defined   |

| Trigger resources:             | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>8 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>4 edge</li> <li>1 timer</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul> | <ul> <li>16 patterns evaluated as =,<br/>≠, &gt;, &gt;=, &lt;, &lt;=</li> <li>8 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>4 edge</li> <li>1 timer</li> <li>1 occurrence counter per<br/>sequence step</li> <li>4 flags</li> </ul>   |
|--------------------------------|--|--|
| Trigger resource conditions:   | Arbitrary Boolean<br>combinations  | Arbitrary Boolean<br>combinations  |
| Trigger actions:               | <ul> <li>Go To</li> <li>Trigger and Go To</li> <li>Trigger and fill memory</li> <li>Trigger, send email, and fill memory</li> <li>Timer start/stop/pause/resume</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul>                               | <ul> <li>Go To</li> <li>Trigger and Go To</li> <li>Trigger and fill memory</li> <li>Trigger, send email, and fill memory</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> <li>Store sample and Turn on default storing</li> <li>Don't store sample and Turn off default storing</li> <li>Timer start/stop/pause/resume</li> <li>Occurrence counter reset</li> <li>Flag set/clear</li> </ul> |
| Maximum occurrence<br>counter: | 2E+24  | 2E+24  |
| Maximum range width:           | 68 bits  | 68 bits  |
| Maximum pattern width:         | 128 bits per bus   | 128 bits per bus   |
| Timer value range:             | 60 ns to 3298.5 seconds  | 60 ns to 3298.5 seconds  |
| Timer resolution:              | 3 ns   | 3 ns   |
| Timer accuracy:                | ±(5 ns + 0.01%)  | ±(5 ns + 0.01%)  |
| Greater than duration:         | 500 ps to 8.3886 ms in 500 ps<br>increments  | 500 ps to 8.3886 ms in 500 ps<br>increments  |
| Less than duration:            | 1 ns to 8.3886 ms in 500 ps<br>increments  | 1 ns to 8.3886 ms in 500 ps<br>increments  |
| Timer reset latency:           | 60 ns  | 60 ns  |
| Flag latency:                  | 50 ns  | 50 ns  |

| Power<br>Requirements | All necessary power is supplied by the backplane connector of the logic analysis system mainframe. |
|-----------------------|--|
|                       | Indoor use only.   |
| Characteristics       | See individual probe Specifications and Characteristics for probe environmental characteristics.   |

- Operating Environment (see page 769)
- Non-operating Environment (see page 769)

#### Operating Environment

| Temperature: | $0^\circ C$ to $40^\circ C$ (+32°F to 104°F). Reliability is enhanced when operating within the range +20°C to +35°C (+68°F to +95°F). |
|--------------|--|
| Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.        |
| Altitude:    | 0 to 3,000 m (10,000 ft)   |
| Vibration:   | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms  |

#### Non-operating Environment

| Temperature:                    | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|---------------------------------|--|
| Humidity:                       | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                       | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately<br>2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak),<br>5-minute resonant dwell at 4 resonances per axis. |

**See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

### **16962 Logic Analyzer Specifications and Characteristics**

Describes the specifications and characteristics of the 16962 logic analyzer.

**NOTE** Complete specifications and characteristics of the 16962 logic analyzer were not available at the time of this software release. For the latest specifications and characteristics, see the a "*16962 Logic Analyzer Data Sheet*" on the Agilent web site.

#### NOTE

Items marked with an asterisk (\*) are specifications. All others are characteristics.

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Module Channel Counts (see page 770)
- State (Synchronous) Analysis Mode (see page 770)
- Timing (Asynchronous) Analysis Modes (see page 771)
- Trigger Characteristics (see page 772)
- Other (see page 773)
- Power Requirements (see page 773)
- Logic Analyzer Mainframe Compatibility (see page 773)
- Environmental Characteristics (see page 773)

#### Module Channel Counts

| Channels per card (unused clock and clock ready inputs can be used as data channels): | 68 channels<br>State: 64 data + 2 clock + 2 clock ready<br>Timing: 68 data channels |
|---|---|
| Maximum channels on single time base and trigger:                                     | 340   |
| Number of mainframe slots per card:   | 1   |
| Number of independent analyzers per module set:                                       | 1   |

#### State (Synchronous) Analysis Mode

|   | 2 Gb/s State Mode                   |
|---|-------------------------------------|
| Maximum state speed <sup>1 (see page 771)</sup> :                       | 2 GHz (single edge, 2 GHz clock)    |
| Maximum state data rate <sup>*</sup> (see page 771), 1 (see page 771) . | 2 Gb/s (DDR, 1 GHz clock)           |
| Channels per module:  | State                               |
| 1-card module:  | 64 data + 2 clocks + 2 clock ready  |
| 2-card module:  | 132 data + 2 clocks + 2 clock ready |
| 3-card module:  | 200 data + 2 clocks + 2 clock ready |
| 4-card module:  | 268 data + 2 clocks + 2 clock ready |
| 5-card module:  | 336 data + 2 clocks + 2 clock ready |
| Maximum memory depth (samples) <sup>3 (see</sup>                        |                                     |
| Option 004 (included standard):   | 4 M                                 |
| Option 016:   | 16 M                                |
| Option 032:   | 32 M                                |
| Option 064:   | 64 M                                |

| Option 100:  | 100 M   |
|--|---|
| Minimum time between active clock edges:   | 500 ps  |
| Minimum state clock pulse width <sup>2 (see page 771)</sup> :                    |   |
| Single edge:   | 250 ps  |
| Multiple edge:   | 500 ps  |
| Number of clocks:  | 2 per card (on odd pods), 1 can be selected         |
| Number of clock ready inputs:  | 2 inputs per card (on even pods), 1 can be selected |
| Time tag resolution:   | 25 ps   |
| Maximum time count between stored states:  | 83.4 days   |
| Automated threshold/sample position,<br>Simultaneous eye diagrams, all channels: | Yes   |
|  |   |

<sup>\*</sup> Items marked with an asterisk (\*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

<sup>1</sup> Requires continuous, periodic clock.

 $^2$  Tested with input signal Vh = 1.125 V, Vl = 0.875 V, threshold = 1.0 V,

 $tr/tf = 180 \text{ ps } \pm 30 \text{ ps} (10\%, 90\%).$ 

<sup>3</sup> Store qualification consumes 1 sample per store qualified block.

|                                    | 2 GHz Full Channel | 4 GHz Half Channel | 8 GHz Quarter<br>Channel |
|------------------------------------|--------------------|--------------------|--------------------------|
| Maximum sample<br>rate:            | 2.0 GHz            | 4.0 GHz            | 8.0 GHz                  |
| Sample period:                     | 500 ps             | 250 ps             | 125 ps                   |
| Maximum memory<br>depth (samples): |                    | (2x memory option) | (4x memory option)       |
| Option 004<br>(included standard): | 4 M                | 8 M                | 16 M                     |
| Option 016:                        | 16 M               | 32 M               | 64 M                     |
| Option 032:                        | 32 M               | 64 M               | 128 M                    |
| Option 064:                        | 64 M               | 128 M              | 256 M                    |
| Option 100:                        | 100 M              | 200 M              | 400 M                    |
| Channels per module:               |                    |                    |                          |
| 1-card module:                     | 68                 | 34                 | 17                       |

| liming         |
|----------------|
| (Asynchronous) |
| Analysis Modes |

**T** 

|                      | 2 GHz Full Channel                | 4 GHz Half Channel                                     | 8 GHz Quarter<br>Channel  |
|----------------------|-----------------------------------|--|---|
| 2-card module:       | 136                               | 68   | 34  |
| 3-card module:       | 204                               | 102  | 51  |
| 4-card module:       | 272                               | 136  | 68  |
| 5-card module:       | 340                               | 170  | 85  |
| Pod usage:           | All pods                          | 1 pod from each pod<br>pair, user selectable           | 1 pod from each pod pair, user selectable   |
| Channel usage:       | All channels                      | All channels of selected pods                          | Even channels of selected pods  |
| Probe connection:    | Direct to logic<br>analyzer cable | Direct to logic<br>analyzer cable for<br>selected pods | E5386A adapter<br>recommended<br>between probe and<br>logic analyzer cable<br>for selected pods |
| Transitional timing: | Available                         | Available  | Available   |

### Trigger Characteristics

| Maximum trigger sequence speed:  | 2 GHz (500 ps)  |
|--|---|
| Trigger resources — create a trigger from any 8<br>of the listed resources (7 in transitional timing): | <ul> <li>16 pattern detectors evaluated as =, ≠, &gt;, &gt;=, &lt;, &lt;=, in range, not in range</li> <li>8 range detectors</li> <li>4 to 8 burst detectors</li> <li>4 edge detectors in timing, 3 in transitional timing</li> <li>4 flags</li> <li>1 timer in timing, transitional timing, or state — state timer's minimum time is 1 us</li> <li>1 arm in</li> </ul> |
| Trigger resource combinations:   | Arbitrary Boolean combinations  |
| Trigger actions:   | <ul> <li>Go To</li> <li>Trigger and fill memory</li> <li>Trigger and Go To</li> <li>Trigger, send email, and fill memory</li> </ul>   |
| Store qualification actions (available in state<br>mode):  | <ul> <li>Store sample</li> <li>Don't store sample</li> <li>Turn on default storage</li> <li>Turn off default storage</li> <li>Store sample and Turn on default storing</li> <li>Don't store sample and Turn off default storing</li> </ul>  |

| Timer actions:                   | <ul> <li>Start from reset</li> <li>Stop and reset</li> <li>Pause</li> <li>Resume</li> </ul> |
|----------------------------------|---|
| Flag actions:                    | <ul> <li>Set</li> <li>Clear</li> <li>Pulse set</li> <li>Pulse clear</li> </ul>              |
| Trigger sequence step branching: | Arbitrary 4-way if/then/else  |
| Trigger position:                | Start, center, end, or user-defined   |
| Maximum pattern width:           | 128 bits — single bus<br>340 bits — AND of multiple buses/signals<br>across multi-card set  |

#### Other

| Supported signal types:        | Single-ended and differential   |
|--------------------------------|---------------------------------|
| Probe compatibility:           | 90-pin cable connector          |
| Voltage threshold:             | -3 V to 5 V in 10 mV increments |
| Threshold accuracy:            | ±(30 mV + 1% of setting)        |
| Threshold setting granularity: | By channel                      |

Logic Analyzer<br/>Mainframe16902B 6-slot modular logic analysis system with software revision 3.82 or<br/>greater.

# Compatibility

**Power** All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics Indoor use only.

Operating Environment

| Temperature: | 0°C to 40°C (+32°F to 104°F). Reliability is enhanced when operating within the range +20°C to +35°C (+68°F to +95°F).          |
|--------------|---|
| Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing. |
| Altitude:    | 0 to 3,000 m (10,000 ft)  |
| Vibration:   | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms   |

#### Non-operating Environment

| Temperature:                    | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|---------------------------------|--|
| Humidity:                       | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                       | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

#### **See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

### **16900-Series Logic Analysis System Frame Characteristics**

- General Information (see page 774)
- Operating Environment Characteristics (see page 775)

### General Power:

Information

16900A: 115/230 V, 48 to 66 Hz, 1300 W max.
16901A: 115/230 V, 48 to 66 Hz, 775 W max.
16902A: 115/230 V, 48 to 66 Hz, 1300 W max.
16902B: 110/240 V, 47 to 63 Hz, 1300 W max.
16903A: 115/230 V, 48 to 66 Hz, 900 W max.

#### **Dimensions:**

16900A/16902A/16903A - 254 mm height (9.99 in), 442 mm width (17.38 in), 559 mm depth (22.0 in)

16902B - 288.13 mm height (11.344 in), 441.13 mm width (17.368 in), 564.33 mm depth (22.218 in)

16901A - 288.22 mm height (11.347 in), 443.23 mm width (17.450 in), 330.32 mm depth (13.005 in)

Weight:

|         | Max Net            | Max Shipping       |
|---------|--------------------|--------------------|
| 16900A: | 16 kg (35.2 lbs)   | 24.6 kg (54.2 lbs) |
| 16901A: | 13.6 kb (30.0 lbs) | 20.4 kg (45.0 lbs) |
| 16902A: | 17.2 kb (37.8 lbs) | 25.8 kg (56.8 lbs) |

| 16902B: | 19.6 kb (43.2 lbs) | 28.0 kg (61.7 lbs) |
|---------|--------------------|--------------------|
| 16903A: | 14.5 kg (32.0 lbs) | 23.2 kg (51.0 lbs) |

\* Logic analyzer or other instrument cards ordered with mainframes will add 0.9 kg (2.0 lb per card).

User interface:

Windows® XP Professional.

Windows 7 (With the 05.20.0000 release of the Agilent Logic Analyzer application, 16900-series logic analyzers having serial number MY51420101 or higher are shipped from the factory with Windows 7 operating system.)

Printers:

Can print to any local or network printer supported by the installed operating system (Windows<sup>®</sup> XP Professional or Windows 7 operating system).

#### Operating Environment Characteristics

| ent<br>ics | Temperature: | 16900A, 16902A, and 16902B: 0°C to 40°C (32°F to 104°F)<br>16901A and 16903A: 0°C to 50°C (32°F to 122°F) |
|------------|--------------|---|
|            | Humidity:    | 8 to 80% relative humidity at 40°C (104°F)  |
|            | Altitude:    | 3000 m (10,000 ft)  |

**See Also** • What is a Specification (see page 785)

• What is a Characteristic (see page 786)

### **U4154A Logic Analyzer Specifications and Characteristics**

Describes the specifications and characteristics of the U4154A logic analyzer.

| NOTE | Complete specifications and characteristics of the U4154A logic analyzer are available in the G U4154A Logic Analyzer Data Sheet (5990-7513EN) on the Agilent web site.   |
|------|---|
| NOTE | Items marked with an asterisk (*) are specifications. All others are characteristics.<br>"Typical" represents the average or median value of the parameter based on measurements<br>from a significant number of units. |

- Module Channel Counts (see page 776)
- State (Synchronous) Analysis Mode (see page 776)
- Timing (Asynchronous) Analysis Modes (see page 777)
- Trigger Characteristics (see page 777)
- Other (see page 778)
- Power Requirements (see page 778)
- Chassis Compatibility (see page 778)
- Environmental Characteristics (see page 779)

#### Module Channel Counts

| Channels per U4154A module (unused<br>clock and clock ready inputs can be used<br>as data channels):: | 136 channels<br>State analysis: 128 data channels + 8 clock<br>channels<br>Timing (Full channel): 128 data channels + 8<br>clock channels<br>Timing (Half channel): 64 data channels + 4<br>clock channels |
|---|--|
| Maximum channels on single time base and trigger:   | 272  |
| Number of AXie chassis slots per card::   | 1  |
| Number of U4154A modules that can be<br>connected in an AXIe chassis to form a<br>multi-card set      | 2  |

### State (Synchronous) Analysis Mode

|                                 | 2.5 Gb/s State data rate with 02G license<br>option<br>1.4 Gb/s State data rate with 01G license<br>option |
|---------------------------------|--|
| Setup/hold window <sup>1</sup>  | 500 ps (350 ps typ)  |
| S/H adjustment resolution       | 5 ps   |
| Sample range                    | -3 ns to + 3 ns  |
| Minimum state clock pulse width | 200 ps   |
| Number of clocks                | 1  |
| Number of qualifiers            | 4  |
| Time tag resolution             | 80 ps  |

| Maximum time count between stored states   | 66 days |  |
|--|---------|--|
| <sup>*</sup> Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical"<br>represents the average or median value of the parameter based on measurements from a<br>significant number of units. |         |  |
| <sup>1</sup> Dependant on probing system   |         |  |

# Timing (Asynchronous) Analysis Modes Sample rate on all channels 2500 MHz Sample rate in 1/2 channel mode 5000 MHz Sample period (full channel) 400 ps to 10 ns Sample period (half channel) 200 ps

| Sample period (full channel)   | 400 ps to 10 ns   |  |
|--|---|--|
| Sample period (half channel)   | 200 ps  |  |
| Maximum time between transitions   | 66 days   |  |
| Minimum data pulse width   | 1 sample period + 200 ps  |  |
| Time interval accuracy   | $\pm$ (1 sample period + 400 ps + 0.01% of time interval reading) |  |
| <sup>*</sup> Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units. |   |  |

### Trigger Characteristics

| Sample rate on all channels         | 2500 MHz   |
|-------------------------------------|--|
| Sample rate in 1/2 channel mode     | 5000 MHz   |
| Sample period (full channel)        | 400 ps   |
| Sample period (half channel)        | 200 ps   |
| Maximum trigger sequence<br>speed   | 2500 MHz   |
| Maximum trigger sequence<br>levels  | 8  |
| Trigger sequence level<br>branching | Arbitrary 4-way if/then/else   |
| Trigger position                    | Start, center, end, or user-defined  |
| Trigger resources                   | 16 patterns evaluated as =, !=, >, >=, <, <=<br>8 double-bounded ranges evaluated as in range, not in range<br>1 timer<br>3 flags<br>1 occurrence counter per sequence level |

| Trigger resource conditions  | Arbitrary Boolean combinations   |  |
|--|--|--|
| Trigger actions  | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Trigger and fill memory     |  |
| Store qualification actions  | Default (global) and per sequence level<br>Store/don't store sample<br>Turn on/off default storing |  |
| Maximum global counter   | N/A  |  |
| Maximum occurrence<br>counter  | 999,999,999  |  |
| Maximum pattern width  | 128 bits – single label<br>272 bits – AND of multiple labels across two-card set                   |  |
| Maximum range width <sup>4</sup>   | 64 bits  |  |
| Timers range   | 100 ns to 27 hours (in timing modes)<br>200 * state clock period to 27 hours (in state mode)       |  |
| Timer resolution   | 5 ns   |  |
| Timer accuracy   | ± (5 ns +0.01%) (in timing modes)<br>± (8 * state clock period +2ns<br>+0.01%) (in state mode)     |  |
| Timer reset latency  | 40 ns (in timing modes)<br>80 * state clock period (in state mode)                                 |  |
| <sup>*</sup> Items marked with an asterisk (*) are specifications. All others are characteristics. "Typical" represents the average or median value of the parameter based on measurements from a significant number of units. |  |  |

#### Other

| Supported signal types:        | Single-ended and differential |
|--------------------------------|-------------------------------|
| Probe compatibility:           | 90-pin cable connector        |
| Voltage threshold:             | -5 V to 5 V                   |
| Threshold accuracy:            | ±(30 mV + 1% of setting)      |
| Threshold setting granularity: | By channel                    |

**Chassis** Agilent AXIe 2-slot or 5-slot chassis with software revision 5.0 or greater. **Compatibility** 

PowerAll necessary power is supplied by the backplane connector of the AgilentRequirementsAXIe chassis.

| Environmental   | Indoor | use | only. |
|-----------------|--------|-----|-------|
| Characteristics |        |     |       |

#### Operating Environment

| Temperature: | $0^{\circ}$ C to $40^{\circ}$ C (+32°F to 104°F). Reliability is enhanced when operating within the range +20°C to +35°C (+68°F to +95°F). |
|--------------|--|
| Humidity:    | 0 to 80% relative humidity at 40°C (+104°F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.            |
| Altitude:    | 0 to 3,000 m (10,000 ft)   |
| Vibration:   | Random vibration 5-500 Hz, 10 minutes per axis, approximately 0.2 g rms  |

#### Non-operating Environment

| Temperature:                    | -40°C to +75°C (-40°F to +167°F). Protect the instrument from temperature extremes which cause condensation on the instrument.   |
|---------------------------------|--|
| Humidity:                       | 0 to 90% relative humidity at 65°C (149°F)   |
| Altitude:                       | 0 to 15,300 m (50,000 ft)  |
| Vibration (in shipping carton): | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

#### See Also

- What is a Specification (see page 785)
- What is a Characteristic (see page 786)

### **16850-Series Logic Analyzer Specifications and Characteristics**

This topic describes the specifications and characteristics of the 16850-series logic analyzers.

NOTE

"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

- Channel Count per Measurement Mode (see page 780)
- Probes (see page 780)
- Timing Zoom (see page 780)
- State (Synchronous) Analysis Mode (see page 780)
- Timing (Asynchronous) Analysis Mode (see page 782)
- Other (see page 784)
- General Information (see page 784)
- Environmental Characteristics (see page 784)

#### 12 Reference

#### Channel Count per Measurement Mode

| 16851A  | 16852A   | 16853A   | 16854A   |
|---|--|--|--|
| 34 (includes 1<br>clock + 1<br>clock<br>qualifier)  | 68 ( includes<br>1 clock + 3<br>clock<br>qualifiers) | 102 (includes<br>1 clock + 3<br>clock<br>qualifiers) | 136 (includes<br>1 clock + 3<br>clock<br>qualifiers) |
| Unused clock channels can be used as data channels. |  |  |  |

**Probes** A probe must be used to connect the logic analyzer to your device under test. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number at "www.agilent.com".

#### **Timing Zoom**

| Timing analysis sample rate: | 12.5 GHz (80 ps sample resolution)   |
|------------------------------|--|
| Timing interval<br>accuracy: | Within a 16 channel block<br>+/-(80 ps + 130ps + 0.01% of time interval reading) |
|                              | Between 16 channel blocks<br>+/-80 ps + 400ps + 0.01% of time interval reading)  |
| Memory depth:                | 256 K samples  |
| Trigger position:            | Start, center, end, or user-defined  |
| Minimum data pulse<br>width: | 1 sample period + 200 ps   |

#### State (Synchronous) Analysis Mode

|   | Default                         | Option 700                      |  |
|---|---------------------------------|---------------------------------|--|
| Minimum setup time (typical)            | 80 ps                           |                                 |  |
| Minimum hold time (typical)             | 80 ps                           |                                 |  |
| Minimum data valid window               | 160 ps                          |                                 |  |
| Sample position adjustment range        | 7 ns typical                    |                                 |  |
| Sample position adjustment resolution   | 20 ps typical                   |                                 |  |
| Maximum state data rate on each channel | 700 Mb/s                        | 1400 Mb/s                       |  |
| Maximum state clock<br>frequency        | single edge clocking<br>350 MHz | single edge clocking<br>700 MHz |  |

| Minimum state clock<br>frequency         | 12.5 MHz (single edge)   |         |
|--|--|---------|
|  | 6.25 MHz (both edges)  |         |
| Number of clocks                         | 1  |         |
|  | Clock on Pod1 of the master card   |         |
| Number of clock qualifiers               | For 16851A - 1   |         |
|  | For 16852A, 3A, 4A models - 3  |         |
| Minimum time between active clock edges  | 1429 ps  | 714 ps  |
| Minimum state clock pulse<br>width       | Single edge: 200 ps  |         |
| Clock qualifier setup time               | 200 ps   |         |
| Clock qualifier hold time                | 200 ps   |         |
| Time tag resolution                      | 80 ps  |         |
| Maximum time count between stored states | 66 days  |         |
| Maximum trigger sequence<br>speed        | 700 MHz  | 1.4 GHz |
| Maximum trigger sequence<br>steps        | 8  |         |
| Trigger sequence step<br>branching       | Arbitrary 4-way if/then/else   |         |
| Trigger position                         | Start, center, end, or user-defined  |         |
| Trigger resources                        | <ul> <li>16 patterns evaluated as =, !=, &gt;, &gt;=, &lt;, &lt;=</li> <li>8 double-bounded ranges evaluated as in range, not in range</li> <li>4 edge detectors in timing, 3 in transitional timing</li> <li>1 occurrence counter per sequence level</li> <li>1 timer</li> <li>3 flags</li> <li>1 arm in</li> </ul> |         |
| Trigger resource conditions              | Arbitrary Boolean combinations   |         |

| Trigger actions            | <ul> <li>Go To</li> <li>Trigger and fill memory</li> <li>Trigger and Go To</li> <li>Trigger, send e-mail, and fill memory</li> </ul> |  |
|----------------------------|--|--|
|                            | Occurrence counter reset     Store qualification   |  |
|                            | <ul> <li>Default (global) and per sequence level</li> <li>Store/don't store sample</li> <li>Turn on/off default storing</li> </ul>   |  |
| Maximum occurrence counter | 999,999,999  |  |
| Maximum pattern width      | 128 bits —single label   |  |
| Maximum range width        | 64 bits  |  |
| Timer value range          | 200 * sample clock period to 27 hours  |  |
| Timer resolution           | 5 ns   |  |
| Timer accuracy             | +/- (8 * sample clock period + 2ns + 0.01%)  |  |
| Timer reset latency        | 80 * sample clock period   |  |
|                            |  |  |

### Timing (Asynchronous) Analysis Mode

|   | Conventional and Transitional<br>Timing  |
|---|--|
| Maximum Sample rate on all channels         | 2.5 GHz  |
| Maximum Sample rate in half<br>channel mode | 5 GHz  |
| Sample period (half channel)                | 200 ps   |
| Sample period (full channel)                | 400 ps to 10 ns  |
| Minimum data pulse width                    | 1 sample period + 200 ps   |
| Time interval accuracy                      | Within a 16 channel pod<br>+/- (1 sample period + 130ps<br>+ 0.01% of time interval<br>reading)1 |
|   | Across 16 channel pods<br>+/- (1 sample period + 400ps<br>+ 0.01% of time interval<br>reading)2  |

|                                    | 1  |
|------------------------------------|--|
| Memory depth in full channel mode  | Up to 128M depth   |
| Memory depth in half channel mode  | Up to 256 M depth  |
| Maximum trigger sequence<br>speed  | 700 MHz  |
| Maximum trigger sequence<br>steps  | 8  |
| Trigger sequence step<br>branching | Arbitrary 4-way if/then/else   |
| Trigger position                   | Start, center, end, or<br>user-defined   |
| Trigger resources                  | <ul> <li>16 patterns evaluated as =,<br/>!=, &gt;, &gt;=, &lt;, &lt;=</li> <li>8 double-bounded ranges<br/>evaluated as in range, not<br/>in range</li> <li>4 edge detectors in timing,<br/>3 in transitional timing</li> <li>1 occurrence counter per<br/>sequence level</li> <li>1 timer</li> <li>3 flags</li> <li>1 arm in</li> </ul> |
| Trigger resource conditions        | Arbitrary Boolean<br>combinations  |
| Trigger actions                    | <ul> <li>Go To</li> <li>Trigger and fill memory</li> <li>Trigger and Go To</li> <li>Trigger, send e-mail, and fill memory</li> <li>Occurrence counter reset</li> </ul>   |
| Flag actions                       | <ul> <li>Set</li> <li>Clear</li> <li>Pulse Set</li> <li>Pulse Clear</li> </ul>   |
| Maximum occurrence counter         | 999,999,999  |
| Maximum range width                | 64 bits  |
| Maximum pattern width              | 128 bits –single label   |
| Timer range                        | 200 * sample clock period to 27 hours  |

#### 12 Reference

| Timer resolution    | 5 ns   |
|---------------------|--|
| Timer accuracy      | +/- (8 * sample clock period +<br>2ns + 0.01%) |
| Timer reset latency | 80 * sample clock period                       |

#### **Others**

| Supported signal types                     | Single-ended, differential |
|--|----------------------------|
| Automated threshold/sample position        | Yes                        |
| Simultaneous eye diagrams, all<br>channels | Yes                        |

#### General Power:

### Information

#### 100-240V $\pm$ 10 %, 50/60Hz, 400 W max

NOTE

The mains supply voltage fluctuations are not to exceed  $\pm$  10 % of the nominal supply voltage.

#### Weight:

| Max Net            | Max Shipping     |
|--------------------|------------------|
| 15.0 kg (33.0 lbs) | 21.7 kg (48 lbs) |

**Operating System:** 

Microsoft Windows 7 Embedded (64-bit)

#### Printers:

Can print to any local or network printer supported by the installed operating system (Windows 7).

EnvironmentalCharacteristicsPollution degree 2

• Installation category II

See individual probe Specifications and Characteristics for probe environmental characteristics.

• Operating Environment (see page 749)

| Operating   |
|-------------|
| Environment |

| Temperature: | 5°C to 40°C (+41°F to 104°F).   |
|--------------|---|
| Humidity:    | 80% to temperatures up to 31°C decreasing linearly to 50% rH at 40°C; |
|              |   |
| Altitude:    | 2000 m (6,561 ft)   |

- **See Also** What is a Specification (see page 785)
  - What is a Characteristic (see page 786)

### What is a Specification?

A specification is a numeric value, or range of values, that bounds the performance of a product parameter. The product warranty covers the performance of parameters described by specifications. Products shipped from the factory meet all specifications. Additionally, products sent to Agilent Customer Service Centers for calibration, and returned, meet all specifications. Specifications are verified by *calibration procedures*.

What is a Calibration
 Procedure?
 Calibration procedures verify that products or systems operate within the specifications. Parameters covered by specifications have a corresponding calibration procedure. Calibration procedures include both performance tests and system verification procedure. Calibration procedures are traceable and must specify adequate calibration standards.

Calibration procedures verify products meet the specifications by comparing measured parameters against a pass-fail limit. The pass-fail limit is the specification less any required guardband.

The term "calibration" refers to the process of measuring parameters and referencing the measurement to a calibration standard rather than the process of adjusting products for optimal performance.

NOTE Self-tests are not a substitute for calibration.

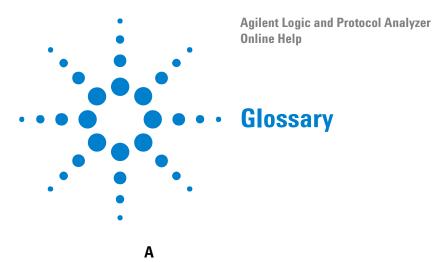
**See Also** • What is a Characteristic (see page 786)

### What is a Characteristic?

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics describe performance that is typical of the majority of a given product, but not subject to the same rigor associated with specifications. Characteristics are verified by *function tests*.

What is a Function tests are quick tests designed to verify basic operation of a product. Function tests include operator's checks and operation verification procedures. An operator's check is normally a fast test used to verify basic operation of a product. An operation verification procedure verifies some, but not all, specifications, and often at a lower confidence level than a calibration procedure.

**See Also** • What is a Specification (see page 785)



**acquisition** Denotes one complete cycle of data gathering by a measurement module. For example, if you are using an analyzer with 200K memory depth, one complete acquisition will capture and store 200K states in acquisition memory.

**acquisition depth** The acquisition depth is the amount of memory that is filled with data on an acquisition. The choices available depend on the maximum memory depth available in the analyzer that is being used.

**action** Actions are things that the analyzer does as a part of triggering, for example "Then Trigger and Fill Memory" or "Start Timer."

**activity indicator** Symbols next to logic analyzer channels that indicate whether a signal is a logic-high, or logic-low, or whether the signal is changing between highs and lows.

**advanced trigger** Advanced triggers provide more power than simple triggers, but are more complex.

**analysis probe** A probe connected to a microprocessor or standard bus in the device under test. An analysis probe provides an interface between the signals of the microprocessor or standard bus and the inputs of the logic analyzer.

**arming** Typically, instruments are armed immediately when Run or Run Repetitive is selected. For example, logic analyzers are commonly used to arm oscilloscopes.

**asynchronous sampling** When the logic analyzer acquires samples from the device under test asynchronously, that is, at regular intervals, such as every 100 ns. Also known as timing mode.

#### В

**beginning of acquisition** The beginning of the acquisition is the point in time where the collection of data begins.



#### **13** Glossary

**bits** A bit is a single signal in a bus. Numbering of bits begins with 0.

**bus** A bus is a group of associated signals, such as ADDR or DATA.

#### C

**captured data** Signal values that have been sampled by the logic analyzer and stored in its memory.

**card** A logic analyzer that can be inserted into a slot (see page 793) in a frame (see page 789). Cards can be combined with others to increase the channel count available in a single time domain.

**channel** A single line of input to the logic analyzer. Each channel corresponds to a lead that is connected to the device under test. Each channel is used to acquire one and only one signal from the device under test.

**chassis** A chassis is a modular instrument chassis that supports complex and high density testing. The Agilent AXIe chassis provides slots for installing multiple instrument modules such as the U4154A module.

**clock channel** A special logic analyzer input channel that can be used to determine the analyzer's sampling. Clock channels are identified on a pod by CLK.

**CLOCK IN BNC** This input is for a 10 MHz reference clock used to synchronize the logic analysis system with other external instruments.

Do not confuse this BNC input with logic analyzer clock inputs (which are present on the logic analyzer pod cables).

#### D

**data channel** A channel that carries data. Data channels cannot be used to clock logic analyzers. Data channels are numbered as opposed to clock channels which are labeled CLK.

**default storage** Default storage means "unless sequence step storage specifies otherwise, this is what should be stored". Sequence step storage always overrides default storage.

**delay** Delay is the horizontal position of the waveform on the screen for the timing analyzer. Delay time is measured from the trigger point in seconds.

**device under test** The system under development whose digital signals are captured by the logic analyzer.

**don't care** A "don't care" means that the state of the signal (high or low) is not relevant to the measurement. The analyzer ignores the state of this signal when determining whether a match occurs on an input bus/signal.

**double-click** When using a mouse as a pointing device, to double-click an item, position the cursor over the item, and then quickly press and release the left mouse button twice.

**drag and drop** Position the cursor over the item, and then press and hold the left mouse button. While holding the left mouse button down, move the mouse to drag the item to a new location. When the item is positioned where you want it, release the mouse button.

#### Ε

**edge** Logic analyzer trigger resources that allow detection of transitions on a signal. An edge term can be set to detect a rising edge, falling edge, or either edge or glitch.

**event** Events are the things you are looking for in your device under test, for example ADDR=0 or ADDR=5.

**external trigger** A signal outside the logic analyzer that is used to synchronize measurements between instruments. For example, the logic analyzer can be armed (activated) by a signal that comes from another instrument. Logic analyzers are commonly used to trigger oscilloscopes through a BNC connection.

#### F

**frame** A modular logic analysis system that has slot (see page 793)s in the back for the insertion of logic analyzer card (see page 788)s. Multiple frames can be connected together to form a multiframe logic analysis system.

#### G

**glitch** A glitch occurs when two or more transitions cross the logic threshold between consecutive timing analyzer samples.

#### I

**inverse assembler** A tool that displays the assembly language instructions for captured machine code.

#### L

**logic analyzer** An instrument that captures and displays digital signal values. A logic analyzer is like an oscilloscope, except that it only displays two voltage levels (a logic high or 1, and a logic low or 0) instead of many voltage levels. Because a logic analyzer only captures 1s and 0s, its sample rate can be slower than an oscilloscope that needs to capture move voltage detail. Consequently, a logic analyzer can capture a greater amount of overall execution time.

#### Μ

#### macro

- In pattern generator modules, "macros" (in the online help) are like subroutines in a programming language; they can have parameters and they can be called multiple times in the vector sequence to generate repeated or similar output vectors.
- In Microsoft Visual Basic for Applications (VBA), "macros" (in the online help) are **Sub** procedures that can be run from the user interface to automate an application.
- In previous Agilent logic analysis systems, macros, or *trigger macros* (see page 449), were what are now called trigger function (see page 795)s: preprogrammed components that are used to build trigger sequences.

**marker** A relocatable reference point in the data display. Markers can be used to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of state in the data.

**menu bar** The menu bar is located at the top of all windows. Use it to select drop down menus that contain tool or system options.

**module** A logical collection of logic analyzer card (see page 788)s that are connected together. This gives you the flexibility to increase channel count by using more than one card. A module can be a single card or several cards, and a single card or several card module can be split into two modules. By definition, a module consists of a single time domain. While a module can consist of a single card, a module is not a physical entity.

#### 0

**occurrence** Occurrence is used in triggering to define how many times something happens during the acquisition.

offline analysis Analyzing previously captured and saved logic analysis data without data acquisition hardware. In other words, you can use the *Agilent Logic Analyzer* application by itself on a Windows XP/Vista computer to analyze data in the waveform, listing, and compare windows.

#### Ρ

**pattern** Logic analyzer resources that represent single states to be found on buses/signals; for example, an address on the address bus or a status on the status lines.

**pod** A physical collection of logic analyzer channels within a card (see page 788). Pods are numbered relative to cards only. Pods are used to physically connect data and clock signals from the device under test to the analyzer.

**pod index** A logical number for a pod (see page 791). If a module (see page 790) has 20 pods, the pod indexes are 1 through 20 with no renumbering at card boundaries. In a multi-card module, numbering begins with the master card then continues from the bottom card up. Pod indexes can be used without considering how many pods are on each card (see page 788), or in which slot (see page 793)s the cards are located.

**pod pair** A group of two pods containing 16 data channels and 1 clock channel each. Pod pairs are used to physically connect data and clock signals from the device under test to the analyzer. Pods are assigned by pairs in the analyzer interface. The number of pod pairs available is determined by the channel width of the instrument.

**pod truncation** This occurs when opening a configuration file that was saved from a logic analyzer module that had more pods. Because the current module has fewer pods, truncation occurs. Any buses/signals assigned to truncated pods are unusable.

**point** To point to an item, move the mouse cursor over the item.

**polarity** Positive polarity is when an incoming low voltage is shown with a high waveform and a logical value of 1. Negative polarity is when an incoming high voltage is shown with a low waveform and a logical value of 0. Polarity affects the display of values and waveforms, and does not affect the trigger.

preprocessor See analysis probe (see page 787).

**probe** A device to connect the various instruments of the logic analysis system to the device under test. There are many types of probes and the one you should use depends on the instrument and your data requirements. As a verb, "to probe" means to attach a probe to the device under test.

**protocol** An agreed-upon format for transmitting data between two devices. The protocol determines: the type of error checking, data compression, encoding, how sending devices indicate they have finished sending a message, and how receiving devices indicate they have received a message.

#### 0

**quick trigger** Quick trigger allows you to quickly set up a simple trigger within the waveform and listing displays, by drawing a rectangle in the display area with the mouse. After a simple trigger has been defined, and the analyzer is run, the trigger is stored and can be recalled at any time.

#### R

**range pattern** Logic analyzer resources which let you set up patterns that represent a range of values, such as "ADDR in range 1000 to 2000". Most logic analyzers support a "not in range" operator as well as the "in range" operator. Range patterns are a convenient shortcut that can be used instead of AND'ing or OR'ing two patterns, such as "ADDR >= 1000 and ADDR <= 2000".

**repetitive measurement** A measurement in which the logic analyzer's trigger condition is searched for, and data storage is filled, repetitively.

**right-click** When using a mouse for a pointing device, to right-click an item, position the cursor over the item, and then quickly press and release the right mouse button.

**run** The single run measurement will save captured data to trace memory one time. The amount of data stored during a single run is equal to the amount of trace memory allotted.

**run repetitive** The run repetitive measurement will save the captured data to trace memory repetitively. The amount of data stored in a repetitive run is the same as a single run. During a repetitive run once the trace memory is full the system clears the trace memory and begins to refill with new data. This cycle will continue until the run is stopped.

**sample** A data sample is a single measurement. When an instrument samples the device under test, it takes a single measurement as part of its data acquisition cycle. The number of samples acquired is equal to the logic analyzers memory depth.

**sample period** The sample period is the period of time between samples. The sample period can be based on an internal sampling clock (also known as timing analysis or asynchronous sampling). Or, the sampling can be based on a signal in the device under test (also known as state analysis, or synchronous sampling).

**sampled data** Signal values that are sampled by the logic analyzer (not necessarily stored).

sampling The process by which the logic analyzer looks at digital signals.

**search** Searches through the acquired data for specified data pattern or value, time value, sample number, or marker. Search criteria can range from specific bits to multiple events, depending on which search option you choose.

**simple trigger** Simple triggers include triggers such as edges and bus patterns.

**single measurement** A measurement in which the logic analyzer's trigger condition is searched for, and data storage is filled, once.

**skew** Skew is the difference in channel delays between measurement channels.

**slot** An opening in the back of a frame (see page 789) where card (see page 788)s can be inserted. The slots are lettered from A to F with A being the topmost slot. Slots are physical entities and are always referred to by slot letter.

**snap to edge markers** Snap to edge markers enable easy placement of markers on waveform edges. When a marker is moved in the data display area, the cursor changes to a green "direction arrow" indicating the direction of the next valid edge. A red "valid edge" bar is placed on the next edge that the marker will be placed on.

**state analyzer** A logic analyzer that samples based on a clock signal in the device under test.

**state measurement** In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

**state mode** When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. For example, the logic analyzer might take a sample whenever there is a rising edge on a signal from the device under test. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also know as synchronous sampling.

**stop** Stops the measurement currently in progress.

**storage qualification** Storage qualification is only available in a state measurement, not timing measurements. Store qualification allows you to specify the type of data (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as wait-loops. Storage qualification lets you filter out specific types of data as the acquisition is running, which saves memory. In contrast filters can hide data after it has been collected.

**symbols** Names assigned to particular bus or signal values. Symbols in a display of captured data values are easy to read. Also, symbols make it easy to set up triggers on particular values. For example, in a communication protocol you could display the value FF as "end of file."

**synchronous sampling** When the logic analyzer acquires samples from the device under test synchronously, in other words, when a signal or signals from the device under test indicates when to acquire a sample. For example, the logic analyzer might take a sample whenever there is a rising edge on a signal from the device under test. Typically, the signal used to set up the sampling is a state machine clock signal or microprocessor clock signal. Also know as state mode.

#### Т

target system See device under test (see page 788).

**threshold voltage** The voltage level that the signal must cross before the logic analyzer recognizes a change in voltage levels. A high voltage level is indicated by a "1" and a low voltage level is indicated by a "0." TTL and ECL are two examples of voltage levels that the signal must cross.

**time/division** Time/division controls the "zooming" of a waveform display. Increasing the time/division zooms out, while decreasing the time/division zooms in.

**timer** Timers are used to create either a user-defined delay or a time standard which valid data duration is evaluated against.

**timing analyzer** A logic analyzer that samples at regular intervals based on an internal clock signal.

**timing measurement** In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the device under test, timing measurements capture traces of electrical activity over time. These measurements are asynchronous with the device under test.

**timing mode** When the logic analyzer samples from the device under test asynchronously, that is, at regular intervals, such as every 100 ns. Also known as asynchronous sampling.

**tool tip** Small information display (text readout) that appears during mouse operations such as hovering over a waveform or bus/signal name, moving markers, or drawing a rectangle in data. Use them as comments (see page 117) or to read current positions, waveform transition widths, or trigger specifications (when setting up quick triggers (see page 152) with mouse).

trace See acquisition (see page 787).

**transitional timing** When the logic analyzer is in transitional timing mode, the timing analyzer samples data at regular intervals, but only stores data when there is a threshold level transition (high-to-low transition, or low-to-high transition). Each time a level transition occurs on any of the bits, data on all channels is stored. A time tag is stored with each stored data sample so the measurement can be reconstructed and displayed later.

**trigger** The event about which acquired data is stored; in other words, the event that you are looking for. For example, you may want to trigger on an edge in order to see the events that lead up to it and the events that happen after it. The event that triggers the logic analyzer becomes a reference point in the data display.

**trigger function** Trigger functions are preprogrammed components that are used to build trigger sequences.

**trigger history** Each time you set up a new trigger and run the measurement, the trigger setup is saved in the configuration file. Each saved trigger can be retrieved and reused. The default number of triggers saved is 10.

**trigger position** The location of the trigger event in trace memory. If you want to view data after, about, or before the trigger event, you set the trigger position to the start, center, or end of trace memory, respectively.

**trigger sequence** A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to trigger.

#### V

**value at measurement** The value at measurement measures the value of a bus or a single signal at a specified marker location in data. Measurement results are displayed in the marker measurement display bar.

#### Ζ

**zooming** To expand and contract the waveform along the time base by varying the value in the time/div field. This action allows you to view specific portions of a particular waveform.

#### **Symbols**

!= operator, pattern trigger, 157, 169
< operator, pattern trigger, 157, 169</li>
<= operator, pattern trigger, 157, 169</li>
= operator, pattern trigger, 157, 169
> operator, pattern trigger, 157, 169
>= operator, pattern trigger, 157, 169

#### **Numerics**

01G license, 686 02G license, 686 1 Gbit low-profile LAN card, E5860A, 617 10 MHz CLOCK IN input, 47 16700 ASCII file format, 507 16700 ASCII format files, 47, 215 16700 data, importing after offline startup, 521 16700 Fast Binary Data, 515 16700 pod and bit association, 235 16700 terminology, 449 16700-series logic analysis system users, tips for. 59 16700-series logic analyzer data, offline analysis, 233, 234 16700-series logic analyzers, offline analysis, 57 16700-series, translating configuration files. 393 16740/41/42 logic analyzer notes, 638 16740/41/42 logic analyzer specifications and characteristics, 717 16750/51/52 logic analyzer notes, 640 16750/51/52 logic analyzer specifications and characteristics. 722 16753/54/55/56 logic analyzer notes, 643 16753/54/55/56 logic analyzer specifications and characteristics, 727 16760 logic analyzer, 51 16760 logic analyzer notes, 645 16760 logic analyzer specifications and characteristics, 734 16760 logic analyzer, eye finder operation in. 649 167xG, translating configuration files, 392 167xx fast binary data, importing, 223 1680/1690-series logic analyzer notes, 637 1680/1690-series logic analyzer product overview, 608 1680/1690-series logic analyzer specifications and characteristics, 714 16800-series logic analyzer front panel operation, 616

16800-series logic analyzer notes, 651 16800-series logic analyzer product overview, 614 16800-series logic analyzer specifications and characteristics, 742 16800-series logic analyzers, 47 16850-series logic analyzer front panel operation, 629 16850-series logic analyzer notes, 711 16850-series logic analyzer specifications and characteristics, 779 16900-series logic analysis system product overview, 617 16901A logic analysis system, 45 16902A/16903A logic analysis system front panel operation, 622 16910/11 logic analyzer notes, 654 16910/11 logic analyzer specifications and characteristics, 749 16950/51 logic analyzer notes, 656 16950/51 logic analyzer specifications and characteristics, 757 16950B logic analyzer, 46 16960 logic analyzer notes, 658 16960 logic analyzer specifications and characteristics, 764 16960 logic analyzer, stop behavior, 676 16960A logic analyzer, 40 16962 logic analyzer notes, 668 16962 logic analyzer specifications and characteristics. 769 16962 logic analyzer, state sampling clock, 674 16962 logic analyzer, state sampling clock restrictions. 675 16962 logic analyzer, stop behavior, 676 16962A logic analyzer, 39 6000 Series oscilloscopes, 51 8b. 334

### A

abbreviated marker name, 272, 282 about, help, 467 absolute time, 267 accessories, 1680/90-series logic analyzer, 608 accessories, 16800-series logic analyzer, 614 accessories, 16900-series logic analysis system, 617 accumulate results, eye finder, 556 accumulate waveforms, 252 accumulations, number of eye finder measurement, 557

acquiring data, 149 acquisition, 787 acquisition depth, 787 acquisition errors, 376 acquisition memory depth, 134, 135, 147, 500, 637, 638, 640, 651, 654, 656, 658, 669, 678.711.715.718.723.727.734.742. 749, 757, 766, 770, 779 acquisition memory depth and channel count trade-offs, 420, 648 acquisition mode. 500 acquisition mode, choosing, 119 acquisition mode, setting, 64 acquisition mode, state, 122 acquisition mode, timing, 120 acquisition speed. 637 acquisition time, transitional timing, 422 action, 787 action statements, 165, 166, 167 action statements, reading, 165 action, counter, 186 action, flag, 187 action, reset occurrence counter, 166, 186 action, storage control, 188 action, timer, 185 actions and events, trigger, 163 actions in trigger sequence, 433, 496 actions, inserting or deleting, 185 activation, software licenses, 361, 535 active software licenses, 360, 534 activity (bus/signal), 104 activity indicator, 787 activity indicators, 499 activity indicators in Listing window, 262 activity indicators in Waveform window, 247 Add Application dialog, 509 add external scope, 456 add icons to toolbar, 474 add logic analysis system, 531 Add or Remove Logic Analyzer Software tool. 367 add software, 367 adding a bus or signal, 105 adding a folder, 118 adding connections, 346 adding display windows, 346, 353 adding system to use list, 87 adding tools, 346 address alignment, trigger in Source window, 539 adjustable delay on state sampling clock input, 424 adjusting state mode sampling positions automatically, 130

advanced 2-way branch trigger function, state mode, 584 advanced 2-way branch trigger function, timing mode, **571** advanced 3-way branch trigger function, state mode, 585 advanced 3-way branch trigger function, timing mode, 571 advanced 4-way branch trigger function, state mode, 585 advanced 4-way branch trigger function, timing mode, 572 advanced clocking, 129 Advanced Clocking Setup dialog, 495 advanced if/then trigger function, state mode, 583 advanced if/then trigger function, timing mode, 570 advanced If/Then trigger functions, 560 advanced pod assignment mode, 541 advanced setup, 456 advanced trigger, 149, 163, 456, 471, 787 Advanced Trigger dialog, 496 advanced trigger example, 416 advanced trigger functions, state mode, 573 advanced trigger functions, timing mode, 560 advanced triggers in 16960/16962 logic analyzers, 660 Agilent Hardware Update dialog, 147 Agilent Logic Analyzer application, 3 Agilent Logic Analyzer application product overview, 631 Agilent Logic Analyzer Upgrade dialog, 497 Agilent symbol reader file, 142 aqLogicSvc.exe service, 402 agSymbolBuild.exe, 142 agSymbolQuery.exe, 143 ALA format, 588 ALA format configuration files, 206, 220, 224 ALA format configuration files, automatic module mapping, 518 ALA format configuration files, offline analysis, 237 ALA format configuration files, won't open, 374 ALA vs. XML format, when to use, 445 ALB module binary file format, 213, 598 ALB module binary file header format, 590 alias bus/signal name, 118 align trigger with, timing zoom, 558 aligning reference data, 306 alignment, bus/signal column, 267 alignment, packet column, 342 alignment, Set Quick Trigger, 315 all reference data, 307 alphanumeric keypad, 1680-series logic analyzer, 609 altitude, 715, 718, 723, 727, 734, 742, 749, 757, 769, 773, 774, 779 ambient temperature, 130 amplitude, 130 analog properties, 257 analog signal row properties, 256

analog signal, Voltage number base in Listing, 267 analog signals, overlaying, 244 analog signals, voltage markers for, 286 analogy, conveyor belt, 431 analysis probe, 81, 787 analysis tool development API, 57 Analyzer Setup dialog, 498 Analyzer Setup toolbar, 471 analyzer triggering, understanding, 431 analyzer, splitting, 98, 541 analyzer, unsplitting, 100 analyzing captured data, 219 analyzing listing data, 259 analyzing waveform data, 239 AND events, 180 AND'ed find events, 302 anything event, 180 API, tool development, 57 application (external), adding to Tools menu, 508 arm from another module, 193 arm from another module, wait for, 570, 582 arm in from event, 180, 182 arming, 787 arrange icons. 466 ASCII format symbol file, 601 Ascii number base, 169, 255, 267 ASCII symbol file, creating, 143 ASCII text file, print to, 354 Assign Names dialog, 108 asynchronous sampling, 120, 787 asynchronous sampling mode, 500 auto sample position setup, 130, 550 auto threshold and sample position setup, 130, 550 auto-connect at application startup, 513 auto-connect, selecting logic analysis system for. 92 automatic FPGA dynamic probe set up, 51 automatic threshold voltage adjustment, 52 automatically adjusting state mode sampling positions, 130 automatically mapping modules, 517 autosize columns, 266 available status, 89 AXIe chassis slots per card, 776

#### B

background color, Listing window, 263 background color, marker, 272, 285 background color, Source window, 314 background color, timing zoom listing, 264 background color, timing zoom waveforms, 251 background color, Waveform window, 249, 250 base, number, 116, 255, 267 base, symbol, 530 beginning of acquisition, 787 beginning of data, 242 Beginning of Data marker, 351

beginning of data, go to, 276 beginning of data, go to in Listing window, 260 best-fit algorithm, module mapping, 518 big endian, 114 Binary number base, 169, 255, 267 bit order, 111 bit reordering, 55, 114 bits, 788 bits of a bus, renaming, 47 block boundary addresses, 315 BNC connectors, trigger in/out, 193 boolean expressions, 435 boolean expressions in trigger sequence, 433 boolean expressions, setting parentheses, 184 boolean expressions, triggering capability, 432 borrow floating licenses, 364, 537 borrow licenses messages, 537 branch expression too complex, 384 branches, 436 brightness, display, 614 browsing source files, 310 buffer, reference, copying data to, 305 burst patterns in 16960/16962 logic analyzers, 661 burst patterns in default storage, 663 burst patterns in Else if clauses. 667 burst patterns in If clauses, 664 burst patterns in U4154A, 689 bus. 788 bus analysis tools, new, 458 bus clock, data valid relative to, 424 bus composite, eye finder data, 130 bus pattern trigger functions, timing mode, 560 bus pattern triggers, 157, 169 Bus vs Bus Sample VbaView window, 467 bus width, 104 bus, group signals into, 248 bus, renaming the bits, 108 bus, source code correlation, selecting, 312 bus, source correlation, 540 bus/signal column alignment, 267 bus/signal column properties, 265 bus/signal column width in Listing window, 266 bus/signal column, finding a, 261 bus/signal columns, re-arranging, 261 bus/signal data color, Listing window, 266 bus/signal data to export, 207 bus/signal data, exporting to CSV file, 55 bus/signal errors, 376 bus/signal event, 180 bus/signal folders, adding, 118 bus/signal name, alias, 118 bus/signal names, quick pick, 55 bus/signal names, setting up, 62 bus/signal names, sorting, 118 bus/signal naming, short or unique, 522 bus/signal number base, 255, 267 bus/signal patterns, finding, 294, 296 bus/signal patterns, finding complex, 302 bus/signal row properties, 253 bus/signal row, finding a, 244

bus/signal setup, 104, 456, 471 bus/signal values displayed as symbols, 269 bus/signal values, symbolic, 146 bus/signal, adding a new, 105 bus/signal, assigning channels in default bit order, 110 bus/signal, assigning channels in selected bit order, 111 bus/signal, deleting a, 106 bus/signal, renaming a, 107 buses, expanding/collapsing, 248 buses/signals in data import module, 229, 516 Buses/Signals tab, 499 buses/signals, define by importing netlist, 520 buses/signals, exporting data from selected, 526 buses/signals, inserting/deleting in Listing window, 262 buses/signals, inserting/deleting in Waveform window. 247 buses/signals, load warning, 386 bus-specific probes, 81 buttons, 16800-series logic analyzers, 616, 629 buttons, 1680-series logic analyzers, 609 buttons, 16902A/16903A logic analysis system. 622

# C

calibration, 785 calibration failed, 379 calibration procedure, 785, 786 cancel, 461 cancel operation, 473 cancel processing, module/tool/window, 542 captured data, 149, 788 captured data, analyzing, 219 captured data, comparing, 305 captured data, exporting to module binary (ALB) files, 213 captured data, exporting to module CSV files, 210 captured data, printing, 354 captured data, saving, 205 card, 788 card, logic analyzer, 503 cards (logic analyzer), combining, 98 cards in frame, 546 cards in module, 548 cascade windows, 466, 469 CDs on 16900A, 16902A, or 16903A frame, problems writing, 400 center about edges, 240 center about marker pair, 277, 460, 472 center alignment, bus/signal columns, 267 center rectangle, go to source line of, 311 center rectangle, showing/hiding, 265 center screen, placing marker at, 274 changing the display scale, 240 changing the time/division, 240 channel. 788 channel and pod connections, 548

channel assignment, split analyzer, 541 channel count and memory depth trade-offs, 420, 648 channel counts, 718, 723, 727, 734, 742, 749, 757, 765, 770, 776, 779 channel naming conventions, 418 channel numbers, 499 channel numbers (bus/signal), 104 channel order selection, enable, 111 channel order, reverse, 114 channel reordering, 55, 114 channel usage, 772 channel width, 120, 637 channels, 637, 638, 640, 651, 654, 656, 658, 669, 678, 711, 715, 727, 734, 742, 749, 757, 765, 770, 776, 779 channels (directions), packet column, 342 channels assigned (bus/signal), 104, 112 channels assigned (bus/signal), reordering, 114 channels on a single time base and trigger, 742, 749, 757, 766, 770, 776, 779 channels per card, 770 channels per module, 770, 771, 776 channels, assigning in default bit order, 110 channels, assigning in selected bit order, 111 channels, data on unassigned, transitional timing, 422 channel-to-channel skew. 715, 718, 723 character names, 334 characteristics, 714, 786 characteristics, 16740/41/42 logic analyzer, 718 characteristics, 16750/51/52 logic analyzer, 723 characteristics, 16753/54/55/56 logic analyzer, 727 characteristics, 16760 logic analyzer, 734 characteristics, 1680/1690-series logic analyzer, 715 characteristics, 16800-series logic analyzer, 742, 779 characteristics, 16900-series logic analysis frame, 774 characteristics, 16910/11 logic analyzer, 749 characteristics, 16950/51 logic analyzer, 757 characteristics, 16960 logic analyzer, 764 characteristics, 16962 logic analyzer, 769 Chart display tool, 449 chart mode, 449 Chart tool, 449 Chart window, 449 chart, viewing Waveform bus data as, 245 charts, custom data visualization, 490 chassis, 788 Chat dialog, 501 chat messages, 93 Chat Select Destination dialog. 502 Choose a Protocol Family and Bus dialog, 502 choose marker button, 1680-series logic analyzers, 609

choose marker button, 16902A/16903A logic analysis system, 622 clear favorite/recently used triggers, 527 clear flag, 167 clear flag action, 187 clear trigger sequence, 192 clearing a remote access password, 94 clearing eye finder measurement data, 130 clearing the trigger sequence, 496 clip board, copying module/tool/window status to. 542 clip board, copying screens to, 355 clip board, copying text to, 355 clipped (show) analog property, 257 clock channel, 110, 112, 788 CLOCK IN BNC, 788 clock mode (state sampling), Demultiplex, 124, 126 clock mode (state sampling), Dual Sample, 125 clock mode (state sampling), Master Only, 124, 125 clock mode (state sampling), Master/Slave, 124, 125 clock mode (state sampling), selecting, 123 clock pod/channel naming, 418 clock qualifier hold time, 727, 734, 742, 749. 757,779 clock qualifier setup time, 727, 734, 742, 749, 757.779 clock qualifiers, 727, 734, 742, 749, 757, 779 clock ready inputs, 766, 771 Clock Ready, latched or enabled, 675 clock setup, state mode, 376 clock threshold voltage, 102, 671 clock, slow or missing, 386 clock, state mode sampling, 415 clock, state mode sampling, setting up, 128 clock, timing mode sampling, 412, 413 clocks, 727, 734, 742, 749, 757, 766, 771, 779 clocks pod, 112 Coff/Stabs symbol files, 143 collapse a bus, 248 color, difference foreground/background, 307 color, filtered data in Waveform window, 250 color, Listing window background, 263 color, overlaid waveform, 250 color, reference data background, 307 color, selected packet box, 339 color, Source window background, 314 color, Source window text, 314 color, waveform, 254 color. Waveform window background, 249 colorize/filter tool, 458 column alignment in Listing window, 267 column autosize, 266 column base in Listing window, 262 column channels (directions), protocol, 322 column headings in Waveform window, 247 column properties, bus/signal, 265 column properties, packet summary, 340 COM Automation Server, 55

COM automation, use of XML format, 445 combining logic analyzer cards, 98 commands, keyboard, 631 comma-separated value files, 207, 588 comments, 117 comments, bus/signal, 104, 499 comments, General-Purpose ASCII symbol file format. 606 comments, If clause, displaying/hiding, 190 comments, marker, 286 comments, system in use, 89, 91, 531 communication timeout, floating license server, 390 compare, 57 compare differences, run until a number, 307 Compare menu, 463 compare operation keyboard commands, 631 Compare Overview bar, 306 compare packets, 329 Compare tool, 449 Compare window, 485 Compare window properties, 307 Compare window, new, 466 compared data, finding differences, 306 comparing a range of samples, 306 comparing captured data, 305 compatible modules, 445 complete scan, eye scan, 555 complex bus/signal patterns, finding, 302 complex triggers, setting up, 443 concepts, 409 conclusions, understanding logic analyzer triggering, 444 conditions in trigger sequence, 433 Config. 449 configuration file header information, 220 configuration file translator, 392 configuration file, ALA format, 588 configuration file, creating new after offline startup, 521 configuration file, mapping modules from, 540 configuration file, new/open/save, 469 configuration file, offline creation of, 503 configuration file, opening, 220 configuration file, opening after offline startup, 521 configuration file, recently-used, 222 configuration file, saving, 206 configuration files, default folders, 522 configuration files, loading/saving, 67 configuration files, new/open/save, 453 configuration files, trigger setup, 201 configuration files, won't open, 374 configuring counters, 166 configuring timers, 165 connect samples analog property, 257 connect samples in chart, 245 connect to logic analysis system, 531 connecting multiple frames, 446 connecting to a LAN, 355 connection attributes, external

oscilloscope, 471

connection rules, 491 connections for disabled modules, 51 connections to device under test, 548 connections, deleting/adding, 346 connectivity, 355 connectorless probing, Soft Touch, 81 consecutive files, storing repetitive run data, 217 contact information, 406 content information, configuration file, 220 control (of logic analyzer), remote, 55 convert old configuration files, 392 convert trigger step to if/then, 190 conveyor belt analogy, 431 copy data to Compare reference buffer, 463 copy to clip board, 454, 469 copying data to reference buffer, 305 copying module/tool/window status to clip board, 542 copying screens to clip board, 355 copying text to clip board, 355 copyright information, 467 correlated source line, showing, 311 Correlation Bus tab, 540 correlation bus, selecting, 312 counter action, 185, 186 counter event, 180, 181, 384 counter event check without increment action. 386 counter in triager sequence, 384 counters, 163 counters, triggering capability, 432 counters, using, 166 counters, using in triggers, 437 creating new markers. 272 CSV file (module) header format, 590 CSV format, 207, 588 CSV format files, offline analysis in Excel, 237 CSV module file format. 210, 589, 596 custom data visualization charts, 490 custom default storage, 179 custom measurement duration, eye finder, 555 customizing toolbars, 474 cut to clip board, 454, 469 cutting trigger sequence steps, 188

#### D

data and setup, loading, 220 data channel, 788 data formats, 588 data import module files, re-reading, 232 data import module setup, 515 data import module, buses/signals, 229, 516 data import module, creating, 227 data import module, file information, 231, 517 data import modules, 49, 227 Data Import toolbar, 472 data in to trigger out, 718, 723 data on unassigned channels, transitional timing, 422 data storage, transitional timing, 422

data valid window, 130, 424 data values in waveform, showing/hiding, 255 data visualization charts, custom, 490 data, buses/signals to export, 526 data, comparing captured to reference, 305 data, copying to reference buffer, 305 data, exporting to module binary (ALB) files. 213 data, exporting to module CSV files, 210 data, finding bus/signal patterns in, 294, 296 data, finding compare differences, 306 data, loading saved, 220 data, print to file, 354 data, printing, 354, 525 data, range to export, 526 data, reference, offset, 306 data, saving, 205 data, viewing saved, 445 date information, configuration file, 220 Decimal number base, 169, 255, 267 default base, 116 default base (bus/signal), 104 default bit order, assigning channels, 110 default bit order, resetting to, 111, 114 default folders. 522 default number base. 499 default setup button, 1680-series logic analyzers, 609 default storage, 163, 179, 439, 496, 788 default storage, action to turn on/off, 188 default storage, burst patterns in, 663 default trigger sequence, 496 defining probes, 548 delay, 788 delay from trigger in waveform display, 242 delay, adjustable, on state sampling clock input, 424 delay, repetitive run, 55, 522 delete Compare window, 463 delete event, 180 delete external scope, 456 Delete Find Event, 302 delete Listing window, 462 delete logic analysis system, 531 delete marker, 460 delete Overview window, 462 delete Source window, 464 delete Waveform window, 462 delete, Overview window, 350 deleting a bus or signal, 106 deleting actions, 185 deleting buses/signals from Listing window, 262 deleting buses/signals from Waveform window, 247 deleting connections, 346 deleting display windows, 346, 353 deleting favorite find patterns, 303 deleting markers. 278 deleting system from use list, 87 deleting tools, 346 deleting trigger sequence steps, 189

demangled symbols, 600 Demo Center, 47, 78 demo data, creating when offline, 522 demo mode, eye finder, 556 Demultiplex state sampling clock mode, 124, 126 depth, acquisition memory, 134, 135, 147, 500, 637, 638, 640, 651, 654, 656, 658, 669, 678, 711, 715, 718, 723, 727, 734, 742, 749, 757, 766, 770, 779 description information, configuration file, 220 description, configuration file, 206 details, module/tool/window, 542 details, trigger, 527 details, viewing system, 90 development (tool) API, 57 device under test, 788 device under test connection, 548 device under test, connecting, 61 device under test, controlling signals in, 83 device under test, loading in the, 376 device under test, probing, 81 device under test, remote control for switches, 549 dialogs, 494 difference foreground/background color. 307 difference pair reference data, 307 differences in compared data, finding, 306 differential probes and single-ended signals. 548 differential signals, eye scan with, 428 differential threshold voltage level, 102, 671 dimensions, 715, 774 directories, source file, 308, 539 directory list, source file, 311 disabling module, 98, 456 disabling modules, 51 disk space, freeing, 369 display brightness, 614 display center rectangle Listing window, 265 display line numbers, 315 display scale, changing the, 240 display window properties, editing, 348 display windows, 476 display windows, adding/deleting, 353 display windows, adding/deleting/duplicating, 346 display windows, lock scrolling, 251, 264 display windows, renaming, 349 display windows, using, 353 displaying symbols, 269 displaying the Overview window, 345 Distribution Sample VbaView window, 467 documenting trigger sequences, 443 don't care, 789 don't store sample action, 188 Dont Care signal pattern value, 169 double-click, 789 drag and drop. 789 drag and drop markers, 274 draw box triggers, 152 draw rectangle in data, 240

Dual Sample state sampling clock mode, 125 dual sample state sampling clock mode, 54, 125, 127 duplicate Compare window, 463 duplicate Listing window, 462 duplicate Source window, 464 duplicate Waveform window, 462 duplicating display windows, 346 duration counts, 184 duration of storage, transitional timing, 422 duration, eye finder measurement, 555 dynamic triggers, 217

#### Ε

E5386A adapter, 648, 670, 772 E5850A time-correlation fixture, 55 E5860A 1 Gbit low-profile LAN card, 617 E5861A multiframe cable, 614, 617 E5865A upgrades for 16910A logic analyzer, 654 E5866A upgrades for 16911A logic analyzer, 654 E5875A upgrades for 16950 logic analyzer, 656 E5876A upgrades for 16801A/16821A logic analyzer, 651, 711 E5877A upgrades for 16802A/16822A logic analyzer, 651, 711 E5878A upgrades for 16803A/16823A logic analyzer, 651, 711 E5879A upgrades for 16804A logic analyzer, 651, 711 E5880A upgrades for 16806A logic analyzer, 651, 711 E5886A upgrades for 16960 logic analyzer. 658 E5887A upgrades for 16962 logic analyzer, 669 early return of borrowed floating licenses, 364, 537 edge, 789 edge (multiple) trigger, 57 edge and pattern trigger function, 562 edge followed by edge trigger function, 563 edge followed by pattern trigger function, 564 edge operator, pattern trigger, 169 edge resources, 384 edge trigger, 156, 414 edge trigger function, 561 edge trigger functions, timing mode, 560 edge, triggering on signal, 158 edges on a bus, triggering on, 157 edges too far apart trigger function, 563 edges, center waveform display about, 240 edges, multiple, 74 edges, state clock, too close, 376 edges, triggering capability, 432 edges, triggering on, 436 Edit Application dialog, 509 Edit menu. 454 edit operation keyboard commands, 631

editing window/tool properties, 348 Either Edge signal edge value, 169 either edge, triggering on, 436 elastomeric probe adapter, 81 ELF/DWARF object file format, 600 ELF/stabs object file format, 600 ELF/Stabs symbol files, 143 else if branches, 436, 571, 572, 584, 585, 586 Else if clauses, burst patterns in, 667 E-mail dialog, 504 e-mail on trigger, 178 e-mail, send on compare differences, 307 e-mail, send on interval marker statistic, 55, 279,280 e-mail, send when marker value found, 274 enable channel order selection, 111 enable module, 456 enabled Clock Ready, 675 enabling modules, 98 end of data. 242 End of Data marker, 351 end of data, go to, 276 end of data, go to in Listing window, 260 end value of symbol, 530 endian, 114 English online help. 467 enter button, 16902A/16903A logic analysis system, 622 Entering, find qualifier, 296 equal to operator, pattern trigger, 157, 169 error dialogs, showing/hiding, 522 error messages, 375 error messages in the status log, 542 errors, 16960/16962 logic analyzer triaaer. 668 evaluation order of events, 184 evaluation order of find events, 302 event. 789 event checks without action. 386 Event Editor dialog, 505 event logging, 522 Event Selector, touch screen, 618 event statements, 165, 166, 167 event statements, reading, 165 event, arm in from, 182 event, counter, 181 event, flag, 182 event, timer, 181 events (advanced trigger), grouping, 55, 184 events and actions, trigger, 163 events in trigger sequence, 496 events, duration or occurrence counts in timing mode. 184 events, inserting or deleting, 180 events, negating, 183 excluding bus/signal transitions, 179 exit, Agilent Logic Analyzer application, 453 Exiting, find gualifier, 296 expand a bus. 248 expand bus into signal waveforms, 245 experienced users, tips for, 59 export bus/signal data to CSV file, 55, 207

export CSV files, 453 Export dialog, 506 export errors, 380 Export file selection dialog, 507 export files, default folders, 522 Export to IE VbaView window, 467 exporting a range of data, 526 exporting data, 207 exporting data from selected buses/signals, 526 exporting data to module binary (ALB) files, 213 exporting data to module CSV files, 210 expressions, boolean, 435 External Application Setup dialog, 508 external arm, wait for, 569, 582 external instrument, trigger in from, 199 external instrument, triggering, 510 external instruments, trigger out to, 198 external oscilloscope data import. 51 External Oscilloscope Setup toolbar, 471 external oscilloscope time correlation, 49, 55 External Scope Web Control VbaView window, 467 external scope, add/delete, 456 external trigger, 182, 193, 456, 789 External Trigger dialog, 510 extra data channels, 110, 112 eve finder. 130. 133 Eye Finder Advanced Options dialog, 555 eye finder feature, 424 eye finder for 1680/1690-series logic analyzers, 53 eye finder info messages, 388, 557 eye finder measurement data, clearing, 130 eye finder measurement, time of, 557 eye finder operation in 16760 logic analyzer, 649 eye finder properties, 557 eve finder selected/suggested sampling positions, 557 eye scan with differential signals, 428 eye scan with threshold and sample position setup, 130, 550 eye scan, complete scan, 555

### F

Falling Edge signal edge value, 169
falling edge, triggering on, 436
fan out/in to tools in Overview window, 491
fast binary data format, 233
fast binary data format files, offline

analysis, 237

fast binary data, importing 167xx, 223
Fast Zoom In option for Waveform

windows, 252
favorite find pattern, 303
favorite packet events, organizing, 177
favorite trigger, 201, 202, 527
feedthrough mode, external trigger, 510

FFT VbaView window, 49 field decode, 334 field patterns (packet), finding, 298 file errors, 379 file format, 237, 588 file format, module binary (ALB), 213, 598 file format, module CSV, 210, 589, 596 file format, netlist, 113 file information in data import module, 231, 517 File menu, 453 file mgr button, 1680-series logic analyzers, 609 file operation keyboard commands, 631 File Out tool (16700-series logic analyzer data), 234 file, print to, 354 file, symbol, 530 files (configuration), opening, 220 files (configuration), recently-used, 222 files (configuration), saving, 206 files (configuration), translating 167xG and 16700-series, 206 files (configuration), won't open, 374 files, source, browsing, 310 files, symbol, 545 fill memory action, 178 fill memory storage qualifiers, 179 filling memory after trigger, 388 Filter tool, 449 filter/colorize tool, 458 filtered data color, Waveform window, 250 find, 454, 458 find a packet trigger function, 580 find anything N times trigger function, state mode. 581 find anything N times trigger function, timing mode, 567 Find Bus/Signal dialog, 244, 261 find button, 1680-series logic analyzers, 609 find data, 469 Find dialog, 511 find events, 302 Find Options dialog, 304 find patterns, favorites, 303 find qualifiers, 296 find symbol name, 530 find, quick, 294 FindEdges macro, 459 finding bus/signal patterns, 294, 296 finding complex bus/signal patterns, 302 finding differences in compared data, 306 fixed unit for time column. Listing window. 268 fixed unit for time column, Protocol Viewer window, 344 flag action, 185, 187 flag action delay, 182 flag actions, 773 flag event, 180, 182 flag latency, 768 flag line used for arming in multiframe systems, 446

flag set/reset to evaluation, 718, 723 flags, 163, 437, 718, 723 flags status, 542 flags, using, 167 FLEXIm License Finder dialog, 534 floating license server communication timeout, 390 floating license servers, 362, 536 floating licenses, 49, 359 flying lead probe type, 548 folder (bus/signal), adding, 118 folders, default, 522 font size, Listing window, 263, 264 font size, Protocol Viewer, 340 font size, Source window, 314 font size, waveform, 251 font size, Waveform window, 249 footers when printing, 354 force prestore, 47, 134 foreground color, marker, 272, 285 format, netlist file, 113 formats, data, 588 Found marker placement, 304 FPGA dynamic probe, 53 FPGA dynamic probe, automatic set up, 51 fragmented hard disk drive, 372 frame, 789 Frame Module Information dialog, 513 frame that module is in. 548 frame, connecting to, 531 frame, slots/cards/modules in, 546 frequency of changes in time interval, 279 front panel operation, 1680-series logic analyzers, 609 front panel operation, 16880-series logic analyzers, 616, 629 front panel operation, 16902A/16903A logic analysis system, 622 full channel timing mode, 120, 637, 638, 640, 643, 645, 651, 654, 656, 659, 669, 678, 711 full screen, 456 full screen button, 16902A/16903A logic analysis system, 622 full screen display, 469 function names, 139 function tests. 786 FUNCTIONS, General-Purpose ASCII symbol file format, 604

# G

general purpose knob, 16800-series logic analyzer, 616, 629
general purpose knob, 1680-series logic analyzer, 609
general purpose knob, 16902A/16903A logic analysis system, 622
general purpose probe, 53
general purpose probing, 81
general state mode, 122, 637, 638, 640, 643, 645, 651, 654, 656, 659, 670, 711

General-Purpose ASCII (GPA) symbol file, 143, 545, 602 General-Purpose ASCII (GPA) symbol file format, 601 generic text only printer, 354 getting started, 59 glitch, 789 glitch (multiple) trigger, 57, 74 glitch drawing, 157, 158 Glitch signal edge value, 169 glitch, triggering on signal, 158 glitch/edge recognizers, 718, 723 glitches on a bus, triggering on, 157 global counter status, 542 global counters, 437, 718, 723 global counters, transitional timing, 422 glossary, 787 go offline, 453 go online, 453 go to action. 433 go to beginning/end/trigger, 454, 469 go to here (in markers overview bar), 272 go to locations in displayed packet data, 320 go to locations in Listing window, 260 go to locations in Waveform window, 242 go to marker. 460, 472 Go To Marker dialog, 276 go to trigger on run, 204, 522 goto actions, 178 GPA (General-Purpose ASCII) symbol file, 143. 545 GPA (General-Purpose ASCII) symbol file format, 601 gray bus and signal icons, 104, 106 greater than duration, 718, 723, 727, 734. 742, 749, 757, 768, 779 greater than operator, pattern trigger, 157, 169 greater than or equal to operator, pattern trigger, 157, 169 grid style/color analog property, 257 group events (advanced trigger), 55, 184 group signals into bus, 248 grouping, numeric, 522

### Η

half channel timing mode, 120, 637, 638, 640, 643, 645, 651, 654, 656, 670, 678, 711 hardware errors, 379 Hardware Update Utility program, 497 hardware upgrades, installing, 147 hardware\_log.txt file, 379 hardware, selecting offline, 503 header (packet), viewing, 332 header format in module CSV and module binary files, 590 headers when printing, 354 height, waveform row, 255 Hello World Sample VbaView window, 467 help, 60 help button, 1680-series logic analyzers, 609

help button, 16902A/16903A logic analysis system, 622 help file errors, 380 Help menu, 467 help operation keyboard commands, 631 help, Japanese, accessing on Windows XP, 397 Hex number base, 169, 255, 267 hibernation, 401 hide marker measurement display bar, 472 hide measurements list. 460 hiding markers, 285 hiding source file line numbers, 315 hiding/showing data values in waveforms, 255 High signal pattern value, 169 high-level source code, viewing, 308 history depth, trigger, 201, 202 horizontal knobs, 1680-series logic analyzer, 609 horizontal knobs. 16902A/16903A logic analysis system, 622 host offline status, 89 hostname, logic analysis system frame, 87, 531 humidity, 715, 718, 723, 734, 742, 749, 757, 769, 773, 774, 779

#### 

I/O channel error, 379 IEEE 1394 interface card/cable, 373, 608 IEEE-695 object file format, 600 If clause comments, displaying/hiding, 190 If clauses, burst patterns in, 664 if/then, show trigger step as, 440 IMB, 449 Import dialog, 514 import errors. 380 import external oscilloscope data, 51 import fast binary output data, 453 import files, default folders, 522 import from module binary (ALB) files, 47 import module files, re-reading, 232 import module setup, 515 import module toolbar, 472 import module, buses/signals, 229, 516 import module, file information, 231, 517 import modules, 49 import netlist, 113 import netlist to define buses/signals, 520 Import Setup dialog, 515 importing 167xx fast binary data, 223 in range operator, pattern trigger, 157, 169 in use status, 89 incompatible remote service, 373 incompatible remote service version status, 89 increment counter action. 186 independent analyzers, 727, 734, 742, 749, 757, 766, 767, 779 independent analyzers per module set, 770 Infiniium oscilloscope time correlation, 55 information messages in the status log. 542 informational dialogs, showing/hiding, 522

informational messages, 388 input only reference data, 307 insert action after, 185 insert action before, 185 insert bus/signal into window, 454 insert event after (AND/OR), 180 insert event before (AND/OR), 180 Insert Find Event After (AND/OR), 302 Insert Find Event Before (AND/OR), 302 inserting buses/signals into Listing window. 262 inserting buses/signals into Waveform window, 247 inserting trigger functions into trigger sequence steps, 169 installation guides, 406 installing a printer, 355 installing on to LAN, 355 Instrument COM Automation Server, 55 interactive self tests. 395 interpreting error messages, 375 intersecting voltage and time markers, 288 interval marker statistics, 55, 279, 280 interval measurement, 475 intrinsic support, 408 inverse assembler, 789 inverse assembler development API, 57 inverse assembler tool, 308 inverse assembler tool. Software Address bus. 312 inverse assembler, locked bus/signals, 104 inverse assembly tools, new, 458 IP address, logic analysis system frame, 87, 531

### J

Japanese help, 58 Japanese help, accessing on Windows XP, 397 Japanese online help, 467

### Κ

keyboard button, 16902A/16903A logic analysis system, 622
keyboard commands, 631
keyboard dialog with touch screen, 618
keyboard, on-screen, 206, 220
keypad, 1680-series logic analyzer, 609
knob, 16800-series logic analyzer, 616, 629
knobs, 1680-series logic analyzer, 609
knobs, 16902A/16903A logic analysis system, 622

### L

label, 449 LAN card, 1 Gbit low-profile, E5860A, 617 LAN, connecting to, 355 lanes (packet), viewing, 334 lanes associated with packet, viewing, 334

language options, Windows XP, 397 language, help, 467 Large System Setup utility program, 224 latched Clock Ready, 675 latency, timer reset, 165 left alignment, bus/signal columns, 267 less than duration, 718, 723, 727, 734, 742, 749, 757, 768, 779 less than operator, pattern trigger, 157, 169 less than or equal to operator, pattern trigger, 157, 169 level, trigger, 449 level, triggering on signal, 158 license activation wizard, 361, 535 license errors, 383 license file, 147 license manager, 49 license not available, 390 license problems, 390 license server communication timeout. 390 license servers, 359 licensed hardware upgrades, installing, 147 Licensed Pattern Generator file, 515 licenses (software), activation, 361, 535 licenses (software), borrow floating, 364, 537 licenses (software), floating license servers, 362, 536 licenses (software), summary, 360, 534 Licensing dialog, 534 licensing host ID. 361, 535 licensing, software, 467 limits in chart, 245 limits, eye finder scan, 556 line number symbols, 308, 312 line number symbols. source correlation bus. 540 line numbers in Source window, 539 line numbers, source file, showing/hiding, 315 listing button, 1680-series logic analyzers, 609 listing button, 16902A/16903A logic analysis system, 622 listing center rectangle, go to source line, 311 Listing menu, 462 listing operation keyboard commands, 631 Listing window, 482 Listing window, analyzing data, 259 Listing window, background color, 263 Listing window, bus/signal column properties, 265 Listing window, bus/signal data color, 266 Listing window, center rectangle, 265 Listing window, column width, 266 Listing window, font size, 264 Listing window, go to locations in, 260 Listing window, inserting/deleting buses/signals, 262 Listing window, lock scrolling, 264 Listing window, marker-relative times, 268 Listing window, new, 466 Listing window, properties, 263 Listing window, Quick Trigger in, 153

Listing window, re-arranging bus/signal columns, 261 Listing window, showing/hiding parts of, 262 Listing window, timing zoom background color, 264 little endian. 114 load, 449 loading in the device under test, 376 loading saved data and setups, 220 loading/saving user-defined symbols, 57 local area network. 355 Local online mode, 85 Local online mode, front panel knobs and buttons, 609, 622 local printer, 355 local session, 373 locate bus/signal patterns, 294 lock chart limits to setup, 245 lock display window scrolling, 55, 249, 263 lock in viewer, marker property, 285 lock scrolling, 251, 264 lock to relative marker, 286 locked bus/signal, 104, 106, 376, 380, 499 lockstep, 328 lockstep window, Protocol Viewer, 340 log. status. 542 logic analysis system details, 513 logic analysis system self tests, 395 logic analysis system, adding, 87 logic analysis system, deleting, 88 logic analysis system, going online, 531 logic analysis systems, refresh list, 89 logic analyzer, 790 logic analyzer basics, 60 logic analyzer cards, combining, 98 logic analyzer memory, 431 logic analyzer notes, 635 logic analyzer pod and channel connections. 548 logic analyzer triggering, understanding, 431 Logic Analyzer Upgrade utility, 497 logic analyzer, setting up, 97 logic analyzer, turning on, 61 logic analyzer, what is, 412 logic analyzer, when should I use, 411 logic analyzers, offline analysis on, 235 long marker name, 272, 282 long measurement duration, eye finder, 555 Low signal pattern value, 169 LTSSM States and Transitions, 336

### Μ

machine, 449 macro, 790 macro (Visual Basic), 473 macro, pattern generator, 470 macro, trigger, 449 macro, VBA, 357, 458 mail applications, 504 mainframe slots per card, 770 manage releases, 369

manually adjusting state mode sampling positions, 133 manually mapping modules, 517 mapping modules, 224, 517 mapping modules from configuration file, 540 margins when printing, 354 marker, 790 marker background color, 272, 285 marker comments, 286 marker display bar, 272, 282 marker for system trigger, 351 marker foreground color, 272, 285 marker knob, 1680-series logic analyzer, 609 marker knob, 16902A/16903A logic analysis system, 622 marker lock in viewer setting, 285 marker measurement display bar, 475 marker measurements, sample interval, 280 marker measurements, time interval, 279 marker pair, center about, 277 marker position, 272 marker properties, comments, 286 marker properties, lock to relative, 286 marker properties, position, 274 marker properties, snap to edge, 274, 277 marker quick measurements, 69 marker tool tip, 272, 282, 286 marker, Found, 304 marker, go to in Waveform window, 242 marker-relative times in Listing window, 267. 268 marker-relative times, Protocol Viewer, 344 markers, 271 markers display bar, 480 markers display bar in Waveform window, 247 markers display bar, reading, 272 markers display in Listing window, 262 Markers menu, 460 markers overview bar. 481 markers overview bar, reading, 272 Markers toolbar, 472 markers, abbreviated name, 272 markers, creating new, 272 markers, deleting, 278 markers, go to, 276 markers, go to in Listing window, 260 markers, hiding/showing, 285 markers, long name, 272 markers, placing in data, 274 markers, placing where data is found, 304 markers, properties, 284 markers, renaming, 282 markers, sending to back, 283 markers, using, 66 markers, value at measurements, 282 master clock, 124, 125, 126, 127 master frame, 446 master frame, front panel knobs and buttons. 622 Master Only state sampling clock mode, 124, 125 master pods, 524, 541

Master/Slave state sampling clock mode, 124, 125, 129 MatLab Analysis VbaView window, 49 MatLab Connectivity and Analysis package, 49 maximized, starting, 522 maximum 128 channels per bus, 376 maximum burst depth, 766 maximum burst events, 766 maximum burst state speed, 766 maximum channels on a single time base and trigger, 727, 734, 742, 749, 757, 766, 767, 770, 776, 779 maximum global counter, 727, 734, 742, 749, 757.779 maximum memory depth, 718, 723, 770, 771 maximum occurrence count value, 715, 718, 723 maximum occurrence counter, 727, 734, 742, 749, 757, 767, 768, 779 maximum pattern width, 727, 734, 742, 749, 757, 767, 768, 773, 779 maximum range width, 727, 734, 742, 749, 757, 767, 768, 779 maximum sample rate, 723, 771 maximum state clock pulse width, 766, 771 maximum state clock speed. 376, 717, 722 maximum state data rate, 770 maximum state data rate on each channel, 727, 734, 742, 749, 757, 765, 779 maximum state sampling speed, 651, 654, 711 maximum state speed, 715, 770 maximum state tag count, 718, 723 maximum time count between states, 715, 718.723 maximum time count between stored states, 727, 734, 742, 749, 757, 766, 771, 779 maximum timing analysis sample rate, 718, 723 maximum timing sample rate, 715 maximum transitions stored, 422 maximum trigger sequence speed, 766, 767, 772 maximum trigger sequence steps, 727, 734, 742, 749, 757, 766, 767, 779 maximum trigger sequencer speed, 718, 723 measure time, 271 measurement data, printing, 525 measurement duration, eye finder, 555 measurement examples, 72, 73 medium measurement duration, eye finder. 555 memory depth, 134, 135, 147, 500, 637, 638, 640, 651, 654, 656, 658, 669, 711, 715, 718, 723, 727, 734, 742, 749, 757, 766, 770.779 memory depth and channel count trade-offs. 420, 648 memory depth in full channel mode, 727, 734, 742, 749, 757, 767, 779

memory depth in half channel mode, 727, 742, 749, 757, 779 memory, logic analyzer, 431 menu (Tools), adding external applications, 508 menu access keyboard commands, 631 menu bar. 790 menu, File, 453 menus, 453 message dialog options, 522 messages, 16960/16962 logic analyzer trigger, 668 messages, borrow licenses, 537 messages, error, 375 messages, return borrowed licenses, 538 MicroBlaze trace core, 47 MicroBlaze version 5, 46 minimum data pulse width, 718, 723, 727, 734, 742, 749, 757, 767, 779 minimum detectable glitch, 158, 715, 718, 723 minimum master-to-master clock, 715, 718, 723 minimum master-to-master clock time, 715, 717, 722 minimum master-to-slave clock, 715, 723 minimum master-to-slave clock time, 727, 742, 749.757.779 minimum PC requirements for offline analysis, 237 minimum setup/hold time, 718, 723 minimum slave-to-master clock time, 727, 742. 749.757.779 minimum slave-to-slave clock, 715, 718, 723 minimum slave-to-slave clock time, 727, 742, 749, 757, 779 minimum state clock pulse width, 715, 718, 723, 727, 734, 742, 749, 757, 779 minimum state data rate on each channel, 765 minimum time between active clock edges, 727, 734, 742, 749, 757, 771, 779 minimum transitions stored, 422 miscellaneous keyboard commands, 631 missing or slow clock, 386 missing pods, 419 mixed button, 16902A/16903A logic analysis system, 622 module, 790 module binary (ALB) file format, 213, 598 module binary and module CSV file header format, 590 Module binary file, 515 module binary file, 507 module CSV file format, 210, 589, 596 Module CSV text file, 515 module CSV text file, 507 module details, 542 module mapping, 224 Module Mapping dialog, 517 module setup information, transferring, 445 module setup, mapping from configuration file, 540 module setups, transferring, 224 Module Skew and System Trigger dialog, 520

Module Summary tab, 548 module upgrade, 467 module, cancel processing, 542 module, disable/enable/rename, 456 module, number of cards in, 503 module, resume canceled processing, 542 module, splitting, 98, 541 module, unsplitting, 100 modules in frame, 546 modules only, loading, 220 modules, configuring, 98 modules, disabling, 51 modules, disabling/enabling, 98 modules, renaming, 349 mouse cursor, placing marker at, 274 mouse shortcuts, 71 moving markers, 274 MSB ordering in bus waveform, 245 multiframe, 446 multiframe cable, 446 multiframe cable, E5861A, 614, 617 multiframe logic analysis system, flags, 167 multiframe remote access passwords, 94 multiframe, front panel knobs and buttons, 622 multi-module systems, transferring setups, 224 multiple conditions, testing in trigger sequence, 436 multiple edge/glitch trigger, 57, 74 multiple frames, 446 multiple-modules, setting up, 224

#### Ν

N consecutive samples with pattern1 trigger function. 575 N number of edges trigger function, 562 name, symbol, 530 naming errors, 382 negating events, 183 negative logic, 117 netlist file format, 113 netlist import, 54 Netlist Import dialog, 520 Netlist Import folder, 113 netlist, importing, 55, 113 network. 355 network printer, 355 network troubleshooting, 402 new Compare window, 466 new configuration file, 453, 469 new file button, 16902A/16903A logic analysis system. 622 new Listing window, 466 new marker, 460, 472 new sample interval measurement, 460, 472 new Source window, 466 new time interval measurement, 460, 472 new toolbar, creating, 474 new value at measurement, 460, 472 new VbaView window, 466 new Waveform window, 466 next data for source line, 309

next difference, 306 next difference in Compare window, 463 next source line, 309 next window, 466, 469 no hardware found, 147 no matching symbol found, 311 node-locked licenses, 359 not equal to operator, pattern trigger, 157, 169 not in range operator, pattern trigger, 157, 169 not in range, triggering on, 437 Not Present for Range, find qualifier, 296 Not Present, find qualifier, 296 notes, 16740/41/42 logic analyzer, 638 notes, 16750/51/52 logic analyzer, 640 notes, 16753/54/55/56 logic analyzer, 643 notes, 16760 logic analyzer, 645 notes, 1680/1690-series logic analyzer, 637 notes, 16800-series logic analyzer, 651, 711 notes, 16910/11 logic analyzer, 654 notes, 16950/51 logic analyzer, 656 notes, 16960 logic analyzer, 658 notes, 16962 logic analyzer, 668, 676 notes, logic analyzer, 635 nothing event, 180 notices, 2 number base, 116, 169, 255, 267 number base, default (bus/signal), 104 number base, packet column, 343 number of accumulations in eye finder measurement. 557 numeric data values, showing/hiding, 255 numeric grouping, 522

### 0

object file formats supported by symbol reader. 600 object file symbols, 139 object file symbols, converting to ASCII, 143 object name, 382 observed value on target control port signals, 549 occurrence, 790 occurrence counter status, 542 occurrence counter, reset action, 185, 186 occurrence counters, 166, 184, 437, 715, 718, 723 Octal number base, 169, 255, 267 offline analysis, 220, 233, 234, 235, 236, 237, 791 offline analysis for 16700-series logic analyzers. 57 offline analysis warnings, 386 offline file formats, 237 offline hardware, selecting, 503 offline mode. 517 offline mode unexpected, 373 offline module setup, 224 Offline Startup Options dialog, 521 offline, creating demo data when, 522 offline. go. 453 offset, 130

offset in Compare window, 463 offset, adding to symbol value, 530 offset, reference data, 306 OMF96 object file format, 600 OMFx86 object file format, 600 online analysis, 85 online help, 467, 469 online, go, 453 online, going after offline startup, 521 on-screen keyboard, 206, 220 on-screen keyboard with touch screen, 618 open configuration file, 453, 469 open file button, 16902A/16903A logic analysis system, 622 open setup button, 1680-series logic analyzers, 609 opening configuration files, 220, 374 opening the Overview window, 345 operating environment, 715 option attributes, external oscilloscope, 471 optional accessories, 1680/90-series logic analyzer, 608 optional accessories, 16800-series logic analyzer, 614 optional accessories, 16900-series logic analysis system. 617 options, 454 options, symbol reader, 143 OR events, 180 or triager, 193 OR'ed find events, 302 order, channel selection, 111 oscilloscope time correlation, 49, 55 oscilloscope, when should I use, 410 other trigger functions, state mode, 573 other trigger functions, timing mode, 560 Outlook Express, setting up, 505 overlaid waveform color, 250 overlaying waveforms, 244 overview, 60 Overview menu, 462 Overview window, 55, 345, 458, 491 Overview window and multiframe systems, 446 Overview window probes column, 53 Overview window, delete, 350 Overview window, open/display, 345, 466, 469 Overview window, redraw, 350 overview, 1680/90-series logic analyzer, 608 overview, 16800-series logic analyzer, 614 overview, 16900-series logic analysis system, 617 overview, Agilent Logic Analyzer application, 631 owner information, configuration file, 220 owner, configuration file, 206

#### Ρ

packet column, width, 342 packet columns, inserting or deleting, 321 packet columns, re-arranging, 321

packet data, analyzing, 316 packet decode column, alignment, 342 packet decode column, channels (directions), 342 packet decode column, number base, 343 packet details, viewing and comparing, 329 packet event editor, 175 packet event, save as favorite, 176 packet event, view as bits, 176 packet events, organizing favorites, 177 packet events, specifying, 175 packet header, viewing, 332 packet information, viewing, 328 packet lanes, 334 packet lanes, viewing, 334 packet patterns, finding, 298 packet payload, viewing, 333 packet summary, 319 packet summary event colors, 337 packet summary, column properties, 340 packet summary, showing/hiding parts of the display, 326 Packet Viewer window, 47 packet, viewing selected, 328 page headers/footers/margins when printing, 354 parentheses in boolean expressions, 184 partial logic analyzer setup, transferring, 445 passwords for remote access, 94 paste from clip board, 454, 469 pattern, 791 pattern absent for greater than time trigger function, 566 pattern absent for less than time trigger function. 567 pattern and pattern trigger function, state mode, 586 pattern and pattern trigger function, timing mode, 572 pattern generator, 52 Pattern Generator Binary file, 515 Pattern Generator CSV text file, 515 pattern generator CSV text file, 507 pattern generator vectors in XML configuration files, 51 pattern N times trigger function, 574 pattern or pattern trigger function, state mode, 587 pattern or pattern trigger function, timing mode, 573 pattern present for greater than time trigger function, 565 pattern present for less than time trigger function, 566 pattern recognizers, 718, 723 pattern resources, 384 pattern too late after edge trigger function, 564 pattern trigger, 157, 169, 414 pattern trigger function, 565 pattern width, 767 pattern1 followed by pattern2 before pattern3 trigger function, 576

pattern1 followed by pattern2 trigger function, 575 pattern1 immediately followed by pattern2 trigger function, 576 pattern2 occurring too late after pattern1 trigger function, 579 pattern2 occurring too soon after pattern1 trigger function, 578 patterns trigger functions, state mode, 573 patterns, finding bus/signal, 294, 296 patterns, finding complex bus/signal, 302 pause timer action, 185 payload (packet), viewing, 333 PC requirements, minimum for offline analysis, 237 PCI Express analysis probe, 53 performance improvements, 54 personal computers, offline analysis on, 236 physical view of cards in system, 546 pin mapping details, 113 place marker on screen, 460, 472 place on edge markers, 277 placing markers in data, 274 placing markers with find, 304 pod, 791 pod and channel connections, 499, 548 pod assignment, 456 Pod Assignment dialog, 524 pod index. 791 pod naming conventions. 418 pod pair, 791 pod pair, reserving for time tag storage, 420 pod truncation, 220, 791 pod usage, 772 pods. missing, 419 point, 791 polarity, 104, 117, 499, 791 polarity, external trigger, 510 position marker property, 274 position, marker, 272 position, trigger, 431 poststore, 134 power management, 401 preprocessor, 81, 791 Present for Range, find qualifier, 296 Present greater than or equal to, find qualifier, 296 Present greater than, find qualifier, 296 Present less than or equal to, find qualifier, 296 Present less than, find qualifier, 296 Present, find qualifier, 296 prestore, 134 previous data for source line, 309 previous difference, 306 previous difference in Compare window, 463 previous source line, 309 previous window, 466, 469 print button, 1680-series logic analyzers, 609 print data. 453, 469 print to file, 354 printer, installing, 355 printers, 715, 774

printing captured data, 354 Printing Data dialog, 525 probe, 792 probe compatibility, 773, 778 probe connection, 772 probe grounding, 376 Probe Summary tab, 548 probes, 727, 734, 742, 749, 757, 765, 779 Probes toolbar, 472 probing, 81 probing documentation, 406 probing options, 81 problems writing CDs on 16900A, 16902A, or 16903A frames, 400 problems, software installation, 372 problems, solving, 371 procedure names, 139 processing, module/tool/window, canceling or resuming, 542 processor-specific probes, 81 product information web sites, 406 product overview, 1680/90-series logic analyzer, 608 product overview, 16800-series logic analyzer, 614 product overview, 16900-series logic analysis system, 617 product overview, Agilent Logic Analyzer application, 631 product overviews. 608 programming the logic analyzer, 55 project information, configuration file, 220 project, configuration file, 206 Properties dialog, 526 properties. Compare window, 463 properties, editing window/tool, 348 properties, eye finder, 557 properties, Listing window, 263, 462 properties, marker, 284, 460, 472 properties, Source window, 313, 464, 538 properties, voltage marker, 292 properties, Waveform window, 249, 462 properties, window, 454 protocol. 792 protocol column channels (directions), 322 Protocol Viewer, 487 Protocol Viewer menu, 464 Protocol Viewer panes, showing/hiding, 337 Protocol Viewer, window properties, 338 pulse clear flag action, 167, 187 pulse set flag action, 167, 187 pulse target control port signals, 549 pulse width in waveform tool tip. 253 pulse width, flag pulse set/clear, 187 pulsed mode, external trigger, 510

### 0

QFP package probing, qualifier, state sampling clock, quarter channel timing mode, quick find, quick pick bus/signal names, 55 quick start for 16700-series users, 59 quick start guides, 406 quick trigger, 792 Quick Trigger alignment, setting, 315 Quick Trigger in Listing window, 153 Quick Trigger in Source window, 154 Quick Trigger in Waveform window, 152 quick triggers, 149, 152

#### R

rack mount kit. 608 range and offset in Compare window, 463 range of data to export, 207 range of samples, comparing, 306 range operator, pattern trigger, 75, 157, 169 range pattern, 792 Range Properties dialog, 526 range recognizers, 718, 723 range width, 715, 718, 723, 767 ranges, triggering capability, 432 ranges, triggering on, 437 RDP (Remote Desktop Protocol), 405 reader, symbol, 143 readers.ini file, 143 reading markers display and overview bars. 272 readme information, 371 re-arranging bus/signal columns, 261 re-arranging waveforms, 243 re-assign pods to split analyzers, 524 recalibrate touch screen, 618 recall recently-used configuration file, 222 recall trigger, 68, 201, 202, 456 Recall Trigger dialog, 527 recalling favorite find patterns, 303 recalling triggers, 496 recent configuration files, 453 recent file list entries, 522 recently used bus/signal names, 169 recently-used configuration file, recalling, 222 recently-used trigger, 201, 202, 527 redraw, Overview window, 350, 462 reference, 451 reference buffer, copy data to, 305, 463 reference buffer, range compare, 306 reference data background color, 307 reference data offset, 306 reference data, comparing to, 305 reference data, display options, 307 refresh logic analysis system, 531 refreshing system to use list, 89 regional and language options, Windows XP. 397 re-group events (advanced trigger), 55, 184 relative marker, lock to, 286 relative time, 267 remote (logic analyzer) programming, 55 remote access, 54 remote access passwords. 94 remote control for switches in DUT, 549

Remote Desktop Protocol (RDP), 405 Remote Desktop, setting up, 405 Remote online mode, 85 remote programming (RPI) commands, 49 remote session, 373 remove bus/signal from window, 454 remove icons to toolbar, 474 remove software, 368 rename bits of a bus, 108 rename Compare window, 463 rename Listing window, 462 rename module, 456 rename Source window, 464 rename trigger, 527 rename Waveform window, 462 renaming a bus or signal, 107 renaming markers, 282 renaming windows/tools/modules, 349 reorder bits, 55, 114 reordering symbols, 139 repetitive measurement, 792 repetitive run, 203, 461, 473 repetitive run delay, 55, 522 repetitive run, go to trigger behavior, 203 repetitive run, stop on compare differences. 307 repetitive run, stop on interval marker statistic, 55, 279, 280 repetitive run, stop when marker value found, 274 repetitive run, storing data to consecutive files, 217 repetitively run eye finder, 556 RepetitiveSaveToFile macro, 459 replacement failed, 384 replacing trigger functions in trigger sequence steps, 169 reporting level, self tests, 395 requirements, minimum PC for offline analysis, 237 re-reading data import module files, 232 reset and start timer trigger function, 580 reset counter action, 186 reset occurrence counter action, 166, 185, 186, 384 reset toolbar, 474 restrictions, 16962 logic analyzer state sampling clock, 675 resume, 461 resume canceled operation, 473 resume canceled processing, module/tool/window, 542 resume timer action. 185 return borrowed floating licenses early, 364, 537 return borrowed licenses messages, 538 reverse channel order, 114 right alignment, bus/signal columns, 267 right mouse button behavior with touch screen, 618 right-click, 792 Rising Edge signal edge value, 169

rising edge, triggering on, 436 row height, 255 row properties, analog signal, 256 row properties, bus/signal waveform, 253 **RPI** (Remote Programming Interface) compatibility package, 49 rules, Overview window connection, 491 run. 792 run buttons, 16800-series logic analyzers, 616, 629 run buttons, 1680-series logic analyzers, 609 run buttons, 16902A/16903A logic analysis system, 622 run eye finder, 130 run mode, eye finder, 556 Run Properties dialog, 529 run repetitive, 792 run status, 203, 542 Run toolbar, 473 run until a number of compare differences. 307 run until user stop trigger function, state mode, 581 run until user stop trigger function, timing mode, 569 run, go to trigger on, 204, 522 run, repetitive, storing data to consecutive files, 217 Run/Stop menu, 461 run/stop operation keyboard commands, 631 running self tests repetitively, 395 running the analyzer, 203

# S

sample, 793 sample interval measurement, 280, 475 sample interval measurement, new, 460, 472 sample period, 715, 727, 734, 742, 749, 757, 767, 771, 779, 793 sample period accuracy, 715, 718 sample period, timing zoom, 138 sample position setup, auto, 130, 550 sample position warnings, eye finder, 556 sample rate in half channel mode, 727, 742, 749, 757, 779 sample rate on all channels, 727, 734, 742, 749, 757, 767, 779 sample rates, 718, 723 sample, go to in Listing window, 260 sample, go to in Waveform window, 242 sample, position marker by, 272, 274 sampled data. 793 samples, comparing range of, 306 samples, how they are stored in memory, 431 samples, storage gualification, 439 sampling, 793 sampling mode, state, 122 sampling options, 120 sampling options, memory depth and channel count trade-offs, 420, 648 sampling options, state, 122 sampling period, 119, 121, 413

sampling period, timing zoom, 558 sampling period, transitional timing mode, 420, 648 sampling position, logic analyzer, 550 sampling positions (state mode), automatically adjusting, 130 sampling positions (state mode), manually adjusting, 133 sampling positions, automatic adjustment for 1680/1690-series logic analyzers, 53 sampling positions, selected/suggested, 557 sampling positions, state mode, understanding, 424 sampling setup, 456, 471, 500 Sampling tab, 500 save configuration file, 453, 469 save file button, 16902A/16903A logic analysis system, 622 save setup button, 1680-series logic analyzers. 609 saved data and setups, loading, 220 saving captured data, 205 saving configuration files, 206 saving trigger sequences, 443 saving trigger setups, 68 saving/loading user-defined symbols. 57 scale of waveform display, 277 scaling analog property, 257 scan limits, eye finder, 556 scope button, 16902A/16903A logic analysis system, 622 screen, copy to clip board, 454 screens, copying to clip board, 355 scroll lock on display windows, 55, 249, 263 search, 793 search for symbol name, 530 search operation keyboard commands, 631 search order of source file directories, 539 search, quick, 294 searching data, 70 searching for bus/signal patterns, 294 searching for text in Source window, 310 SECTIONS, General-Purpose ASCII symbol file format, 603 Select Offline Hardware dialog, 503 Select Symbol dialog, 530 Select System to Use dialog, 531 selected bit order, assigning channels, 111 selected packet box color, 339 selected sampling position, 557 selected source line, go to data for, 309 self test, 395, 467 send e-mail on trigger, 178 sending markers to the back, 283 SendToExcel macro, 459 SendToExcel VBA macro, 49 SendToMatLab VBA macro. 49 SendToPatternGeneratorModule macro. 459 SendToPatternGeneratorModule VBA macro, 49 separator rows in Waveform window, 47, 248 sequence step branching, 718, 723

sequence step branching, transitional timing, 422 sequence step storage, 179, 439 sequence steps, trigger, 384, 433, 435, 436 sequencer speed, 715 Serial To Parallel tool, 51 sessions, saving and loading, 445 set flag action, 167, 187 Set Quick Trigger alignment, 315 setup button, 1680-series logic analyzers, 609 setup button, 16902A/16903A logic analysis system, 622 Setup menu, 456 setup only, loading, 220 setup/hold time, 715, 717, 722 setup/hold time, logic analyzer, 376 setup/hold window, logic analyzer, 130, 424, 550 setups, loading saved, 220 short bus/signal names. 522 short measurement duration, eye finder, 555 shortcut buttons, 1680-series logic analyzers, 609 shortcut buttons, 16902A/16903A logic analysis system, 622 show axis in chart. 245 show clipped analog property, 257 show correlated source line, 311 show marker measurement display bar, 472 show measurements list. 460 show trigger step as if/then, 189, 440 show values in waveform tool tip, 253 showing markers, 285 showing source file line numbers, 315 showing/hiding data values in waveforms, 255 signal activity envelope, 130, 424, 550 Signal Extractor tool, 47 signal names, 104 signal, grouping into a bus, 248 signal/bus column alignment, 267 signal/bus column properties, 265 signal/bus column width in Listing window, 266 signal/bus data color, Listing window, 266 signal/bus errors, 376 signal/bus folders, adding, 118 signal/bus name, alias, 118 signal/bus names, sorting, 118 signal/bus naming, short or unique, 522 signal/bus patterns, finding, 294, 296 signal/bus patterns, finding complex, 302 signal/bus row properties, 253 signal/bus values displayed as symbols, 269 signal/bus, adding a new, 105 signal/bus, assigning channels in default bit order, 110 signal/bus, assigning channels in selected bit order, 111 signal/bus, deleting a, 106 signal/bus, renaming a, 107 signals/buses, define by importing netlist, 520

signals/buses, exporting data from selected, 526 signals/buses, inserting/deleting in Listing window, 262 signals/buses, inserting/deleting in Waveform window, 247 signals/buses, load warning, 386 Signed Decimal number base, 169, 255, 267 simple compare, 57 simple trigger, 149, 156, 456, 793 simple trigger example, 416 simple trigger in Listing window, 262 simple trigger in Waveform window, 247 simple trigger, setting up, 64 single measurement, 793 single run, 203 single-ended signals and differential probes, 548 skew, 793 skew and system trigger, 456 skew and system trigger, setting, 351 skew between modules, 54 skew, module, 520 slave clock, 124, 125, 126, 129 slave frame, 446 slew rates. 130 slot, 793 slot naming, 418 Slot Summary tab, 546 slot. starting, 503 slots of cards in module, 548 slow or missing clock, 386 snap to edge markers, 274, 277, 793 Soft Touch connectorless probing, 81 Software Address bus. 312, 540 software installation problems, 372 software licenses, 49 software licenses, activation, 361, 535 software licenses, borrow floating, 364, 537 software licenses, floating license servers, 362, 536 software licenses, summary, 360, 534 software licensing, 467 software, updating, 367 solving problems, 371 sorting bus/signal names, 118 source code correlation bus, selecting, 312 Source Code Directories tab, 539 source code directory list, 311 source code, viewing, 308 source correlation, 540 Source Correlation Toolset, 449 Source display window, 486 source file line numbers, 139 source files, browsing, 310 source line numbers, showing/hiding, 315 source line symbol values, adjusting, 315 source line, go to data for, 309 source line, showing correlated, 311 SOURCE LINES, General-Purpose ASCII symbol file format, 606 source lines, step by, 309

Source menu, 464 source of data export, 207 Source Properties tab, 539 Source Viewer Properties dialog, 538 Source window, 54 Source window background color, 314 Source window font size, 314 Source window properties, 313 Source window tab width, 315 Source window text color, 314 Source window, new, 466 Source window, Quick Trigger in, 154 Source window, text search, 310 specifications, 714, 785 specifications, 16740/41/42 logic analyzer, 717 specifications, 16750/51/52 logic analyzer, 722 specifications, 16753/54/55/56 logic analyzer, 727 specifications, 16760 logic analyzer, 734 specifications, 1680/1690-series logic analyzer, 715 specifications, 16800-series logic analyzer, 742, 779 specifications, 16910/11 logic analyzer, 749 specifications, 16950/51 logic analyzer, 757 specifications, 16960 logic analyzer, 764 specifications, 16962 logic analyzer, 769 Specify Mapping dialog, 540 split analyzer, 98, 456, 541 Split Analyzer Setup dialog, 541 split logic analyzer modules, 54 spreadsheet, importing CSV files, 205, 207, 453 spreadsheet, pasting into from clip board, 355 stable region, 130 stack of channels, eye finder data, 130 standard CSV text file, 507 standard threshold voltage level, 102, 671 Standard toolbar, 469 START ADDRESS, General-Purpose ASCII symbol file format, 606 start from reset timer action. 185 start maximized, 522 start value of symbol, 530 startup options, offline, 521 state acquisition mode, 500 state analyzer, 412, 793 state analyzer, triggering, 416 state clock edges too close, 376 state clock pulse width, 766, 771 state clock/qualifiers, 715, 718, 723 state clocks, 718, 723 state measurement, 794 state mode, 73, 119, 149, 415, 573, 794 state mode sampling positions, automatically adjusting, 130 state mode sampling positions, manually adjusting, 133 state mode sampling positions, understanding, 424

state mode, default storage, 179 state mode, selecting, 122 state sampling clock, 128 state sampling clock mode, Demultiplex, 124, 126 state sampling clock mode, Dual Sample, 125 state sampling clock mode, Master Only, 124, 125 state sampling clock mode, Master/Slave, 124, 125 state sampling clock mode, selecting, 123 state sampling clock, 16962 logic analyzer, 674 state sampling mode, 122 state sampling mode, memory depth and channel count trade-offs, 420, 648 state sampling options, 122 state sampling setup, 471 state sequence steps, 718, 723 state speed, 147 statistics, interval marker, 55, 279, 280 status bar, 456 Status dialog, 54, 542 status, system, 461 step to next/previous source lines, 309 steps in trigger sequence, cutting, 188 steps in trigger sequence, deleting, 189 steps, trigger sequence, 163, 384, 433 stop, 794 stop and reset timer action, 185 stop behavior, 1696016962 logic analyzers, 676 stop button, 16800-series logic analyzers, 616, 629 stop button, 1680-series logic analyzers, 609 stop button, 16902A/16903A logic analysis system, 622 stop measurement, 461, 473 stopping self tests on fail, 395 stopping the analyzer, 203 storage control action, 163, 179, 185, 188, 496 storage qualification, 179, 439, 794 storage qualification, triggering capability, 432 storage qualifier when filling memory, 178 store action, 384, 439 store qualification, 718, 723, 727, 734, 742, 749, 757, 767, 779 store qualification actions, 772 store qualified (transitional) timing mode, 120, 637, 638, 640, 643, 645, 651, 654, 656, 659, 670, 679, 711 store qualified (transitional) timing mode, default storage, 179 store sample action, 188 store trigger, 201, 456 storing favorite find patterns, 303 storing triggers, 496 strategies for setting up triggers, 440 stylus, using on touch screen, 618 subdirectories, searching for source files, 539 suggested sampling position, 557 summary of triggering capabilities, 432

summary, module, 548 summary, system, 546 supplied accessories, 1680/90-series logic analyzer, 608 supplied accessories, 16800-series logic analyzer, 614 supplied accessories, 16900-series logic analysis system, 617 support, intrinsic, 408 supported signal types, 773, 778 switch endian. 114 symbol decode, 334 symbol file, ASCII format, 601 symbol file, creating ASCII, 143 symbol information, XML format, 445 symbol lookup, 139 Symbol number base, 169, 255, 267 symbol reader options, changing, 143 symbol reader, object file formats supported, 600 symbol reader, running outside the application, 142 symbol search, 530 symbol selection, 530 symbolic bus/signal values, 146 symbols, 139, 454, 456, 530, 794 symbols (user-defined), saving/loading, 57 Symbols dialog, 545 symbols from object file, 54 symbols with same name, 139 symbols, displaying for bus/signal values, 269 symbols, line number, 308, 312 symbols, loading from file, 141 symbols, user-defined, 139 synchronous sampling, 122, 500, 794 system clock failure, 379 system details, 513 system details, viewing, 90 system in use comments, 89, 91, 531 system options, 522 system summary, 462 System Summary dialog, 54, 546 system to use list, adding frame, 87 system to use list, deleting frame, 88 system trigger, 54, 520 system trigger and skew, 456 system trigger and skew, setting, 351

### Т

tab width in Source window, 315, 539 tabbed windows, 239, 259, 353, 456 target connector probing, 81 target control port, 83, 456 Target Control Port dialog, 549 target system, 794 temperature, 715, 718, 723, 727, 734, 742, 749, 757, 769, 773, 774, 779 terminating slave frame, 446 terminology, 16700, 449 testing the logic analyzer, 395 text color, Source window, 314

text data, copying to clip board, 355 text file, print to, 354 text search in Source window, 310 third party tools, 458 tHold, 727, 734, 742, 749, 757, 765, 779 threshold (bus/signal), 104 threshold accuracy, 715, 717, 722, 773, 778 threshold and sample position setup, auto, 130, 550 threshold level, trigger in/out, 510 Threshold Settings dialog, 102, 671 threshold value, 376 threshold voltage, 102, 499, 671, 794 threshold voltages (state mode), automatically adjusting, 130 Thresholds and Sample Positions dialog, 550 TI COFF object file format, 600 Ticoff symbol files, 143 tile windows horizontally, 466, 469 tile windows vertically, 466, 469 time axis in Waveform window, 247 time correlation fixture, 49, 55 time duration in find qualifiers, 296 time interval accuracy, 715, 727, 734, 742, 749, 757, 767, 779 time interval measurement, 279, 460, 472, 475 time measured, transitional timing, 422 time of eye finder measurement, 557 time tag resolution, 715, 718, 723, 727, 734, 742.749.757.766.771.779 time tag storage, memory requirements, 420, 648 time tag storage, reserve pod pair for, 524 time tag storage, transitional timing, 422 time trigger occurred, 548 time, absolute, 267 time, go to in Listing window, 260 time, go to in Waveform window, 242 time, marker-relative, 268 time, position marker by, 272, 274 time, relative marker, 267 time, relative previous, 267 time/division, 240, 795 timeout, floating license server communication, 390 timer, 795 timer accuracy, 715, 718, 723, 727, 734, 742, 749.757.768.779 timer action, 185 timer actions, 773 timer event, 180, 181 timer event check without start action, 386 timer in trigger sequence, 384 timer reset latency, 165, 718, 723, 727, 734, 742, 749, 757, 768, 779 timer resolution, 715, 718, 723, 727, 734, 742, 749, 757, 768, 779 timer status, 542 timer value range, 715, 718, 723, 727, 734, 742, 749, 757, 768, 779 timers, 163, 438, 715, 718, 723 timers, number available, 420, 648

timers, triggering capability, 432 timers, using, 165 timing acquisition mode, 500 timing analysis sample rate, 727, 734, 742, 749, 757, 779 timing analyzer, 412, 795 timing analyzer, triggering, 414 Timing Compare VbaView window, 49, 467 timing interval accuracy, 718, 723, 727, 734, 742, 749, 757, 779 timing measurement, 795 timing mode, 72, 119, 149, 413, 795 timing mode sampling period, 121 timing mode trigger functions, 560 timing mode, duration or occurrence counts for events, 184 timing mode, selecting, 120 timing sampling mode, 120 timing sampling options, 120 timing sequence steps, 723 timing zoom, 136, 638, 640, 643, 645, 651, 654, 656, 711 timing zoom background color, Listing window, 264 timing zoom background color, Waveform window, 251 timing zoom sample period, 138 timing zoom trigger position, 138 timing zoom, aligning with trigger in split analvzer. 138 timing zoom, turning on or off, 138 timing/state sampling setup, 471 timing/state setup, 456 TimingZoom Setup dialog, 558 tips for experienced users. 59 toggle target control port signals, 549 too few states between pattern1 and pattern2 trigger function, 577 too many states between pattern1 and pattern2 trigger function, 578 tool details, 542 tool development API, 57 tool errors, 383 tool name, 382 tool properties, editing, 348 tool tip, 795 tool tip display, Waveform window, 253 tool tip, marker, 272, 282, 286 tool tips, 71, 117 tool tips, Waveform window, 249 tool, cancel processing, 542 tool, resume canceled processing, 542 toolbars, 456, 469 toolbars and mouse shortcuts, 71 toolbars, customizing, 474 Tools menu, 458 Tools menu, adding external applications, 508 tools, adding/deleting, 346 tools, help on, 467 tools, renaming, 349 tools/viewers, loading, 220 topics, help, 467

touch screen tips, 618 trace, 795 trace memory, 203 trademarks, 2 transferring setups to/from multi-module systems, 224 transition width in waveform tool tip, 253 transitional default storage, 179 transitional timing, 120, 422, 795 transitional timing mode, counters in, 166 transitional timing sampling mode, memory depth and channel count trade-offs, 420, 648 transitional timing, 16962, 772 Transitioning, find qualifier, 296 translating 167xG and 16700-series configuration files, 392 translator errors, 380 trigger, 156, 163, 201, 795 trigger actions, 178, 433, 727, 734, 742, 749, 757, 766, 768, 772, 779 trigger analyzer from another instrument, 199 trigger and fill memory action, 178 trigger and goto action, 178 trigger attributes, external oscilloscope, 471 trigger button, 1680-series logic analyzers, 609 trigger button, 16902A/16903A logic analysis system, 622 trigger errors, 384 trigger errors, 16960/16962 logic analyzer, 668 trigger function, 496, 795 trigger functions, 163, 560 trigger functions, converting to if/then, 190 trigger functions, replacing or inserting, 169 trigger functions, state mode, 573 trigger functions, timing mode, 560 trigger functions, understanding triggering, 440 trigger history, 796 trigger history depth, 201, 202, 522 trigger in, 193, 510 trigger in arms logic analyzer, 715 trigger in from external instrument, 199 Trigger In/Out and multiframe systems, 446 trigger inhibited during prestore, 388 trigger level, 449 trigger macro, 449 trigger other instruments, 198 trigger out, 193, 510 trigger out to external instruments, 198 trigger overview, 47 trigger point, 242, 431 trigger position, 134, 431, 500, 718, 727, 734, 742, 749, 757, 766, 767, 773, 779, 796 trigger position, timing zoom, 138, 558 trigger position, transitional timing, 422 trigger reference point skew, 520 trigger resource combinations, 772 trigger resource conditions. 727, 734, 742. 749, 757, 766, 768, 779 trigger resources, 715, 727, 734, 742, 749, 757, 766, 768, 772, 773, 778, 779

trigger sequence, 496, 796 trigger sequence in U4154A, 688 trigger sequence step branching, 727, 734, 742, 749, 757, 766, 767, 773, 779 trigger sequence step, show as if/then, 189 trigger sequence steps, 163, 384, 433, 715 trigger sequence steps, cutting, 188 trigger sequence steps, deleting, 189 trigger sequence steps, replacing or inserting trigger functions, 169 trigger sequence, clearing, 192 trigger sequences, save and document, 443 trigger setup file, 201, 202 trigger setups, saving/recalling, 68 trigger specification file, 527 trigger specification too complex, 384 trigger step status, 542 trigger to trigger out, 715 trigger, go to, 276 trigger, go to in Listing window, 260 trigger, go to on run, 204, 522 trigger, multiple edge/glitch, 57 trigger, recalling, 202, 527 trigger, send e-mail, and fill memory action, 178 triager, system, 520 trigger, system, setting, 351 trigger, time trigger occurred, 548 triggering, 156, 163, 201 triggering after external data analysis. 217 triggering capabilities, summary of, 432 triggering the state analyzer, 416 triggering the timing analyzer, 414 triggering, understanding logic analyzer, 431 triggers, advanced, in 16960/16962 logic analyzers, 660 triggers, dynamic, 217 triggers, quick, 152 triggers, recalling, 201 triggers, storing, 201 triggers, strategies for setting up, 440 troubleshooting, 371 tSample accuracy, manual adjustment, 727, 734, 742, 749, 757, 779 tSample adjustment resolution, 727, 734, 742, 749, 757, 765, 779 tSample range, 727, 734, 742, 749, 757, 765, 779 tSetup, 727, 734, 742, 749, 757, 765, 779 turbo state mode, 122, 640, 643, 645, 651, 654, 656, 711 turbo state mode, flag actions, 167 turn off/on default storage action, 188 tutorial, 60 tutorial configuration file, 65 tWidth, 727, 734, 742, 749, 757, 765, 779 two's complement, 255, 267 two's complement, 169 type, symbol, 530 types, probe, 548 TZ (timing zoom), 136

## U

U4154A. 626 U4154A Characteristics. 775 U4154A clock channels, 681 U4154A data channels, 680 U4154A eyescans, 690 U4154A logic analyzer notes, 676 U4154A pod, 680 U4154A Specifications, 775 U4154A state clock gualifiers, 687 U4154A state sampling clock, 687 unassigned channels, data on, transitional timing, 422 understanding logic analyzer triggering, 431 undo, 454, 469 undo trigger sequence step shown as if/then, 189 unique bus/signal names, 522 unsplit analyzer, 100, 456 update software, 367 upgrade, module, 467, 497 upgrades, E5865A, for 16910A logic analyzer, 654 upgrades, E5866A, for 16911A logic analyzer, 654 upgrades, E5875A, for 16950 logic analyzer, 656 upgrades, E5876A, for 16801A/16821A logic analyzer, 651, 711 upgrades, E5877A, for 16802A/16822A logic analyzer. 651, 711 upgrades, E5878A, for 16803A/16823A logic analyzer, 651, 711 upgrades, E5879A, for 16804A logic analyzer, 651, 711 upgrades, E5880A, for 16806A logic analyzer, 651, 711 upgrades, E5886A, for 16960 logic analyzer, 658 upgrades, E5887A, for 16962 logic analyzer, 669 upgrades, licensed hardware, 147 user interface, 609, 616, 622, 629, 715, 774 user threshold value, 376 USER, General-Purpose ASCII symbol file format, 604 user-defined symbols, 139, 545 user-defined symbols, saving/loading, 57 user-defined threshold voltage level, 102, 671

### V

value at marker measurement, 282, 460, 472, 475 value at measurement, 796 value, position marker by, 272, 274 value, symbol, 530 variable names, 139 variable size, 600 VARIABLES, General-Purpose ASCII symbol file format, 605

VBA (Visual Basic for Applications), 52 VBA macros in XML configuration files, 51 VBA, extending capture capabilities, 217 VbaView menu, 465 VbaView window, 490 VbaView windows in XML configuration files, 51 version information, 467 version information, configuration file, 220 vertical knobs, 1680-series logic analyzer, 609 vertical knobs, 16902A/16903A logic analysis system, 622 vibration, 718, 723, 727, 734, 749, 757, 769, 773.779 View As dialog, 245 View menu, 456 view operation keyboard commands, 631 view packet event as bits, 176 viewers/tools, loading, 220 viewing bus data as chart. 245 viewing captured data, 219 viewing tabbed windows, 353 virtual analyzer, 503 Visual Basic Editor, 473 Visual Basic for Applications (VBA), 52 Visual Basic toolbar, 473 visualization, data, custom charts, 490 voltage interval measurements, 290 voltage marker properties, changing, 292 voltage markers for analog signals, 286 voltage markers, creating new, 287 voltage markers, deleting, 289 voltage markers, placing, 288 voltage markers, renaming, 291 voltage markers, sending to back, 291 Voltage number base for analog signal in Listing, 267 voltage threshold, 773, 778

### W

wait for arm from another module, 193 wait for arm from another module trigger function, state mode, 582 wait for arm from another module trigger function, timing mode, 570 wait for external arm, 199 wait for external arm trigger function, state mode, 582 wait for external arm trigger function, timing mode. 569 wait N external clock states trigger function, 583 wait T seconds trigger function, 568 waiting in trigger step, 388 warning dialogs, showing/hiding, 522 warning messages, 386 warning messages in the status log, 542 waveform button, 1680-series logic analyzers, 609 waveform button, 16902A/16903A logic analysis system, 622

waveform color, 254 waveform display scale, changing, 240 waveform display, changing the delay, 242 waveform font size, 251 waveform height, 255 Waveform menu, 462 waveform numeric data values, showing/hiding, 255 waveform operation keyboard commands, 631 waveform tool tip display, 253 Waveform window, 476 Waveform window background color, 250 Waveform window, analyzing data, 239 Waveform window, bus/signal row properties, 253 Waveform window, filtered data color, 250 Waveform window, finding a bus/signal row, 244 Waveform window, go to locations in, 242 Waveform window, group signals into bus, 248 Waveform window, inserting/deleting buses/signals, 247 Waveform window, lock scrolling, 251 Waveform window, new, 466 Waveform window, overlaid waveform color. 250 Waveform window, properties, 249 Waveform window, Quick Trigger in, 152 Waveform window, showing/hiding parts of. 247 Waveform window, timing zoom background color, 251 Waveform window, viewing bus data as chart, 245 Waveform windows. Fast Zoom In option, 252 waveforms, accumulate, 252 waveforms, overlaying, 244 waveforms, re-arranging, 243 web control, external oscilloscope, 51 web sites, 406 weight, 715, 774 what's new, 19 what's new, version 01.10, 58 what's new, version 01.20, 57 what's new, version 01.40, 55 what's new, version 02.00, 54 what's new, version 02.50, 53 what's new, version 03.00, 52 what's new, version 03.20, 51 what's new, version 03.30, 49 what's new, version 03.50, 47 what's new, version 03.55, 46 what's new, version 03.60, 45 what's new, version 03.65, 44 what's new, version 03.67, 43 what's new, version 03.70, 41 what's new, version 03.80, 40 what's new, version 03.82, 39 what's new, version 03.83, 37 why are pods missing?, 419 width (bus/signal), 104 width of buses/signals, 499

width violation on pattern or pulse trigger function, 568 width, packet decode column, 342 width, tabs in Source window, 315 window details, 542 window menu, 466 window operation keyboard commands, 631 window properties, 454 window properties, editing, 348 window tabs, turning on/off, 353 window, cancel processing, 542 window, Overview, 55, 345, 491 window, resume canceled processing, 542 windows, 476 Windows XP support, 408 windows, adding/deleting, 353 windows, adding/deleting/duplicating, 346 windows, display, using, 353 windows, help on, 467 windows, renaming, 349 workspace, 449 writing CDs on 16900-series frames, 400 writing to target control port signals, 549

# X

XML format configuration file, 206, 220, 224
XML format configuration files, automatic module mapping, 518
XML format configuration files, pattern generator vectors, 51
XML format configuration files, VBA macros, 51
XML format configuration files, VbaView windows, 51
XML format configurations, setting up multiple-modules with, 224
XML format files, offline analysis, 237
XML tag errors, 380
XML vs. ALA format, when to use, 445

# Ζ

zoom in on data, 67, 240 zoom out/in, 456, 469 zooming, 796 zooming fast in Waveform windows, 252