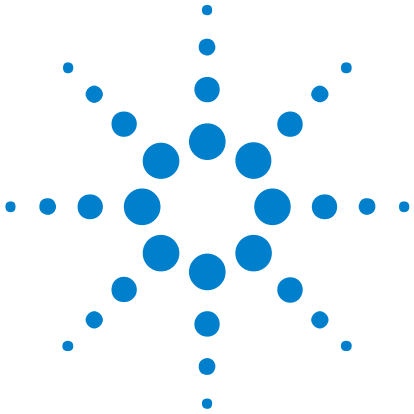

DDR Setup Assistant

Online Help

Agilent Technologies

Notices

Sales and Technical Support

To contact Agilent for sales and technical support, refer to the "support" links on the following Agilent web resources:

www.agilent.com/find/(product-specific information and support, software and documentation updates)

www.agilent.com/find/assist (worldwide contact information for repair and service)

Information on preventing damage to your Agilent equipment can be found at www.agilent.com/find/tips.

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1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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CAUTION

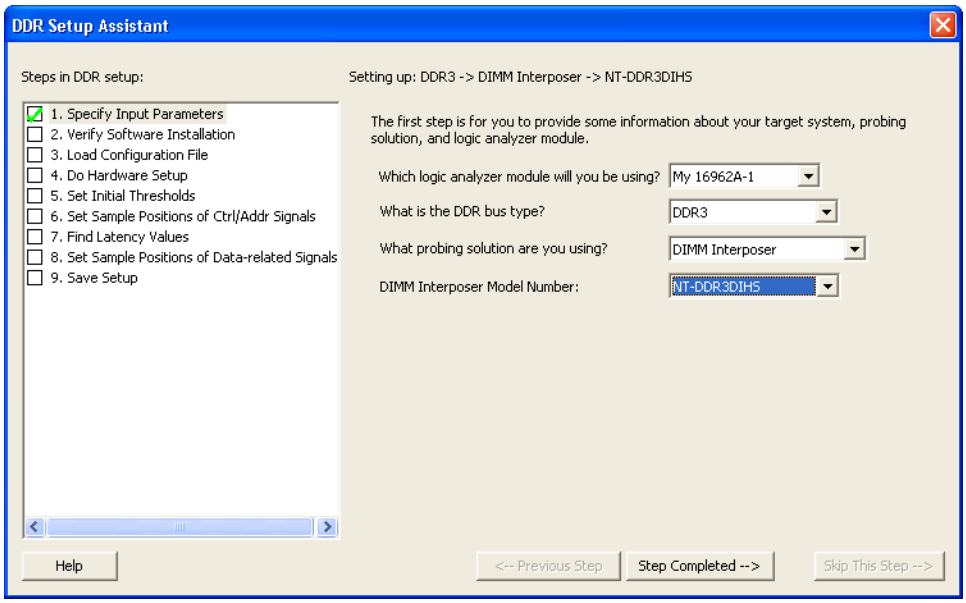
A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

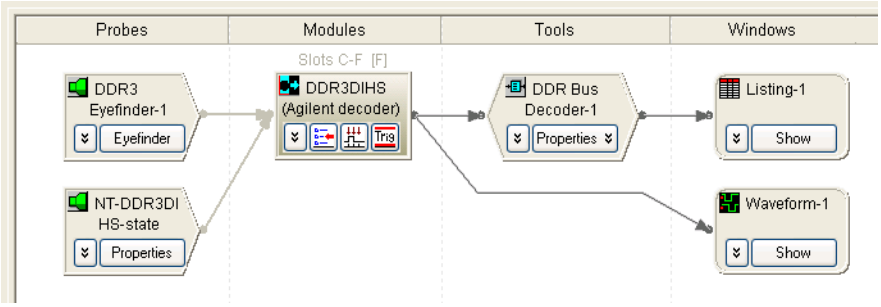
A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

DDR Setup Assistant—At a Glance

The DDR Setup Assistant is a wizard-like application that helps you set up your logic analyzer properly for DDR/LPDDR data capture and analysis.



Once you have completed the set up steps using the DDR Setup Assistant, the *Agilent Logic and Protocol Analyzer* application will have the appropriate Probes, Modules, Tools, and Windows set up, similar to those shown in the example Overview tab below.



Typically, the resulting Overview tab will contain:

- DDR3 Eyefinder — used to set up the appropriate sample positions for capturing DDR data.
- General purpose probe tool — shows how to connect the probe to logic analyzer pods.
- Four-card logic analyzer module (16962A or 16960A) or U4154A Logic Analyzer module.

- DDR Bus Decoder — decodes the captured data.
- Listing window — to display decoded data.
- Optional Waveform window — to display state or timing waveforms.

  It is best to add Waveform windows immediately after the logic analyzer module because, when displaying large amounts of waveform data, decoding can slow down the waveform display.

See
- "In This Guide" on page 5

In This Guide

For an overview and list of features, see: "DDR Setup Assistant–At a Glance" on page 3

First, this guide describes the options for probing DDR devices and the logic analysis system hardware and software required before you can use the DDR Setup Assistant.

Next, this guide provides more in-depth information about the steps taken when using the DDR Setup Assistant:

Then, there is more in-depth information on using the logic analyzer's automated Thresholds and Sample Positions set up (also known as normal logic analyzer *eye finder*), using DDR3 Eyefinder, and validating DDR setups once you have completed the sampling position set up.

Finally, this guide introduces you to the other tools used for capturing and analyzing data from DDR systems and provides pointers to additional documentation.

- Chapter 8, “Capturing Data (Triggering),” starting on page 109
- Chapter 9, “Decoding Captured Data,” starting on page 113

For a printable version of this online help, see: *"DDR Setup Assistant Online Help"*.

See Also

- DDR probe manuals.
- DDR Bus Decoder Online Help
- DDR Compliance Tool online help.

Contents

3 Using the DDR Setup Assistant

4 Setting Up Thresholds and Sample Positions on DDR Address/Control Signals

1 Options for Probing DDR Devices

There are several different Agilent and third-party options for probing a DDR device under test (DUT).

DDR3

DDR2

LPDDR

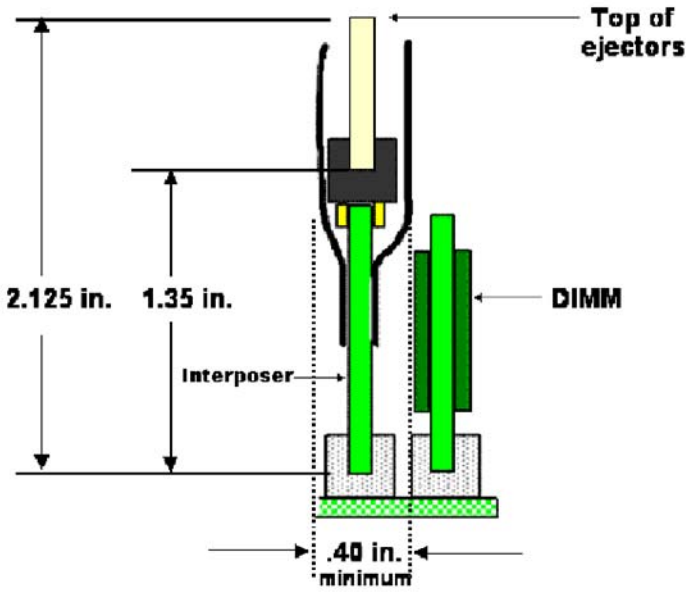
Custom

DDR3 DIMM Interposers

Handling DIMM Interposers

Handle interposers carefully.

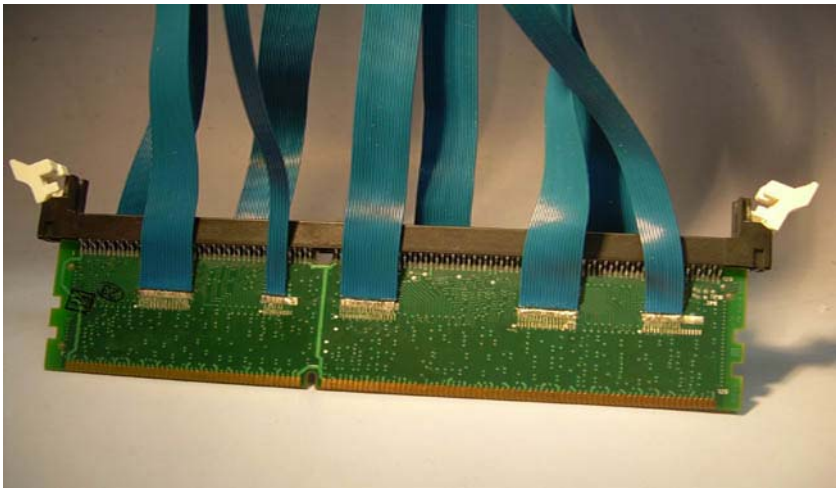
- Provide strain relief for cables.
- Store and ship flat.



Using DIMM Interposers

1. First, make sure that the device under test boots without the interposer.
2. Power down the device under test.
3. Insert interposer into the DIMM socket.
4. Fan headers out on either side of interposer.
5. Insert the DIMM into the interposer.
6. Make connections to the logic analyzer pod cables as shown in the configuration file's general-purpose probe tool.

FS2352 1867 DDR3 DIMM Probe from FuturePlus



FS2352 1867 DIMM probe from FuturePlus works with 16962A logic analyzer modules only.

Configuration Files for FS2352

The default location for FuturePlus configuration files is: C:\Documents and Settings\All Users\Shared Documents\Agilent Technologies\Logic Analyzer\Default Configs\FuturePlus

For More Information

- Search for "FS2352" on the "FuturePlus web site".

Nexus DDR3 DIMM Interposer

The Nexus DDR3 DIMM interposer works with 16962A logic analyzer modules only.

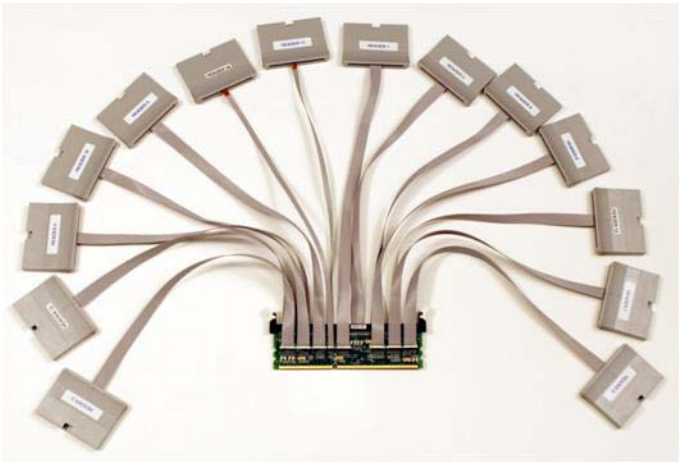
Configuration Files for Nexus DDR3 DIMM Interposer

The default location for Nexux configuration files is: C:\Documents and Settings\All Users\Shared Documents\Agilent Technologies\Logic Analyzer\Default Configs\Nexus

For More Information

- See "NT-DDR3DIHS information on the Nexus Technology web site".

N4835A (FS2351) DDR3 DIMM Interposer (Discontinued)



N4835A (FS2351) works with 16960A or 16962A logic analyzer modules.

Configuration File for N4835A

There is one configuration file for the N4835A DDR3 DIMM interposer at all data rates.

* CK0 is double probed on N4835A. You can run eye finder and eye scan (that is, logic analyzer Thresholds and Sample Positions set up) on the sample of CK0 that is not used as the actual clock.

CAUTION

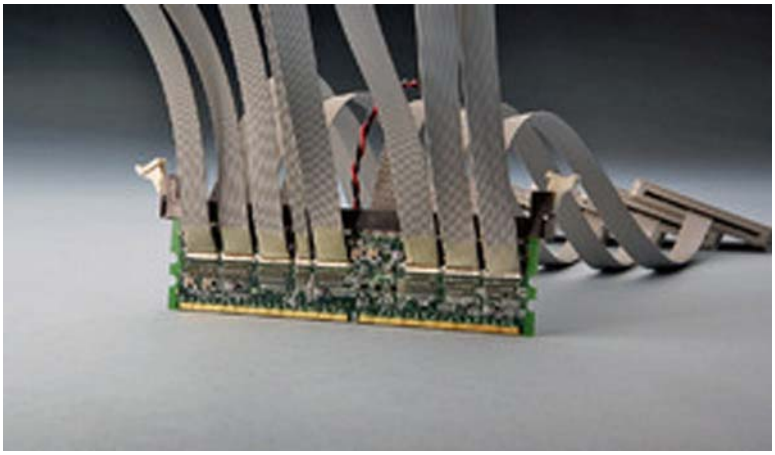
Make sure you have the proper N4835A configuration file for the N4835A (FS2351) interposer. While the pod connections are the same as with the N4821B (FS2350) interposer's 1066/1333 configuration, the signal mapping is not the same!

See "To load a configuration file" (in the online help).

For More Information

- See *Agilent N4835A DDR3 DIMM Interposer Installation Guide* which can be found on the "Agilent web site".

N4821B (FS2350) DDR3 DIMM Interposer (Discontinued)



N4821B (FS2350) works with 16960A or 16962A logic analyzer modules.

Configuration Files for N4821B

There is one configuration file for the 16962A logic analyzer at all data rates. There are two configuration files for the 16960A logic analyzer module: one for 800/1600 data rates, and one for 1066/1333 data rates.

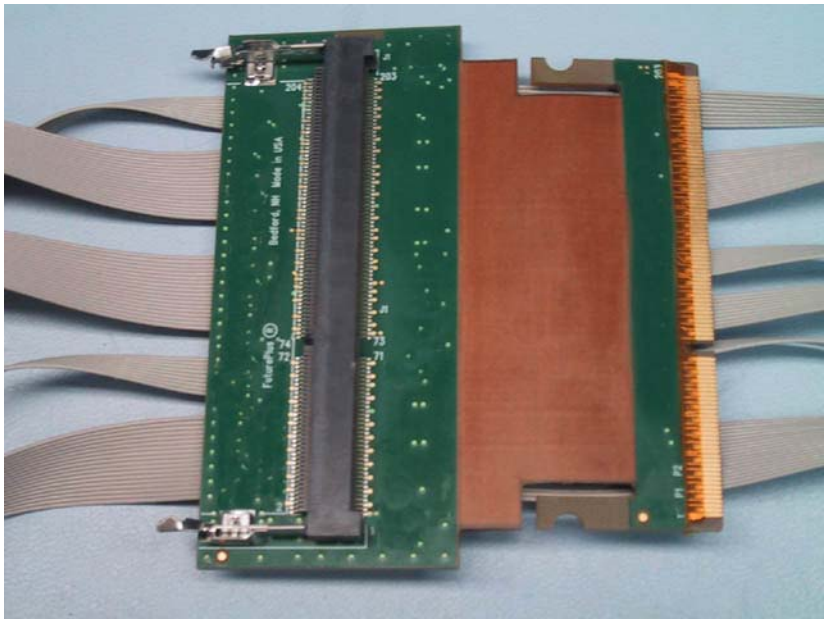
See "To load a configuration file" (in the online help).

For More Information

- Search for "FS2350" on the "FuturePlus web site".

DDR3 SODIMM Interposers

FS2354 DDR3 SODIMM Interposer



FS2354 SODIMM works with 16962A logic analyzer modules only.

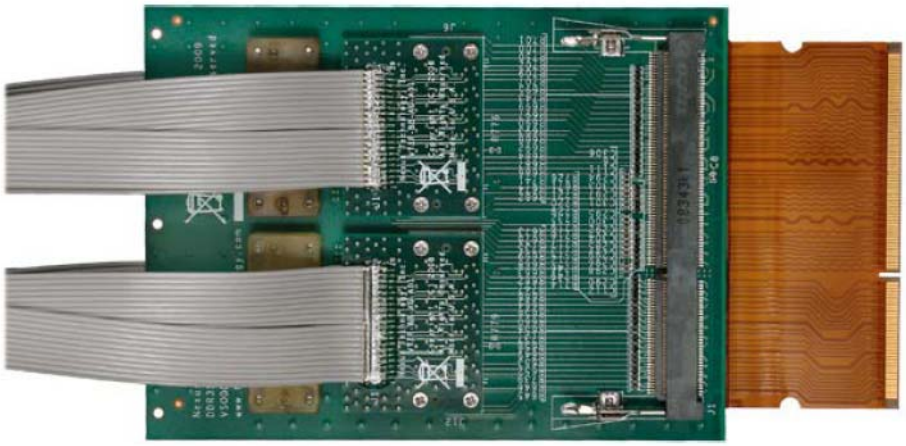
Configuration Files for FS2354

The default location for FuturePlus configuration files is: C:\Documents and Settings\All Users\Shared Documents\Agilent Technologies\Logic Analyzer\Default Configs\FuturePlus

For More Information

- Search for "FS2354" on the "FuturePlus web site".

Nexus DDR3 SODIMM Interposer



Nexus DDR3 SODIMM interposer works with 16962A logic analyzer modules only.

Configuration Files for Nexus DDR3 SODIMM Interposer

The default location for Nexux configuration files is: C:\Documents and Settings\All Users\Shared Documents\Agilent Technologies\Logic Analyzer\Default Configs\Nexus

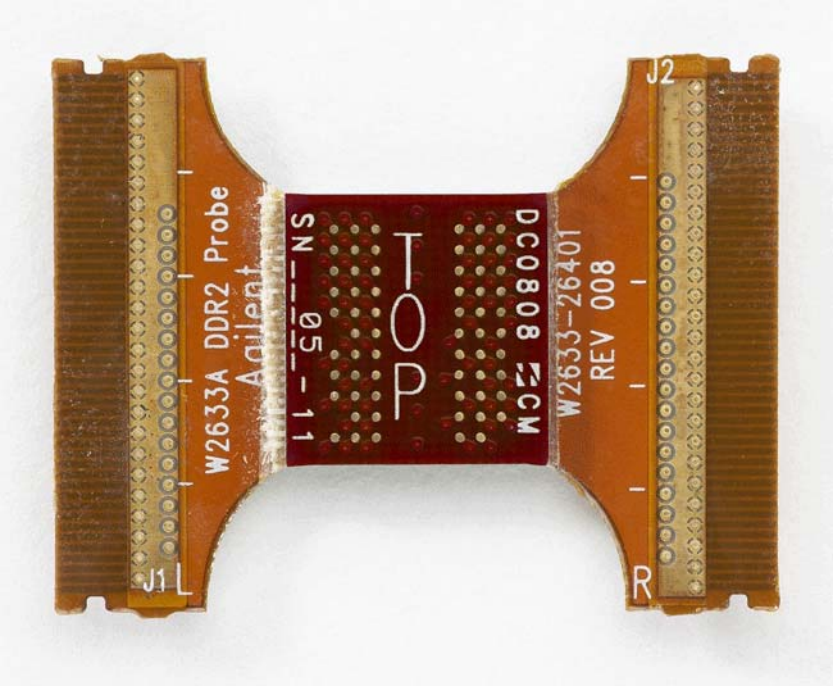
For More Information

- See "NT-DDR3SOIHS information on the Nexus Technology web site".

DDR3 BGA Probes

The DDR3 BGA probes work with 16950A/B or 16962A logic analyzer modules, and there separate configuration files for each. There are also separate configuration files for the x8 and x16 probes.

W3633A DDR3 BGA x8 Probe



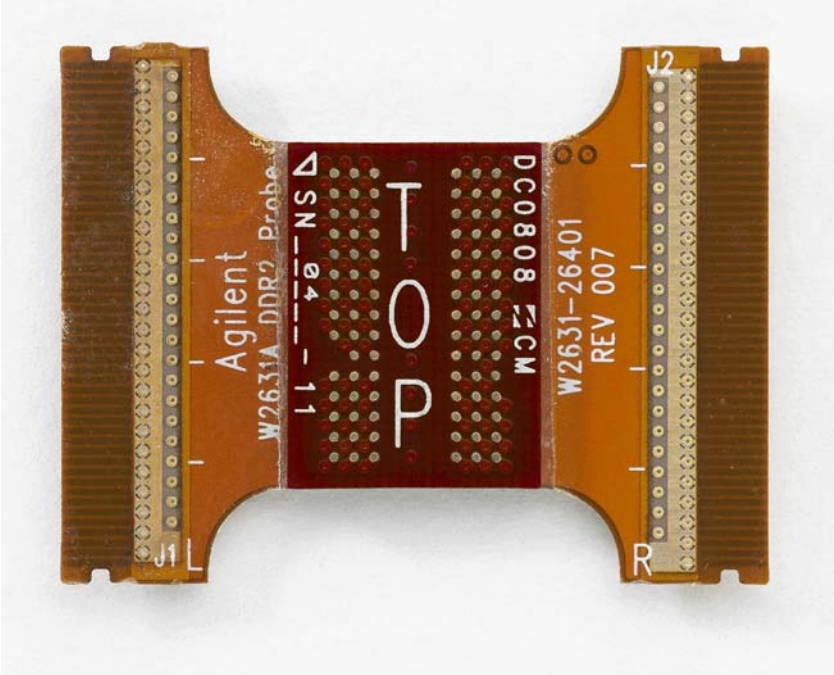
Configuration Files for W3633A Probe

See "To load a configuration file" (in the online help).

For More Information, See

- *Agilent W3630 Series DDR3 DRAM BGA Probes Installation Guide* which can be found on the "Agilent web site".

W3631A DDR3 BGA x16 Probe



Configuration Files for W3631A Probe

See "To load a configuration file" (in the online help).

For More Information, See

- *Agilent W3630 Series DDR3 DRAM BGA Probes Installation Guide* which can be found on the "Agilent web site".

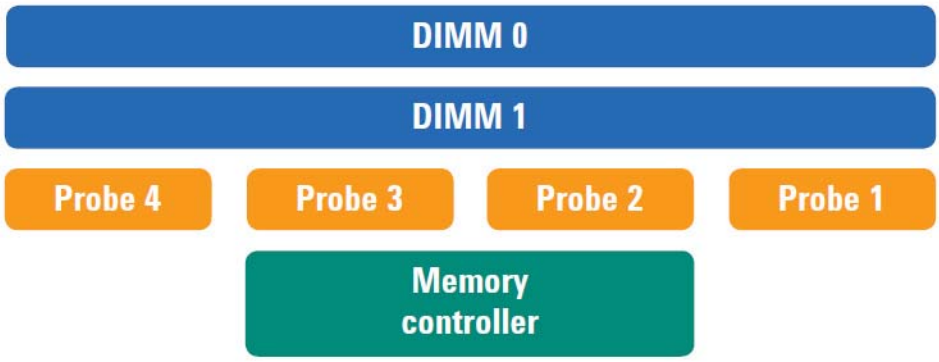
DDR3 Midbus Probes

DDR3 midbus probes require special footprints to be designed into the device under test, and they require double probing. Limited quantities of these probes were available.

• "N4834A DDR3 Midbus Probe (Discontinued)" on page 20

N4834A DDR3 Midbus Probe (Discontinued)

For embedded DDR3 design or validation board design with no constraints on board spaces, the N4834A double probed soft touch probe can be used for midbus probing. The N4834A comes in sets of 4 double probed soft touch probes for connection to four footprints on the board.



The N4834A DDR3 midbus probe works with 16960A or 16962A logic analyzer modules.

Configuration Files for N4834A Probe

See "To load a configuration file" (in the online help).

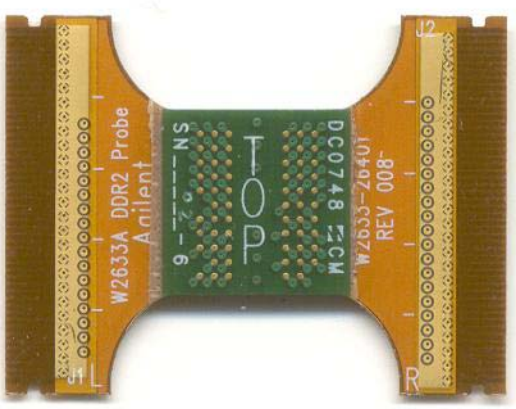
For More Information

- Search for "N4834A" on the "Agilent web site".

DDR2 BGA Probes

The DDR2 BGA probes work with 16950A/B or 16962A logic analyzer modules, and there separate configuration files for each. There are also separate configuration files for the x8 and x16 probes.

W2633A/B, W2634A DDR2 BGA x8 Probe



Configuration Files for W2633A/B, W2634A Probes

See "To load a configuration file" (in the online help).

For More Information, See

- *Agilent W2630 Series DDR2 DRAM BGA Probes Installation Guide* which can be found on the "Agilent web site".

W2631A/B, W2632A DDR2 BGA x16 Probe

Configuration Files for W2631A/B, W2632A Probes

See "To load a configuration file" (in the online help).

For More Information, See

- *Agilent W2630 Series DDR2 DRAM BGA Probes Installation Guide* which can be found on the "Agilent web site".

LPDDR BGA Probes

The LPDDR BGA probes work with 16950A/B or 16962A logic analyzer modules, and there separate configuration files for each.

W2638A LPDDR BGA x32 Probe

Configuration Files for W2638A Probe

See "To load a configuration file" (in the online help).

For More Information, See

- *W2637A and W2638A LPDDR BGA Probes / W2639A Oscilloscope Adapter Board User's Guide* which can be found on the "Agilent web site".

W2637A LPDDR BGA x16 Probe

Configuration Files for W2637A Probe

See "To load a configuration file" (in the online help).

For More Information, See

- *W2637A and W2638A LPDDR BGA Probes / W2639A Oscilloscope Adapter Board User's Guide* which can be found on the "Agilent web site".

Custom Midbus Probing

For custom midbus probing, you can design Soft Touch or Soft Touch Pro footprints into your device under test and route signals to the footprint pads.

• "Soft Touch / Soft Touch Pro Embedded Custom Midbus Probing" on page 24

Soft Touch / Soft Touch Pro Embedded Custom Midbus Probing

You can design Soft Touch or Soft Touch Pro footprints into your device under test (DUT) and route signals to the footprint pads. Because this type of probing is *custom*, DUT designs are unique. However, there are some common things to consider.

Because DDR data reads and writes occur at different times relative to the bus (and sampling) clock, you must use the logic analyzer's dual sample sampling clock mode (see "Dual Sample Sampling Clock Mode" (in the online help)). This affects how signals are probed and mapped to logic analyzer pods.

Other considerations for embedded Soft Touch footprints for 16962A or 16960A logic analyzers:

- The CK0, Address, and Control bits should be placed on one Soft Touch footprint. This is a requirement for DDR3 Eyefinder. Also, you must connect the address and control signals to a different logic analyzer module than the data /strobe signals. Solutions for DDR logic analysis require a module minimum of two logic analyzer modules.
- The CK0 signal must be probed differentially and must be connected to the pod 1 clock of the clocking module (this is the second card up from the bottom of the mainframe).
- The CKE0 signal should be connected to the clock input on pod 2 of the master module. When setting up the state sampling clock options in the logic analyzer, select:
  - CKE0 – latched high for capture out of reset.
  - CKE0 – enabled high as clock qualifier.
- Make sure there are no signal stubs!
- Optional: consider routing a copy of the CS#0 signal to the Pod 4 clock input on the master module.
- The minimum signals required for DDR logic analysis tools are:
  - CK0, COMMAND, CS#, Data_W, Data_R, CKE*, BA, ADDR, RowADDR, and ColADDR.
  - Custom triggers may require additional signals.

Configuration Files for Soft Touch Probes

With custom probing, you will likely have custom configuration files. Be sure to include a general-purpose probe tool in your Overview configuration to describe how logic analyzer pod connectors should be connected to the probes.

To simplify the procedure of custom configuration file creation, Agilent provides the DDR/LPDDR Custom Configuration Creator tool. The tool ensures that all the layout information needed by DDR/LPDDR Decoder is included in the created configuration file. This tool is a part of the Agilent DDR Setup Assistant and Eyefinder software package. Therefore, the tool is available only after you install this package. To know more about this tool, refer to its online help that gets installed with this tool's software.

For More Information, See

- *Agilent Technologies E5400-Pro Series Soft Touch Connectorless Probes User's Guide* which can be found on the "Agilent web site".
- *Agilent Technologies Soft Touch Connectorless Probes User's Guide* which can be found on the "Agilent web site".

1 Options for Probing DDR Devices

2
Before Using the DDR Setup Assistant

Once you have chosen a solution for probing your DDR device, you must make sure you have the required logic analysis system hardware and software. This includes any necessary probe to logic analyzer cable adapters.

There are also some things you can do to prepare your DDR device under test in order to make the best measurements.

Logic Analysis System Hardware Requirements

To capture DDR Command, Address, Control, and Data signals, a four-card, 68-channel per card, logic analyzer card set with sufficient state analysis speed is required. The 16962A and 16960A logic analyzer cards meet these requirements.

A six-slot logic analysis system frame is required for the four-card logic analyzer. The 16902B logic analysis system frame meets the requirement.

Besides these, you can also use the 136 channel U4154A Logic Analyzer module installed in the Agilent AXIe chassis to capture DDR signals.

Installing Required and Optional Software

NOTE

While the DDR Setup Assistant works with the *Agilent Logic Analyzer* application on a computer remotely connected to logic analyzer hardware, we recommend you run the DDR Setup Assistant on the logic analysis system that contains the logic analyzer hardware. This is because the logic analyzer's automated Thresholds and Sample Positions set up (also known as logic analyzer *eye finder*) and DDR3 Eyefinder run faster in this configuration.

You can use the Windows operating system's Remote Desktop Connection feature to log into the logic analysis system that has the logic analyzer hardware. The Remote Desktop Connection provides good performance.

Before you begin using the DDR Setup Assistant, make sure the required software (and any desired optional software) is installed.

This software can be downloaded from the Agilent web site at: "www.agilent.com/find/la-sw-download"

Required Software

The following software is required in order to use the DDR Setup Assistant:

- Agilent Logic Analyzer Application Software, version 04.00 or higher.
- DDR2 and DDR3 Bus Decoder (B4621B, requires a license), version 04.00 or higher. This software decodes the captured signals, showing commands, cycle types, etc. DDR configuration files are included with the bus decoder and many of them assume the bus decoder is present.
- DDR3 Eyefinder, version 04.00 or higher. This software is necessary to set sample positions for Data signals.
- If you have a third-party (non-Agilent) probe, there may be third-party software that is also required.

Optional DDR Tools

The following software is optional but is useful for DDR analysis:

- DDR2/3 Protocol Compliance and Analysis Tool (B4622B, requires a license), version 04.00 or higher. This is an automated test application that evaluates captured LPDDR/LPDDR2 and DDR/DDR2/DDR3 data against a set of user-defined limits to help you validate that a memory system is operating properly. When used with the U4154A module, it can evaluate LPDDR3 and DDR4 data as well.

Tuning Your DDR DUT to Make the Best Measurements

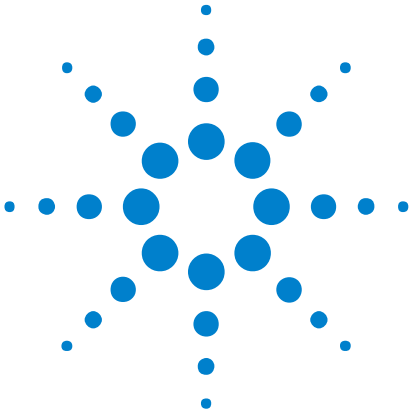
There are a couple things you can do to prepare your DDR device under test for making measurements:

- Turn off data scrambling.
- Turn off power management (for initial measurements).

Setting Up Read and Write Traffic in the DUT

READ and WRITE traffic in the DDR device under test (DUT) is required for both Read and Write signal sampling set up. For example:

- Random pattern data tests:
  - Memtest 86 test #7.
- Memory test with alternating patterns:
  - Memtest 86 test #5.
- Video clips.



3
Using the DDR Setup Assistant

Starting the DDR Setup Assistant

NOTE

While the DDR Setup Assistant works with the *Agilent Logic Analyzer* application on a computer remotely connected to logic analyzer hardware, we recommend you run the DDR Setup Assistant on the logic analysis system that contains the logic analyzer hardware. This is because the logic analyzer's automated Thresholds and Sample Positions set up (also known as logic analyzer *eye finder*) and DDR3 Eyefinder run faster in this configuration.

You can use the Windows operating system's Remote Desktop Connection feature to log into the logic analysis system that has the logic analyzer hardware. The Remote Desktop Connection provides good performance.

1 After installing the DDR Setup Assistant, double-click the **DDR Setup Assistant** icon on your desktop to start the DDR Setup Assistant.

   The DDR Setup Assistant automatically starts the *Agilent Logic Analyzer* application if it is not already started.

Step - Specify Input Parameters

In this step, you give the DDR Setup Assistant relevant information about your DDR test setup.

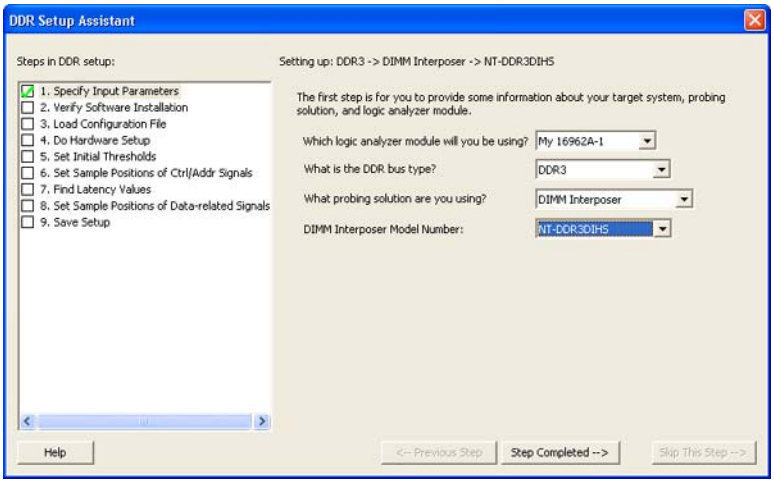
1 Select the name of the logic analyzer module that will be used to capture DDR signals.

2 Select the **DDR bus type**.

3 Specify your **probing solution** (see Chapter 1, “Options for Probing DDR Devices,” starting on page 11).

Depending on the probing solution you select, you may have additional input parameters to specify. For example:

- When you select the **BGA** probing solution, you have an additional selection for your **DRAM type and data width**.
- When you select the **DIMM Interposer** probing solution, there is an additional selection for the model number.
- When you select the **Softtouch** probing solution, there are no other input parameters to specify.



4 When you are finished selecting input parameters, click **Step Completed -->**.

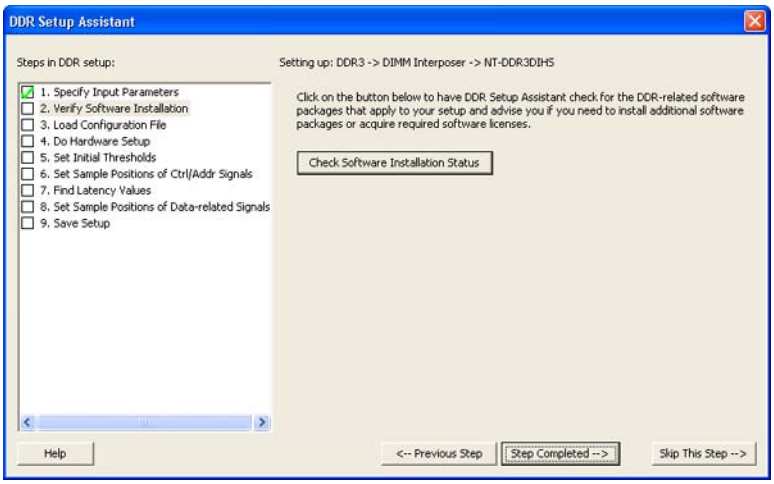
The selections you make in this step identify your setup for the automated DDR Setup Assistant actions that follow.

Next • "Step - Verify Software Installation" on page 36

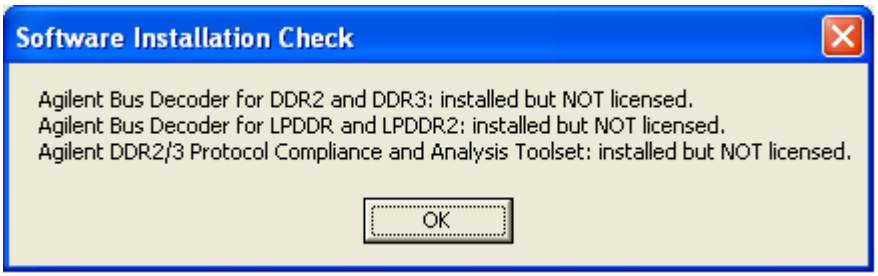
Step - Verify Software Installation

In this step, the DDR Setup Assistant checks to see if the required and optional DDR analysis software has been installed.

1 Click **Check Software Installation Status**.



When the check is complete, an information with the software installation status appears.



2 If you need to install software:

- **a** Close the DDR Setup Assistant.
- **b** Close the *Agilent Logic Analyzer* application.
- **c** Install the software (see "Installing Required and Optional Software" on page 29).
- **d** Restart the *Agilent Logic Analyzer* application.
- **e** Restart the DDR Setup Assistant.
- **f** Continue with the DDR set up steps.

3 Click **Step Completed -->**.

Next • "Step - Load Configuration File" on page 37

Step - Load Configuration File

In this step, the DDR Setup Assistant loads the selected XML configuration file.

1 Select whether you want to load an Agilent-supplied standard configuration file (if you are using an Agilent probing solution) or a custom configuration file (if you are using a custom probing solution).

If you select to load a standard configuration file, the DDR Setup Assistant automatically tries to locate and load an appropriate configuration file based on the input parameters you selected in the first step. The file is loaded from the set of standard configuration files. The default location for these standard configuration files is:

C:\Documents and Settings\All Users\Documents\Agilent Technologies\Logic Analyzer\Default Configs\Agilent

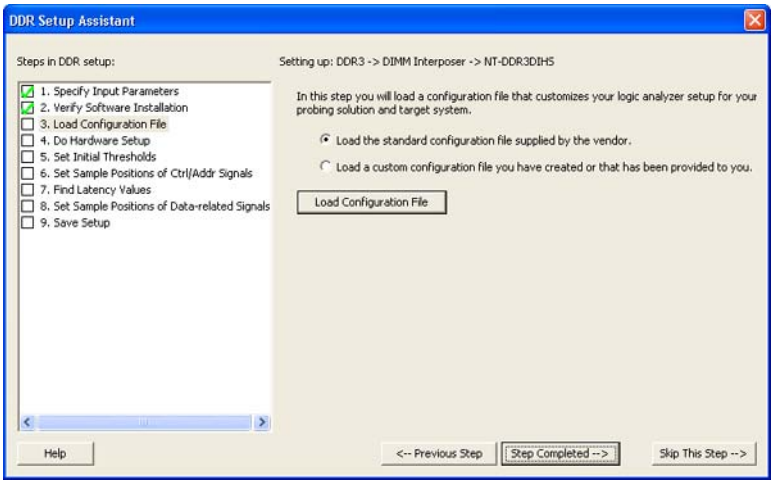
If you select to load a custom configuration file, the DDR Setup Assistant allows you to navigate to the custom configuration file location and select it for loading.

NOTE

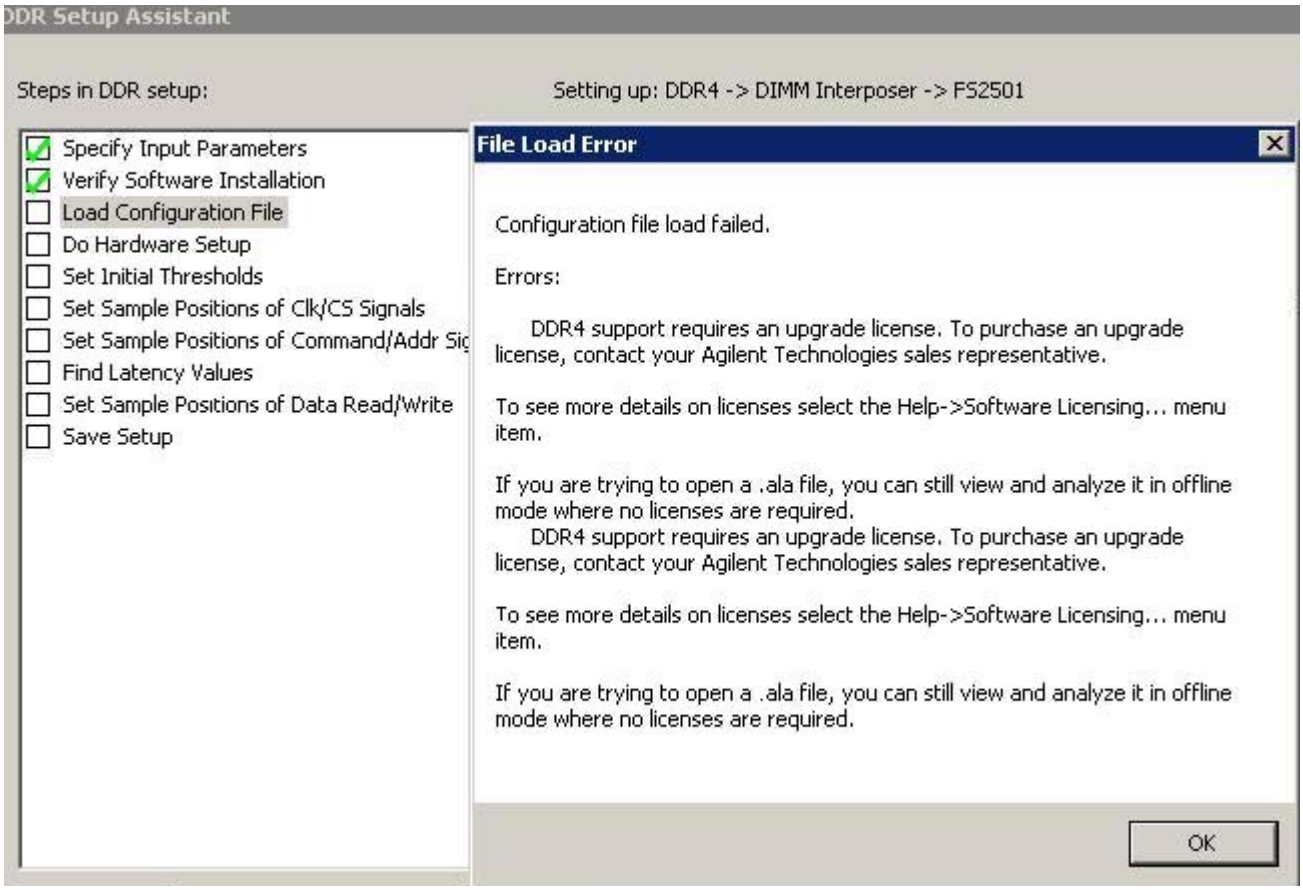
To simplify the procedure of custom configuration file creation, Agilent provides the DDR/LPDDR Custom Configuration Creator tool. The tool ensures that all the layout information needed by DDR/LPDDR Decoder is included in the created configuration file. This tool is a part of the Agilent DDR Setup Assistant and Eyefinder software package. Therefore, the tool is available only after you install this package.

To know more about this tool, refer to its online help that gets installed with this tool's software.

2 Click **Load Configuration File**.



- If the DDR Setup Assistant cannot find the configuration file for a probe, an error dialog is displayed, and you are given an opportunity to browse for the file.
- If you are using a Soft Touch probing solution, a file browser appears for you to select the configuration file for your custom probing solution.
- In some cases, you may know of a modified configuration file that should be used for a particular probing setup. In this case, you can manually load the configuration file.
- If you selected DDR4 or LPDDR3 as the DDR Bus Type in Step 1 of the wizard and you do not have the B4621B (for DDR) and B4623B (for LPDDR) software licenses installed, then you will not be able to load a standard or a custom DDR4/LPDDR3 configuration file in this step. In such a situation, the following error message will be displayed. To get DDR4 and LPDDR3 support, you must purchase the B4621B and B4623B license respectively.



3 If necessary, navigate to the configuration file.

The default location for standard configuration files is:

C:\Documents and Settings\All Users\Documents\Agilent Technologies\Logic Analyzer\Default Configs\Agilent\

Then, select the file and click **Open**.

4 Click **Step Completed -->**.

Configuration files typically include:

- A general purpose probe tool to define the mapping between device under test signals and logic analyzer pods. If the configuration file doesn't include one, you can add it yourself. See "To define probes" (in the online help).
- A DDR Bus Decoder tool for decoding the captured data. If the configuration file doesn't include one, you can add it yourself. See "To add new tools" (in the online help).

For more information about the configuration files provided for the different DDR probing options, see Chapter 1, “Options for Probing DDR Devices,” starting on page 11.

Next

- "Step - Do Hardware Setup" on page 40

Step - Do Hardware Setup

The DDR Setup Assistant takes no actions in this step; it just waits until you tell it the step is completed.

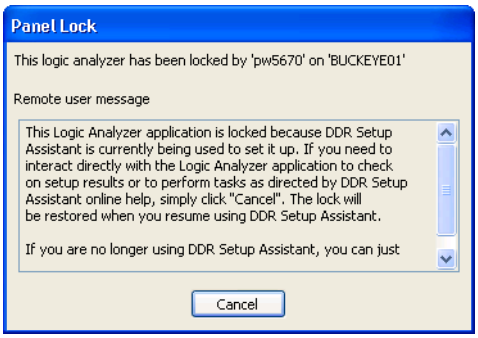
In this step, you must make the proper connections between the device under test and the logic analyzer. This includes:

- Connecting the probing solution to the device under test. (For more information, see Chapter 1, “Options for Probing DDR Devices,” starting on page 11.)
- Connecting the probing solution to the logic analyzer.

When connecting the probing solution to the logic analyzer, the configuration's probe set maps out the probing solution to logic analyzer connection. To access the probe set's mapping:

1 Go to the *Agilent Logic Analyzer* application.

2 You may have to click **Cancel** in the Panel Lock dialog.

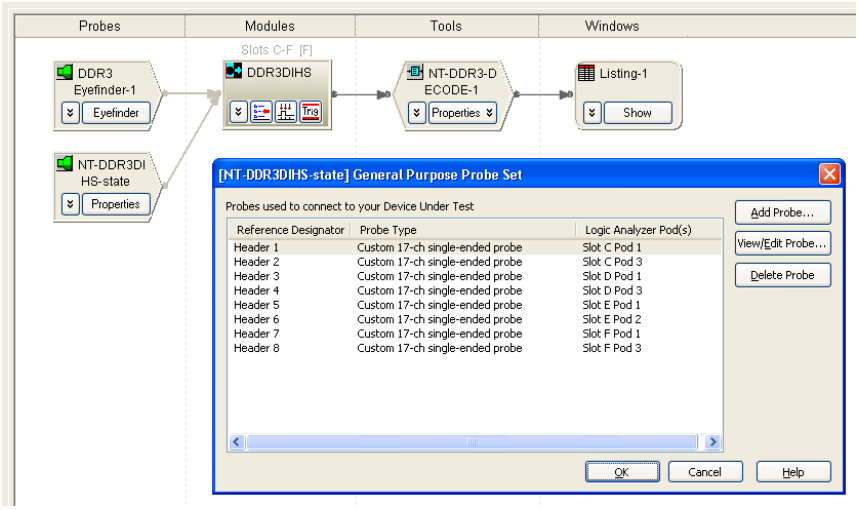


3 In the *Agilent Logic Analyzer* application, click the **Overview** tab (or the System Overview icon) to view the Overview window.

In the Overview window, you see a picture of the Probes, Modules, Tools, and Windows used in the configuration.

4 Click the probe's **Properties** button.

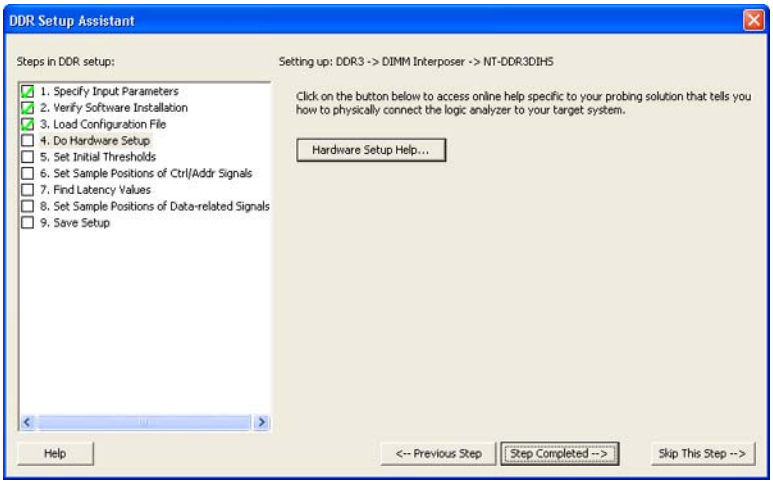
The General Purpose Probe Set dialog shows how the probe's reference designators map to the logic analyzer pod cables. For example:



NOTE The General Purpose Probe Set mapping is different for each configuration. Yours will like be different than the one shown in the previous screen.

5 Carefully connect the probes to the logic analyzer pod cables using the mapping shown in the General Purpose Probe Set dialog.

After you have made the proper probing solution to device under test and probing solution to logic analyzer connections, click **Step Completed -->**.



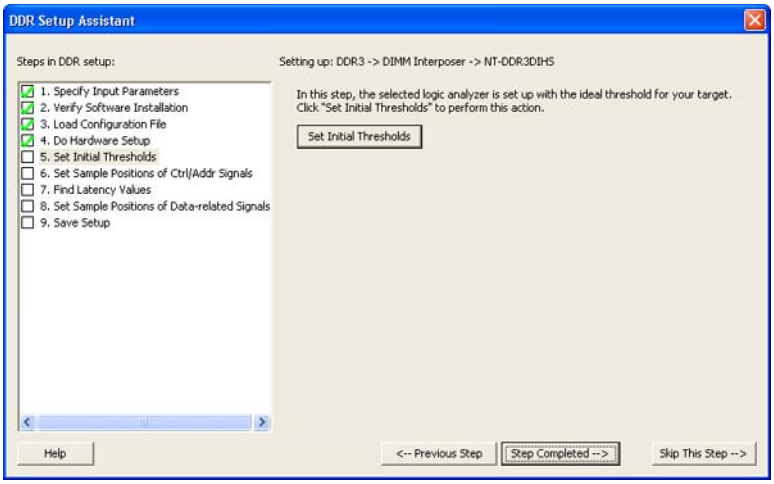
Next • "Step - Set Initial Thresholds" on page 42

Step - Set Initial Thresholds

In the **Set Initial Thresholds** step, the DDR Setup Assistant automatically sets the initial threshold voltages and detects if there are any problems with the settings.

1 Set up your device under test to have read and write traffic (see "Setting Up Read and Write Traffic in the DUT" on page 31).

2 Click **Set Initial Thresholds**.



The DDR Setup Assistant analyzes the swing of certain control signals to determine the best threshold voltage settings.

3 If there are problems with the automated initial threshold voltage settings, use the default threshold specified by the configuration file.

4 Click **Step Completed -->**.

Next

- "Step - Set Sample Positions of Ctrl/Addr Signals (not applicable to U4154A Logic Analyzer)" on page 47

Step - Set Sample Positions of Clk/CS Signals (only applicable to U4154A Logic Analyzer)

In this step, you set the sample positions of clock and chip select signals when using the U4154A Logic Analyzer module. For this step, DDR Setup Assistant runs the eyescan feature of the U4154A Logic Analyzer module to automatically calculate and set the optimal sample positions for the clock and chip select signals.

This step is only applicable to the U4154A Logic Analyzer.

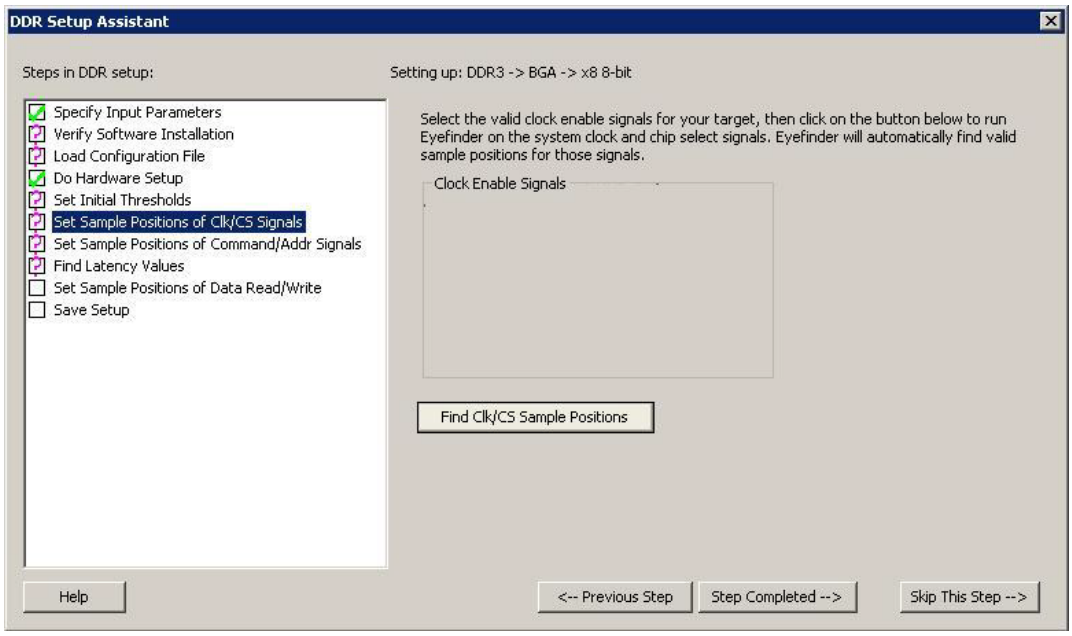
NOTE

If you selected DDR4 as the bus type in step 1 - Specify Input Parameters, then an additional field **DDR4 Command Latency** is displayed in this step.

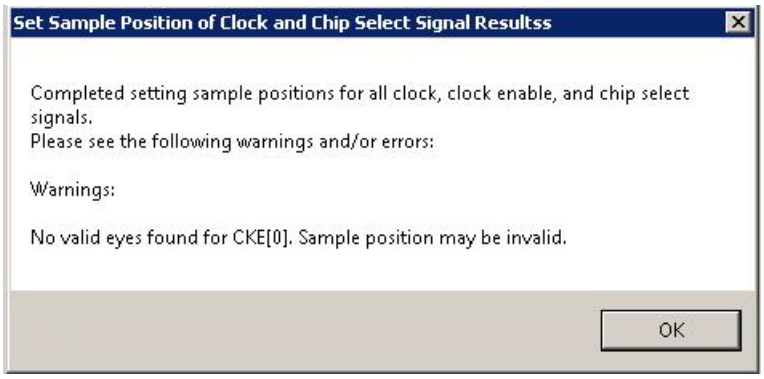
DDR4 Command latency is defined as the number of clocks from chip select going low until the command and address busses are valid.

Select valid clock enable signals and specify a value (ranging from 0 to 6) for DDR4 Command Latency.

1 Click **Find Clk/CS Sample Positions**.



2 If the eyescan run completes but gives you warnings, you should check the warnings and re-run if necessary.



3 When the clock and chip select signal sample positions have been properly set, click **Step Completed** -->.

Next

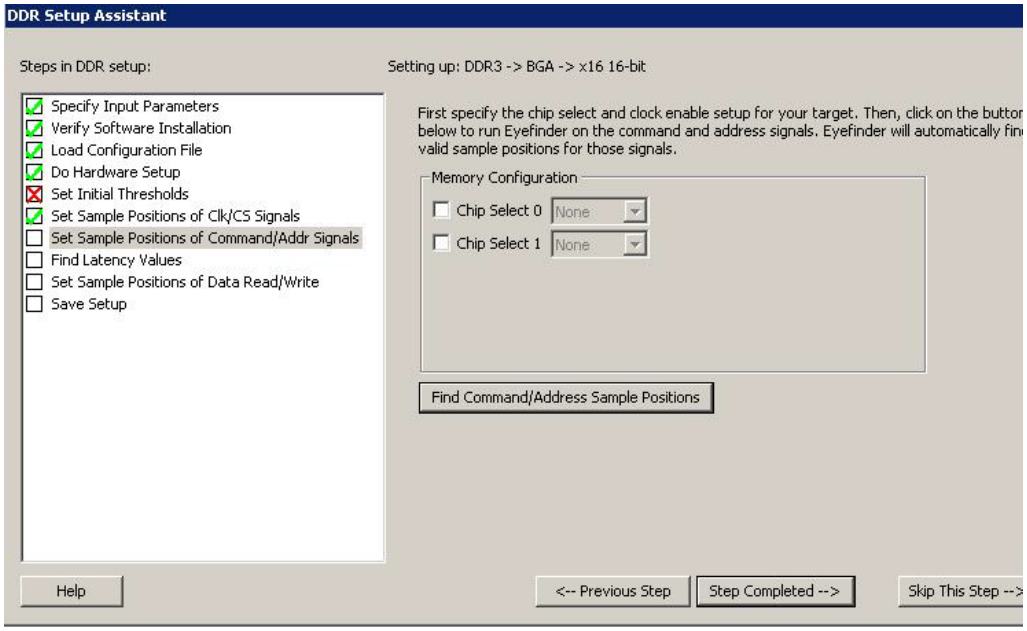
- "Step - Set Sample Positions of Command/Addr Signals (only applicable to U4154A Logic Analyzer)" on page 45

Step - Set Sample Positions of Command/Addr Signals (only applicable to U4154A Logic Analyzer)

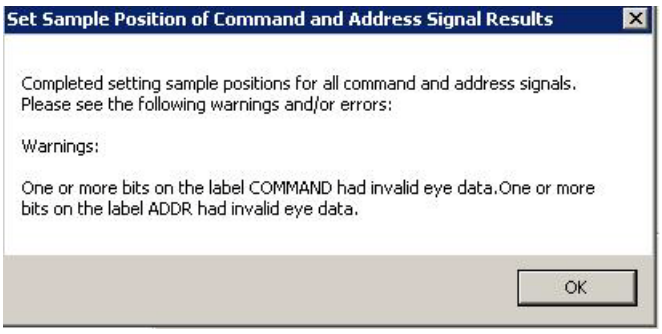
In this step, you set the sample positions of command and address signals when using the U4154A Logic Analyzer module. For this step, DDR Setup Assistant runs the eyescan feature of the U4154A Logic Analyzer module to automatically calculate and set the optimal sample positions for the command and address signals.

This step is only applicable to the U4154A Logic Analyzer.

1 Click **Find Command/Address Sample Positions**.



2 If the eyescan run completes but gives you warnings, you should check the warnings and re-run if necessary.



You should determine the cause of these messages by looking at the Agilent Logic Analyzer application's Thresholds and Sample Positions dialog and perhaps re-running the set up. See "Setting Up Thresholds and Sample Positions on DDR Address/Control Signals" on page 67.

3 When the command and address signal sample positions have been properly set, click **Step Completed -->**.

Next

- "Step - Find Latency Values" on page 49

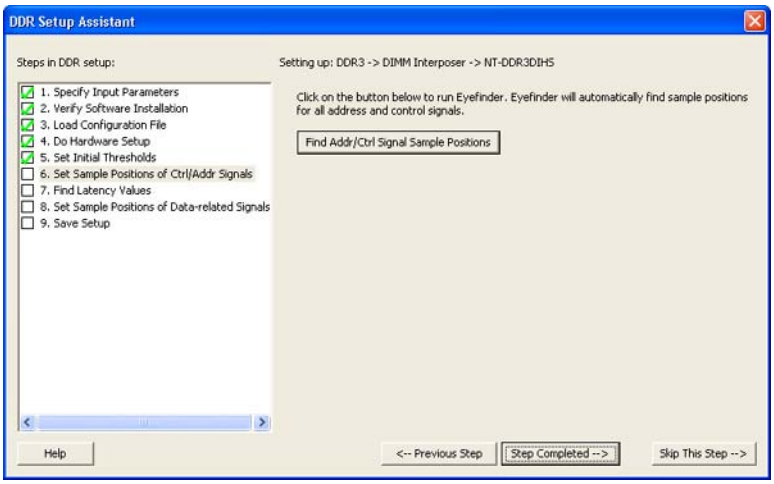
Step - Set Sample Positions of Ctrl/Addr Signals (not applicable to U4154A Logic Analyzer)

In this step, the DDR Setup Assistant runs the logic analyzer Thresholds and Sample Positions set up (also known as normal logic analyzer *eye finder*) to set the sample positions of the Control and Address signals.

This step is not applicable to the U4154A Logic Analyzer.

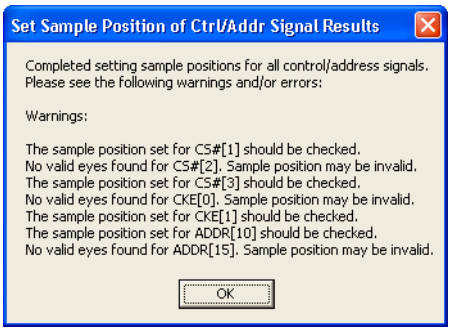
1 Again, make sure your device under test has read and write traffic (see "Setting Up Read and Write Traffic in the DUT" on page 31).

2 Click **Find Addr/Ctrl Signal Sample Positions**.



3 If the Thresholds and Sample Positions set up cannot run for some reason, click **Addr/Ctrl Signal Sample Position Help...** (which directs you to "If there are problems with finding Ctrl/Addr sample positions" on page 48).

4 If the Thresholds and Sample Positions set up run completes but gives you warnings, you should check the warnings and re-run if necessary.



For example, in the previous dialog, it may be that the CS#1-3, CKE0-1, ADDR15 signals are not being used, and these messages can safely be ignored. However, ADDR10 is generally used, so you should determine the cause of these messages by looking at the *Agilent Logic Analyzer* application's Thresholds and Sample Positions dialog and perhaps re-running the set up. See Chapter 4, “Setting Up Thresholds and Sample Positions on DDR Address/Control Signals,” starting on page 67.

5 When the Addr/Ctrl signal sample positions have been properly set, click **Step Completed -->**.

Next
- "Step - Find Latency Values" on page 49

If there are problems with finding Ctrl/Addr sample positions

Generally, problems finding the Ctrl/Addr signal sample positions are basic. Check these things:

- Make sure the device under test is powered on and that the probing solution connections to the device under test and to the logic analyzer are good.
- Make sure there is memory traffic on the DDR bus. Dense traffic is better than sparse traffic when running the logic analyzer Thresholds and Sample Positions set up to determine the Ctrl/Addr signal sample positions.

See Also
- "Solving Problems with Thresholds and Sample Positions Set Up" on page 72

Step - Find Latency Values

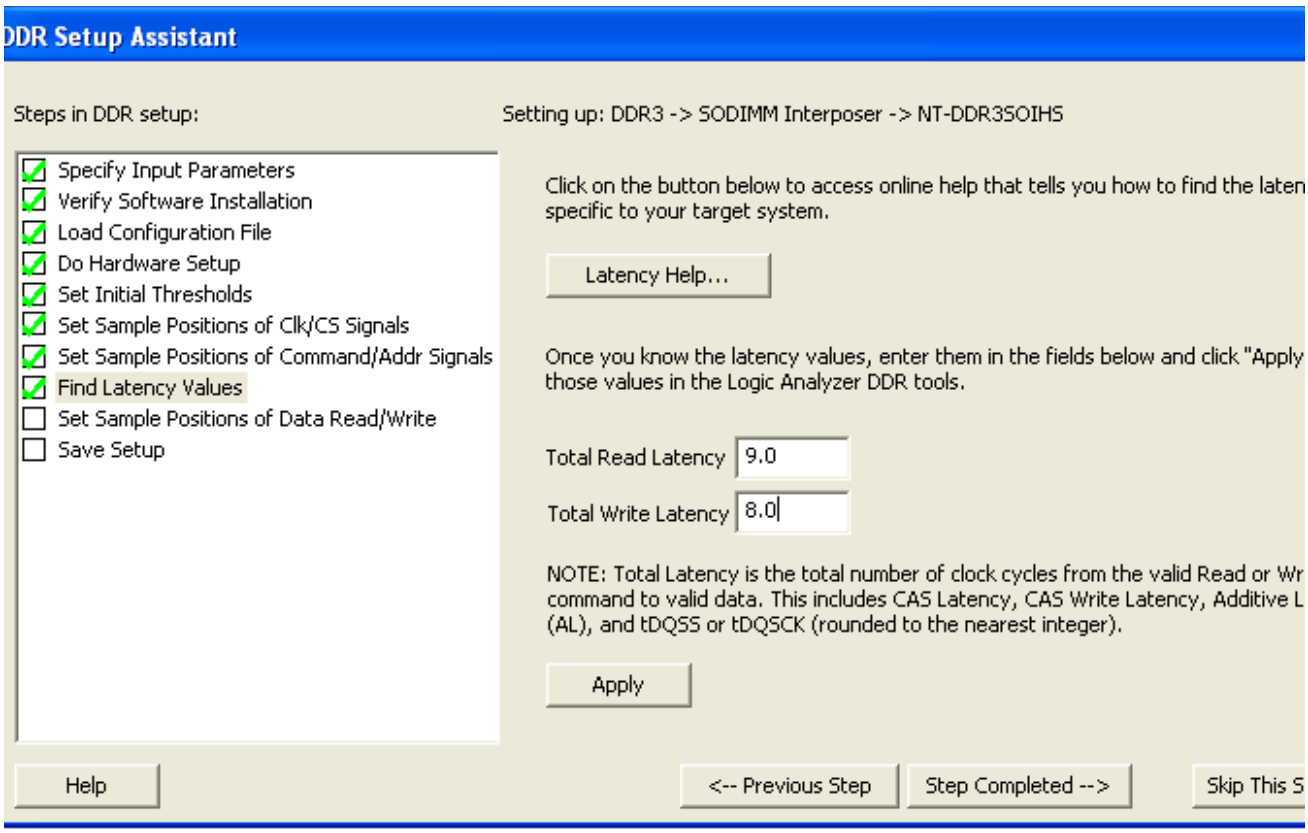
In this step, if you don't already know the latency values of the device under test, you set up the Mode Register Settings (MRS) trigger, take a trace, and scan it for latency values. See:

- "Taking a Mode Register Settings (MRS) Trace" on page 50

When you have the proper latency values for the device under test, enter the values into the DDR Setup Assistant; then, click **Apply**.

NOTE

The latency values that you specify in this step represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.



When you apply the latency values settings, the DDR Setup Assistant automatically transfers these settings to the DDR Bus Decoder and in the DDR3 Eyefinder / Eyescan.

You can also modify the DDR Bus Decoder and DDR3 Eyefinder / Eyescan settings yourself (or edit them later) by following these instructions:

- "Setting Latency Values in DDR Bus Decoder" on page 53
- "Setting Latency Values in DDR3 Eyefinder" on page 55
- "Setting Latency Values in Eyescan" on page 56

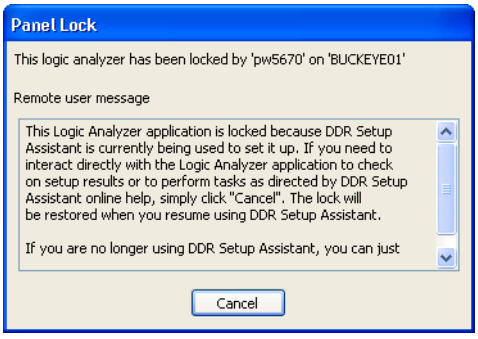
When you have found and transferred the latency values, click **Step Completed -->**.

Next

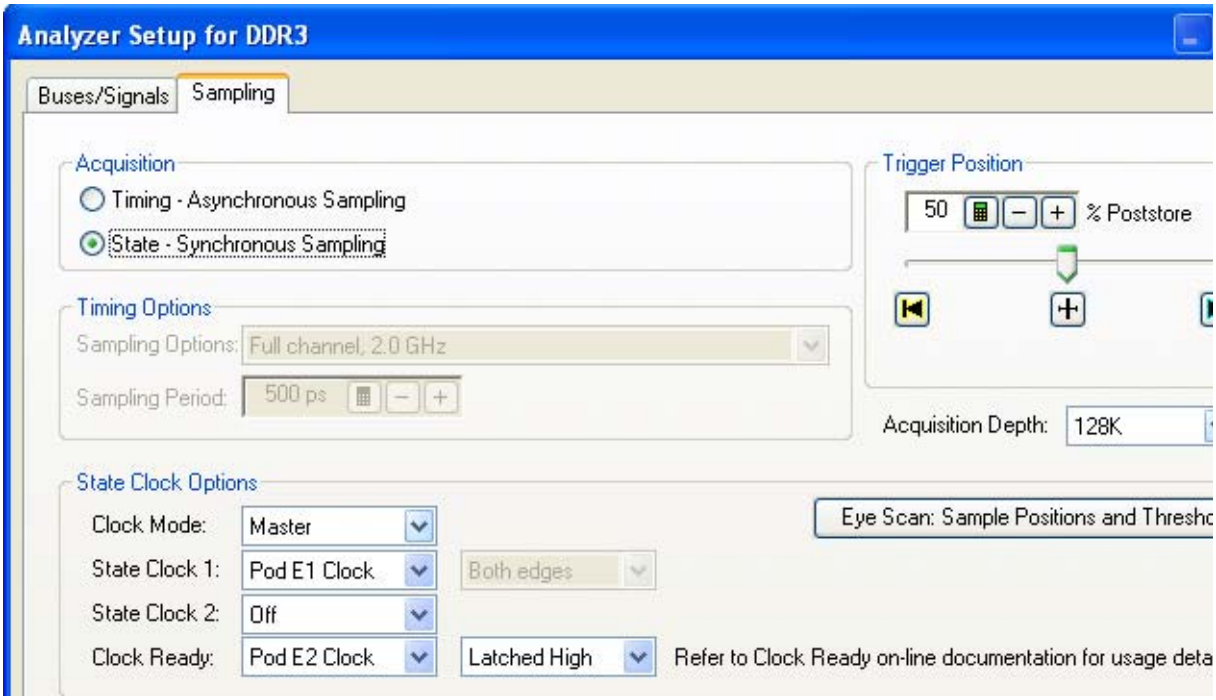
- "Step - Set Sample Positions of Data-related Signals (not applicable to U4154A logic analyzer)" on page 60
- "Step - Set Sample Positions of Data Read/Write (only applicable to U4154A Logic Analyzer)" on page 61

Taking a Mode Register Settings (MRS) Trace

1. Go to the *Agilent Logic and Protocol Analyzer* application.
2. You may have to click **Cancel** in the Panel Lock dialog.

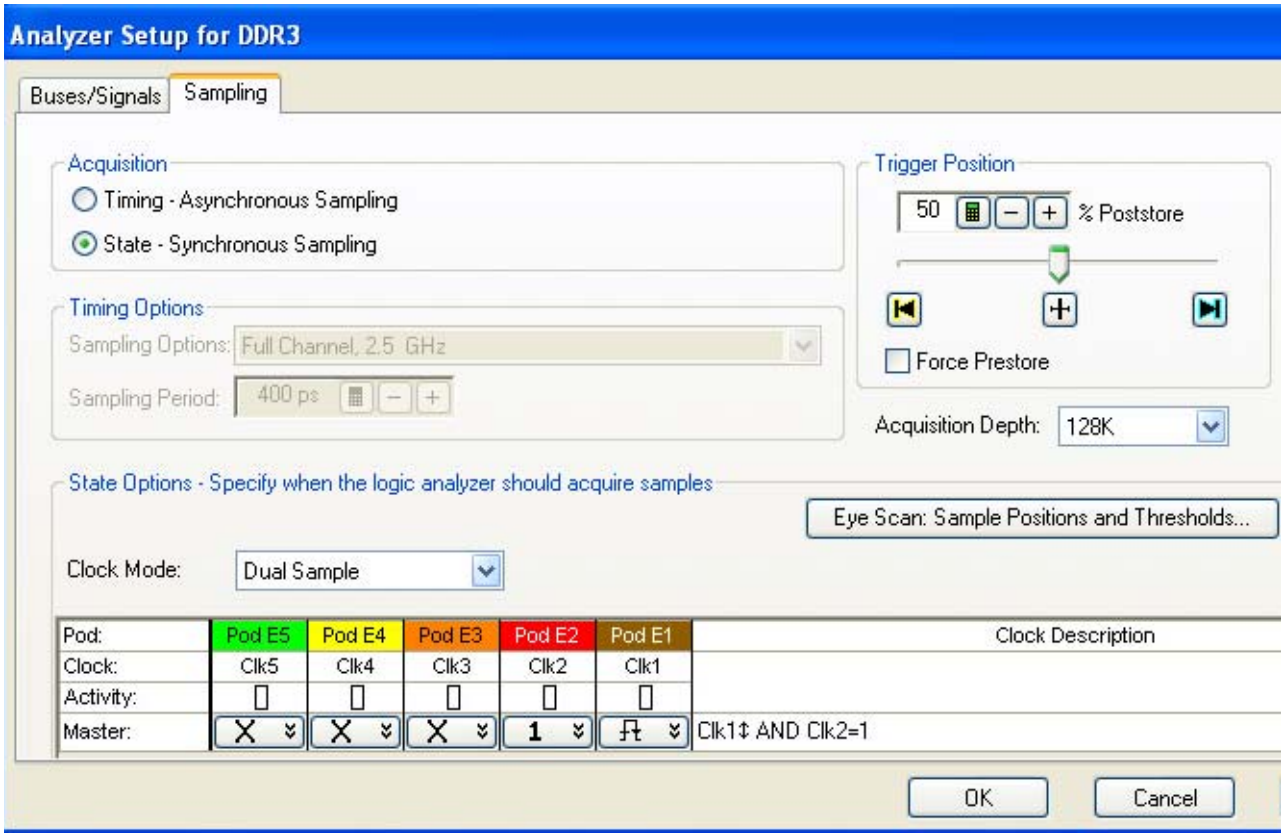


3. **For 16962A or 16960A Logic Analyzers** - In the Agilent and Protocol Logic Analyzer application's Sampling Setup, change the **Clock Ready** state clock option to **Latched High** for the clock input of Pod 2 (Clk2) as displayed in the following screen.



The CKE0 signal is routed to the CLK input on pod 2 of the logic analyzer module and CK0 is routed to the CLK input on pod 1.

For U4154A Logic Analyzers - In the Agilent Logic and Protocol Analyzer application's Sampling Setup, set the clock input of Pod 2 (Clk2) as the state clock qualifier - **Qualifier - High** as displayed in the following screen. Notice that the Qualifier - High option is represented by "1" in the following screen.



4 Power off the device under test.

5 In the *Agilent Logic Analyzer* application's Advanced Trigger dialog, recall the **Mode Register Settings** trigger.

NOTE If your device under test does not complete Mode Register Setting before the first memory write, change the Mode Register Settings trigger by replacing the sequence step that triggers on the first memory write with the "Run until user stop" trigger function. (Do not change the default storage.)

6 Run the logic analyzer with Mode Register Settings trigger (clock ready latched high on CKE0_qual)

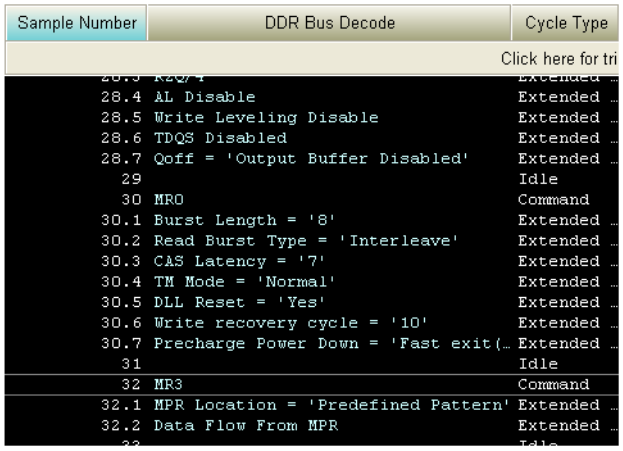
The logic analyzer runs status shows "Waiting for trigger in Trigger Step 1...".

7 Power on the device under test.

8 In the *Agilent Logic Analyzer* application's Listing window, go to the trigger.

The trigger is the first Write to Memory.

9 Scroll backward from the trigger to find the last Latency settings before the memory write.



10 Record the values for:

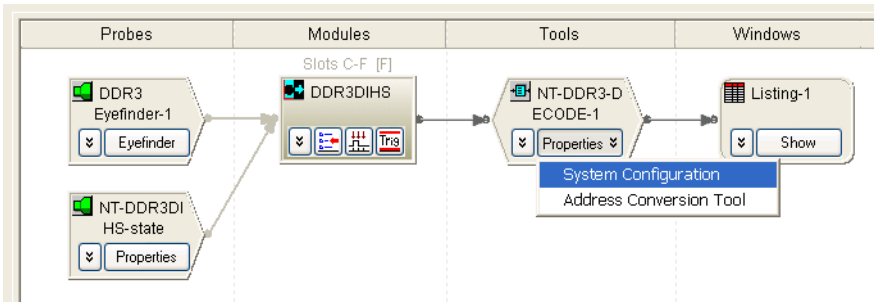
- Read latency.
- Write latency.
- Burst length.
- Burst type (sequential or interleaved).

Setting Latency Values in DDR Bus Decoder

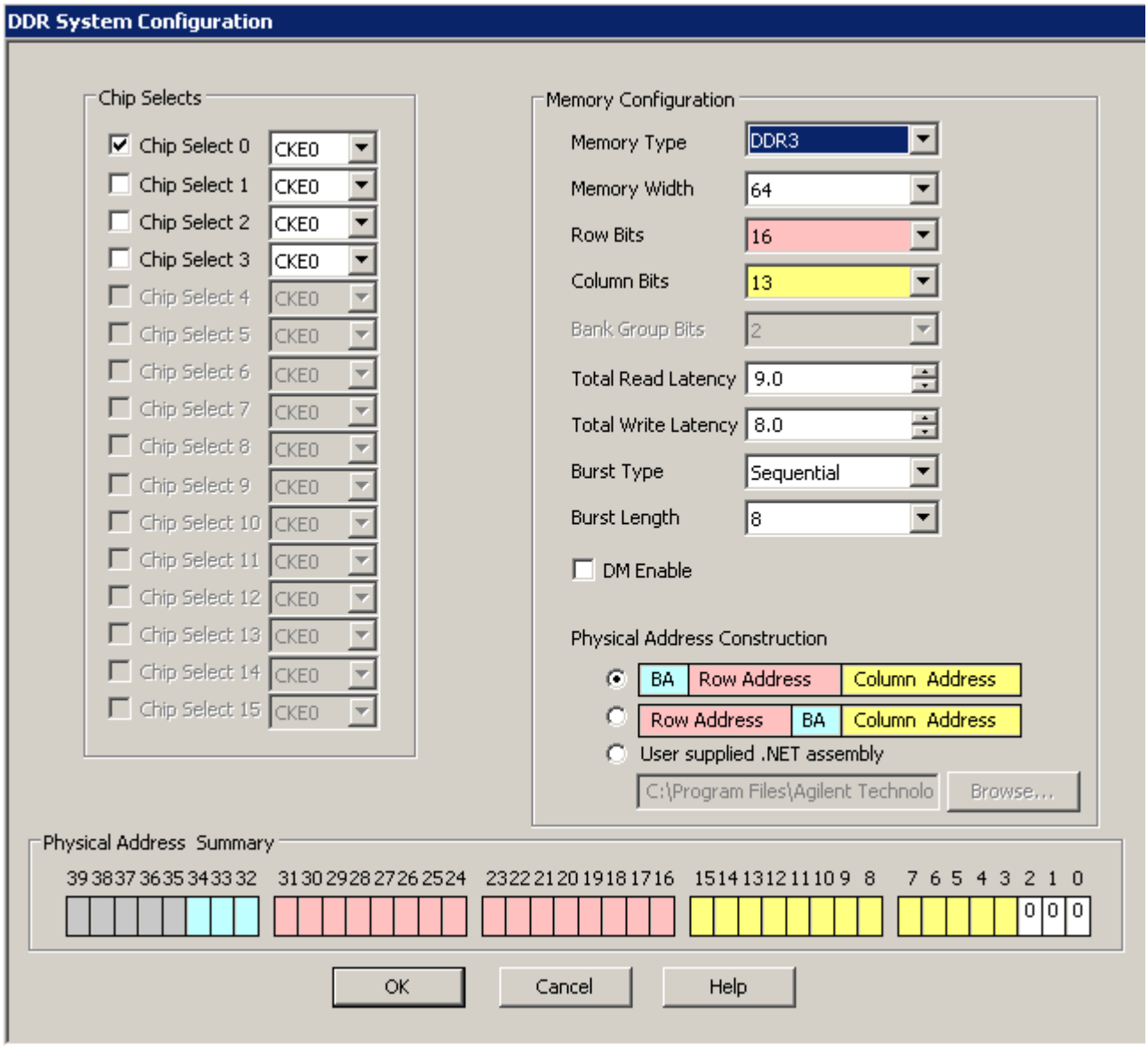
To set the device under test's latency and burst values in the DDR Bus Decoder:

1 In the *Agilent Logic and Protocol Analyzer* application, click the **Overview** tab (or the System Overview icon) to view the Overview window.

2 In the DDR Bus Decoder tool (in the Tools column), click the **Properties** button and choose **System Configuration**.



The **System Configuration** dialog is displayed.



3 In the **System Configuration** dialog, enter or select:

- The appropriate **Chip Select** and **CKE** for the device under test.
- **Total Read Latency**(or **Read Offset**in some decoders) — Enter the total Read latency value recorded earlier.
- **Total Write Latency**(or **Write Offset**in some decoders) — Enter the total Write latency value recorded earlier.

NOTE

The latency values that you specify in the System Configuration dialog represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.

- **Burst Type**— Enter the Burst type value recorded earlier.
- **Burst Length**— Enter the Burst length value recorded earlier.

4 Click **OK**.

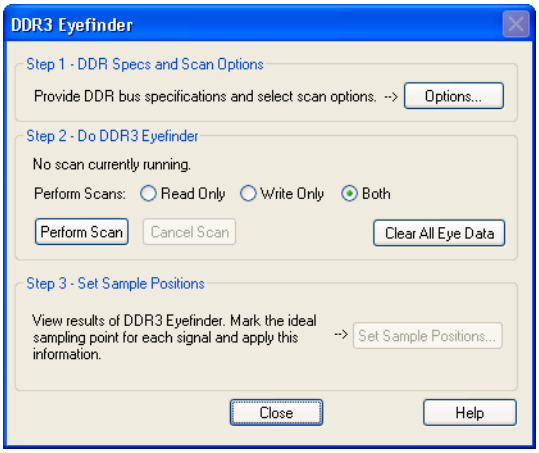
Setting Latency Values in DDR3 Eyefinder

To set the device under test's latency and burst values in DDR3 Eyefinder:

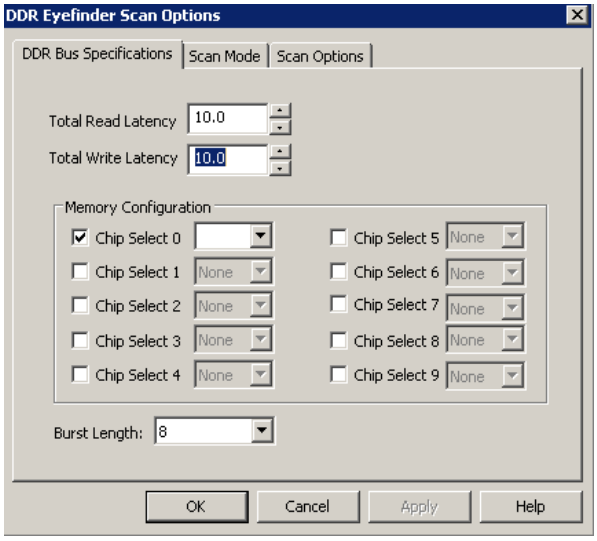
1 In the *Agilent Logic and Protocol Analyzer* application, click the **Overview** tab (or the System Overview icon) to view the Overview window.

2 In the DDR3 Eyefinder probe (in the column on the left), click the **Eyefinder** button.

3 In the DDR3 Eyefinder dialog, click **Options...**.



4 In the DDR3 Eyefinder Scan Options dialog's DDR Bus Specifications tab, enter or select:



- **Total Read Latency**— Enter the total read latency value recorded earlier.
- **Total Write Latency**— Enter the total Write latency value recorded earlier.

NOTE

The latency values that you specify in the DDR3 Eyefinder represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.

- **Memory Configuration**— Choose the appropriate Chip Select(s) for the memory path being traced.
- **Burst Length**— Enter the Burst length value recorded earlier.

5 Click **OK**.

Setting Latency Values in Eyescan

When using the U4154A Logic Analyzer module, you can modify the device under test's latency and burst values in Eyescan. The Eyescan feature of U4154A displays the default latency values or the latency values that you initially set using the DDR Setup Assistant tool. If required, you can modify these values for subsequent eyescan runs.

To modify the latency and burst values using the Eyescan feature:

1 In the Agilent Logic and Protocol Analyzer application, click the Overview tab (or the System Overview icon) to view the Overview window.

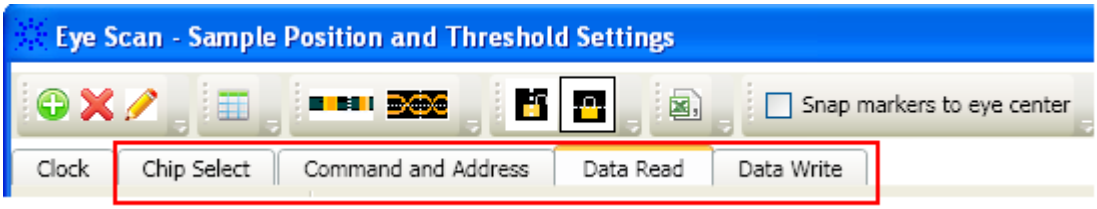
2 Click the **Sampling Setup** icon in the U4154A logical module displayed under the Modules column in the Overview window.

The **Sampling** tab of the **Analyzer Setup** dialog box is displayed.

3 Click the **Eye Scan: Sample Positions and Thresholds...** button.

The **Eye Scan - Sample Position and Threshold Settings** dialog box is displayed.

4 In the **Eye Scan - Sample Position and Threshold Settings** dialog box, select the tab for **Chip Select**, **Command and Address**, **Data Read** or **Data Write** to modify the scan qualification for the appropriate signals.



5 Click the **Edit Current Measurement** toolbar button.

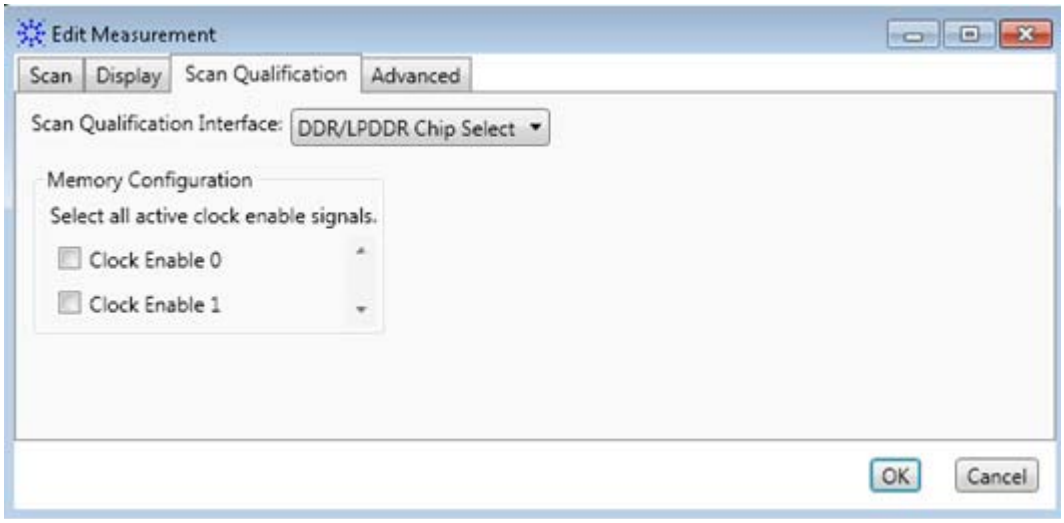
The **Edit Measurement** dialog box is displayed.

6 Click the **Scan Qualification** tab in this dialog box.

7 Based on the signals tab you selected in step 4, the options are displayed in the Scan qualification interface listbox. Select one of the following options from this listbox:

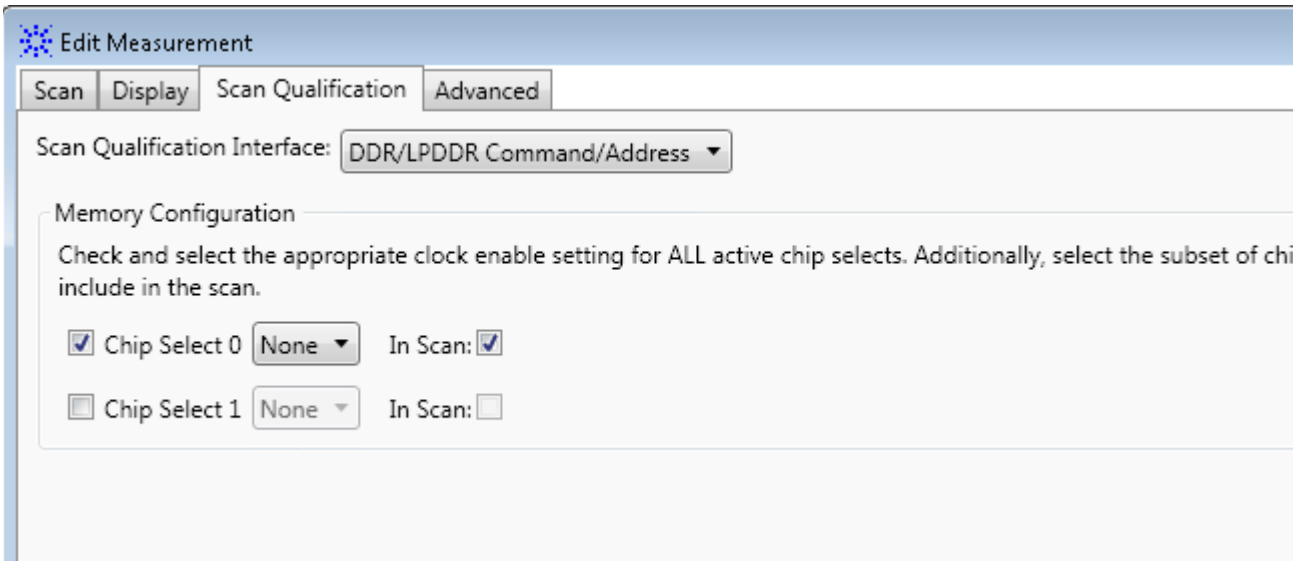
- DDR/LPDDR Chip Select option - to modify the scan qualification for chip select signals.
- DDR/LPDDR Command and Address option - to modify the scan qualification for command and address signals.
- DDR Data Read option - to modify the scan qualification for data read signals.
- DDR Data Write option - to modify the scan qualification for data write signals.

On selecting the DDR/LPDDR Chip Select option in the previous step, the following fields are displayed for chip select scan qualification:



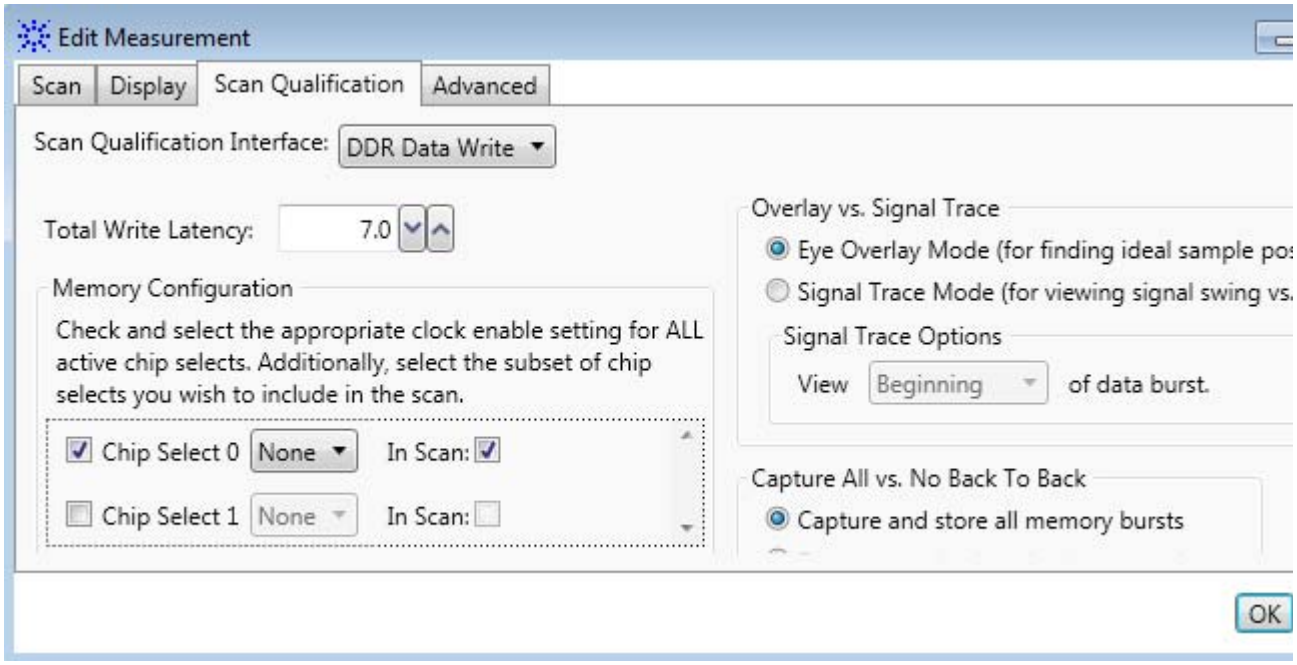
8 For the DDR/LPDDR Chip Select signals, make the appropriate selections based on the active clock enable signals.

On selecting the DDR/LPDDR Command and Address option in the step 7, the following fields are displayed for scan qualification:



9 For the DDR/LPDDR Command and Address signals, make the appropriate Memory Configuration selections based on the chip selects used in the DUT.

On selecting the **DDR/LPDDR Data Read** or **Data Write** interface in step 7, the following fields are displayed for scan qualification:



10 For DDR Data Read or Write signals:

g The DUT's Total Read/Write Latency value that you set up in the initial DDR setup is displayed. If needed, modify this value. To find an appropriate value of Total Read/Write Latency, you can set up the Mode Register Settings (MRS) trigger, take a trace, and scan it for latency values.

NOTE

The latency values specified here represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.

h In the **Memory Configuration** section, choose the appropriate Chip Select(s) for the memory path being traced.

i In the **Burst Length** field, specify the number of words read or written for each read/write command. To find appropriate value of Burst Length for the DUT, you can set up the Mode Register Settings (MRS) trigger, take a trace, and scan it for burst length.

11 Click **OK** to confirm the settings.

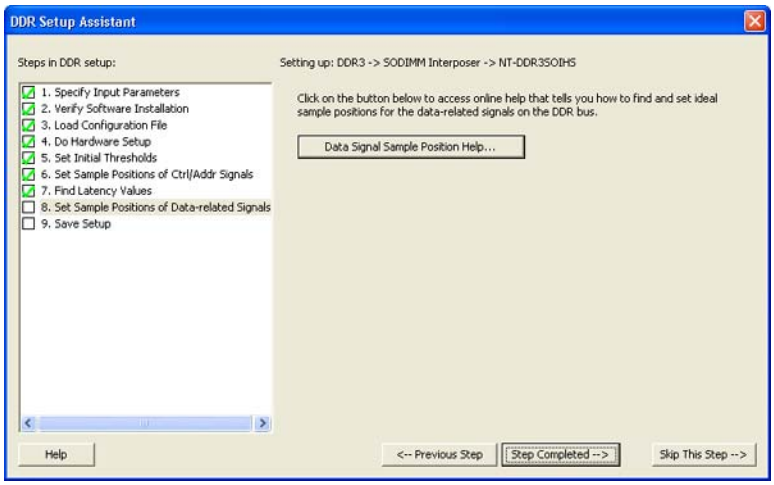
You can save the modified latency and burst values in the Logic Analyzer .ala or .xml configuration file.

Step - Set Sample Positions of Data-related Signals (not applicable to U4154A logic analyzer)

In this step, you set the sample positions of Data signals.

- With the 16960A or 16962A logic analyzers, use DDR3 Eyefinder to set the sample positions of data signals. See "Your First DDR3 Eyefinder Scan (16962A logic analyzers only)" on page 76.
- With the 16950A/B or 16951B logic analyzers, use the logic analyzer's *timing zoom* feature to set the sample positions of data signals. See Appendix A, "Setting Data Sample Positions with the 1695x Logic Analyzers," starting on page 115.

This step is not applicable to U4154A Logic Analyzer module. For setting the sample positions of Data signals when using the U4154A module, refer to the topic "Step - Set Sample Positions of Data Read/Write (only applicable to U4154A Logic Analyzer)" on page 61.



After setting the sample positions of Data signals, click **Step Completed -->**.

Next

- "Step - Save Setup" on page 65

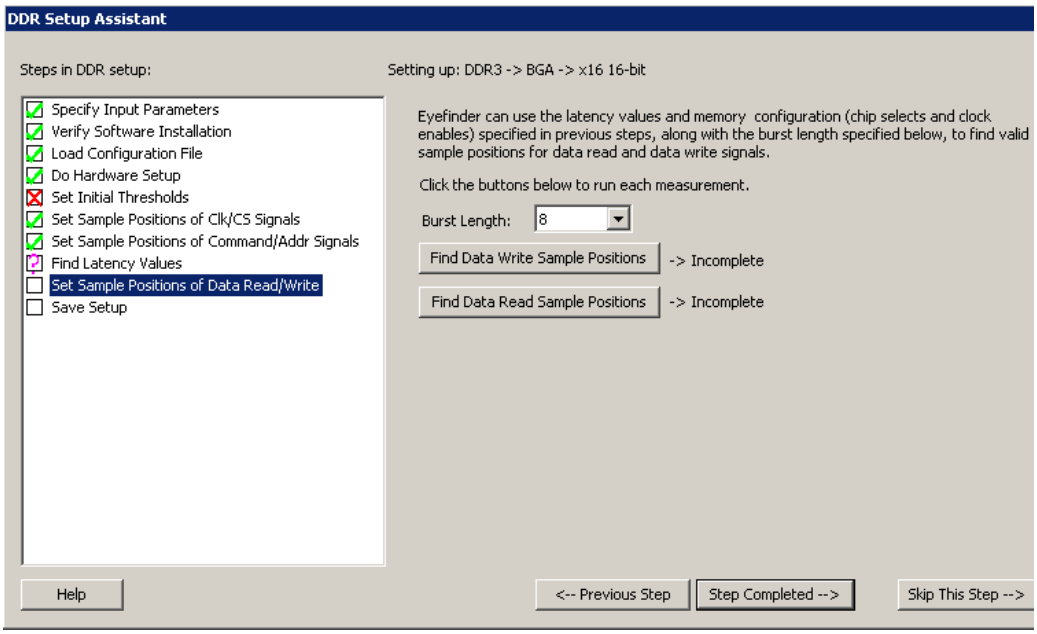
Step - Set Sample Positions of Data Read/Write (only applicable to U4154A Logic Analyzer)

In this step, you set the sample positions of Data signals when using the U4154A Logic Analyzer module.

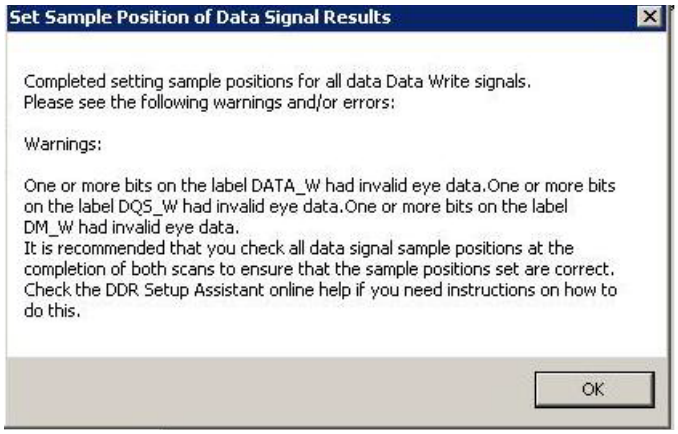
NOTE The fields displayed in this step differ if you selected DDR4 bus type in step 1. Therefore, the procedure for setting sample positions for DDR4 Data signals is described separately in this topic.

For this step, DDR Setup Assistant runs the eyescan feature of the U4154A Logic Analyzer module to automatically calculate and set the optimal sample positions for the data signals.

- Click **Find Data Write Sample Positions** to find the optimal and valid sample positions for the data write signals.
- Click **Find Data Read Sample Positions** to find the optimal and valid sample positions for the data read signals.

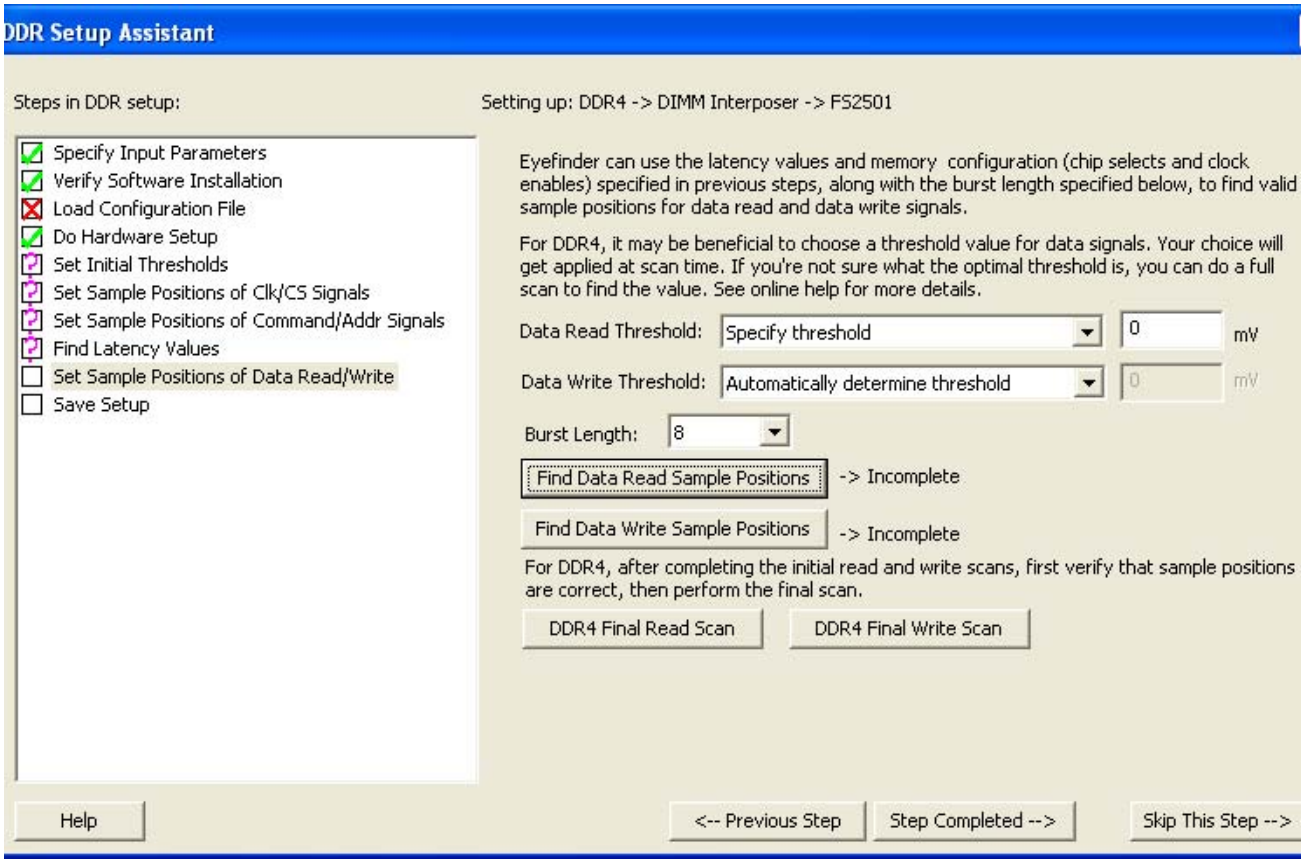


If the eyescan run completes but gives you warnings, you should check the warnings and re-run the eyescan in this step.



After setting the sample positions of Data signals, click Step Completed -->.

To find and set sample positions for DDR4 Data related signals



1 Set the threshold for DDR4 data read and write signals. You can set the threshold in either of the following two ways:

- From the **Data Read Threshold** and **Data Write Threshold** listboxes, select the **Automatically determine threshold** option to let DDR Setup Assistant automatically determine the best threshold setting. The middle of the signal swing is used in this case.
- From the **Data Read Threshold** and **Data Write Threshold** listboxes, select the **Specify threshold** option to manually specify the threshold value. This is particularly useful in case of DDR4 signals for which the automatically determined threshold value may not be an ideal threshold to use.

  If you selected to manually specify the threshold value for DDR4 data signals, you can determine the best threshold setting by performing the following steps:

  i Access the already open Logic and Protocol Analyzer application. To do this, you need to cancel the "Panel Lock" dialog displayed by DDR Setup Assistant.

  ii Open the **Setup** dialog box of the logic analyzer module.

  iii Click the **Sampling** tab.

  iv Click the **Eye Scan: Sample Positions and Thresholds** button

  v Click the **Data Read** measurement tab.

  vi Click **Edit Current Measurement** toolbar button and then select **Do full time/voltage scan** in the **Scan** tab.

  vii Click **OK**.

  viii Run the eyescan measurement by clicking **Run this measurement**.

  ix View the eyescan results to decide which threshold is likely to result in the best eye openings. Note down the threshold value. If required, you can unlock the threshold settings to move the threshold marker.

  x Click the **Data Write** measurement tab.

  xi Repeat steps vi- ix to view threshold for the Data Write measurement.

  xii Once you have noted down the threshold that would result in best eye openings, click **Cancel** to cancel the Eye scan - Sample Positions and Threshold Settings dialog.

  xiii Click **Cancel** again to cancel the Analyzer Setup dialog.

  xiv Access the already open DDR Setup Assistant and specify the obtained threshold values in the **Data Read Threshold** and **Data Write Threshold** fields.

2 Select the **Burst Length**.

3 Click **Find Data Read Sample Positions** to find the optimal and valid sample positions for the data read signals based on the specified threshold settings.

4 Click **Find Data Write Sample Positions** to find the optimal and valid sample positions for the data write signals based on the specified threshold settings.

5 Once you have verified that the obtained sample positions for DDR4 data read and write signals are correct, perform a final scan. You perform a final scan by clicking the **DDR4 Final Read Scan** and **DDR4 Final Write Scan** buttons.

   A final scan is a comparatively shorter scan than a main scan and is used to perform a final setting to fine tune the obtained sample positions. A final scan verifies that the sample positions are optimal not just for the first bit but for all 8 bits in the burst.

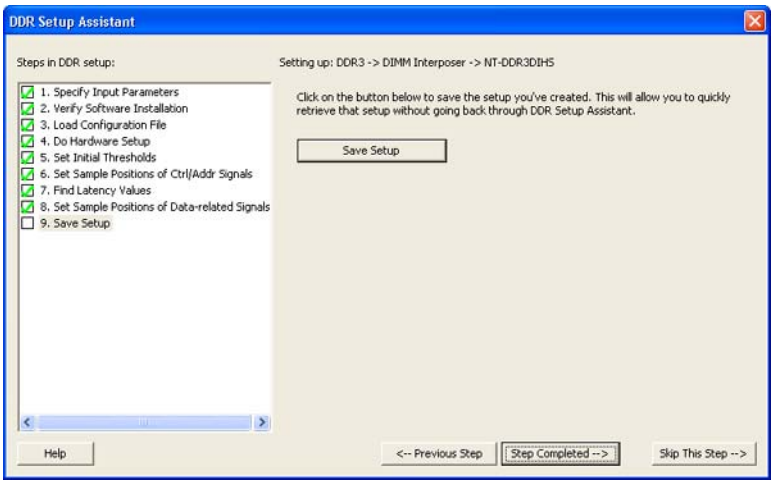
   Based on the fine tuning needed, a final scan may result in only a minor change or no change at all to the sample positions.

Next "Step - Save Setup" on page 65

Step - Save Setup

In this step, save your logic analyzer setup so that it can be opened later without having to perform the DDR Setup Assistant steps again..

1 Click **Save Setup**.



2 In the Save Setup dialog, browse to the location where you want to save the setup file, enter the file name, and click **Save**.

3 In the message dialog that says the setup was saved successfully, click **OK**.

4 Click **OK**.

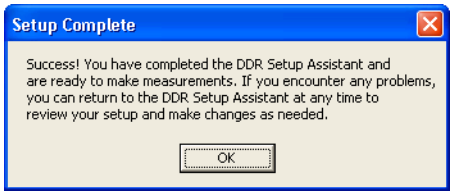
After saving the configuration, click **Step Completed -->**.

Next

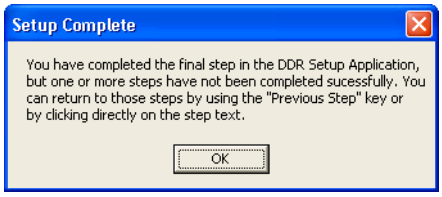
- "Setup Complete" on page 66

Setup Complete

After clicking **Step Completed -->** in the last step of the DDR Setup Assistant, you get a Setup Complete message.



The Setup Complete mesasge will tell you if any of the steps still need to be completed.



When the DDR setup is complete, you can use the DDR bus decoder and other tools to analyze captured data.

See Also

- Chapter 4, “Setting Up Thresholds and Sample Positions on DDR Address/Control Signals,” starting on page 67
- Chapter 5, “Using DDR3 Eyefinder,” starting on page 75
- Chapter 7, “Validating the DDR Setup,” starting on page 107
- Chapter 8, “Capturing Data (Triggering),” starting on page 109
- Chapter 9, “Decoding Captured Data,” starting on page 113

4 Setting Up Thresholds and Sample Positions on DDR Address/Control Signals

The Thresholds and Sample Positions dialog in the *Agilent Logic Analyzer* application's sampling setup tab (also known as normal logic analyzer *eye finder*), is used to set the sampling positions of the DDR address and control signals. This is necessary before DDR3 Eyefinder can be used to set the data signal sample positions on 16960A or 16962A logic analyzers.

For U4154A logic analyzer, the DDR Setup Assistant sets the sampling positions on DDR command, address, and data read and write signals using the U4154A eyescan feature. This feature is also available in the Agilent Logic Analyzer application. You can also set the threshold and sample positions on individual channels of U4154A using the Eye Scan - Sample positions and Threshold Settings dialog box accessible by clicking the Eye scan: Sample Positions and threshold button in the Sampling tab of the Setup dialog box.

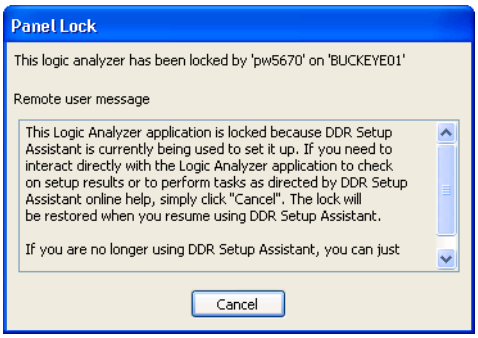
The DDR Setup Assistant runs the Thresholds and Sample Positions set up for you; however, it may run into some problems that require you to open and re-run the set up.

Setting Up Thresholds and Sample Positions

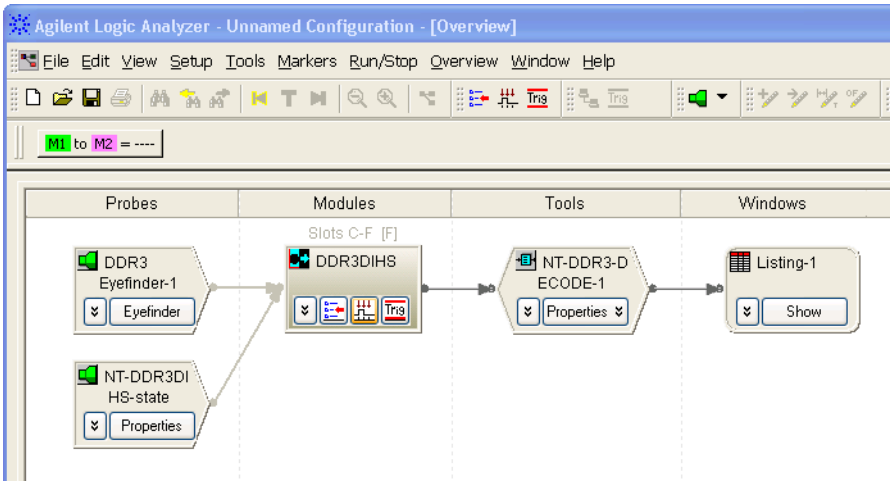
The Thresholds and Sample Positions set up (also known as normal logic analyzer *eye finder*) is used to set the sampling positions of the DDR address and control signals. This is necessary before DDR3 Eyefinder can be used to set the data signal sample positions (on 16962A and 16960A logic analyzers).

1 Go to the *Agilent Logic Analyzer* application.

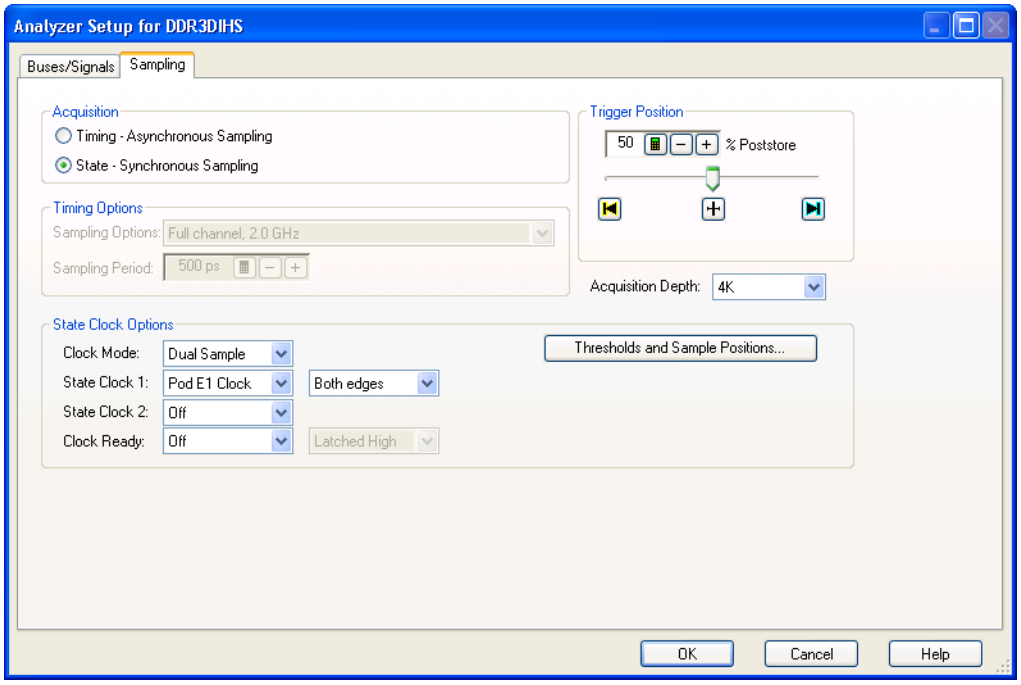
2 If you are currently using the DDR Setup Assistant, you may have to click **Cancel** in the Panel Lock dialog.



3 In the *Agilent Logic Analyzer* application, click the Sampling Setup icon.



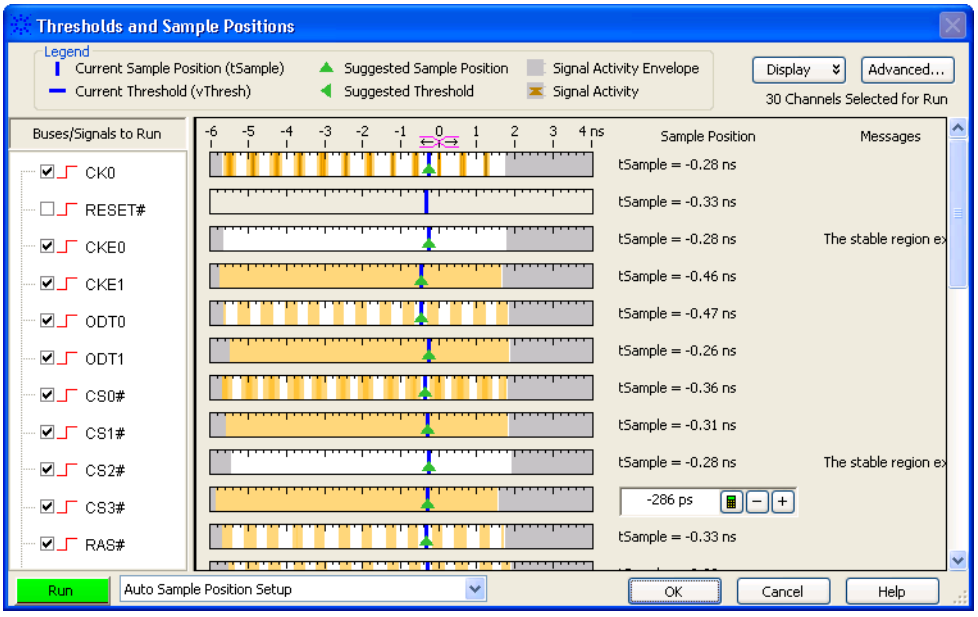
4 In the Sampling Setup dialog, click **Thresholds and Sample Positions...**.

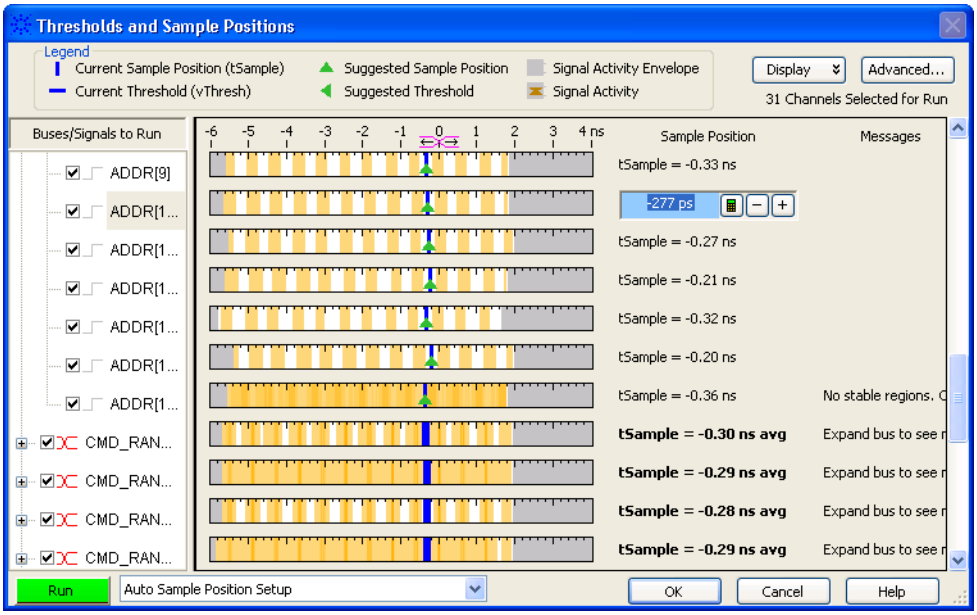


5 In the Thresholds and Sample Positions dialog, make sure the address and control signal sample positions are aligned.

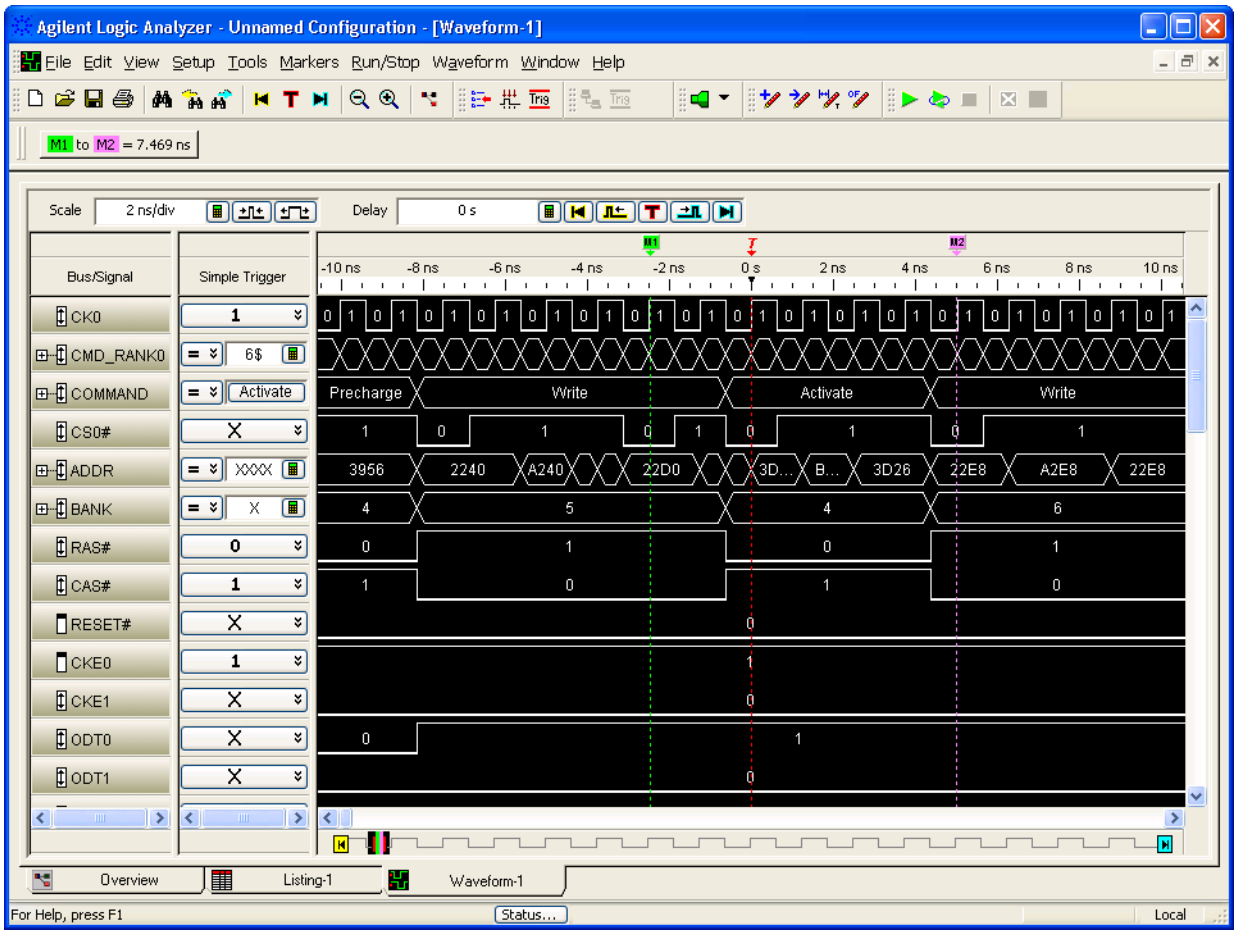
6 If necessary, click **Run** to rerun the Thresholds and Sample Positions set up.

The resulting sampling positions should be aligned and just left of zero (0).





7 Take a trace to ensure that Command, CK, BANK, and ADDR are sampled correctly.



Because we are sampling on both the rising and falling edges of CK, you want to check that the rising edge of CK must be in the middle of CS# low.

Solving Problems with Thresholds and Sample Positions Set Up

No eye finder or eye scan eyes for Address and Command

Possible Cause:	Possible Solution:
The DDR device under test's power saving mode allows Address and Control signals to float when CKE is low.	Try these steps: **1** To verify the issue: **a** In Timing mode, trigger on CKE = low. **b** Check if the Address and Command signals appear to be tri-stated while CKE=low, that is, there are rapid changes in signals during CKE=low relative to activity during CKE=high. **2** Disable Power saving mode in target BIOS until sample positions are set. **3** Or Clock Ready set to Enable High.
With 2T signaling, Address is only valid while CS# is low.	• Set Sample positions for Address/Ctrl to same position as CS#.

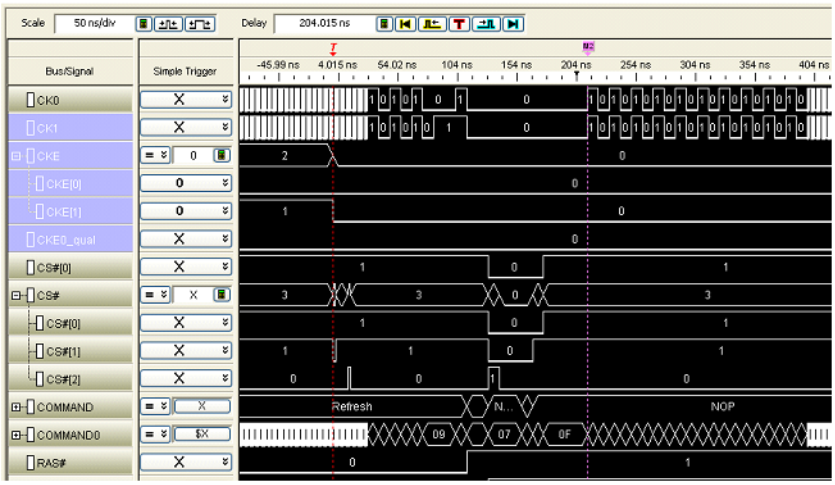
Clock edges "too close together" error message on Run

Possible causes and solutions:

Possible Cause:	Possible Solution:
Poor signal integrity on clock signal.	Check the clock signal quality by sampling the signal in timing mode, by using the logic analyzer Thresholds and Sample Positions set up in state mode, or by using an oscilloscope.

Possible Cause:	Possible Solution:
You are attempting to take a trace from reset.	In the sampling setup, set Clock Ready to latch high on CKE0.
Power management (clocks tri-state).	Try these steps: **1** To verify the issue, in timing mode, Trigger on both CKE = low. Check if the clock appears to stop or tri-state when both CKEs are low. **2** Change the CK0 threshold voltage setting from "differential" to 50 mV. This helps prevent the Clock edge error message as CK0 fluctuates at 0 V during tri-state. **3** Or, disable Power Management mode in target BIOS. **4** Or, use Clock Ready set to Enable High. (For older interposers, this works for single rank DIMMs if used on Dual Rank DIMMs. Some data from CKE1 rank could be lost when CKE0 is low when CKE1 isn't low. Newer FuturePlus interposers OR the CKE0 and CKE1 signals which is good for Dual and Quad Rank DIMMs.) **5** Or, consider using the 4 GHz (250 ps) half channel timing mode on Addr/Ctrl signals for power management debug. You can also use the 8 GHz (125 ps) quarter channel timing mode, where E5386A adapters are typically used to reduce the number of probes and connectors required.

What to Expect if Clocks Tri-State



When CKE and CKE1 are both low – system entering self refresh - clocks will turn off.

When the clock tri-states, the Waveform display will be different:

- Time tags will be wrong for approximately 40 cycles before and after the clock tri-states.
- However, sampled data is accurate.
- The DDR Bus Decoder decodes self refresh and power down modes.

- It is best to view the Listing display in this situation.

5
Using DDR3 Eyefinder

DDR3 Eyefinder is similar to the logic analyzer Thresholds and Sample Positions set up (also known as normal logic analyzer *eye finder*) except that it is specifically designed to find DDR3 data signal eyes, given the relationship between DDR3 control/address signals and data signals. DDR3 Eyefinder also provides additional features to help you locate data signal eyes and properly set sample positions, including the ability to analyze scan data using different scales, color schemes, and filtering.

NOTE

DDR3 Eyefinder can be used with the 16960A and 16962A logic analyzers. It cannot be used with the 16950A/B logic analyzers.

DDR3 Eyefinder is unable to perform threshold scans when used with the 16960A logic analyzer, and only time scans are available.

See Also

- Logic analyzer Thresholds and Sample Positions set up ("To automatically adjust state sampling positions and threshold voltages" (in the online help))

Getting Started with DDR3 Eyefinder (for 16962A/16960A)

Before Running DDR3 Eyefinder

Before running DDR3 Eyefinder, you must set the sample positions for the control/address signals using the DDR Setup Assistant (see Chapter 3, “Using the DDR Setup Assistant,” starting on page 33) or the logic analyzer Thresholds and Sample Positions set up (also known as normal logic analyzer *eyefinder*, see "To automatically adjust state sampling positions and threshold voltages" (in the online help)).

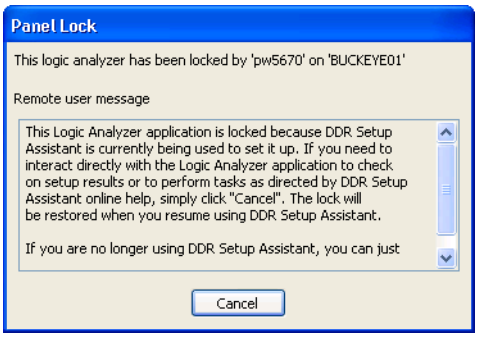
After setting the control/address signal sample positions, you can set up and run DDR3 Eyefinder scans.

Your First DDR3 Eyefinder Scan (16962A logic analyzers only)

We recommend your first DDR3 Eyefinder scan be a "threshold" scan to give you a good first picture of the signal eyes and proper sampling positions. This type of scan can take about an hour to complete, but the results are worthwhile.

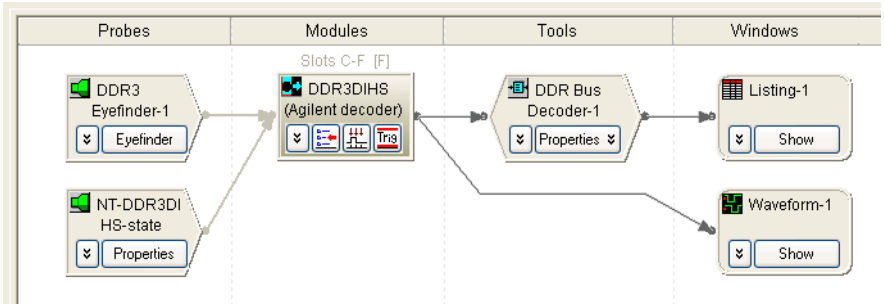
1 Go to the *Agilent Logic Analyzer* application.

2 If you are using the DDR Setup Assistant, you may have to click **Cancel** in the Panel Lock dialog.

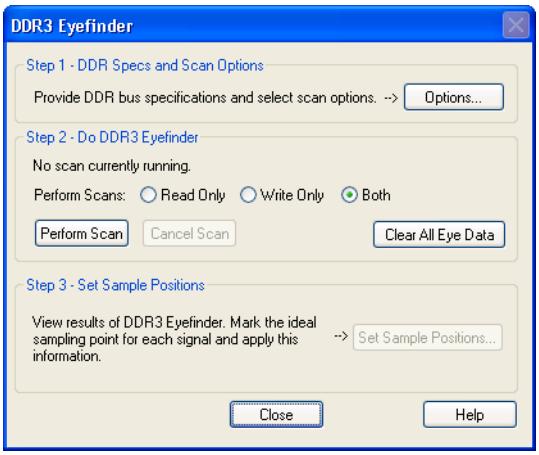


3 In the *Agilent Logic Analyzer* application, click the **Overview** tab (or the System Overview icon) to view the Overview window.

4 In the DDR3 Eyefinder probe (in the column on the left), click the **Eyefinder** button.

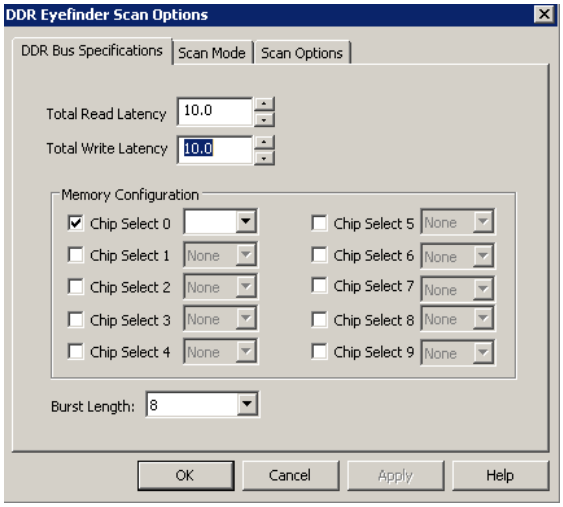


5 In the DDR3 Eyefinder dialog, first provide the scan values:



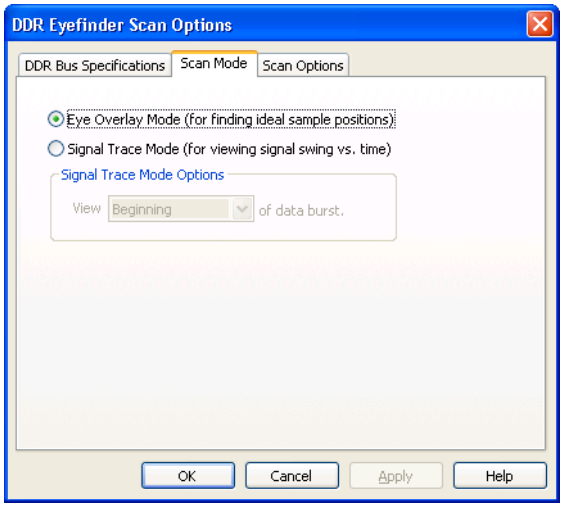
a Click **Options...**.

b In the DDR Eyefinder Scan Options dialog's DDR Bus Specifications tab, enter the appropriate **Total Read Latency**, **Total Write Latency**, **Memory Configuration**, and **Burst Length** values.

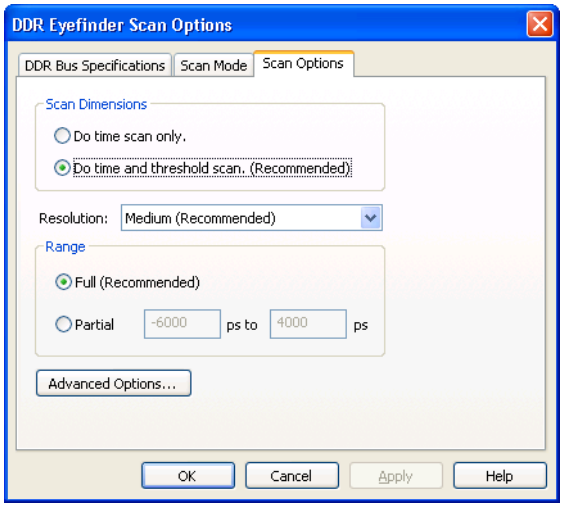


If you do not know the appropriate values for your device under test, you can find the appropriate scan values using an Mode Register Settings (MRS) trigger as described in "Step - Find Latency Values" on page 49 and "Setting Latency Values in DDR3 Eyefinder" on page 55.

c In the **Scan Mode** tab, use the recommended settings (eye overlay mode).



d In the **Scan Options** tab, use the recommended settings (time and threshold scan, medium resolution, and full range).

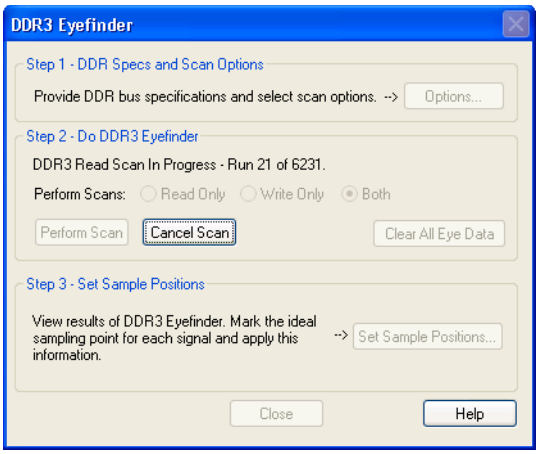


e Click **OK** to save the scan values/options and close the dialog.

For more information on setting scan values and options, see "Setting Scan Options" on page 87.

6 Back in the DDR3 Eyefinder dialog, select **Both** read and write scans; then, click **Perform Scan** to run DDR3 Eyefinder scan.

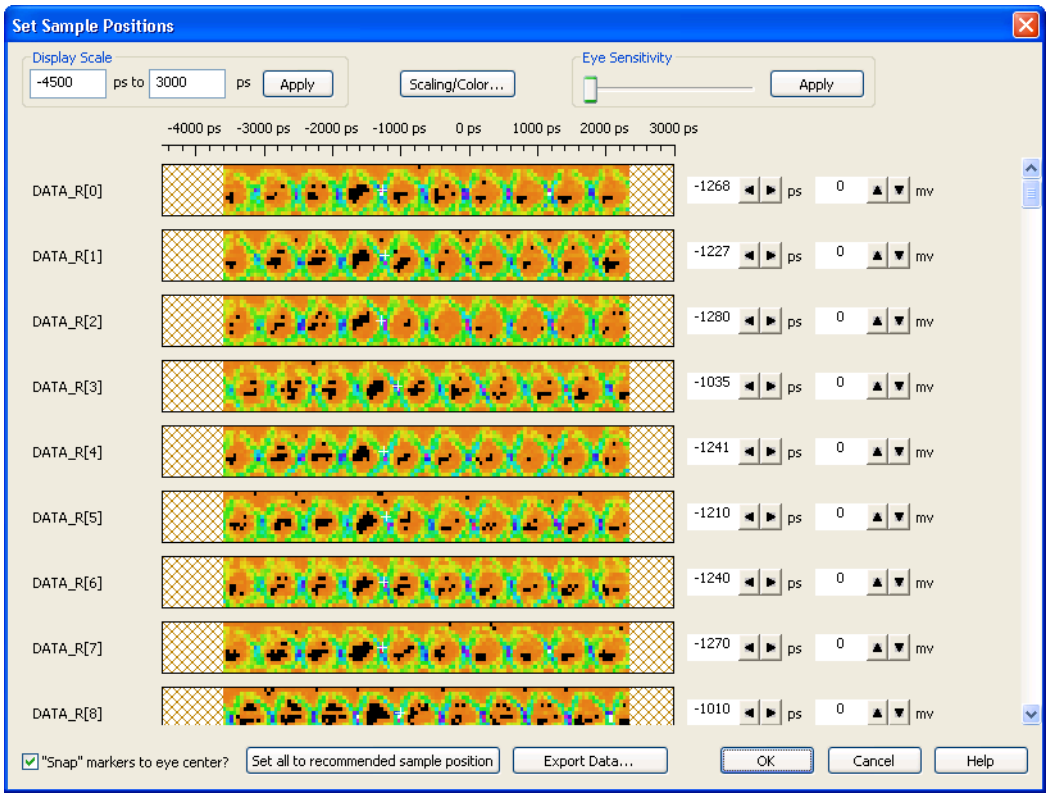
As configured in the previous steps, the scan takes over an hour to complete. The DDR3 Eyefinder run status is shown in the dialog.



For more information on performing scans, see "Performing Scans" on page 93.

7 After the read and write scans complete, click **Set Sample Positions...** to view the scan results and set the sample positions.

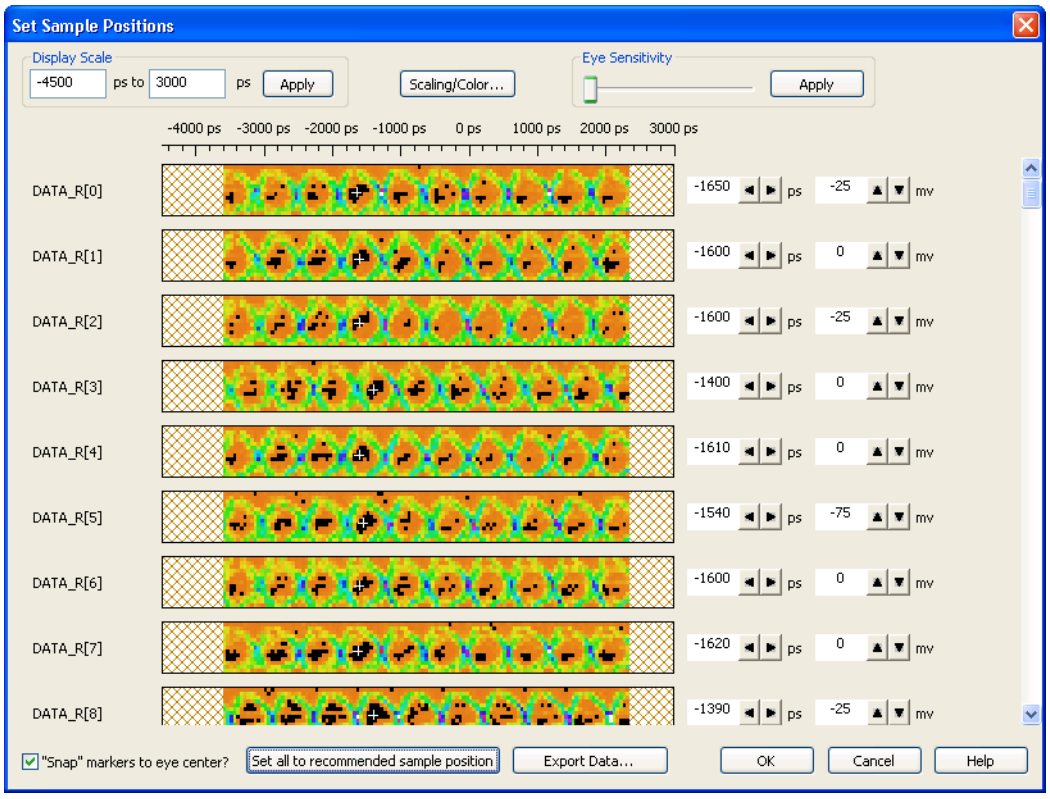
8 In the Set Sample Positions dialog:



a Click **Set all to recommended sample position**.

The white crosshair markers show the recommended sample positions (see the following example).

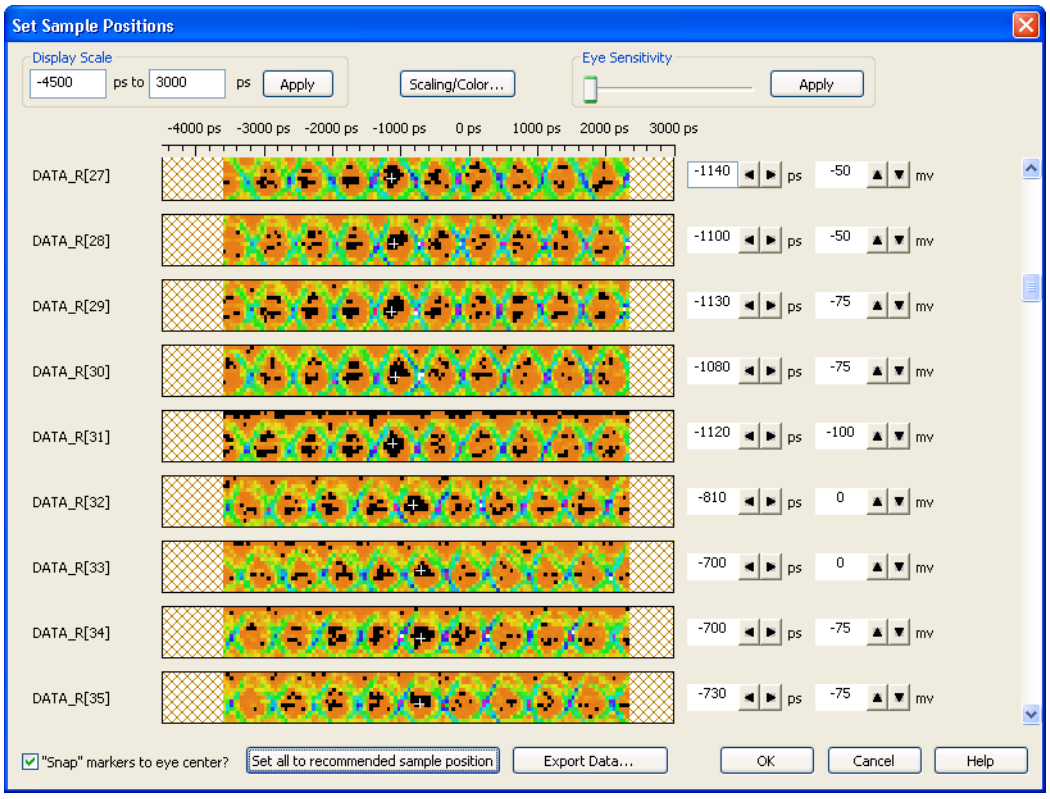
CAUTION Recommended sample positions might be at incomplete eyes nearest the last sample position settings. Always visually inspect the results of setting all to the recommended sample positions (see the next step).



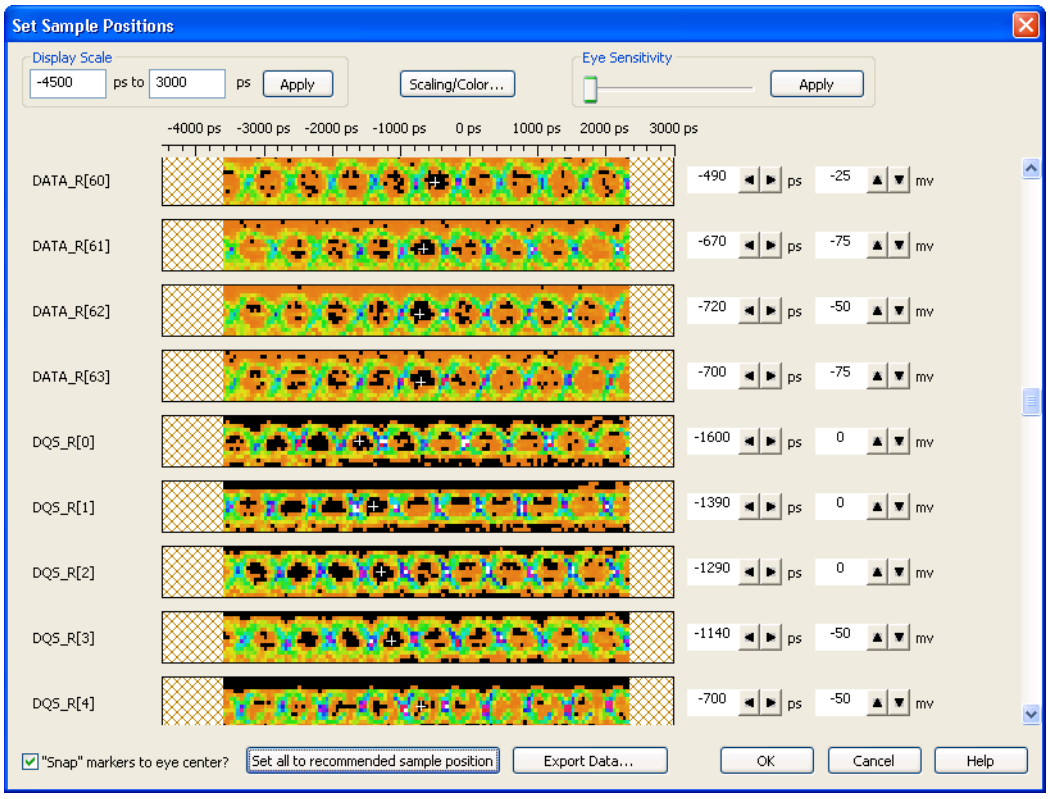
b Scroll though the signals and adjust sample positions as necessary. You can uncheck the **"Snap" markers to eye center?** option for greater control over the sample position placement.

- Single-click to move to center of suggested eyes.
- When there is only one obvious eye, pick that eye.
- If there are problems, see "Solving DDR3 Eyefinder Problems" on page 100.

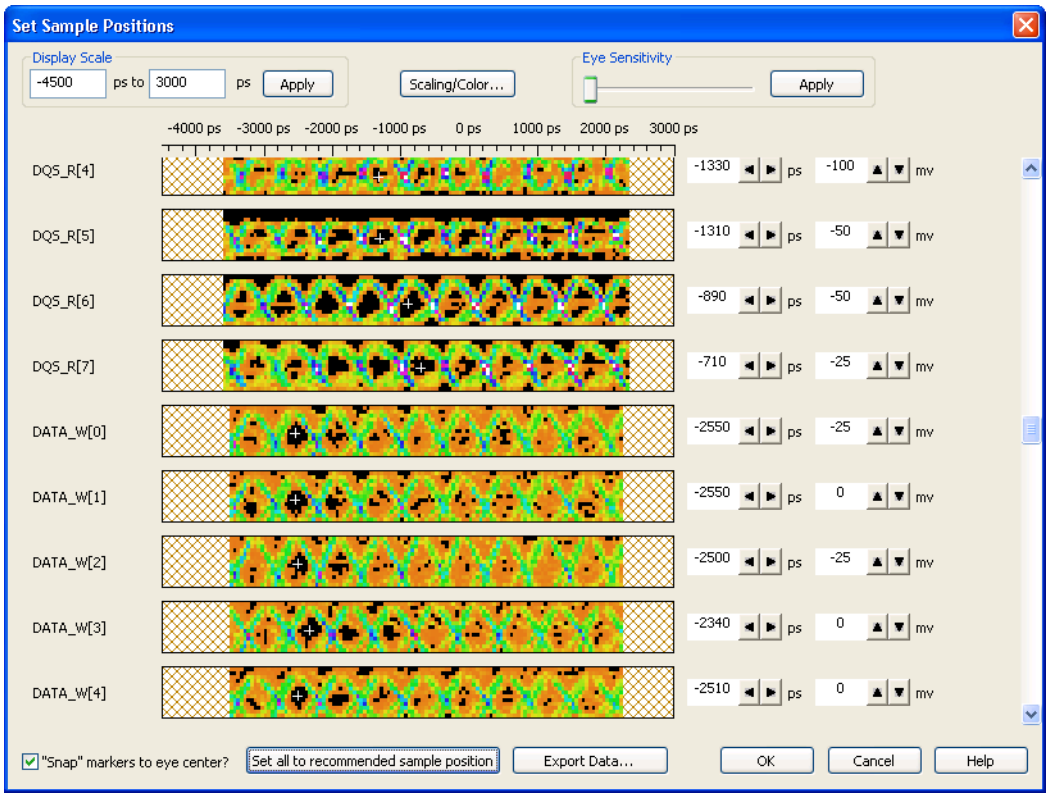
Take note of the eye positions for each group of eight signals. You may notice *byte shifts* on eight bit boundaries as shown in the following example.



It's important to note the eye positions for each byte lane (set of eight signals) because the strobe signal eyes are roughly at the same position as the corresponding byte lane. Knowing this can help you select the correct eyes for the strobe signals. The following example shows strobe eye position differences.

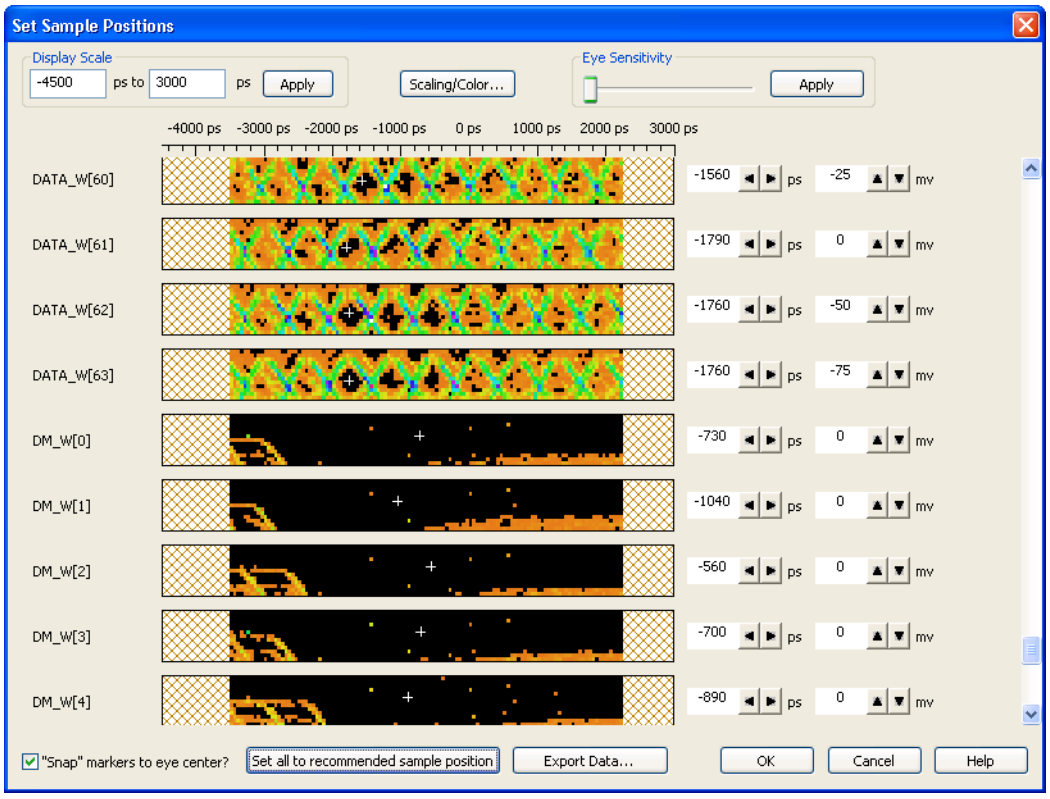


Data write signal eyes appear in different positions than data read signal eyes, as shown in the following example.

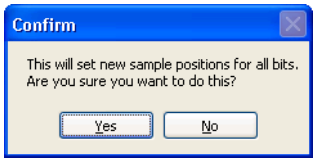


Sometimes for data read or write signals, two eyes appear. You can use the **Do not store back-to-back memory bursts** advanced scan option to prevent this (see "Setting Advanced Scan Options" on page 91). Higher resolution scans will also help clear up uncertainties.

You may notice signals that are not used, as in the following example.



c When you are done setting sample positions, click **OK**. Then, click **Yes** in the confirmation dialog.



d In the message dialog that says the sample positions have been successfully applied, click **OK**.

9 Click **Close** to close the DDR3 Eyefinder dialog.

If you are running the DDR Setup Assistant, you have completed "Step - Set Sample Positions of Data-related Signals (not applicable to U4154A logic analyzer)" on page 60. Return to the DDR Setup Assistant, and continue with "Step - Save Setup" on page 65.

After running DDR3 Eyefinder to set sample positions for read and write signals, you are ready to capture DDR3 traces with the logic analyzer.

See Also

- "Setting Scan Options" on page 87
- "Performing Scans" on page 93

- "Setting Sample Positions" on page 94
- "Solving DDR3 Eyefinder Problems" on page 100

Setting Scan Options

The first step in using DDR3 Eyefinder is to set the scan values and options. In the DDR Eyefinder Scan Options dialog, there are tabs fo

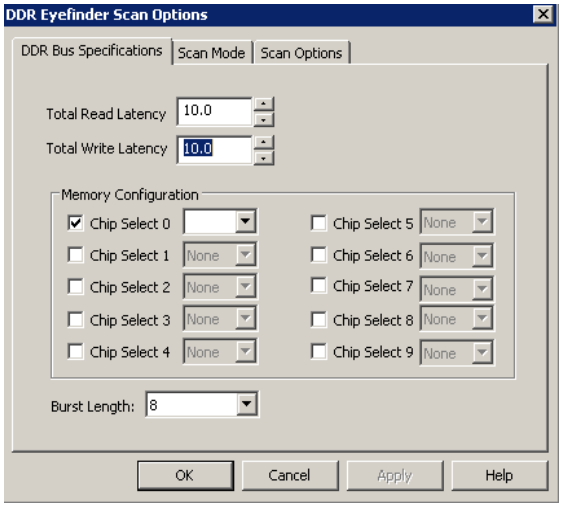
- "Setting DDR Bus Specifications" on page 87
- "Setting Scan Options" on page 89
- "Setting Scan Mode" on page 88

There is also a dialog for:

- "Setting Advanced Scan Options" on page 91

Setting DDR Bus Specifications

In the DDR Eyefinder Scan Options dialog's DDR Bus Specifications tab, you enter the basic characteristics of the DDR bus.



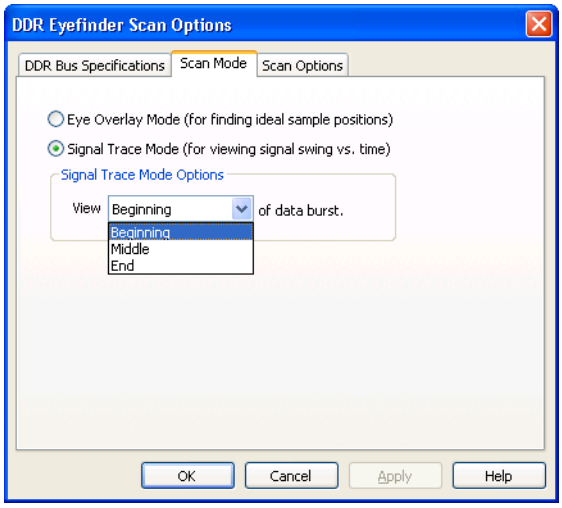
Total Read Latency	The total number of clock cycles from the valid Read command to valid data.
Total Write Latency	The total number of clock cycles from the valid Write command to valid data.
Note: The latency values that you specify here represent the total latency for your system and therefore should include parameters that affect total latency. For instance, if your system has Additive Latency (AL), then you must include it in the Total Latency values. Similarly, if tDQSS or tDQSCK parameters are greater than one full clock cycle, then you must add these values (rounded to the nearest integer) in the Total Latency values.	

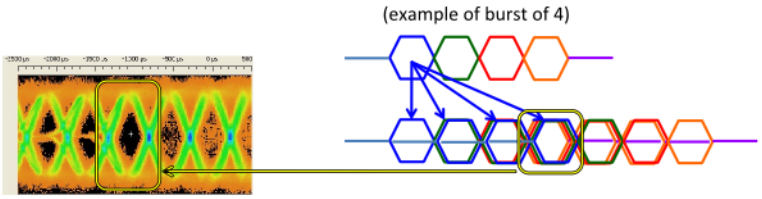
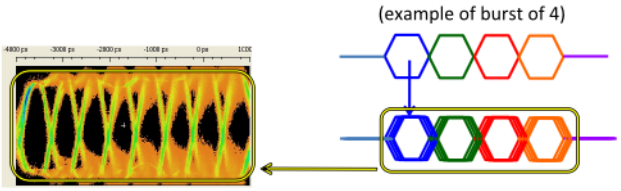
Memory Configuration	Make the appropriate **Memory Configuration** selections based on the chip selects used in the device under test.
Burst Length	This is the number of words read or written for each read/write command.

You can find the appropriate values for **Total Read Latency**, **Total Write Latency**, and **Burst Length** using an Mode Register Settings (MRS) trigger as described in "Step - Find Latency Values" on page 49 and "Setting Latency Values in DDR3 Eyefinder" on page 55.

Setting Scan Mode

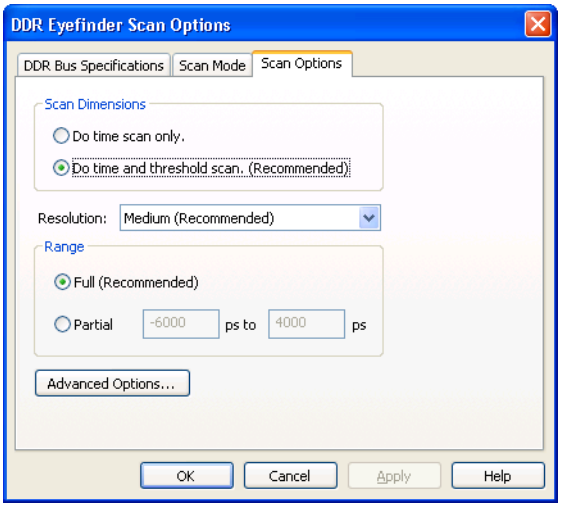
In the DDR Eyefinder Scan Options dialog's Scan Mode tab, you can specify the scan mode.



Eye Overlay Mode	Use this mode when setting sample positions for data signals. In this mode, DDR3 Eyefinder overlays the eyes for each bit in a burst in order to show a composite eye, without tri-state or noise, that helps you locate the best sample position. **Eye Overlay Mode: Overlaying each bit of 4, 8, or 16 bursts on top of each other** 
Signal Trace Mode	Use this mode for viewing signal swing vs. time. Although sample positions can be checked and modified in this mode, it is generally not recommended. In this mode, DDR3 Eyefinder overlays complete bursts in order to provide additional qualitative insight into the signal integrity on the DDR system at the logic analyzer probe location. **Signal Trace Mode: Overlaying multiple captures of 4, 8, or 16 bursts on top of each other**  When the Signal Trace Mode is selected, you can select from these data burst areas to view: • **Beginning**— Scans are made at the beginning of a data burst. • **Middle**— Scans are made at the middle of the data burst. • **End**— Scans are made at the end of the data burst. For more information, see "Viewing Signal Swing vs. Time" on page 99.

Setting Scan Options

In the DDR Eyefinder Scan Options dialog's Scan Options tab, you can specify the scan type, the scan resolution, and the scan range.



Scan Type	Time scans divide the sample position time range into "buckets". During the scan, many samples are taken at different signal delay settings (and one threshold voltage), and the number of signal transitions that occur in the buckets is recorded. When the scan completes, buckets that have a greater number of transitions are colored brighter or with more intensity than buckets with fewer transitions. Buckets with no transitions have no color. This gives you a picture of where signal crossing points occur and can tell you where to set sample positions. Time scans are done at a single threshold voltage setting and provide the fastest scan for setting sample positions. Time and threshold scans divide time buckets vertically into voltage range buckets. During the scan, different threshold voltage settings are used as well as different delay settings. The scan results show more signal detail and help you better identify eyes and proper sampling positions. Threshold scans take longer because they scan voltages as well as time.

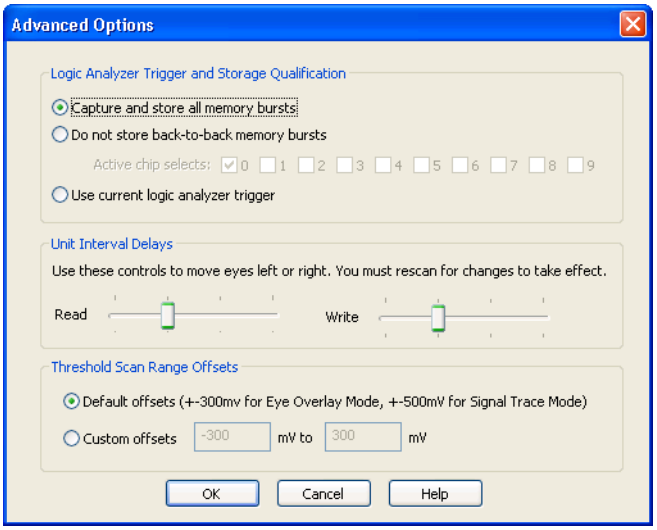
Resolution	You can select from these resolutions: • **Ultra Fine (Slowest)**— 5 ps time, 5 mV threshold resolution — uses the most buckets, and the scan takes longest to run. • **Fine**— 10 ps time, 10 mV threshold resolution — uses many buckets, and the scan takes longer to run. • **Medium-Fine**— 25 ps time, 20 mV threshold resolution — uses setting between Fine and Medium. • **Medium (Recommended)**— 50 ps time, 50 mV threshold resolution — uses an intermediate number of buckets and results in an intermediate scan time. • **Coarse (Fastest)**— 50 ps time, 75 mV threshold resolution — uses fewer buckets, and scans complete in a shorter amount of time.
Range	Full performs the scan over the full sample position time range. Partial lets you narrow the time range and perform faster scans. However, be careful when changing these values. If you scan too short a time range, you could miss the proper signal eyes. Generally, you use this option when there is a portion of a signal you want to view in more detail and you want to shorten the time it takes the scan to run.

See Also

• "Setting Advanced Scan Options" on page 91

Setting Advanced Scan Options

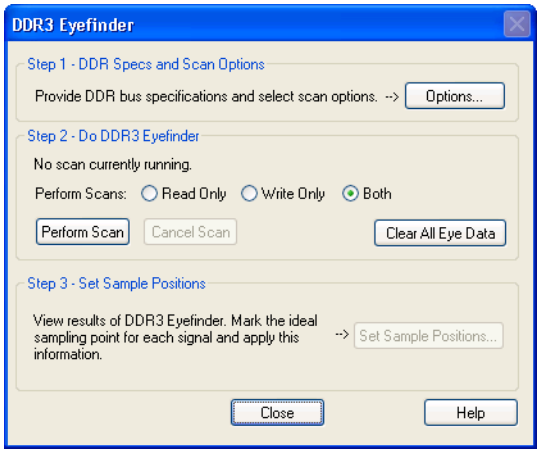
In the DDR Eyefinder Scan Options dialog's Scan Options tab, you can click **Advanced Options...** to change advanced scan options.



Logic Analyzer Trigger and Storage Qualification	Capture and store all memory bursts — this is the default setting. Do not store back-to-back memory bursts — you can use this to eliminate the "double eye" effect in scan results. Use current logic analyzer trigger — this lets you further customize the samples that are used in scans.
Unit Interval Delays	If the eyes in which you want to set the sampling position are outside of the adjustment range, you can use these "coarse delay" adjustments to move the signals left or right (in relation to the zero time) by Unit Interval (clock cycle) amounts. It is unlikely that you will have to change the unit interval delays when using the proper configuration files and Total Read Latency and Total Write Latency settings. After making coarse delay adjustments, you must rescan and set the sampling positions again. **Background:** There are two ways to move the DDR3 Eyefinder display window and scan the appropriate location for the Read and Write data valid windows: **1** By adjusting the Total Read Latency setting for the Read eyes and Total Write Latency for the Write eyes. See "Setting DDR Bus Specifications" on page 87. **2** By adjusting the Unit Interval Delays sliders. In the extreme right position, the delay is zero between the qualified clock edge and the data. Each mark to the left represents a whole clock cycle. The Unit Interval Delays sliders are usually used only for two scenarios: • When setting up a new configuration for a new probe or embedded midbus application where delays from the routing require adjustment in the DDR3 Eyefinder display. • When adjusting for significant changes in the data rate compared to the range of the specification for a specific configuration. For instance, most DDR3 probes are set up expecting DDR 3 800-1600. Moving the slider to the left results in the data eyes moving left in the display after rerunning a scan. If the slider is all the way to the right and the data eyes need to move further to the right, reduce the Total Read Latency and Total Write Latency settings in the DDR3 Eyefinder tool. Once you determine the correct Latency settings to capture the data eyes, use the same latency values in the DDR Bus Decoder.
Threshold Scan Range Offsets	Lets you specify a custom vertical range to use for threshold scans. This option lets you either: • See a portion of a signal in more detail (and shorten the scan time). • See more of the signal swing (and lengthen the scan time). Note that the default offsets are different depending on the selected Scan Mode.

Performing Scans

When performing DDR3 Eyefinder scans, you can perform read only scans or write only scans, you can cancel scans, and you can clear eye data.



To run scans

1 Click **Perform Scan** to start a scan using the currently set options (see "Setting Scan Options" on page 87).

To select Read Only, Write Only, or Both read and write scans

- If you are only interested in setting the sample positions of data read or data write signals, you can choose **Read Only** or **Write Only**.

To cancel a scan

1 Click **Cancel Scan** to stop a currently running scan.

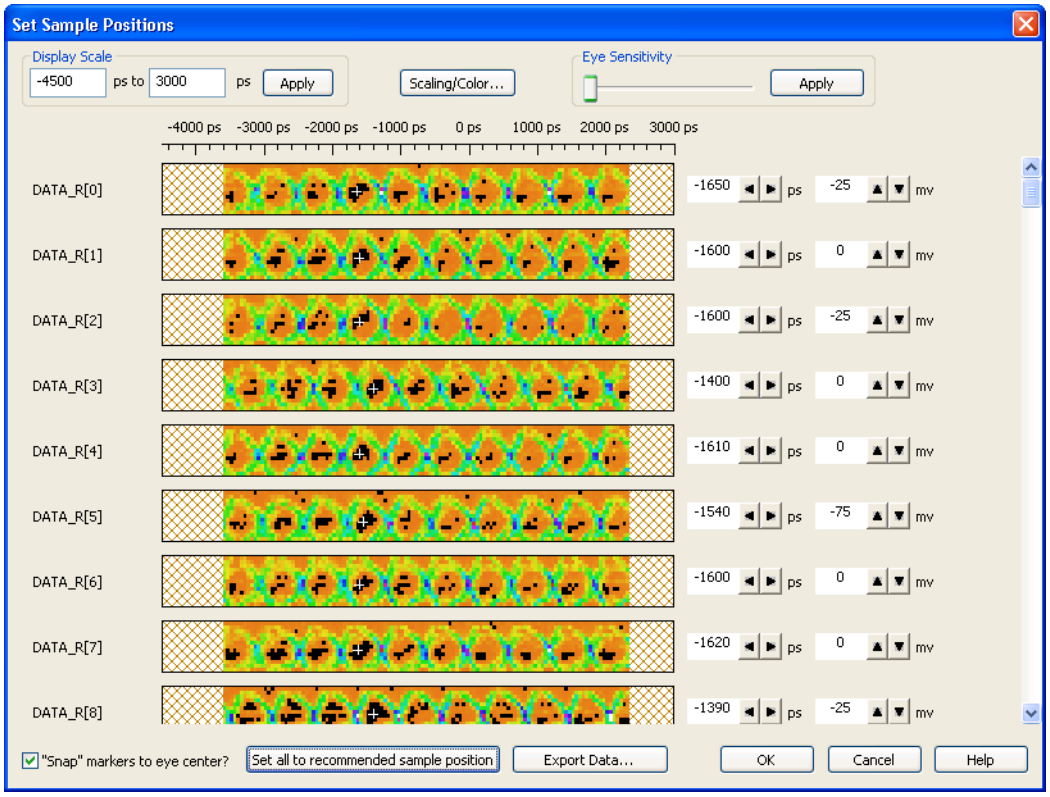
To clear all eye data

1 Click **Clear All Eye Data** to clear all DDR3 Eyefinder scan data.

Setting Sample Positions

After performing DDR3 Eyefinder scans, when setting sample positions, you can change the display settings to help identify the proper eye locations, and you can adjust the recommended sample positions.

To do this, click **Set Sample Positions...** in the DDR3 Eyefinder dialog. This opens the Set Sample Positions dialog.



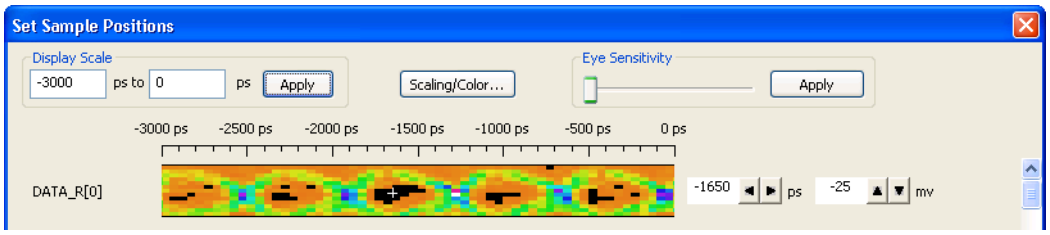
The Set Sample Positions dialog gives you these capabilities:

- "Adjusting the Display Scale" on page 95
- "Changing the Time Bucket Scaling and Colors" on page 95
- "Adjusting the Eye Sensitivity" on page 97
- "Adjusting Sample Positions" on page 98

The **Export Data...**button lets you export the underlying eye scan data to a CSV format file that can be imported into Microsoft Excel or other data visualization tools. For more information on the format of the exported CSV data, please contact your local Agilent sales representative.

Adjusting the Display Scale

In the upper left corner of the Set Sample Positions dialog, there is a **Display Scale** box for adjusting the scale of the display. This lets you zoom in on a particular eye(s) or zoom out to the full scale of the data that was scanned. After you enter the desired values of the range, click **Apply**.

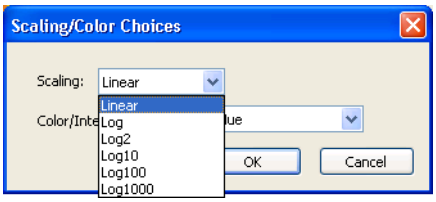


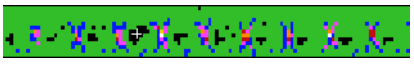
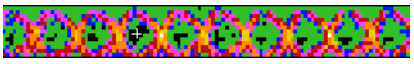
Changing the Time Bucket Scaling and Colors

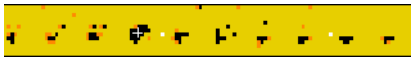
To change the time bucket scaling and color/intensity settings in the Set Sample Positions dialog:

1 Click **Scaling/Color...**.

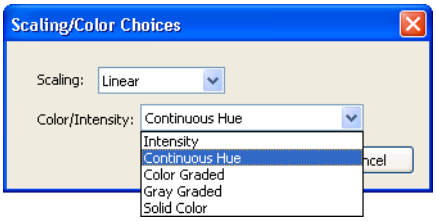
2 In the Scaling/Color Choices dialog, select the **Scaling** drop-down and choose the desired scaling:

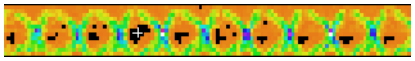


Scaling:	Example	Notes
Linear		(Color graded)
Log		(Color graded)
Log2		(Golor graded)

Scaling:	Example	Notes
Log10		(Color graded)
Log100		(Color graded)
Log1000		(Color graded)

3 In the Scaling/Color Choices dialog, select the **Color/Intensity** drop-down and choose the desired color scheme or intensity:



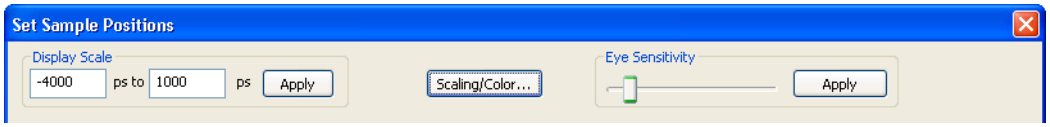
Color/Intensity:	Example	Notes
Intensity		(Linear scaling)
Continuous Hue		(Linear scaling) Continuous hue appears the same for all Log scales.
Color Graded		(Linear scaling)
Gray Graded		(Linear scaling)
Solid Color		(Linear scaling)

4 Click **OK** to make the scaling color change.

Adjusting the Eye Sensitivity

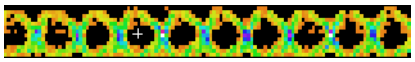
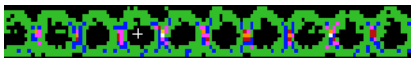
To adjust the eye sensitivity in the Set Sample Positions dialog:

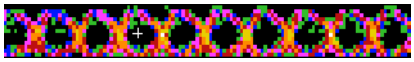
1 Drag the **Eye Sensitivity** slider; then, click **Apply**.



Changing the sensitivity does not affect any of the collected data, it just hides lower intensity values so that you can more easily identify the signal eyes.

Some examples of decreased sensitivity are shown in the following table.

Color/Intensity:	Example	Notes
Intensity		(Linear scaling, decreased sensitivity)
Continuous Hue		(Linear scaling, decreased sensitivity)
Color Graded		(Linear scaling, decreased sensitivity)
Gray Graded		(Linear scaling, decreased sensitivity)
Solid Color		(Linear scaling, decreased sensitivity)

Color/Intensity:	Example	Notes
Intensity		(Log2 scaling, decreased sensitivity)
Continuous Hue		(Log2 scaling, decreased sensitivity) Continuous hue appears the same for all Log scales.
Color Graded		(Log2 scaling, decreased sensitivity)
Gray Graded		(Log2 scaling, decreased sensitivity)
Solid Color		(Log2 scaling, decreased sensitivity)

Adjusting Sample Positions

In the Set Sample Positions dialog, you can do these things to adjust the sample positions:

- Click **Set all to recommended sample position**.

  The white crosshair markers show the recommended sample positions.

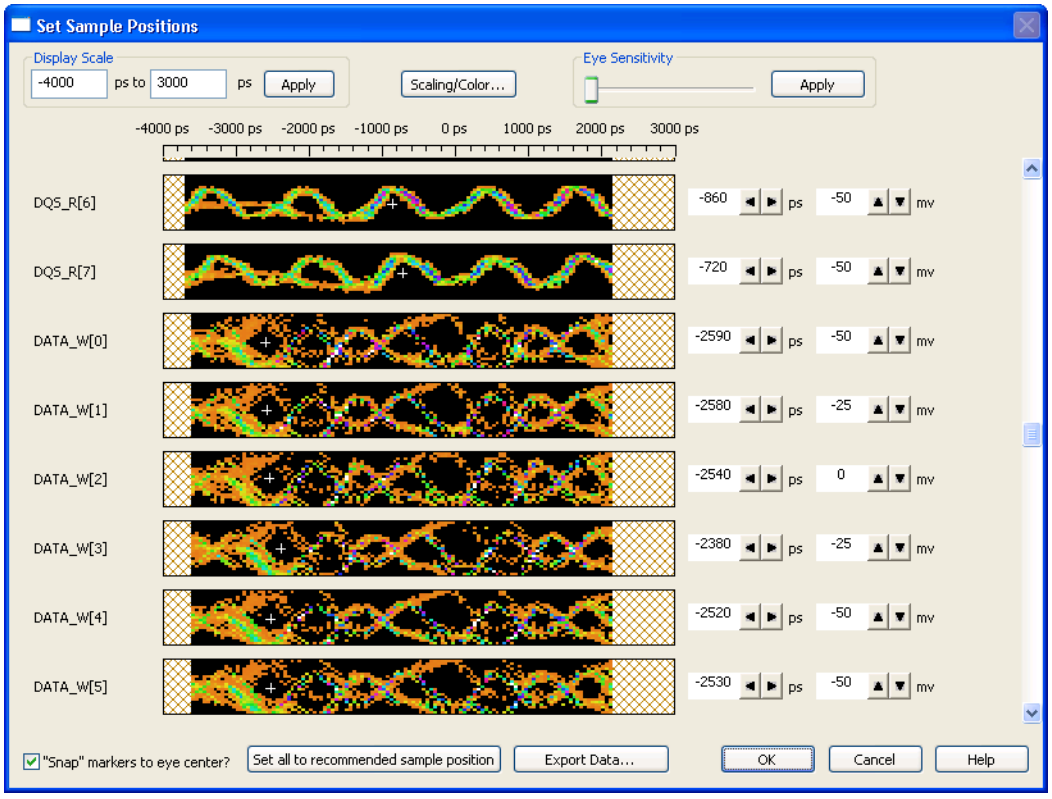
- Single-click to move to the center of suggested eyes.
- Uncheck the **"Snap" markers to eye center** option for greater control over the sample position placement.
- Use the fine controls to the right of the signal pictures.

Viewing Signal Swing vs. Time

If you have selected the Signal Trace Scan Mode (see "Setting Scan Mode" on page 88) and performed a scan (see "Performing Scans" on page 93), you can click **Set Sample Positions...** in the DDR3 Eyefinder dialog to view the signal swing vs. time. This view:

- Provides additional qualitative insight into the signal integrity on the DDR system at the logic analyzer probe location.
- Lets you check and modify sample positions although it is generally not recommended.
- Can show how the bits in a complete burst compare to one another.
- Can show how bursts from different byte lanes compare to one another.

For example, the following picture shows signal trace scan results at the beginning of an x8 data burst.



Solving DDR3 Eyefinder Problems

If you run into these problems, see:

If scans stick on Runs in DDR3 Eyefinder

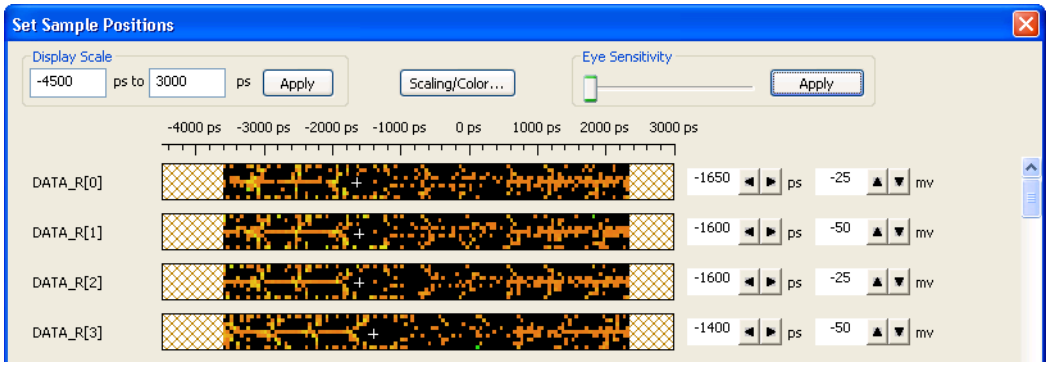
If scans stick on Runs in DDR3 Eyefinder, this means triggers are not happening in the logic analyzer. You can verify this by looking at the status in the *Agilent Logic Analyzer* application. If this is the case, cancel the scan and look for possible solutions.

Possible Solutions:

- Take a trace in the logic analyzer to make sure reads and writes are occurring.
- Make sure there is consistent memory traffic *on the channel you are probing*.

If there are no transitions in DDR3 Eyefinder

The following picture is of an example scan showing no transitions.

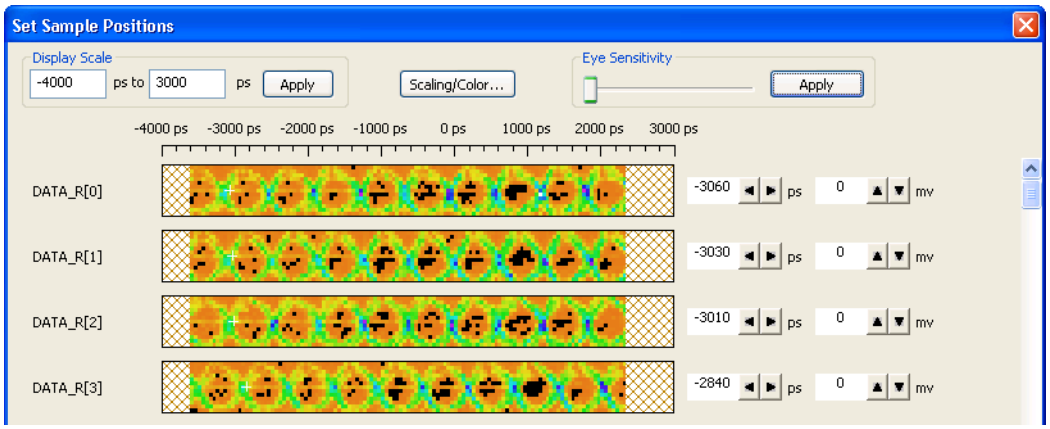


Possible Solutions: Take a trace and observe the data. If the data is not changing during the burst, then DDR3 Eyefinder will not show transitions.

Example: Entire burst is the same pattern. Resulting in no transitions in DDR3 Eyefinder.

If eyes show tri-stating

Horizontal lines through the middle of eyes show tristating, as in the following picture.

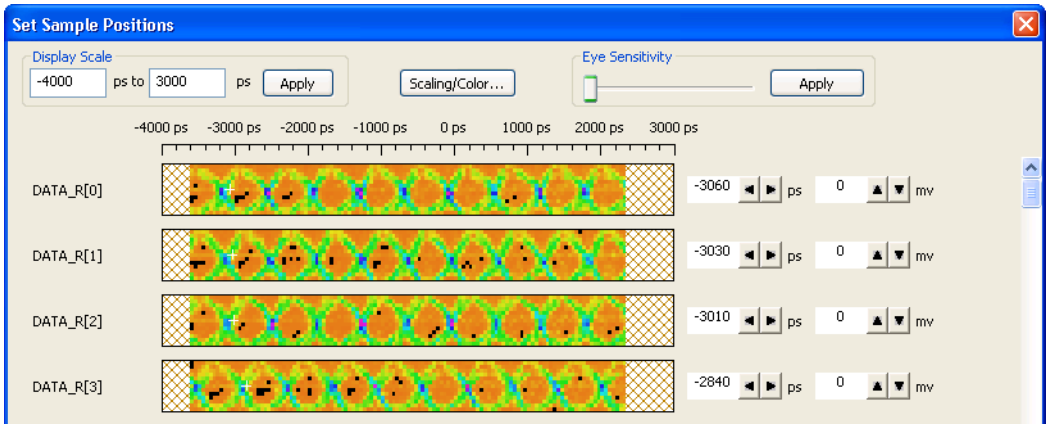


Possible Solutions:

- Check the Total Read Latency and Total Write Latency values in the DDR3 Eyefinder options dialog are correct.
- Adjust the Unit Interval Delays in the DDR3 Eyefinder advanced options dialog and re-run the scan.
- Make sure the clock signal is "clean" with crisp transitions.
- Make sure the Burst Length value in the DDR3 Eyefinder options dialog is not set too high (for example, set at 8 when the real burst length is 4).

If eyes are closed

The following picture is of an example scan showing closed or "noisy" eyes.



Possible Solutions:

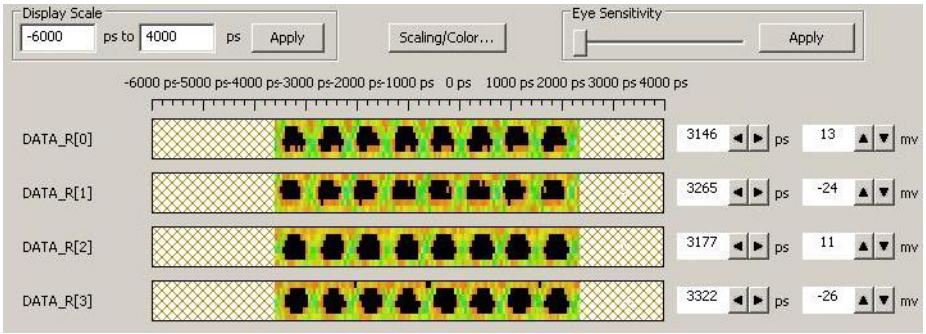
- Check the Total Read Latency and Total Write Latency values in the DDR3 Eyefinder options dialog are correct.
- Try adjusting the Eye Sensitivity slightly and click **Apply**. A slight adjustment of the sensitivity may help you identify the proper eye for setting the sample position.

CAUTION Be sure to reset the Eye Sensitivity after setting the sample position so that you are not hiding scan information for additional signals.

- Try scanning at the next finer setting, but stay within the **Medium** or **Medium-Fine** range. The **Fine** or **Ultra Fine** settings are generally not necessary for setting sample positions and they take much longer to run.
- Make sure the clock signal is "clean" with crisp transitions.
- Check the stimulus.
- Make sure the Burst Length value in the DDR3 Eyefinder options dialog is not set too high (for example, set at 8 when the real burst length is 4).

If there are multiple eyes

The following picture is of an example scan showing multiple eyes. In this case, it is hard to identify the proper eye in which to set the sample position.

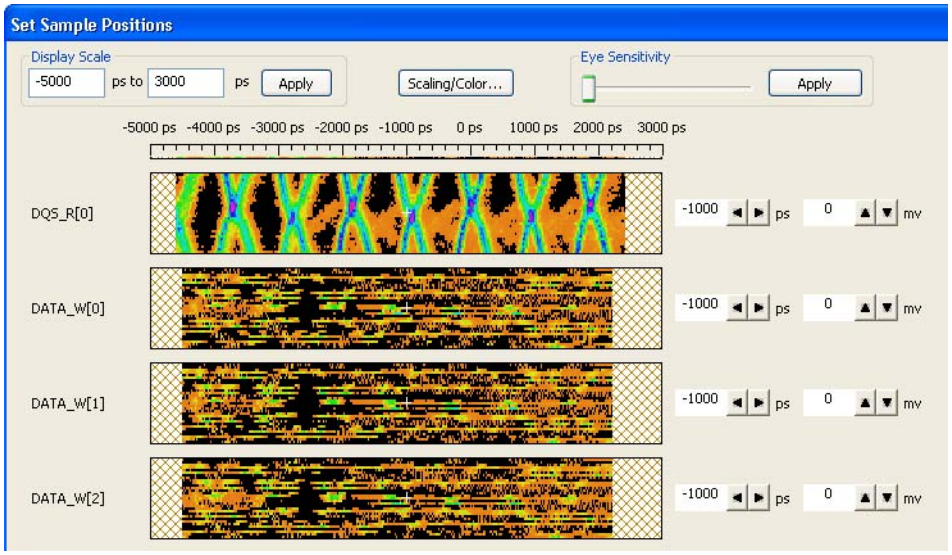


Possible Solutions:

- Make sure the Eye Sensitivity adjustment is not being used.
- Use the "Do not store back-to-back memory bursts" option (see "Setting Advanced Scan Options" on page 91).
- Try scanning at the next finer setting, but stay within the **Medium** or **Medium-Fine** range. The **Fine** or **Ultra Fine** settings are generally not necessary for setting sample positions and they take much longer to run.
- Specify a greater voltage scan range (Threshold Scan Range Offsets) in the DDR3 Eyefinder advanced options dialog and re-run the scan.
- Make sure the Burst Length value in the DDR3 Eyefinder options dialog is not set too low (for example, set at 4 when the real burst length is 8).
- Note that while byte lane eyes can shift, there are seldom shifts within byte lanes. Also, note that strobe eyes are aligned with the eyes of the signals in the corresponding byte lane.

If eye scan results are noisy

The following picture shows eyescan results that are noisy.



Possible Solutions:

- Make sure there are consistent memory reads and writes (see "Setting Up Read and Write Traffic in the DUT" on page 31). For example, these sort of results can occur when running multiple memory tests instead of a consistent memory test.
- Make sure the memory being tested is not switching to a different rank for a long periods of time.

6 Using Eyescan (for U4154A Logic Analyzer Module)

The Eyescan feature is used to set Thresholds and Sample Positions when using the U4154A Logic Analyzer module. Eyescan is used to perform general eyescans as well as to specifically find DDR data signal eyes. You can also use the Eyescan feature to customize DDR eyescans and to modify the scan qualification parameters that you initially set using the DDR Setup Assistant tool.

NOTE For 16960A and 16962A logic analyzers, you use the DDR3 Eyefinder tool to set thresholds and sample positions and find DDR3 data signal eyes.

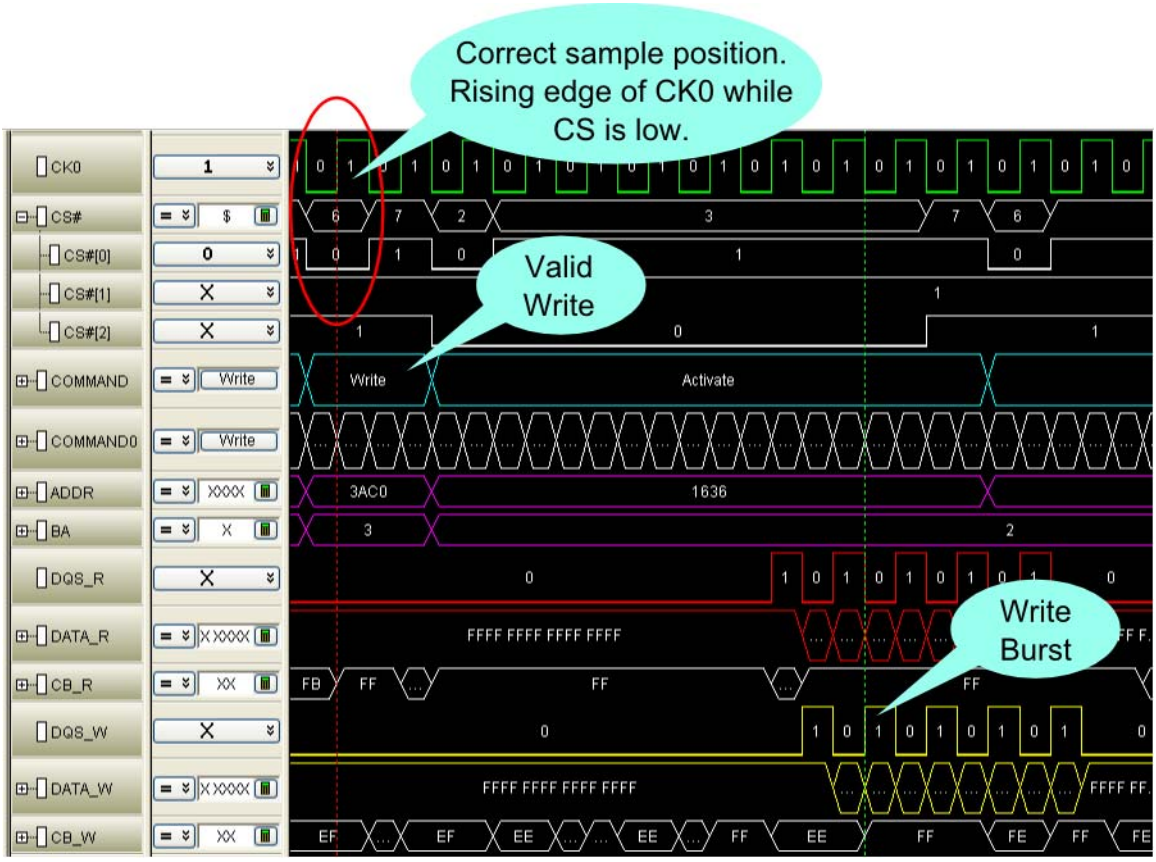
You can then choose to set the sampling position and threshold voltages suggested in the eye scan run or manually adjust these settings based on the suggested values. You use the **Eye Scan - Sample Position and Threshold Settings** dialog box to set up and run eye scan measurements for U4154A. In this dialog box, first you create an eyescan measurement and customize it to suit your specific requirements and then run this eyescan measurement. This allows U4154A logic analyzer to determine and suggest optimal values for sample positions and thresholds.

To know about the eyescan feature in detail and how to set up and run an eyescan, refer to the topic ***Setting up and Running Eyescans in U4154A Logic Analyzer*** in the Logic Analyzer online help.

7
Validating the DDR Setup

Validating Data in the Trace

After sampling positions have been set up, click the Run button to take a trace. Then, view the results in the Waveform window.



The previous picture shows a valid write and write burst.

8
Capturing Data (Triggering)

Recalling DDR Favorite Triggers

The configuration files provided with the DDR Bus Decoder include these DDR favorite triggers:

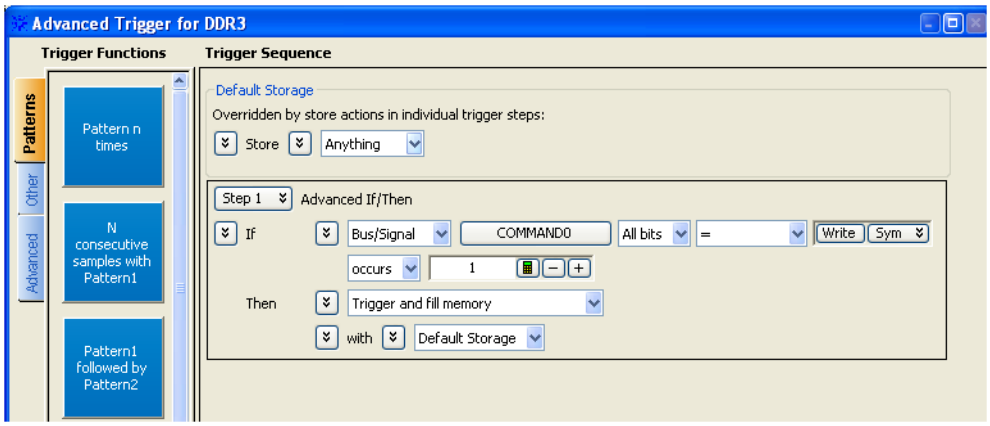
DDR Favorite Trigger	Description
Burst 4 Write Data	Triggers on four write burst data values.
Burst 8 Write Data	Triggers on eight write burst data values.
Mode Register Settings (MRS)	Captures mode register settings as the DDR device under test starts up. This trace will show the Total Read latency, Total Write latency, burst length, and burst type (sequential or interleaved) values of the DDR device under test. See "Taking a Mode Register Settings (MRS) Trace" on page 50.
Basic Trigger	Lets you specify command, CS#, CKE, and CS0 values to trigger on.
Filter NOPs	Uses trigger sequence step storage qualifiers and branched to prevent NOPs from being stored in the trace.

To recall the DDR favorite triggers:

1. In the *Agilent Logic Analyzer* application, open the Advanced Trigger Setup dialog.
2. Click **Recall...** at the bottom of the dialog.
3. In the Recall Trigger dialog, select the favorite trigger; then, click **OK**.

Triggering on Valid Commands

With DDR signals, you can set up the logic analyzer to trigger on valid commands. For example, you can trigger on Command0 and qualify it with CS#0.



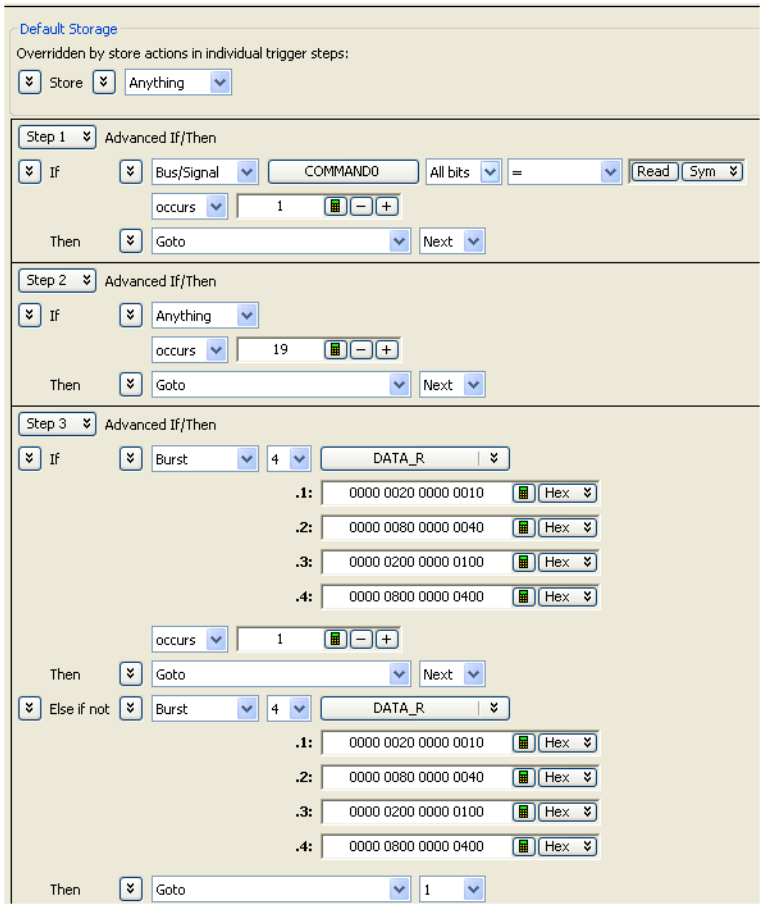
Note that you can use pre-defined symbols to easily select commands.

For more information os setting up triggers, see "Specifying Advanced Triggers" (in the online help).

Burst Triggering

With the 16960A and 16962A logic analyzers, you can use the burst triggering feature to capture sequential data capture.

The trigger setup for sequential data triggering looks like:



NOTE The trigger will be at the end of the burst pattern specified in the burst trigger.

For more information on burst triggering, see "Specifying Advanced Triggers in the 16960/16962 Logic Analyzers" (in the online help).

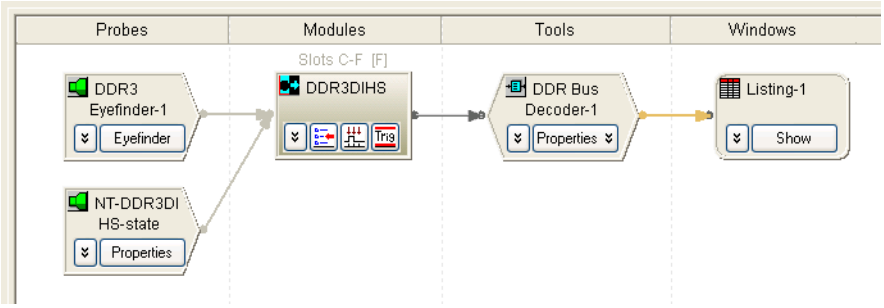
9 Decoding Captured Data

The DDR Bus Decoder is used to decode data captured from the DDR device under test.

Third party probes may provide their own, similar bus decoder tools.

DDR Bus Decoder

The DDR Bus Decoder appears in the *Agilent Logic Analyzer* application's Overview window, as shown in the following example.



For more information, see "Using the DDR Bus Decoder" (in the online help).

A
Setting Data Sample Positions with the 1695x Logic Analyzers

When using 16950A/B or 16951B logic analyzers (to capture DDR2 data), the DDR3 Eyefinder cannot be used to determine the proper sample positions for data signals. Instead, you can use the logic analyzer's *timing zoom* feature as outlined in this appendix.

This procedure uses Timing Zoom to identify the time difference between the CK0 (rising and falling edges) and the center of the read and/or write eyes. If dual sampling is used, there is one set of bus/signal names for reads and another for writes, and the sample position can be set independently for each.

The sample position for each bus/signal is set to the middle of the data valid region for the burst type the bus/signal supports.

1 The DDR Bus Decoder requires the proper parameters to be entered in order to decode valid states.

In the *Agilent Logic Analyzer* application's Overview window, select **System Configuration** from the DDR Bus Decoder's Properties drop-down.

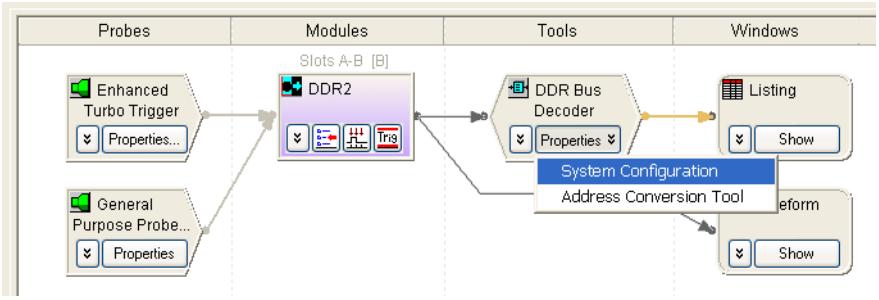


Figure 1 Opening the DDR Bus Decoder System Configuration

The information required is generally available from the specifications sheet of the memory device being used or by querying the BIOS of the device under test.

- Additive Latency – Defined by the chipset.

- Number of Chip Selects – This is either 1 or 2 based on the whether either CS0 is being probed and incorporated into the DDR Bus Decoder or both CS0 and CS1.
- Total Read Latency – The delay from a valid Read command to when the Read data is strobed on the bus.
- Burst Length – Usually fixed at 2, 4, or 8.

The DDR System Configuration dialog for entering this information is shown in the following figure.

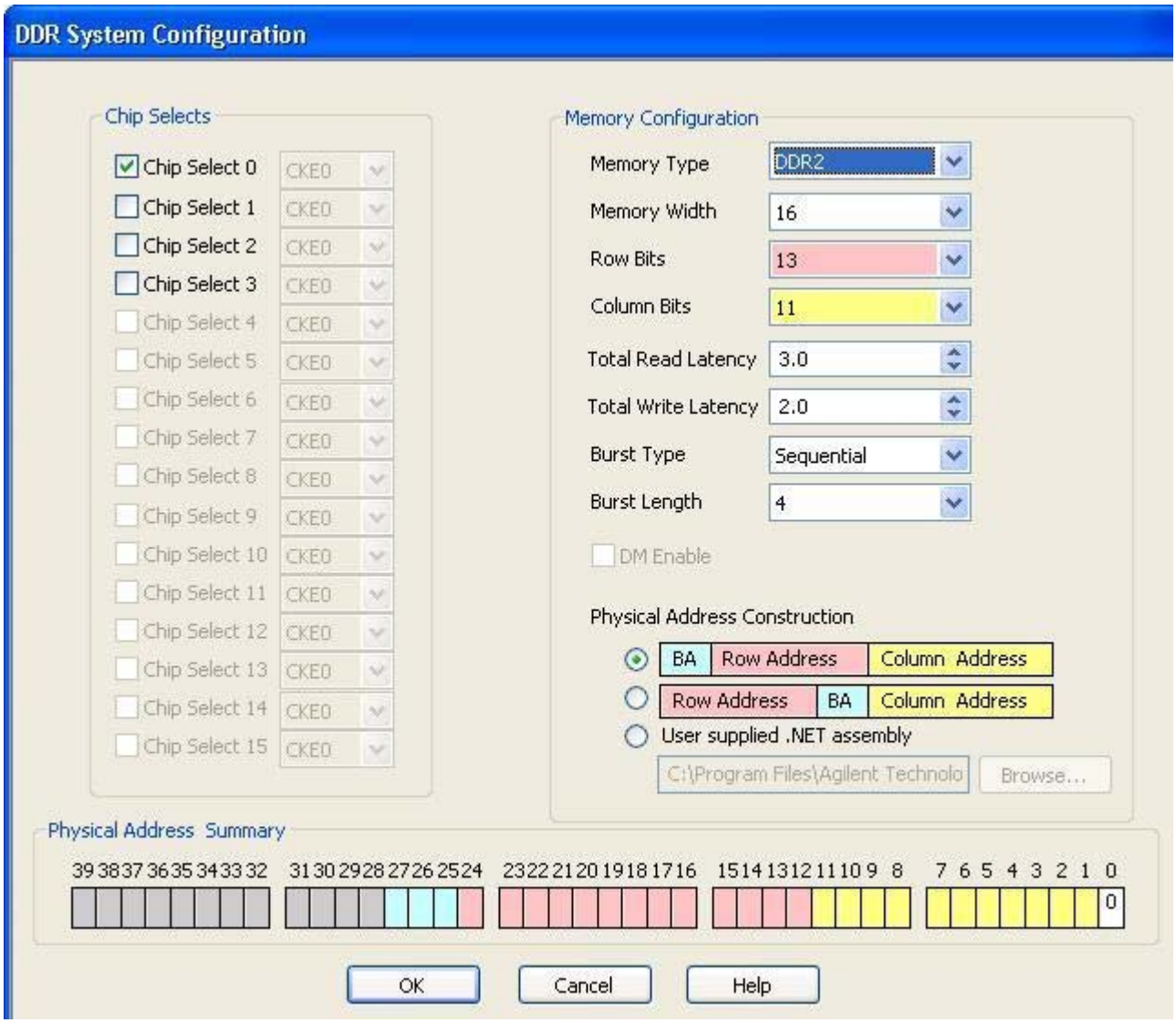


Figure 2 Setting the DDR Bus Decoder System Configuration

2 Start a memory test program that creates a good mixture of reads and writes, ideally with bursts of both types close enough together to fit several cycles of each type of burst in a single Timing Zoom trace.

A trigger on a write may be required if the test program does not have a mix or reads and writes in close proximity.

3 Trigger the analyzer on a burst. This can be done by using the logic analyzer trigger function "Find pattern n times" as shown in the following figure:

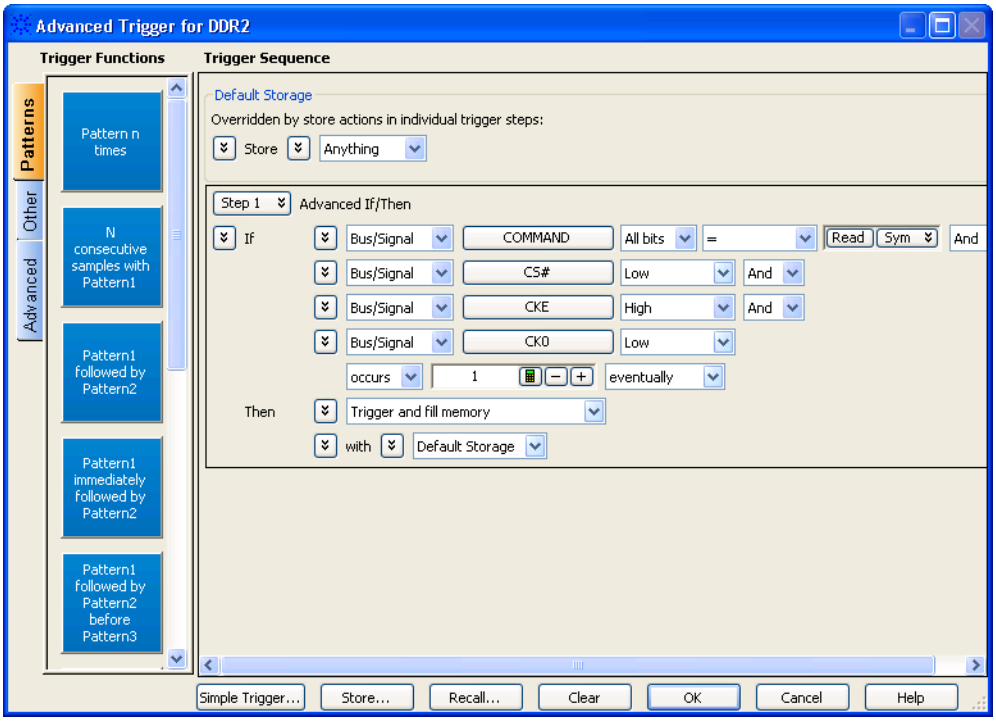


Figure 3 Trigger on a read

Note that in addition to looking for the DDR commands, the CS# signal is used to determine if the command is actually addressing a memory chip, and the CK0 signal is used to make sure the command sampled on the rising edge of the CK0 is used (since that is when the DDR command bus is valid).

This example uses CS# to identify valid commands. Any chip select that addresses an actual rank of memory may be used. If more than one chip select signal is needed (such as when there are several DIMMS on the bus), each of those chip select signals may be OR'ed together in the trigger event.

4 Run the logic analyzer to capture a trace.

5 Open the Waveform window.

If they are not already added by the supplied configuration file, add the Timing Zoom bus/signal names for:

- command clock, CK0 (TZ)
- chip selects, CS# (TZ)
- DQS, DQS (TZ)
- bus bus/signal names for data reads, DATA_R (TZ)
- bus bus/signal names for data writes, DATA_W (TZ)

Scroll the waveforms to find the start of a read burst. You will see this by finding where the DQS strobe becomes active.

6 The following figure shows an example Waveform window being used to locate the start of a read burst.

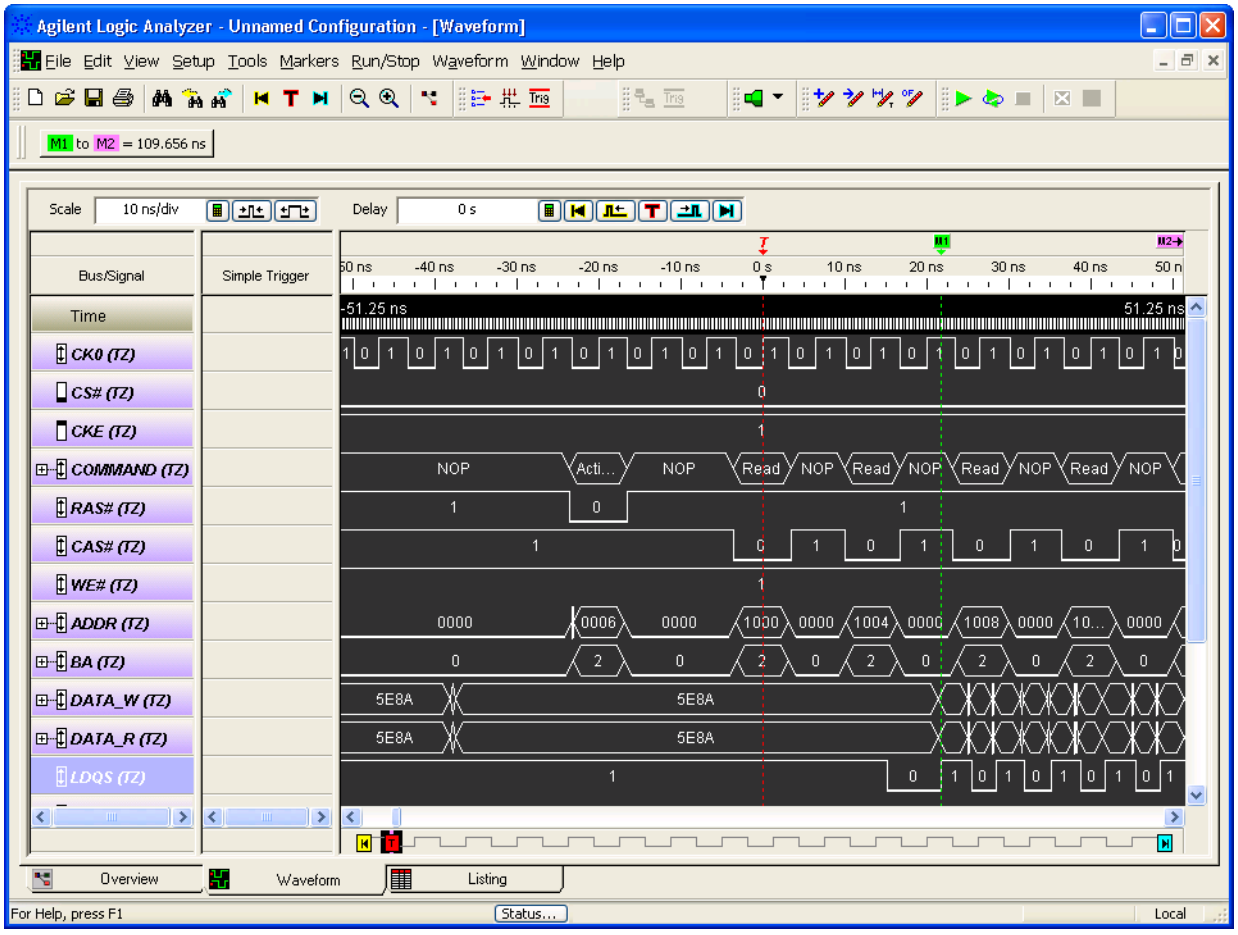


Figure 4 Locating a Read Burst

NOTE Your display may differ from the previous figure. This is okay. To measure the timing differences you can use just the DATA (TZ) bus/signal names and not the DATA_R (TZ) bus/signal names.

7 Now, measure the time delay from the closest edge of CK0 prior to the center of the read data eyes.

Place a marker on that edge of the CK0. Place the other marker in the center of the data valid region for the read data bus/signal name.

You may find it easier to identify this point by locating the point on one of the DQS signals that is equal distances from the edges. Note the delay between the markers as shown in the following figure.

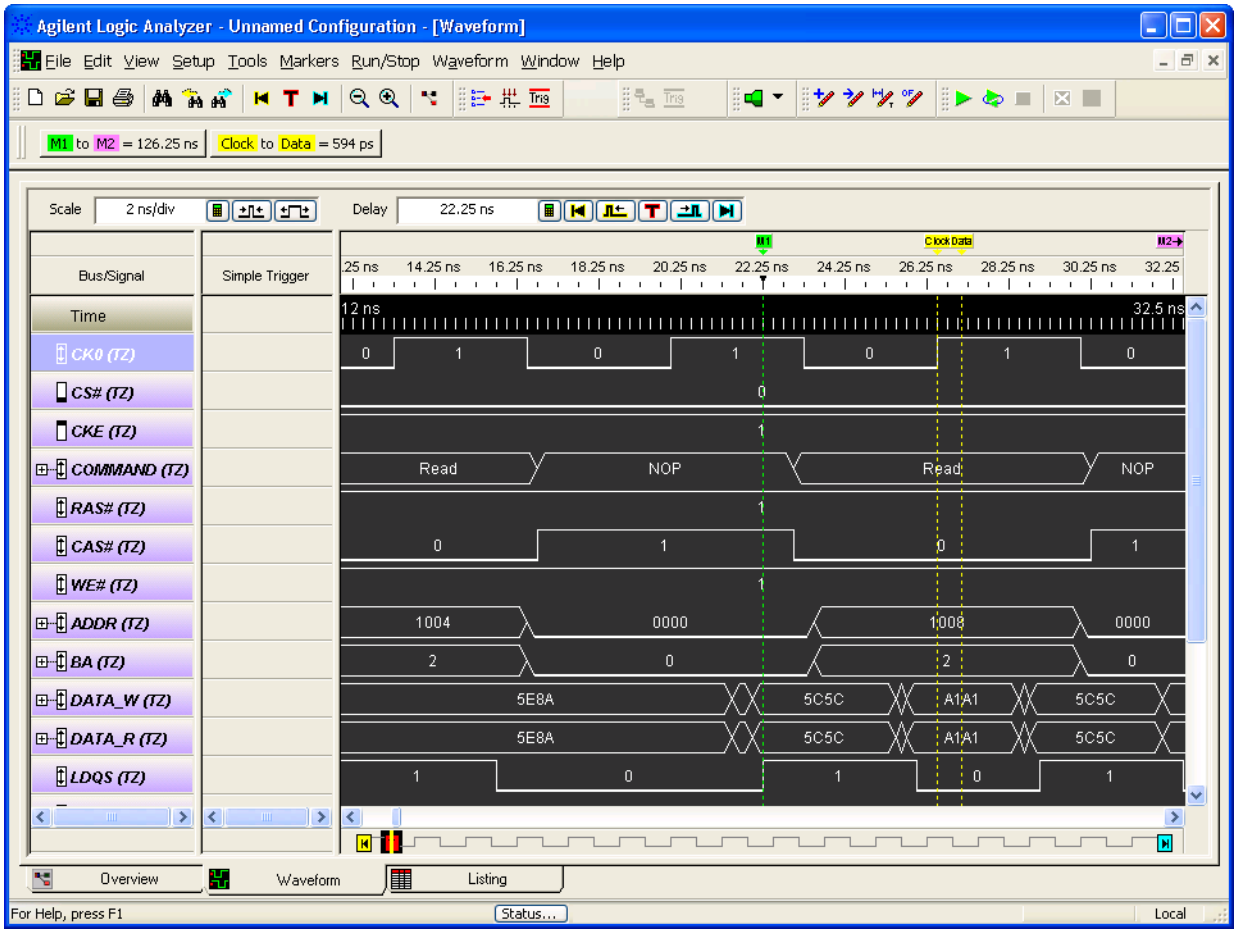


Figure 5 CK0 rise to center of read data eye

8 Repeat this procedure using the next edge of CK0 and the corresponding data burst cycle (it will be right next to the burst cycle you just looked at).

9 Repeat this procedure for several cycles of the burst. You may do this for other read bursts as well if you wish to cover different types of data burst patterns and account for possible edge jitter sources.

Compute the average of the times for all the burst cycles (combining those for the rise of CK0 and the fall). This will be your sample position delay value, for example 300 ps.

10 Now, it is time to use this delay information to set the logic analyzer sample position.

In the logic analyzer's Sampling Setup dialog, click **Thresholds and Sample Position...**.

In the Thresholds and Sample Positions dialog, you can set the sample positions for the read and write data bus/signal names.

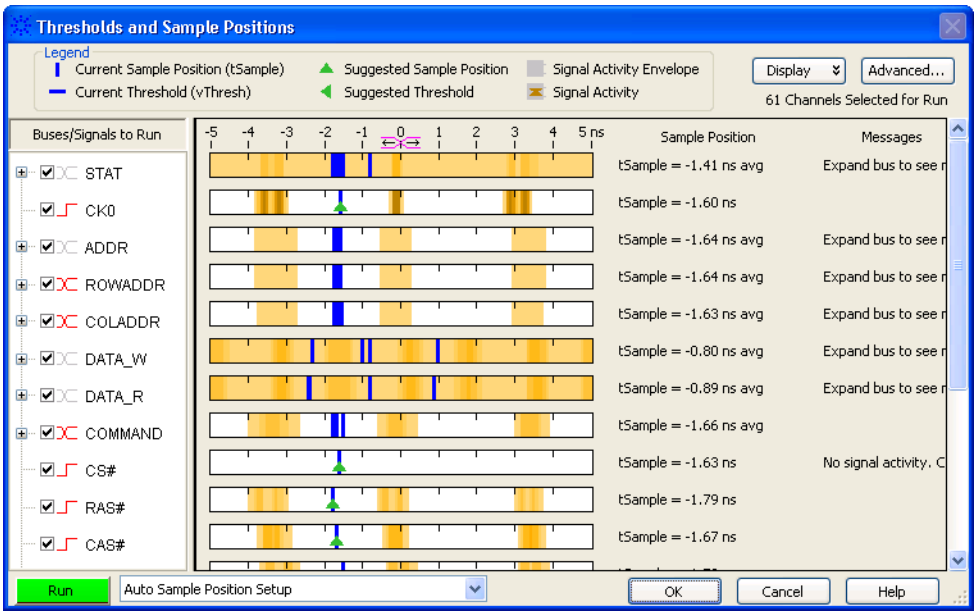


Figure 6 Setting the Sample positions

11 Set the sample position to be equal to the average time you computed earlier.

The easiest way to do this is to point to the blue vertical sample position bar with the mouse and press and hold the left mouse button while dragging the blue bars as far to the left side of the display as

possible. This will cause all the blue bars for that bus/signal name to be set to the same value. Then, you can drag the blue sample position bar back to the right to place it in the position you measured earlier.

The sample position is indicated on the scale at the top of the display as well as on the side under the "Sample Position" column.

The following figure shows the DATA_R bus/signal name sample position set to +309 ps as an example. This means that if you measured a 309 ps average delay to the center of the data eye for the DATA_R bus after a valid CK0 edge, you would set the logic analyzer sample position for DATA_R to +309 ps (as shown in in the following figure).

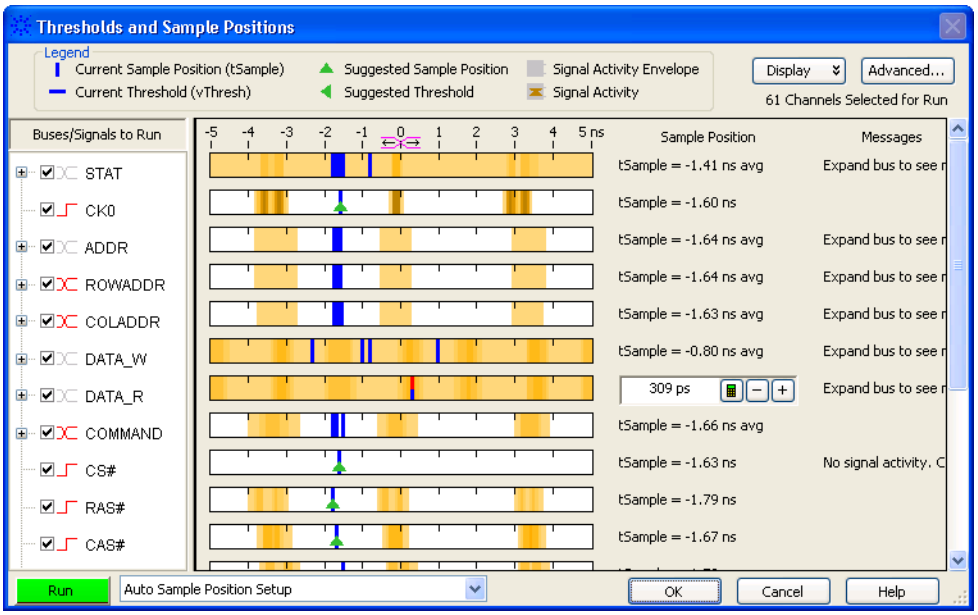


Figure 7 DATA31-0 set to +1.86ns

12 Repeat this procedure as well for the ECC bits and the data strobes.

13 For the DDR command/address bus you can repeat this procedure also, except that time is measured only from the rising edge of CK0 since those signals are only valid at that time.

This completes the procedure for the read configuration.

Use the same procedure using write bursts and the write data bus/signal names. The only difference is that you can easily find the center of the data valid window by setting the second marker to the EDGE of the DQS signal. (Write data eyes are centered on the edge of the strobes whereas reads straddle the DQS strobes.)

14 If you are using the Dual Sample Mode, repeat the calibration procedure for Writes.

You should now be ready to take state traces and be confident you will capture bus traffic correctly.

For more information, see "To manually adjust state sampling positions" (in the online help).

DDR Glossary

D

DUT Device Under Test.

I

interposer Describes a probing method where the probe is located between a slot and a DIMM.

M

midbus probe Describes a probing method where Soft Touch footprints are designed into a DUT board between the memory and the memory controller. The N4834A midbus probe is one specific footprint and configuration for midbus probing. Other custom Soft Touch footprints are possible.

B DDR Glossary

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