Universal Serial Bus Implementers Forum Host High-Speed Electrical Test Procedure for Tektronix TDS7254/B, TDS7404/B, CSA7404/B, TDS6604/B, TDS6804/B, TDS6404, DPO7254, DPO7354, and DPO/DSA70000 series

Revision 1.4

Mar 2008

Revision History

Rev	Date	Filename	Comments
0.8	26-Jun-2001	Host HS Test.DOC	Initial draft revision
0.81	12-Jul-01	Host HS Test.DOC	Changed el_17 on page 36 to reference Section 7.1.6.2.
0.9 (Beta)	Aug-31-2001	Host HS Test.DOC	Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification
1.0	Dec-23-2001	Host HS Test.DOC	Edit for final release. Delete TDR section.
1.1	Sept-9-2002	HS System Test.DOC	Added Legacy free test instructions
1.2	April-1-2003	Host HS Test Tektronix.DOC	Update procedure for Tektronix TDS7040, TDS7254, CSA7404 and TDS6604 for use with TDSUSB Compliance test software
1.3	Feb, 2007	Host HS Test Tektronix.doc	Changes made according to the new test fixture
1.4	Mar, 2008	Host HS Test Tektronix.doc	Updated the model numbers

Please send comments via electronic mail to techsup@usb.org

USB-IF High-speed Electrical Test Procedure
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Table of Contents

1 Introduction

The USB 2.0 Compliance Committee under the direction of USB-IF, Inc develops the USB-IF High-speed Electrical Test Procedures. There are three High-speed Electrical Test Procedures.

- The Host High-speed Electrical Test Procedure is for EHCI host controllers.
- The Hub High-speed Electrical Test Procedure is for high-speed capable hubs.
- The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

This test procedure is an update of the USB-IF Host Electrical High-speed Test Procedure written for the Tektronix TDS694C and the USB-IF MatLab scripts. This updated procedure is written to support Tektronix TDS7404/B, CSA7404/B, TDS7704B, TDS7254/B, TDS6604/B, TDS6804/B, TDS6404, DPO7254, DPO7354 and DPO/DSA70000 series running TDSUSB2 Compliance Test Application Software. The TDSUSB2 software is used in place of the MatLab scripts and NI GPIB DAQ software.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high speeds. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one-of-a- kind prototype of peripherals, add-in cards, motherboards, or systems.

This test procedure refers to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.3.

This Host USB-IF High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Hub USB-IF High-speed Electrical Test Procedure and Device USB-IF High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Recommended Equipment

The commercial test equipment listed here are base on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

Tektronix Digital Oscilloscope:

- This procedure supports Tektronix TDS7404/B or CSA7404/B or TDS7704B, TDS7254/B, DPO7054, DPO7104, DPO7254, DPO7354, DPO/DSA70404, DPO/DSA70604 and DPO/DSA70804 series of Digital Phosphor Oscilloscopes.

- Tektronix Probes and accessories (Refer to www.tektronix.com for complete scope-to-probe compatibility requirements)

  o A DPO7254, DPO7354, TDS7254/B, TDS7404/B, CSA7404/B or TDS7704B or greater bandwidth oscilloscope is required to test the high-speed USB hosts, devices, or hubs

  o A DPO7054 or TDS5034B or greater bandwidth oscilloscope is required to test low-speed and full-speed USB devices and hubs

  o A P6330 or P6248 1.7 GHz differential probe or greater bandwidth probe. For example, P63301, P7330, P7360, P7380, qty = 2

  o Tektronix P6245 FET probes, qty = 2

  o Tektronix TCA to BNC adapters, qty = 3

  o TDS7000 Deskew Fixture, part number: 067-0405-xx, shipped as a standard accessory to the oscilloscope.

- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent

  Mini-clip DMM lead – one each of black and red

- High-speed USB Electrical Test Fixtures

- Tektronix TDSUSBF signal quality test fixture, qty = 1

  o Disconnect test fixture, qty = 1 (source: USB-IF)

  o Female Serial B to female Serial A adapter, qty = 1

  o 6-INCH AB Cable with USB-IF compliance logo tag, qty =1

- Known good HS device – any HS capable device that is on the USBIF integrators list.

- Miscellaneous Cables

  o 1M USB cable, qty = 1

  o 1.5M USB cable, qty = 1

  o Modular AC power cord, qty = 2

- High-speed Signal Quality Analysis Computer

  This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. The OS

on this computer is Windows 2000 or XP Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

Note: The Tektronix USB compliance test software operates internally to the oscilloscope and automatically configures the oscilloscope settings so that external GPIB control of the oscilloscope is not required. One can consolidate the High-speed Signal Quality Analysis Computer and the High-speed USB Test Bed Computer into one single PC.

3.1 Equipment Setup

3.1.1 Test Equipment Setup Diskettes

Some tests described in this procedure are not automated by the Tektronix TDSUSB2 Compliance Test Software application. For those tests, the application includes setup files for the test equipment used in this procedure. The setup files simplify equipment setup. Copy the HS Scope Setup files to floppy disks. Insert the Tektronix TDS7000/6000, DPO7000/6000 setup floppy diskette into the Tektronix TDS7254/7404, DPO7254/7354/7404, or TDS/DPO6000 oscilloscopes.

3.1.2 Digital Sampling Oscilloscope

Before turning on the oscilloscope, attach a P6330 or P6248 differential probe to Channel 1 and Channel 4. TPA-BNC adaptors are required for the DPO7000 series. Attach two P6245 FET probes, one to Channel 2 and one to Channel 3. The probe assignment will be used through out the entire test procedure. Turn on the oscilloscope to allow for 20 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the Utility menu of the Tektronix oscilloscope if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

A higher resolution view of the USB signaling is possible by turning on the scope's Hi Resolution mode. On the scope's menu bar, select Horiz/acq > Horizontal/Acquisition Setup > Acquisition > Hi Res.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes will be cancelled later as a part of the test procedure process. The offset of the differential probe will be adjusted by the step identified in the test procedure.

For P6247/P6248 differential probes, the following setting will be used through out the entire test procedure:

o   DC Reject <OFF>   (P6247 only)
o   BW <Full>   (P6247 only)
o   Attenuation <÷1>

The use of a Tip Saver accessory on the P6247 or P6248 probe is highly recommended to prolong probe tip life. Please note that the Tip Saver will wear out after repeated use and start degrading signal quality measurements. Replace the Tip Saver when measurements made without it provide better results.

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up

and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.2   Operating Systems, Software, Drivers, and Setup Files

3.2.1   Operating Systems

Microsoft Windows 2000 or XP Professional is required on the High-speed Electrical Test Bed Computer. Microsoft Windows 2000 or XP Professional is required on the High-speed Signal Quality Analysis Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3   Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.

- Proprietary EHCI Driver Stack – The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result is a much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.

- TDSUSB2 Tektronix TDSUSB2 Compliance Test Application software

3.3.1   Test Equipment Setup Files

These are 3 ½ inch floppy diskettes that contain the setup files for the test equipment. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these setup disks.

HS Scope Setup Disk – Contain setup files for Tektronix TDS7000/6000 DSO (Digital Storage Oscilloscope).

3.4 Test fixture

The table matches the pins of the two most recent versions of TDSUSBF test fixtures. This procedure document is based on using the pin locations of the "New Fixture" shown in the following table.

Section	Old Fixture	New Fixture
Host SQ section	J17	J15
		J16

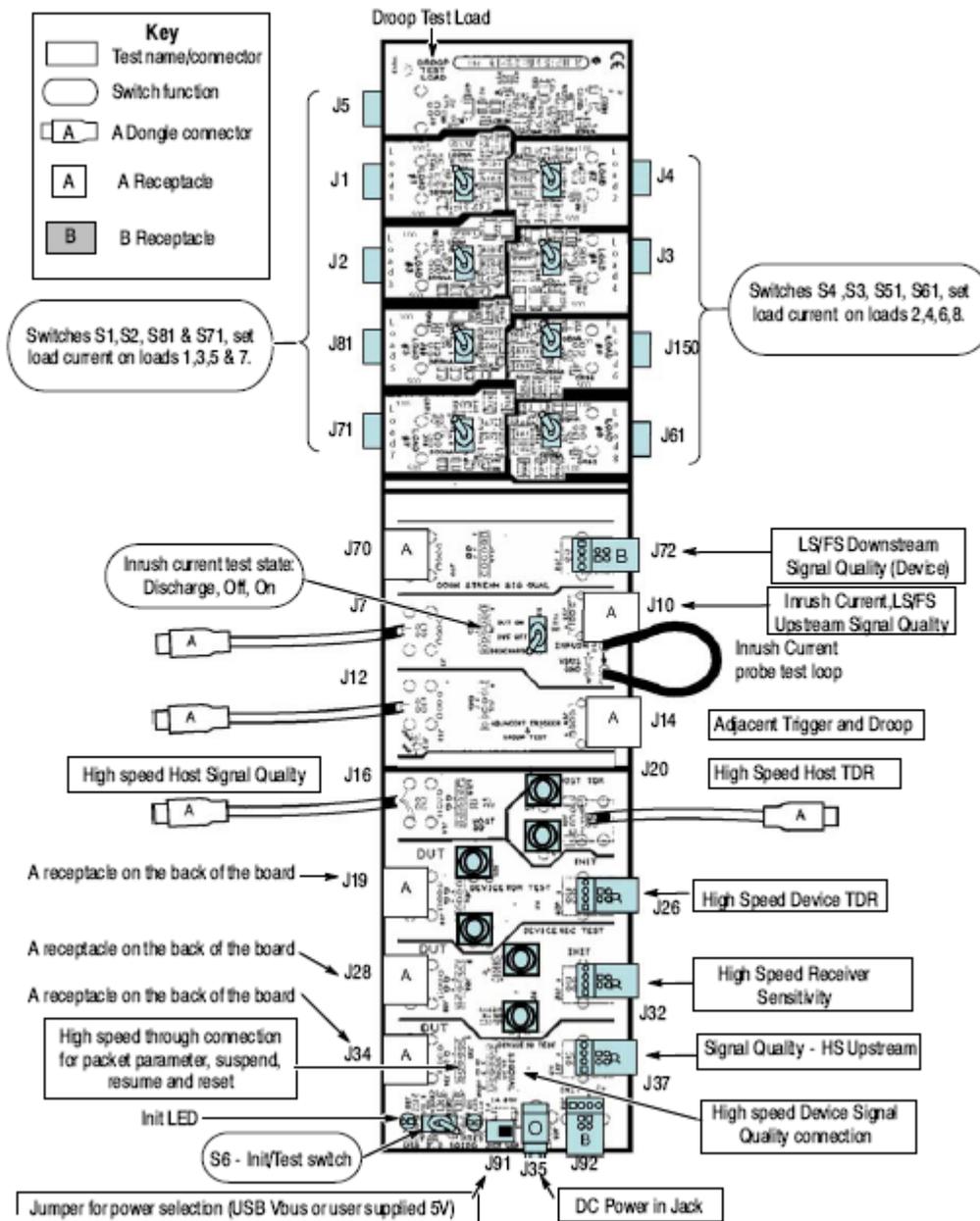| DUT	Test	Position Test	Position Probe	Test Mode
High-Speed Host	SQ	J16	J15	Downstream
	Packet Parameter	J37	J310	
	CHIRP	J37	J310	
	Suspend	J37	J310	
	Resume	J37	J310	
	Reset	J37	J310	
	J	J37	J310	
	K	J37	J310	
	SE0_NAK	J37	J310	

Figure 1: Tektronix New TDSUSBF Test Fixture

4 Test Procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

- Test date

- Vendor name

- Vendor address and phone, and the contact name

- Test submission ID number

- Product name

- Product model and revision

- USB silicon vendor name

- USB silicon model

- USB silicon part marking

- USB silicon stepping

- Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the host controller under test must also pass the following compliance tests applicable to the EHCI Host Controller:

- Low speed signal quality

- Full speed signal quality

- Drop/Droop

- Interoperability

Perform all these tests; record the measurements and summarize the Pass/Fail status in Appendix A.

4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

1. Attach the differential probe to J15 of the TDSUSBF test fixture, Host SQ segment. Ensure the "+" symbol on probe lines up with D+ on fixture. Turn on the oscilloscope if not have already done so. Allow about 20 minutes for warm up. Connect the short USB cable from the Host SQ fixture segment to the host port under test.

2. Launch the TDSUSB software application on the Tektronix oscilloscope by selecting with a mouse or touch screen.

3. Press the Default setup button on the oscilloscope front panel.

4. In the applications menu bar select, File> Recall Default Setup.

5. In the Measurement select menu of the USB2.0 compliance test application, select the High Speed tab.

6. Within the Signal Quality area of the application, select the High Speed Signal Quality tests> Eye Diagram, Signal Rate, Rise time, Fall Time, and EOP Width.

   Note: The Monotonic property test is available but not required as it may generate false failures due to slight variations in the signal edge due to high frequency noise and/or oscilloscope quantization error.
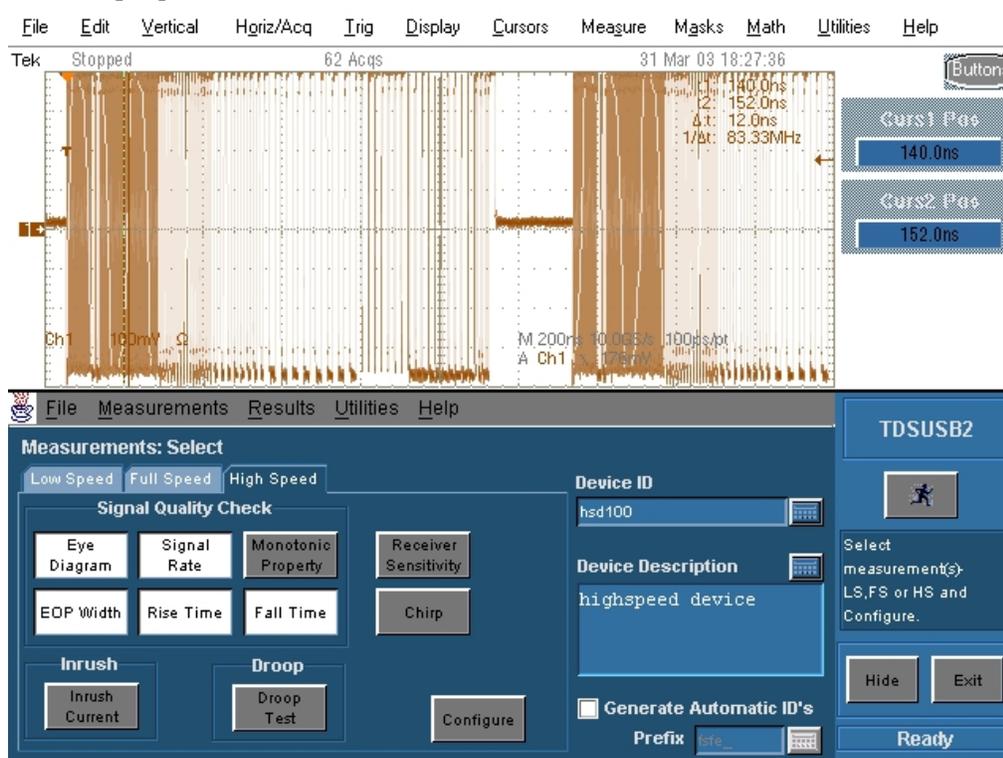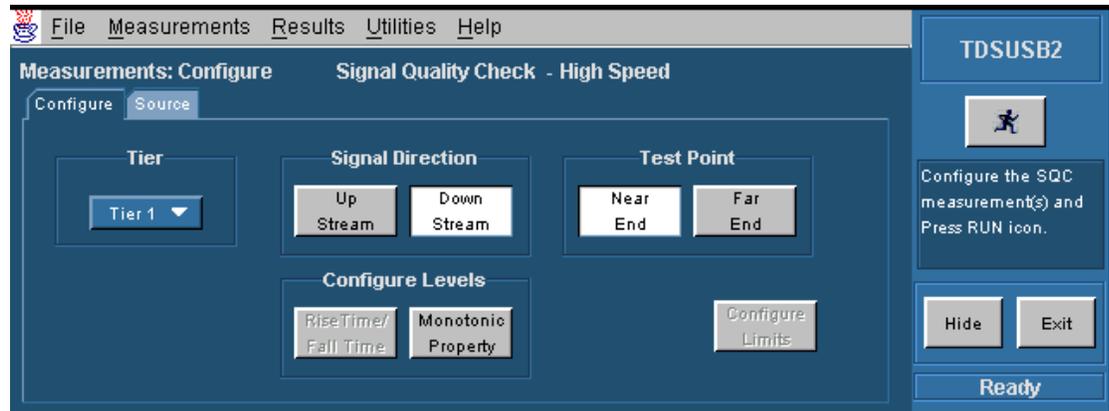

Figure 2: Tektronix TDSUSB Software

7. Enter a device ID (for example, TIDxxxxxxx USNE.tsv) in the device ID dialog box and a device description into the device description dialog box.

8. Press Configure to configure TDSUSB according to the system under test.

9. Press the [icon] icon. Verify that the oscilloscope display is NOT reporting "clipping". If it is, adjust the vertical amplitude until the "clipping" message does not appear. Do not press OK until the correct waveform is displayed.

10. Press OK when the correct waveform is acquired. Press OK when done.
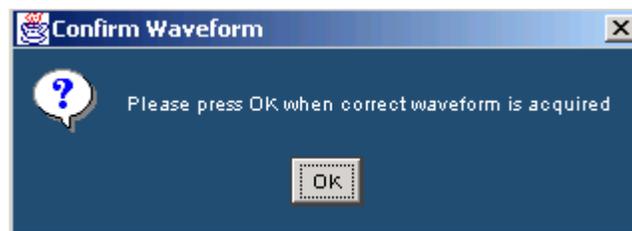
11. Invoke the High-speed Electrical Test Tool software on the high-speed computer under test. The main menu appears and shows the USB2.0 host controller.
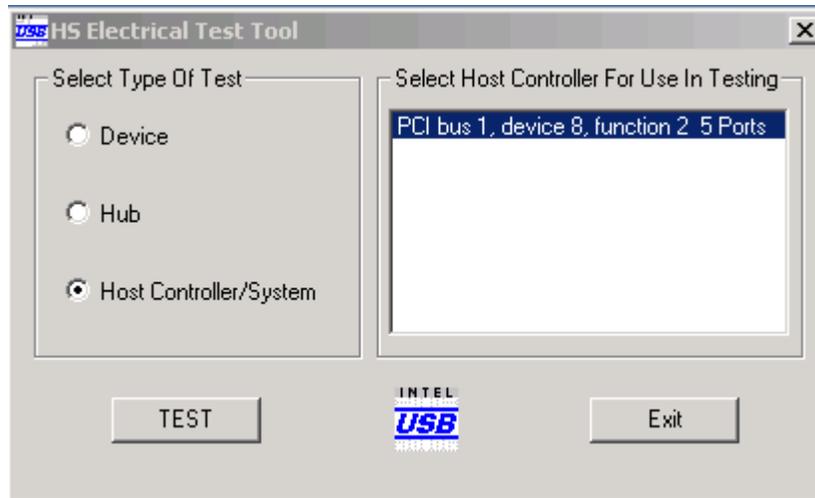

Figure 3: Main Menu

12. Select Host Controller/System and click TEST to enter the Host Test menu.
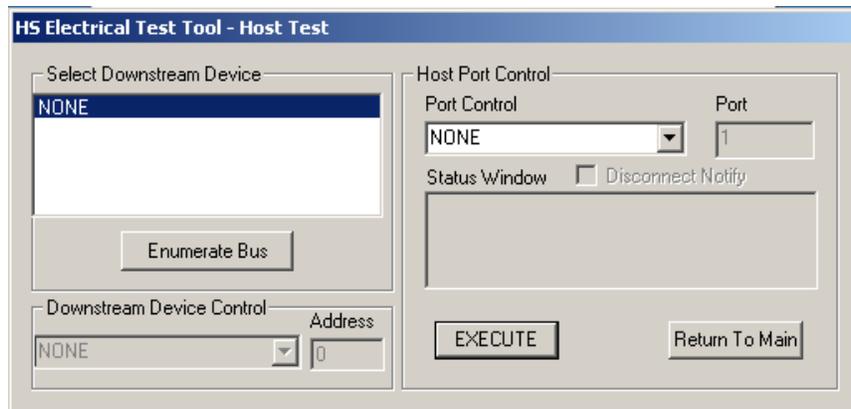

Figure 4: Host Test Menu

13. Connect the Test port of the Host High-speed Signal Quality test fixture to the port under test of the Host controller.

14. Select TEST_PACKET from the Port Control dropdown menu. Enter the port number of the port being tested and click Execute. This forces the port under test to continuously transmit test packets
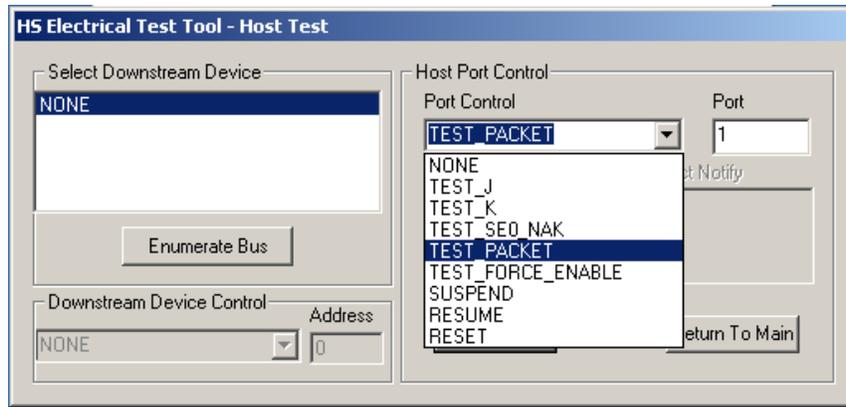

Figure 5: TEST_PACKET

15. Using the oscilloscope, verify that test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try a slight change to the trigger hold-off.

16. Once the test packet is displayed properly, press OK in the application dialog box.

17. The Tektronix USB application generally triggers and displays the correct test packet without the need to place cursors. Should cursors be required, they may be enabled by selecting within the application, File> Preferences> Advanced and clicking the optional Packet Identification by user using Cursors.

18. If cursors measurement is enabled on the oscilloscope place the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure. Press OK on the USB2 application dialog box to begin acquisition and analysis of the test packet.
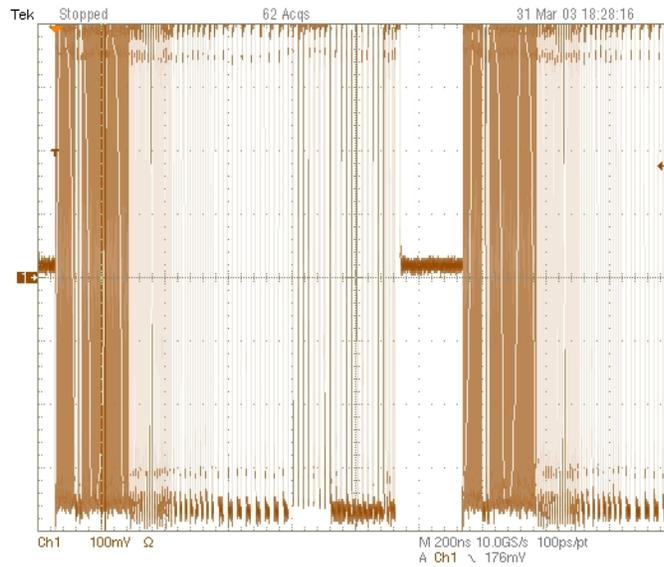

Figure 6: High-speed Test Packet

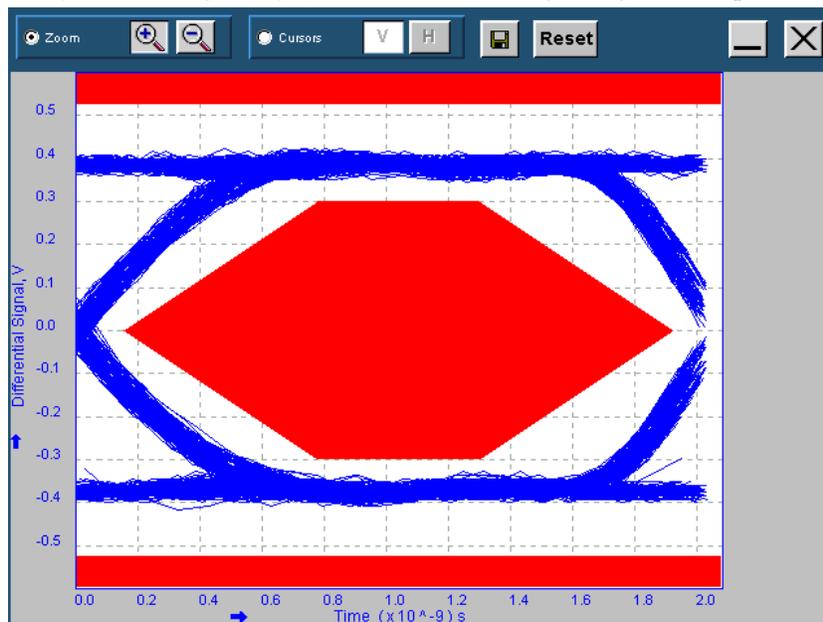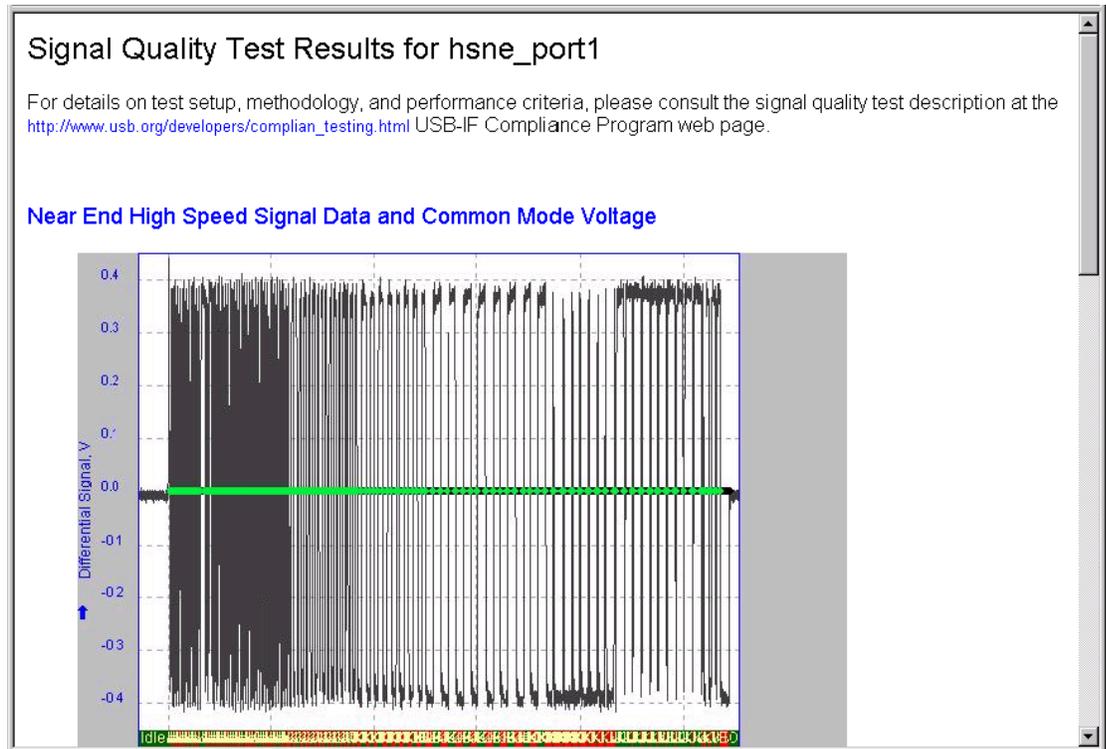19. Verify that the Signal Eye, EOP Width, and Signaling Rate all pass.

Figure 7: HTML Report for High Speed Signal Quality Test

20. Record the test result in EL_2, EL_3, EL_6, and EL_7.

21. Remove the TDSUSB test fixture from the port.

22. Repeat steps 9 through 19 for all remaining ports.

23. Save all files created during the tests. Remove the Host Signal Quality test fixture from the port under test.

4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

1. Connect the TDSUSBF Device Signal Quality test segment's short dongle (DUT Port) to the B receptacle of a known good high-speed device. Apply power to the known good device. Using a 1M USB cable, connect the INIT side of the fixture to the Port Under Test.
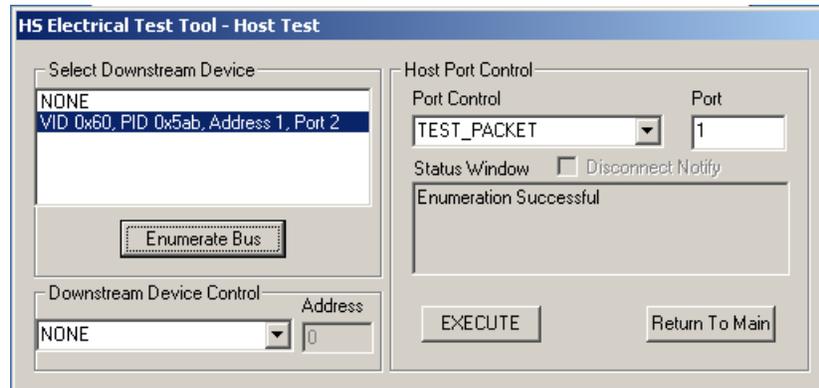
Figure 8: Known-Good Device Enumerated

Note: The use of the TDSUSBF Device High-speed Signal Quality test fixture segment makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, therefore the device packets are larger in amplitude.

2. Attach the differential probe to J36 on the fixture near the device connector. Ensure the "+" symbol on probe lines up with D+ on fixture.

3. Verify that the Test Init switch is in the Init position. Connect the TDSUSBF Device Signal Quality test fixture segment (Init Port) into host controller port under test with a short USB cable. Click Enumerate Bus and verify that the device enumerates properly.

4. Select Packet Parameter measurement from the High-Speed tab and configure the device for EL_21, EL_23, EL_25. Run the measurements.
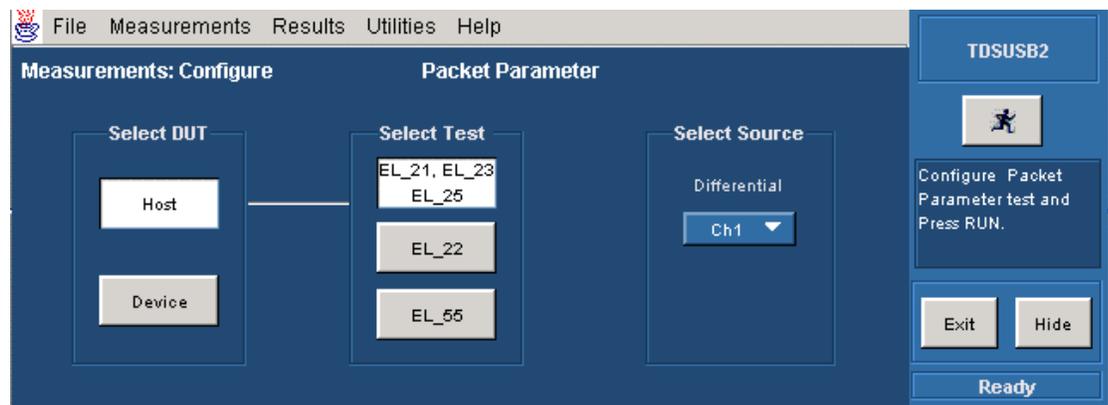
5. Using the oscilloscope, verify SOFs (Start Of Frame packets) are being transmitted on port under test.

6. In the Host Test menu of the High-speed Electrical Test Tool software, ensure the device under test is selected (highlighted). Select SINGLE STEP GET DEV DESC from the Downstream Device Control menu and click Execute once.
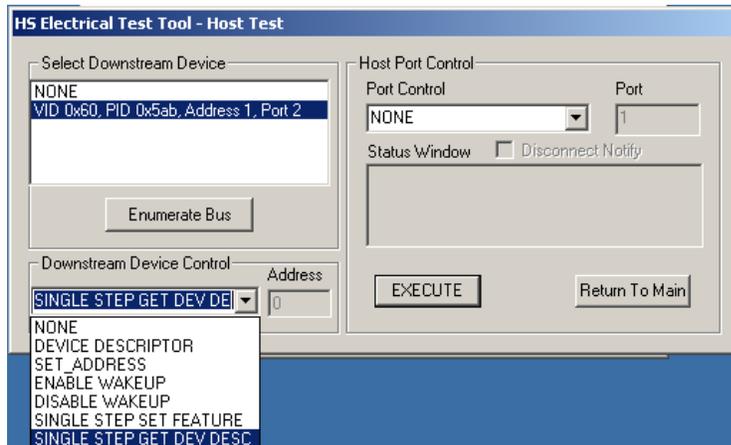
Figure 9: Device Single Step Get Descriptor

7. The oscilloscope capture should appear as follows.
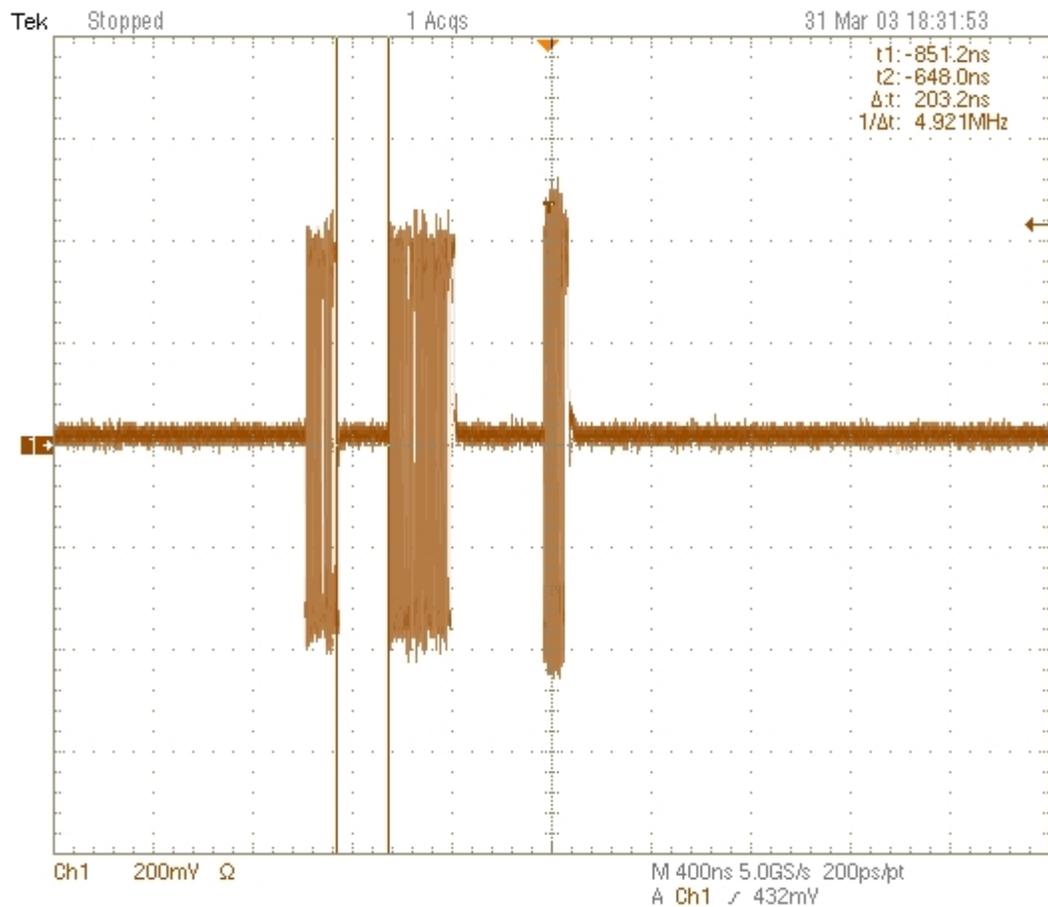
Figure 10: Packet from Host and Device

8. From the application menu, select Results> Summary. Click any of the test result buttons to get the details of that test.

9. The result contains EL_21 the sync field length (number of bits) of the first and second packets on the oscilloscope and should be of 32 bits. Refer to the figure below. Note that the Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero).

Figure 11: Host Packet Sync Field

10. The results consist of EL_25 the EOP length (number of bits) of the second packet on the oscilloscope and should be 8 bits.
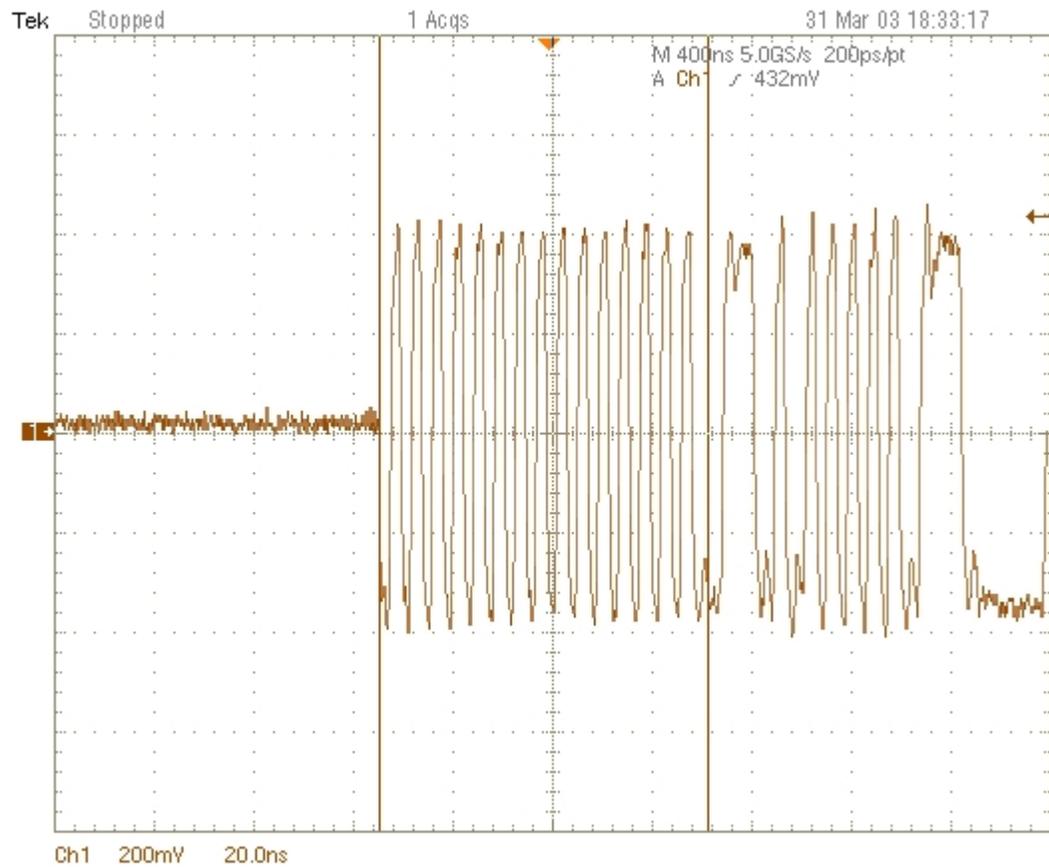
Note: Please note that the EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The following figure illustrates the positive going pulse.
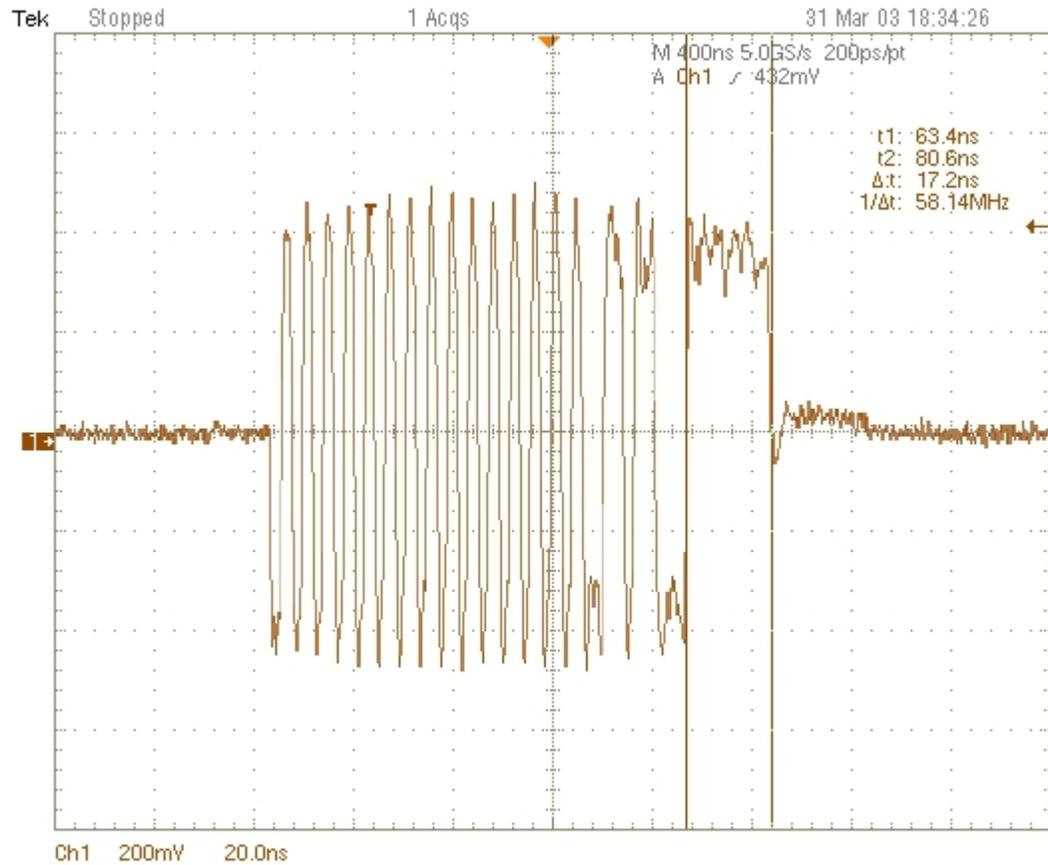
Figure 12: Host Packet EOP

11. The results consist of EL_23 the inter-packet gap between the first two packets shown on the oscilloscope. These are back-to-back packets from the host. The requirement is that it must be between 88 bits and 192 bits. (EL_23). The oscilloscope display should appear as shown in the following figure.

Figure 13: Inter-packet Gap – Between Packets from Host

12. Select the Packet Parameter measurement from the High-Speed tab and configure for device EL_22 and run the measurements.

13. On the Host Test menu click Execute once. The oscilloscope capture should appear as in the following figure. Pause the oscilloscope with the run/stop button.

14. The results consist of the inter-packet gap between the second and the third packets shown on the oscilloscope. The second (of higher amplitude) is a device packet and the third is the host response. The requirement is it must be between 8 bits and 192 bits. (EL_22).
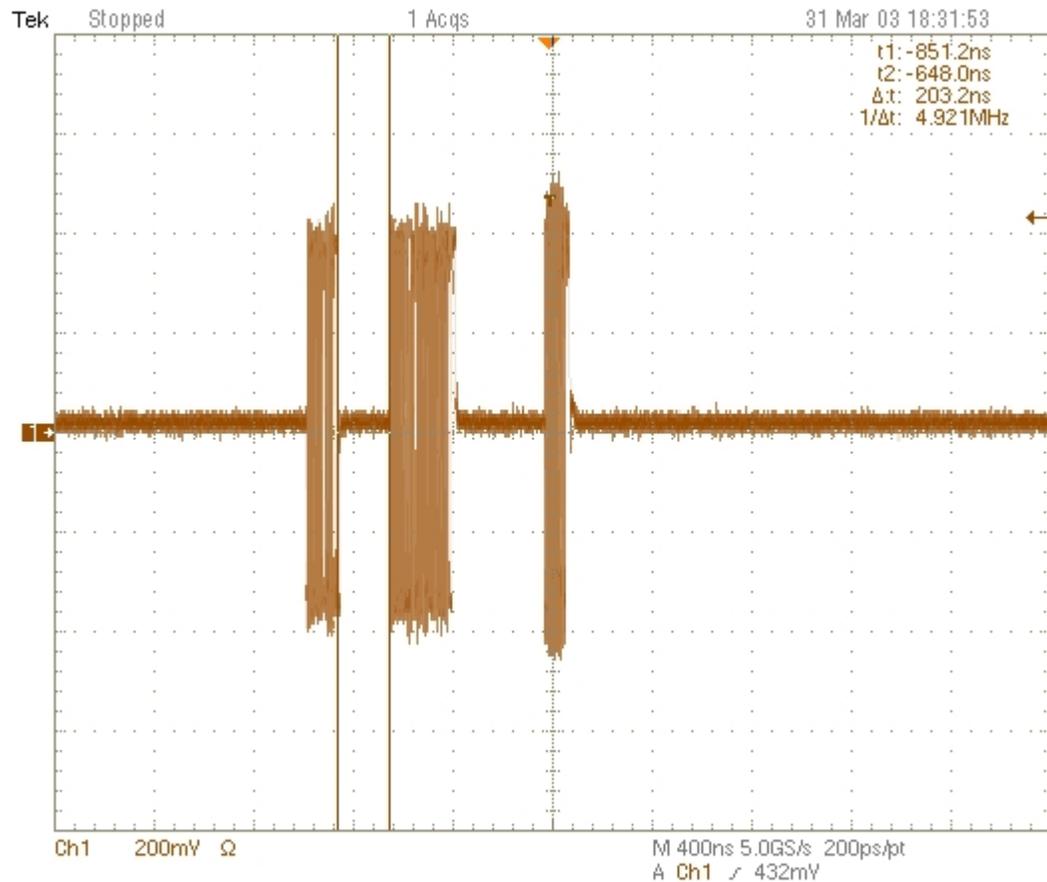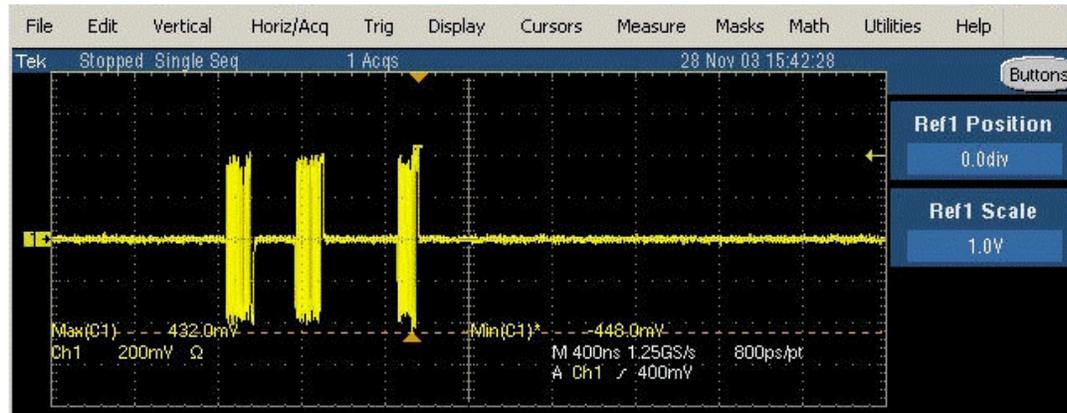

Figure 14: Inter-packet Gap – Host Respond to Device

15. Select the Packet Parameter measurement from the High-Speed tab and configure for device EL_55 and run the measurements. The application measures the time period of the EOP width. The application computes the number of bits by dividing the time measured by 2.08 ns. The EOP width must be 40 bits.

Figure 15: EOP Width – SOF Packet

16. Repeat step 4 through 15 for the remaining ports.

17. Remove the Device Signal Quality test fixture and the known good device from the host controller port under test.

4.6 Host Disconnect Detect (EL_36, EL_37)

This section uses the Disconnect test fixture to verify the disconnect thresholds of the port under test by simulated disconnect condition. (Contact the USB-IF to acquire this fixture. The TDSUSBF test fixture does not support this test.)

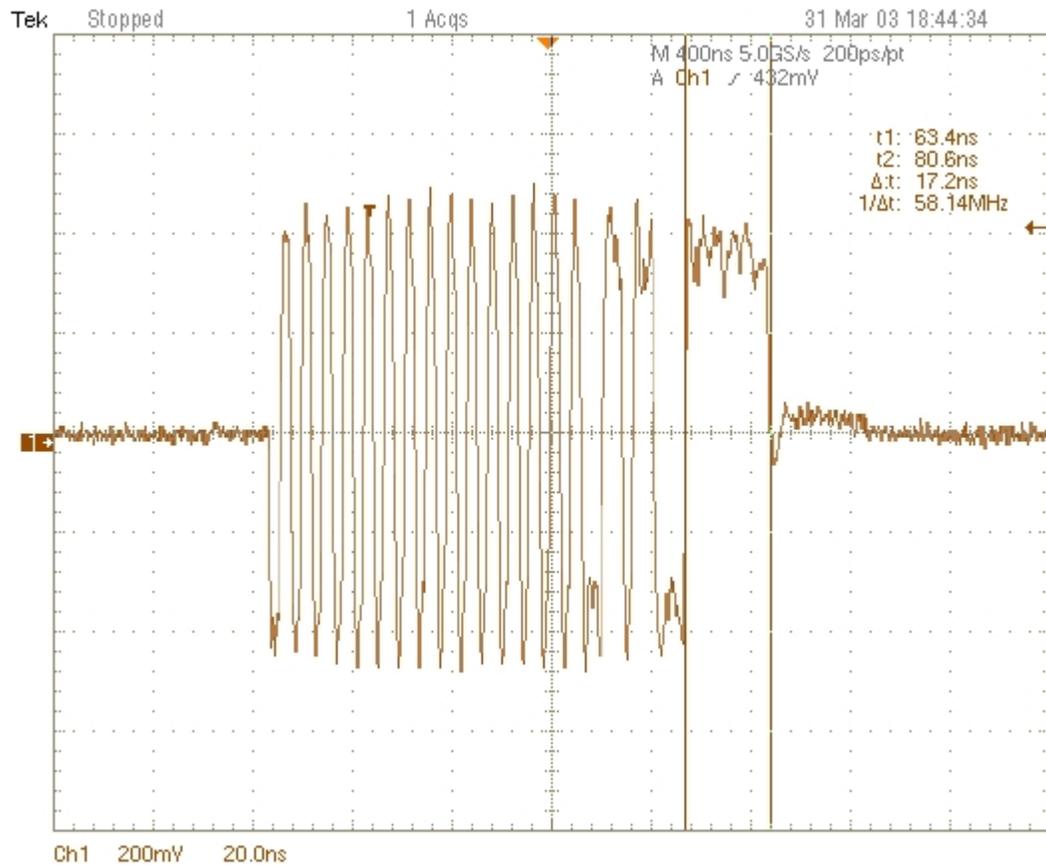When the TEST switch on the test fixture is in the Test position, the port under test is subjected to a threshold < 525 mV. The port should not detect a disconnection.

When the TEST switch is in the Normal position, the port under test is subjected to a threshold > 625 mV. The port should detect a disconnection.

1. Attach the 5 V power supply to Disconnect test fixture (J8).

2. Attach the differential probe to J7. Ensure the + tip on probe lines up with D+ on the fixture. Recall the DISCDETE.SET oscilloscope setup.

3. Set the TEST switch to the Test position. Verify that the green Power LED (D1) is lit, and the yellow Test LED (D2) is also lit. This sets the test fixture to emulate a must-not-disconnect threshold.

4. Attach the Test port of the test fixture to the port under test. In the Host Test menu of the High-speed Electrical Test Tool software select TEST_FORCE_ENABLE from the Port Control window. Enter the port number and click Execute once and in the Status Window ensure that the operation is successful.
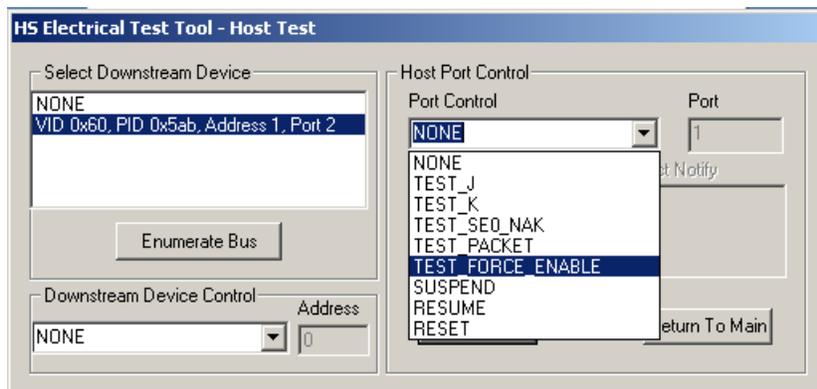
5. Click the Disconnect Notify check box to monitor the disconnect status in the Status Window.
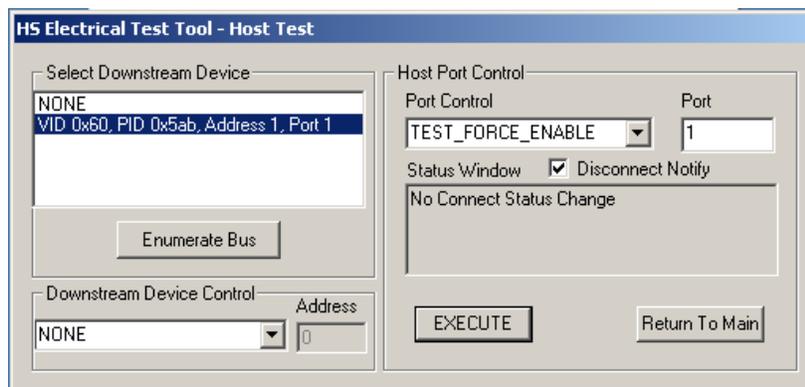
6. Using the oscilloscope, verify that the SOF packets are being transmitted from the port under test. The differential amplitude should be less than +/- 525 mV. Verify that the Status Window does not display Disconnect Event Detected. Record the pass/fail result in EL_37.

7. Set the TEST switch of the Disconnect test fixture to the Normal position and verify the yellow TEST LED (D2) is not lit.

8. Use the oscilloscope to monitor the differential amplitude of the SOF. It should be greater than +/- 625 mV. Verify that the Status Window now displays the Disconnect Event Detected. Record the pass/fail result in EL_36.
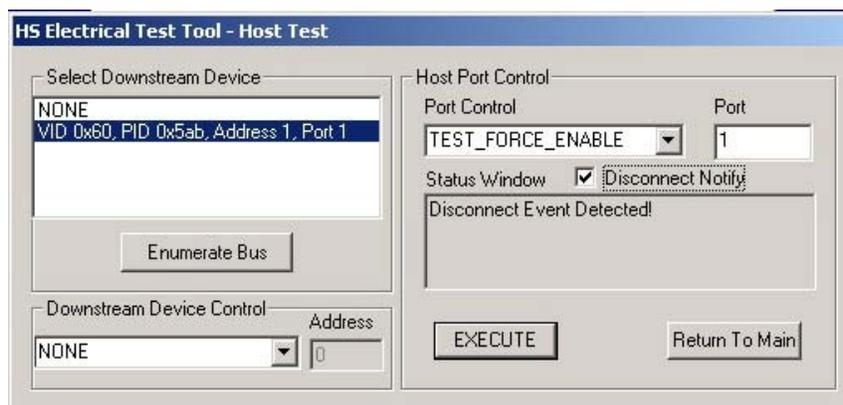
9. Return the TEST switch on the fixture back to the TEST position and verify the yellow TEST LED (D2) is lit.

10. Repeat steps 4 through 9 for all the remaining ports.

11. Remove the Disconnect test fixture from the port under test before proceeding.

4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.

2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds.

3. Launch the TDSUSB software application on the oscilloscope. For more details, refer to Starting the application.

4.   In the applications menu bar select, File> Recall Default Setup.

5. Within the USB2.0 compliance test application, select the High Speed tab.

6. Select Measurement > Select > Chirp on the TDSUSB2 application.

7. Click the Chirp button on the application and select Host option EL_33, EL_34. Click Run.

8. Connect the downstream facing port of the device under test into the TEST port of the test fixture.

9. Click Enumerate Bus using the High Speed Electrical Test Tool and capture the CHIRP handshake as in the following figure.

   Note: Instead of enumerating the device, an alternative method to generate the chirp signal, is to disconnect and reconnect the unit under test (device) to the port.
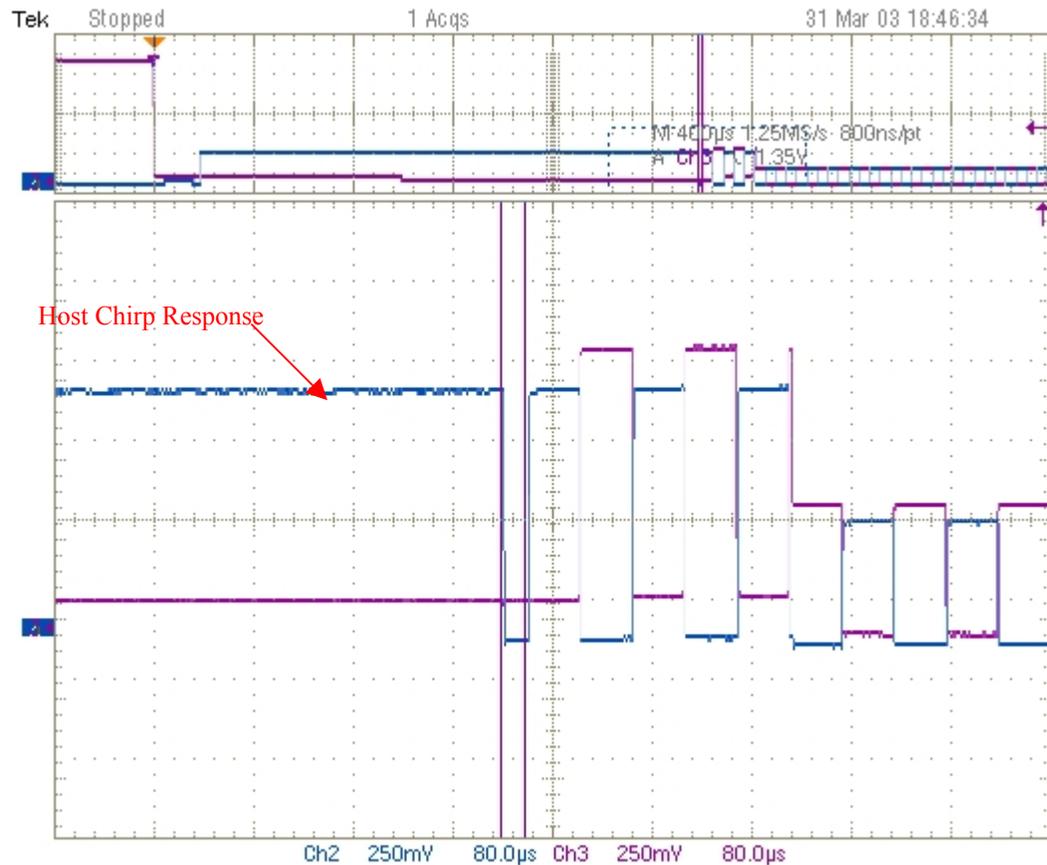
Figure 16: High Speed Chirp

10. The application measures the host's Chirp response timing (TWTRSTFS) EL_33.. This is the time between the device's de-assertion of Chirp-K and the start of alternate Chirp-K and Chirp-J sent by the host. The timing should be ≤ 100 μs.

11. The application measures (EL_34) and record the durations of the individual Chirp-K and Chirp-J states and verifies that both are between 40 μs ≤ TDCHBIT ≤ 60 μs (EL_31).

12. Click Chirp on the application and select Host option EL_35. Click Run.

13. Unplug the known good device and then reattach it.

14. Ensure the oscilloscope trigger is armed.

15. Click Enumerate Bus. The oscilloscope capture should appear as follows.

Figure 17: Time between SOF and Last Chirp- (J or K)

16. The application measures the time from the end of host Chirp-J/K to the first SOF sent out by the host. The result (EL_35) should be this $100\ \mu s \le TDCHSE0 \le 500\ \mu s$.

17. Repeat steps 5 through 16 for the remaining down stream facing ports.

4.8 Host Suspend/Resume timing (EL_39, EL_41)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the host port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.

2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36. Connect Channel 2 to D- and Channel 3 to D+. Connect the probe grounds to the outside pins of J36.

3. Select the High Speed measurement tab> More > Suspend measurement.

4. Set the input Signal Direction and run the measurements.

5. Attach the INIT port of the fixture into the port under test at the host controller.

6. On the Host Test menu, select SUSPEND from the Port Control dropdown menu and enter the port number. Click Execute once to place the port into suspend. The captured suspend transition should appear as in the following figure.
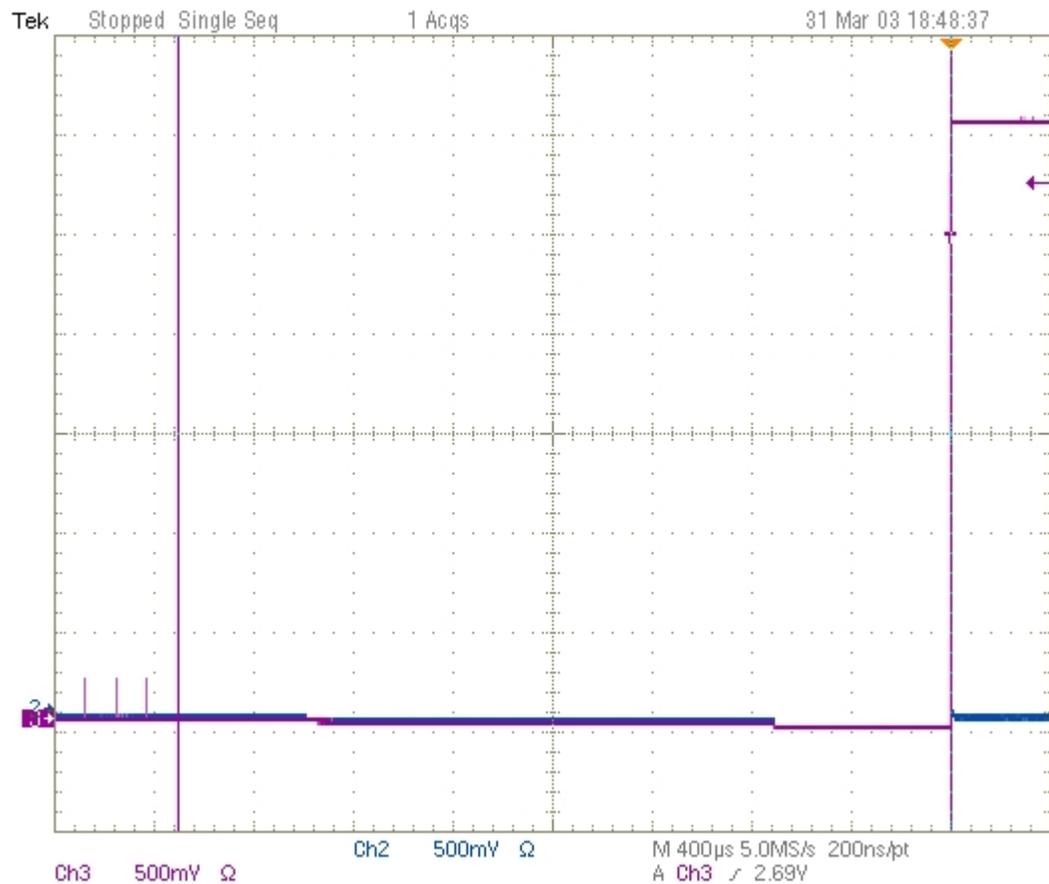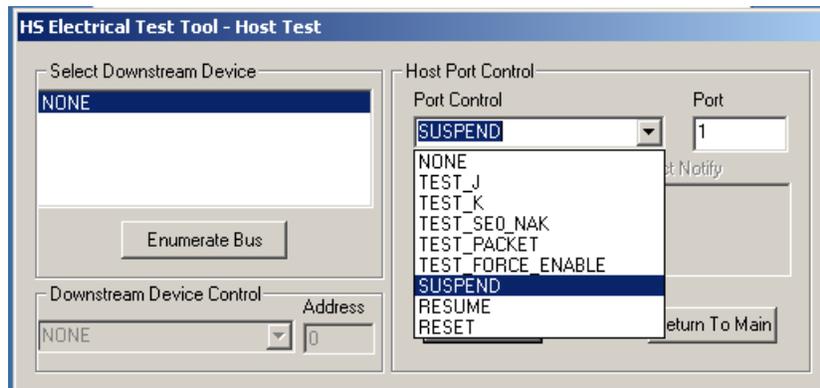
Figure 18: Device Enters Suspend

7. The result contains EL_39, which is the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+ (transition to full speed J-state). This time should be between 3.000 ms and 3.125 ms.

8. Select the High Speed measurement tab> More > Resume measurement.

9. Set the input Signal Direction and run the measurements.

10. On the Host Test menu, select RESUME from the Port Control dropdown menu and enter the port number. Click Execute once to resume the port. The captured suspend transition should appear as in the following figure.
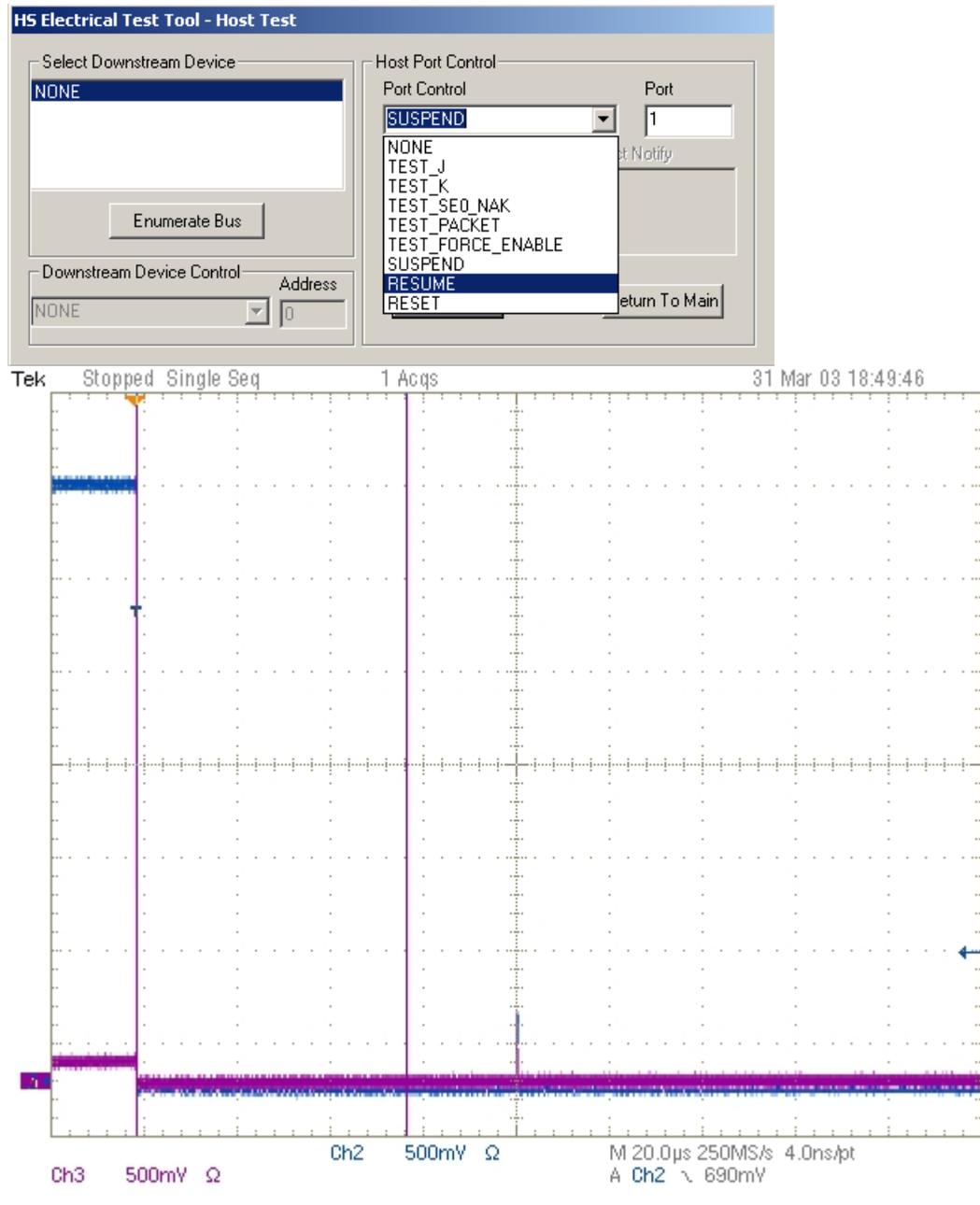
Figure 19: Time to First EOP from Start of HS Idle

11. The result consists of the time from the falling edge of D+ to the first SOF issued by the host (EL_41) as shown in the figure above. This is EL_41.

    Note: Repeat the suspend and resume a number of times and verify that the time from the falling edge of D+ to the first SOF issued by the host never exceeds 3 ms.

12. Repeat steps 4 through 9 for all the remaining ports.

13. Unplug the known good device from the test fixture. Click Enumerate Bus before proceeding. Remove the FET probes from the test fixture.

4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.

2. Select TEST_J from the Port Control dropdown menu. Enter the port number and click Execute once to place the port under test into TEST_J test mode.

Figure 20: Host Port TEST_J

3. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground (outside pins of J36 are the ground pins). Record in section EL_8.

4. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground. Record in section EL_8.

5. On the Host Test menu, select TEST_K from the Port Control dropdown menu. Enter the port number and click Execute once to place the port under test into TEST_K test mode.
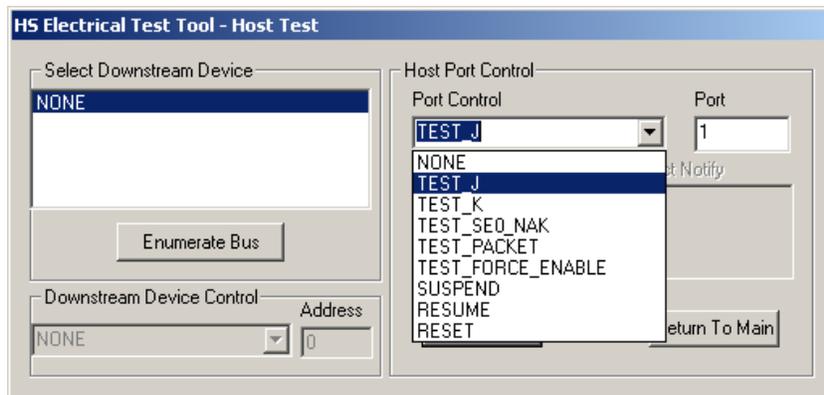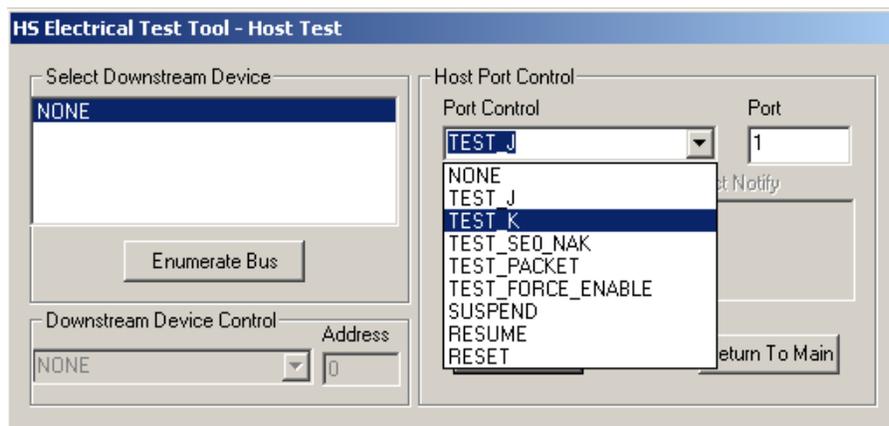

Figure 21: Host Port TEST_K

6. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_8.

7. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground. Record in section EL_8.

8. On the Host Test menu, select TEST_SE0_NAK from the Port Control dropdown menu. Enter the port number and click Execute once to place the port under test into TEST_SE0_NAK test mode.
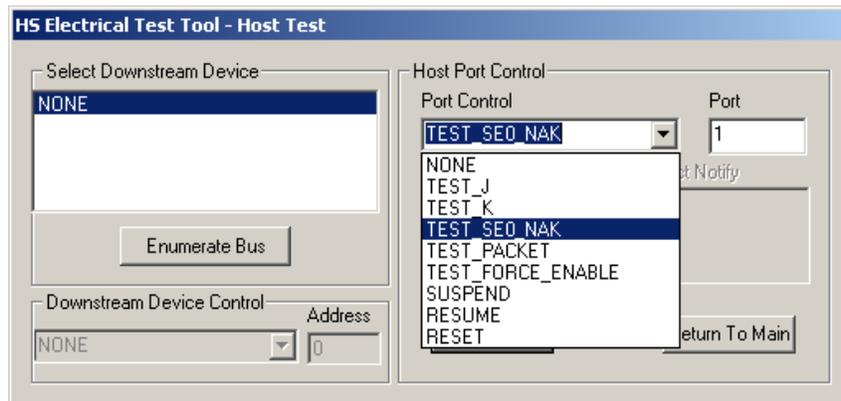

Figure 22: Host Port TEST_SE0_NAK

9. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_9.

10. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_9.

11. Repeat step 2 through 11 for the remaining ports.

Appendix A

A.1 Host High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.1.1 Vendor and Product Information

	Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information
Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.1.2   Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Downstream Ports					Comments
	P1	P2	P3	P4	P5	
LS SQ						
FS SQ						
Drop/Droop						
Interop						

P = PASS

F = FAIL

N/A = Not applicable

A.1.3   Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

EL_2   A USB 2.0 high-speed transmitter data rate must be 480 MBps ±0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

❑   Pass
❑   Fail
❑   N/A

Comments:

EL_3   A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measured at TP2 (each host downstream port).

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_6   A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_7   A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification, Section 7.1.2.2.*

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

❑ Pass

❑ Fail

❑ N/A

❑ Comments:

A.1.4   Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

EL_21   The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification, Section 8.2.*

SOF SYNC field

❑ Pass

❑ Fail

❑ N/A

Comments:

Data Packet SYNC field

❑ Pass

❑ Fail

❑ N/A

❑ Comments:

EL_25   The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (Note, that a longer EOP is waiverable)

Reference documents: *USB 2.0 Specification, Section 7.1.13.*

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_23   Hosts transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.

Reference documents: USB 2.0 Specification, Section 7.1.18.2.

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_22   When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: USB 2.0 Specification, Section 7.1.18.2.

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_55   Hosts transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

❑   Pass
❑   Fail
❑   N/A
❑   Comments:

A.1.5   Host Disconnect Detect (EL_36, EL_37)

EL_37   A USB 2.0 downstream facing port must not detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is <= 525 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

❑   Pass
❑   Fail
❑   N/A
❑   Comments:

EL_36   A USB 2.0 downstream facing port must detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≥ 625 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

A.1.6   Host CHIRP Timing (EL_33, EL_34, EL_35)

EL_33   Downstream ports start sending and alternating sequence of Chirp Ks and Chirp Js within 100 μs after the device Chirp K stops.

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_34   Downstream port Chirp K and Chirp J durations must be between 40 μs and 60 μs.

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

❑   Pass

❑   Fail

❑   N/A

❑   Comments:

EL_35   Downstream ports begin sending SOFs within 500 μs and not sooner than 100 μs from transmission of the last Chirp (J or K).

Reference documents: *USB 2.0 Specification, Section 7.1.7.5.*

❑   Pass
❑   Fail
❑   N/A
❑   Comments:

A.1.7   Host Suspend/Resume timing (EL_39, EL_41)

EL_39   A device must support the Suspend state.

Reference documents: *USB 2.0 Specification, Section 7.1.7.6.*

❑   Pass
❑   Fail
❑   N/A
❑   Comments:

EL_41   After resuming a port, the host must begin sending SOFs within 3 ms of the start of the idle state.

Reference documents: *USB 2.0 Specification, Section 7.1.7.7.*

❑   Pass
❑   Fail
❑   N/A
❑   Comments:

A.1.8   Host Test J/K, SE0_NAK (EL_8, EL_9)

EL_8   When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification, Section 7.1.1.3.*

Port	1		2		3		4		5	
Test	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
TEST_J										
TEST_K										

❑ Pass

❑ Fail

❑ N/A

❑ Comments:

EL_9   When either D+ or D- are not being driven, the output voltage must be 0 V ±10 mV when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification, Section 7.1.1.3.*

Port	1		2		3		4		5	
Signal	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
Measure WRT Ground (mV)										

❑ Pass

❑ Fail

❑ N/A

❑ Comments: