# Universal Serial Bus Implementers Forum Device High-Speed Electrical Test Procedure for Tektronix TDS7254/B, TDS7404/B, CSA7404/B, TDS6604/B, TDS6804/B, TDS6404, DPO7254, DPO7354, and DPO/DSA70000 series

Revision 1.4

Mar 2008

# Revision History

| Rev | Date | Filename | Comments |
|---|---|---|---|
| 0.8 | 26-Jun-2001 | Device HS Test.DOC | Initial draft revision |
| 0.81 | 12-Jul-01 | Device HS Test.DOC | Changed el_17 on page 34 to reference Section 7.1.6.2. |
| 0.9 (Beta) | Aug-31-2001 | Device HS Test.DOC | Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; remove TDR test; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification |
| 1.0 | Dec-23-2001 | Device HS Test.DOC | Edit for final release. |
| 1.1 | August 27 -2002 | Device HS Test.DOC | Edit to add procedures to accommodate testing using the Tektronix TDS7000 series oscilloscopes and TDSUSB, USB compliance test application |
| 1.2 | April 1, 2003 | Device HS Test Tektronix.doc | Edit and clean up – for publication |
| 1.3 | Feb, 2007 | Device HS test tektronix.doc | Changes made according to the new test fixture. |
| 1.4 | Mar, 2008 | Device HS test tektronix.doc | Updated the model numbers. |
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# USB-IF High-speed Electrical Test Procedure

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# Table of Contents

# 1 Introduction

The USB 2.0 Compliance Committee under the direction of USB-IF, Inc. develops the USB-IF High-speed Electrical Test Procedures. There are three High-speed Electrical Test Procedures.

- The Host High-speed Electrical Test Procedure is for EHCI host controllers.
- The Hub High-speed Electrical Test Procedure is for high-speed capable hubs.
- The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

This test procedure is an update of the USB-IF Host Electrical High-speed Test Procedure written for the Tektronix TDS694C and the USB-IF MATLAB scripts. This updated procedure is written to support Tektronix TDS7404/B, CSA7404/B, TDS7704B, TDS7254/B, TDS6604/B, TDS6804/B, TDS6404, DPO7254, DPO7354 and DPO/DSA70000 series running TDSUSB2 Compliance Test Application Software. TDSUSB2 software is used in place of the MATLAB scripts and NI GPIB DAQ software.

# 2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high speeds. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one-of-a-kind prototype of peripherals, add-in cards, motherboards, or systems.

This test procedure refers to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.3.

This Device High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Host High-speed Electrical Test Procedure and Hub High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

# 3 Recommended Equipment

The commercial test equipments listed here are based on the positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models used to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

- Digital Phosphor Oscilloscope:
  - Tektronix TDS7404/B or CSA7404/B or TDS7704B, TDS7254/B, DPO7054, DPO7104, DPO7254, DPO7354, DPO/DSA70404, DPO/DSA70604 and DPO/DSA70804
    - A DPO7254, DPO7354, TDS7254/B, TDS7404/B or CSA7404/B or TDS7704B, or greater bandwidth oscilloscope is required to test the high-speed USB hosts, devices, or hubs
    - A DPO7054 or TDS5034B or greater bandwidth oscilloscope is required to test low-speed and full-speed USB devices and hubs
    - A P6330 or P6248 1.7 GHz differential probe or greater bandwidth probe. For example, P63301, P7330, P7360, P7380
    - For use with DPO7000 series:

      TDP1500 or TDP3500 (3 each)

      TAP1500 1.5 GHz Active Probe (3 each)

      P6248, P6330, or P6245 1.5 GHz 10X Probe (3 each) [1]
    - A TCP202 current probe[1] or TCP0030 current probe for use with the DPO7000 series oscilloscopes

      [1]Requires TPA to BNC adapter for use on DPO7000 series oscilloscopes
- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent

  Mini-clip DMM lead – one each of black and red
- Digital Signal Generator
  - Tektronix DTG5334, DTG5274, or DTG5078 with a DTGM21 Output module; or the AWG 5000 series (AWG5002) or AWG7000 series
    - 5x attenuator – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2
    - 50-ohm coaxial cable with female SMA connectors at both ends, qty = 4
- High-speed USB Electrical Test Fixtures
  - Tektronix TDSUSBF test fixture, qty = 1

    *6-INCH AB Cable with USB-IF compliance logo tag, qty =1

    *Female Serial B to female Serial A adapter, qty = 1

    *Included with Tektronix TDSUSBF test fixture
- Miscellaneous Cables

  1M USB cable, qty = 5
- High-speed USB Test Bed Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. The OS on this computer is Windows 2000 or XP Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

**Note:** The Tektronix USB compliance test software operates internally to the oscilloscope and automatically configures the oscilloscope settings so that external GPIB control of the oscilloscope is not required.

## 3.1 Equipment Setup

### 3.1.1 TDS7000, DPO7000 and DPO/DSA70000 series oscilloscopes

Before turning on the oscilloscope, attach a P6330or P6248 differential probes to Channel 1 and Channel 4. TPA-BNC adaptors are required for the DPO7000 series. Attach two P6245 FET/TAP1500 probes, one to Channel 2 and one to Channel 3. This probe assignment will be used throughout the test procedure. Turn on the oscilloscope to allow for 20 minutes of warm up time before use. Perform the signal path compensation procedure built into the oscilloscopes (in the Utility menu) if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the differential probes should be cancelled using the Deskew utility of the TDSUSB software. From the TDSUSB application, select Utilities> Deskew. Follow the procedure in the applications online help.

For the P6248 differential probes, the following setting will be used throughout the test procedure:

Attenuation <÷1>

The use of a Tip Saver accessory on the P6248 probe is highly recommended to prolong the probe tip life. Please note that the Tip Saver will wear out after repeated use and start degrading signal quality measurements. Replace the Tip Saver when measurements made without it provide better results.

**Note:** In certain test situations, there may not be a ground connection between the oscilloscope and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the oscilloscope ground to the DUT ground is required to establish a common ground reference.

### 3.1.2 Digital Signal Generators

A digital signal generator (For example, Tektronix DTG5334, DTG5274 or DTG5078 with a DTGM21 output module; or the AWG 5000 series or AWG7000 series) is needed to perform the receiver sensitivity test that is described toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the digital signal generator about 15 minutes before performing the measurement.

## 3.2 Operating Systems, Software, Drivers

### 3.2.1 Operating Systems

Microsoft Windows 2000 or XP Professional is required on the High-speed Electrical Test Bed Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

## 3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.
- Proprietary EHCI Driver Stack – The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. Using this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result is a much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon starting of the HS Electrical Test Tool application software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exiting the HS Electrical Test Tool application software, the driver stack will automatically switch to the Microsoft EHCI driver stack.
- TDSUSB2 – Tektronix USB2.0 Compliance Test Software Application

## 3.4 Starting the Application

For the TDS series oscilloscopes, select File> Run Application> USB2.0 Test Package. For the TDS B and C series oscilloscopes, select App> USB2.0 Test Package from the menu bar to run the application. For the DPO series oscilloscopes, select Analyze> USB2.0 Test Package.

## 3.5 Test fixture

The table matches the pins of the two most recent versions of TDSUSBF test fixtures. This procedure document is based on using the pin locations of the "New Fixture" shown in the following table.

| Section | Old Fixture | New Fixture |
|---|---|---|
| Device SQ section | J36 | J310 |
| | - | J31 |
| | J34 | J34 |
| Device Receiver Test | J38 | J35 |
| | J29 | J25 |
| | J31 | J27 |
| | J30 | J24 |

| DUT | Test | Position DUT | Position Probe | Test Mode |
|---|---|---|---|---|
| High-Speed Device | SQ | J34 | J310 | Upstream |
| | Packet Parameter | J34 | J31 | |
| | Chirp | J34 | J31 | |
| | Suspend | J34 | J31 | |
| | Resume | J34 | J31 | |
| | Reset | J34 | J31 | |
| | J | J34 | | |
| | K | J34 | | |
| | SE0_NAK | J34 | | |
| | Receiver Sensitivity | J28 | J25 | |

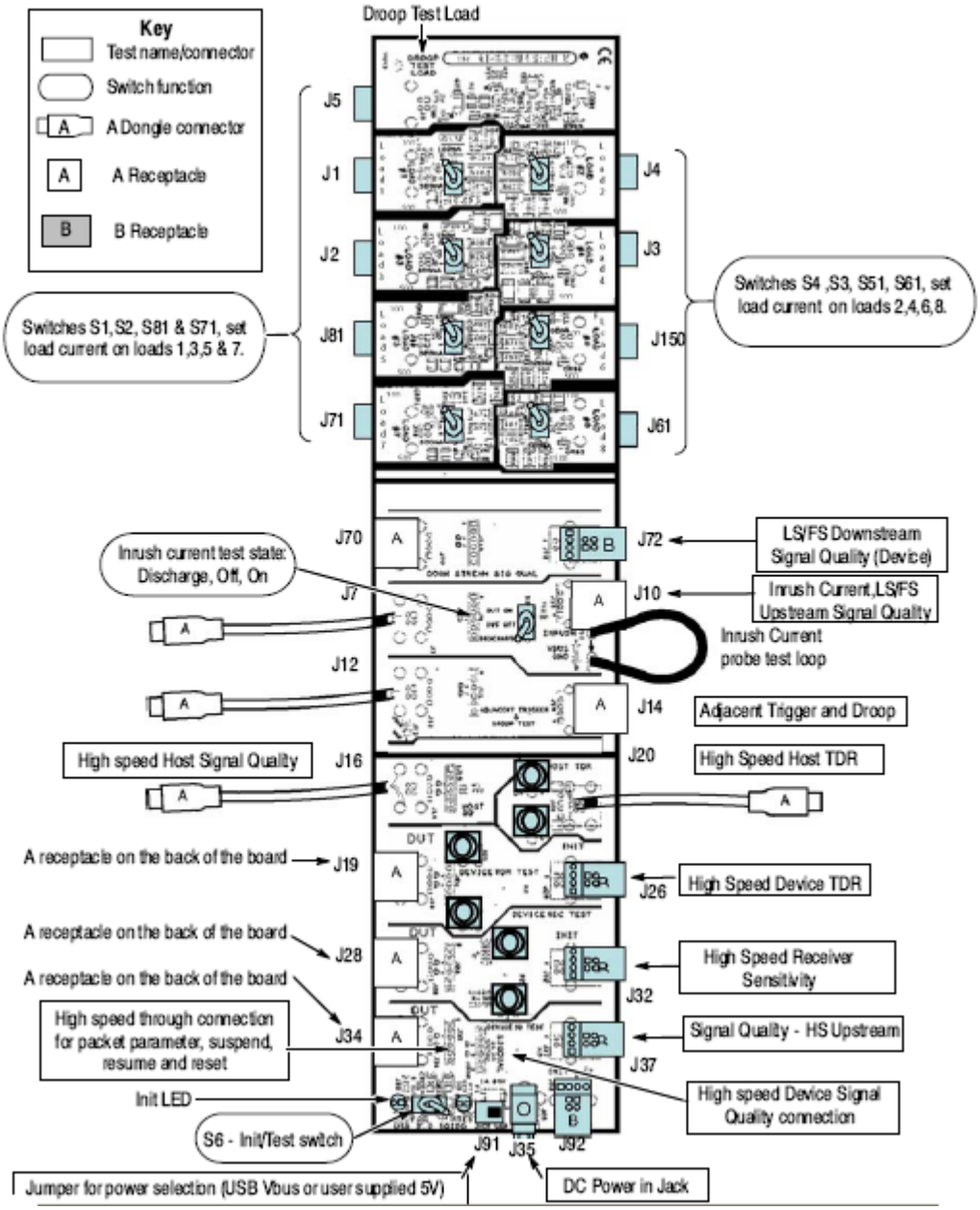


Figure 1: Tektronix TDSUSBF Test Fixture

# 4 Test Procedure

## 4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop as applicable) shall be retained for compliance test submission.

## 4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

- Test date
- Vendor name
- Vendor address and phone, and the contact name
- Test submission ID number
- Product name
- Product model and revision
- USB silicon vendor name
- USB silicon model
- USB silicon part marking
- USB silicon stepping
- Test conducted by

## 4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the device under test must also pass the following compliance tests applicable to high-speed capable device:

- Full speed signal quality
- Back-drive voltage
- Inrush current
- Interoperability

Perform all these tests, record the measurements and summarize the Pass/Fail status in Appendix A.

## 4.4 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

**Note:** Please take care in determining if the device under test incorporates a captive cable, or it has a normal series B or mini-B receptacle. Captive cable designs require the signal quality measurement to be made at the far end (hsfe). Detachable cable designs require the measurement to be made at the near end (hsne).

1. Turn on the oscilloscope if you have not already done so. Allow about 20 minutes for warm up.
2. Launch the TDSUSB software application on the oscilloscopes. For more details, refer to Starting the application.
3. Press the Default Setup button on the oscilloscope front panel.
4. In the applications menu bar select, File> recall default.
5. Within the Measurement select menu of the USB2.0 compliance test application, select the High Speed tab.
6. Within the Signal Quality area of the application, select the High Speed Signal Quality tests> Eye Diagram, Signal Rate, Rise time, Fall Time, and EOP Width.

   **Note:** The Monotonic property test is available but not required as it may generate false failures due to slight variations in the signal edge due to high frequency noise and/or scope quantization error.

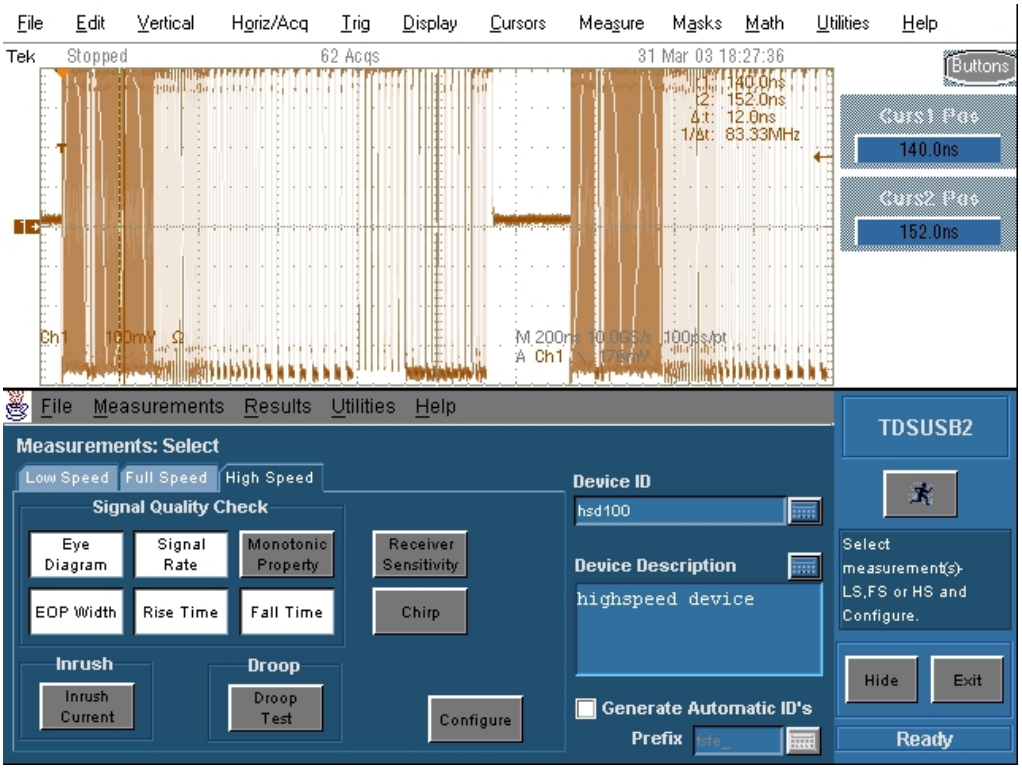


Figure 2: Tektronix TDSUSB Software

7. Enter a device ID (for example, TIDxxxxxxx USNE.tsv) in the device ID dialog box and a device description in the device description dialog box.

8. Press Configure on the application screen. Select upstream and far end for devices with captive cables or near end for devices without a captive cable.
9. Press the  icon. Verify that the oscilloscope display is NOT reporting “clipping”. If it is, adjust the vertical amplitude until the “clipping” message does not appear. Do not press OK on the screen until the correct waveform is displayed.
10. Attach the USB cable to the designated power supply port of the compliance test fixture.
11. Verify that red Power LED and the red Init LED are lit.
12. Connect the upstream facing port of the device under test to USB connector of the Device SQ segment of the test fixture. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device.
13. Attach the differential probe to J310 of the test fixture. Ensure that the + polarity on the probe lines up with D+ on the fixture.

14. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.

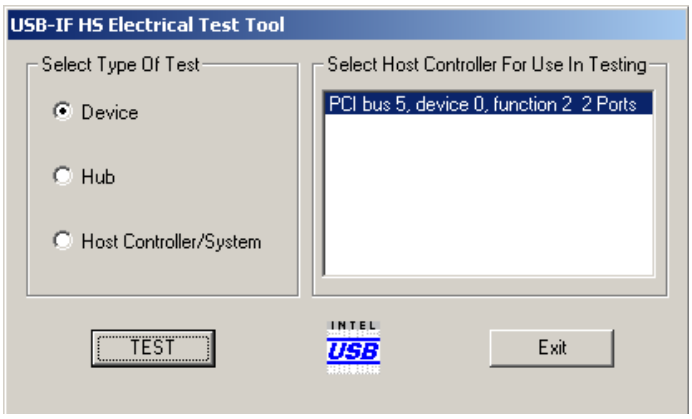


Figure 3: High-speed Electrical Test Tool – Main Menu

15. Select Device and click TEST to enter the HS Electrical Test Tool application - Device Test menu. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

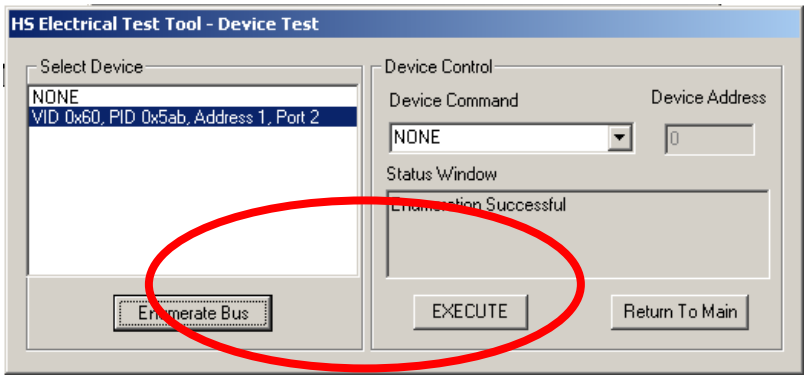


Figure 4: High-speed Electrical Test Tool – Device Test Menu

16. Select TEST_PACKET from the Device Command dropdown menu and click EXECUTE. This forces the device under test to continuously transmit test packets.

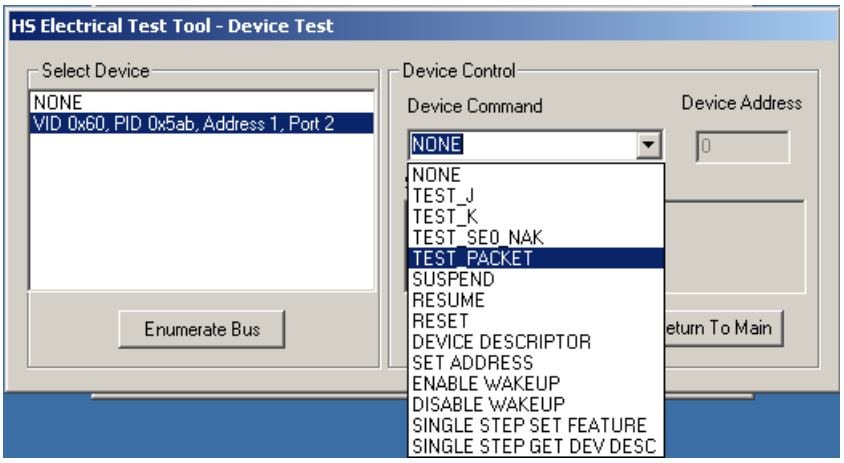


Figure 5: Test Device Packet

17. Place the Test Switch (S6) in the TEST position. Verify that the red TEST LED is lit.
18. Using the oscilloscope, verify that test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try a slight change to the trigger holdoff.
19. Once the test packet is displayed properly, press OK in the application dialog box.
20. The Tektronix USB application generally triggers and displays the correct test packet without the need to place cursors. Should cursors be required they can be enabled from the application by selecting, File> Preferences> Advanced and clicking the option “Packet Identification by user using Cursors”.

21. If cursors measurement is enabled (see step 17) on the oscilloscope, place the two vertical cursors around one test packet. Place one cursor just before the sync field (about one bit time) and the other cursor just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure. Press OK on the USB2 application dialog box to begin acquisition and analysis of the test packet.

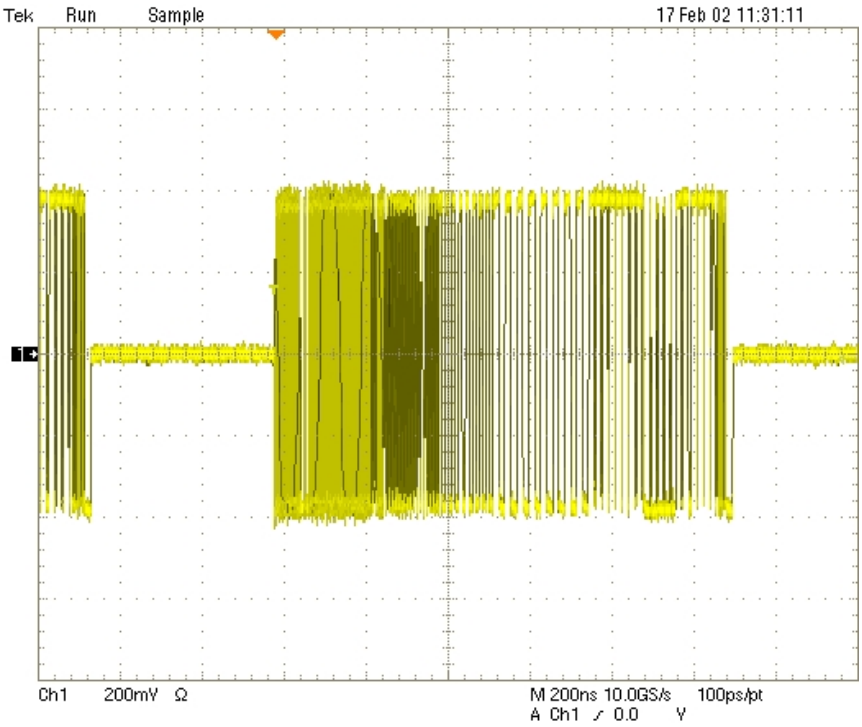


Figure 6: Test Packet from Device

22. Verify that the Signal Eye, EOP Width, Rise and Fall time and Signaling Rate all pass. The results displayed on oscilloscope can also be recorded to an HTML report located on the oscilloscope hard drive at the following path: C:\TekApplications\tdsusb2\report. For more details, refer to the Report Generator section of TDSUSB2 Online Help.

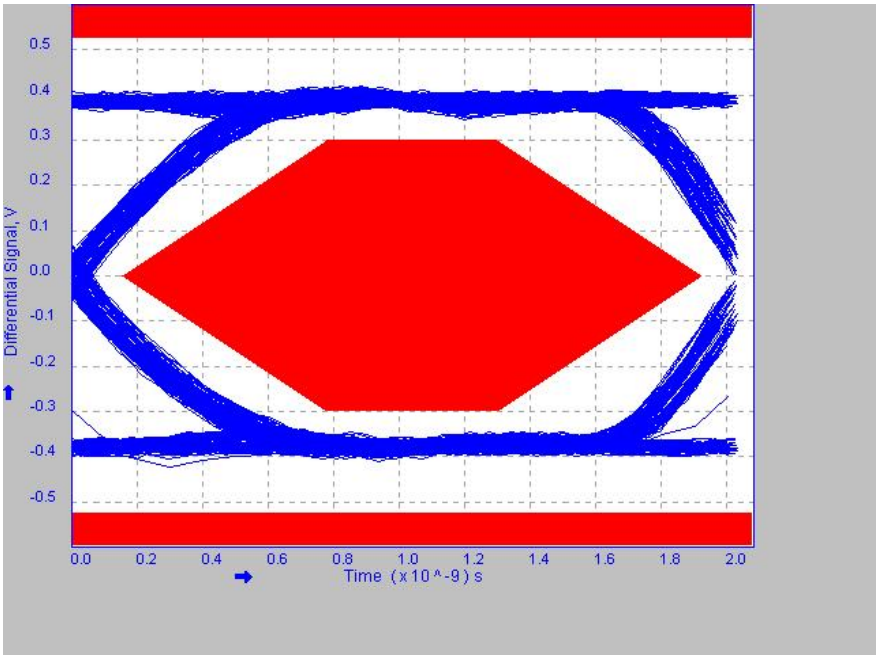


Figure 7: High-speed Near End SQ Eye Diagram

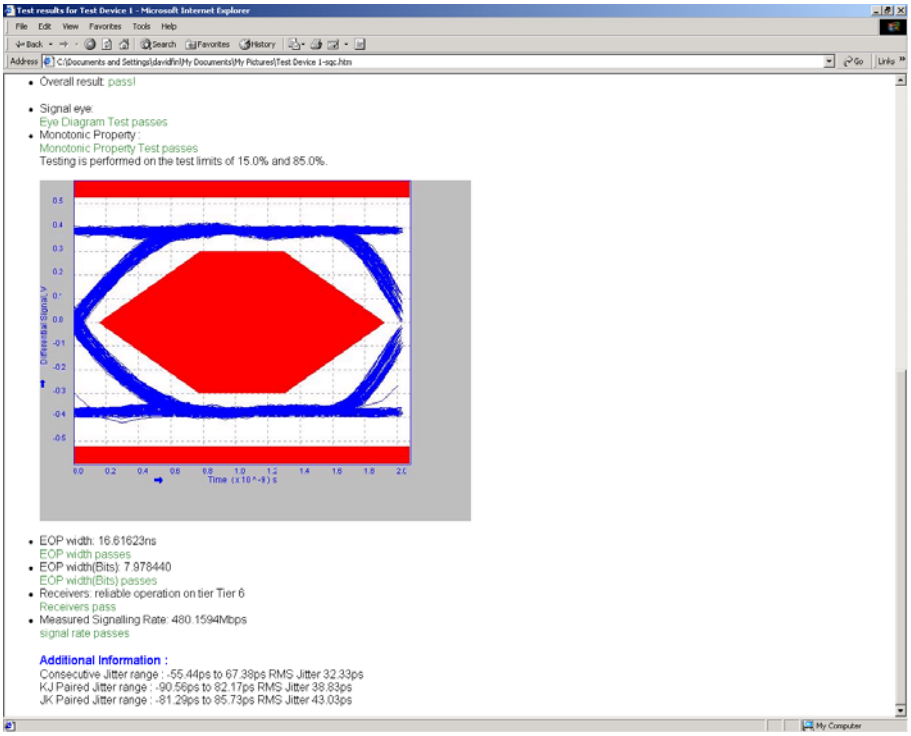


Figure 8: High-speed SQ HTML Report

23. Save all the report files created during the tests. The report contains the test result in EL_2, EL_4 or EL_5, EL_6 and EL_7.

    **Note:** EL_4 and EL_5 requirements are mutually exclusive. If EL_4 is tested then EL_5 is not applicable, and vice versa.

24. Return the Test switch (S6) of the test fixture to the Normal position and verify the Red TEST LED is not lit. Recycle power of the device to prepare for subsequent tests.

## 4.5 Device Packet Parameters (EL_21, EL_22, EL_25)

1. Connect the Init port of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.
2. Connect the upstream facing port of the device under test to the USB connector of the Device SQ segment of the test fixture. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device. Verify that the device enumerates properly.

   **Note:** The use of the Signal Quality segment of the compliance test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the differential probe to J31 on the fixture near the device connector. Ensure that the + polarity on the probe lines up with the D+ on the fixture.
4. Use the oscilloscope to verify that, SOFs (Start Of Frame packets) are being transmitted on the port under test.
5. Select Packet Parameter measurement from the High-Speed tab and configure the device for EL_21, EL_22, and EL_25. Run the measurements.

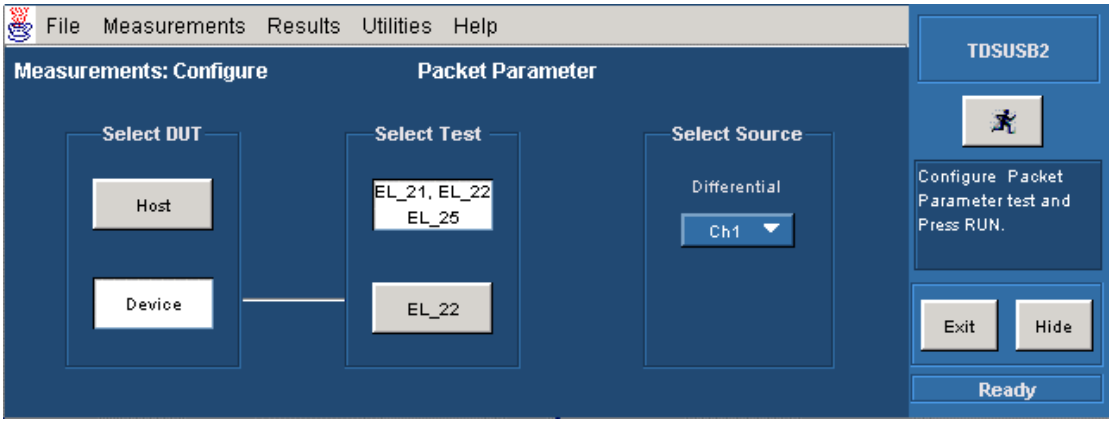


Figure 9: Device Packet Parameter

6. Use the oscilloscope to verify that, SOFs (Start Of Frame packets) are being transmitted on the port under test.

7. In the HS Electrical Test Tool application- Device Test menu of the High-speed Electrical Test Tool application software. Ensure that the device under test is selected (highlighted). Select SINGLE STEP SET FEATURE from the Device Command window and click EXECUTE once.

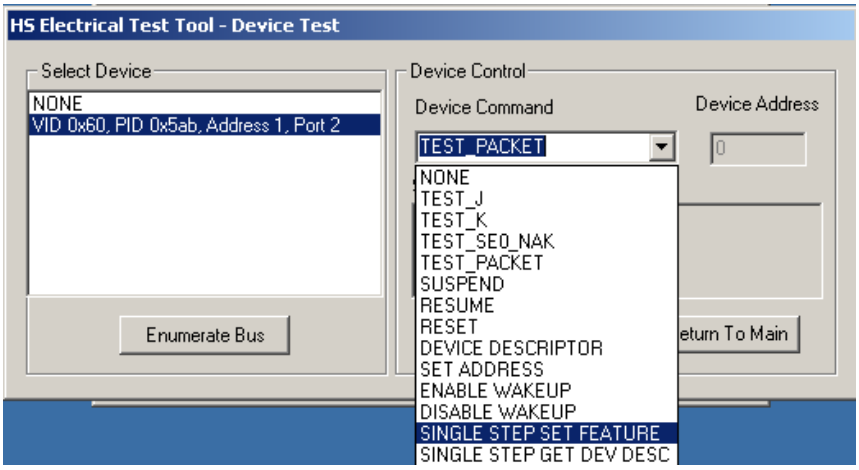


Figure 10: Device Single Step Set Feature

8. The oscilloscope capture should appear as follows:

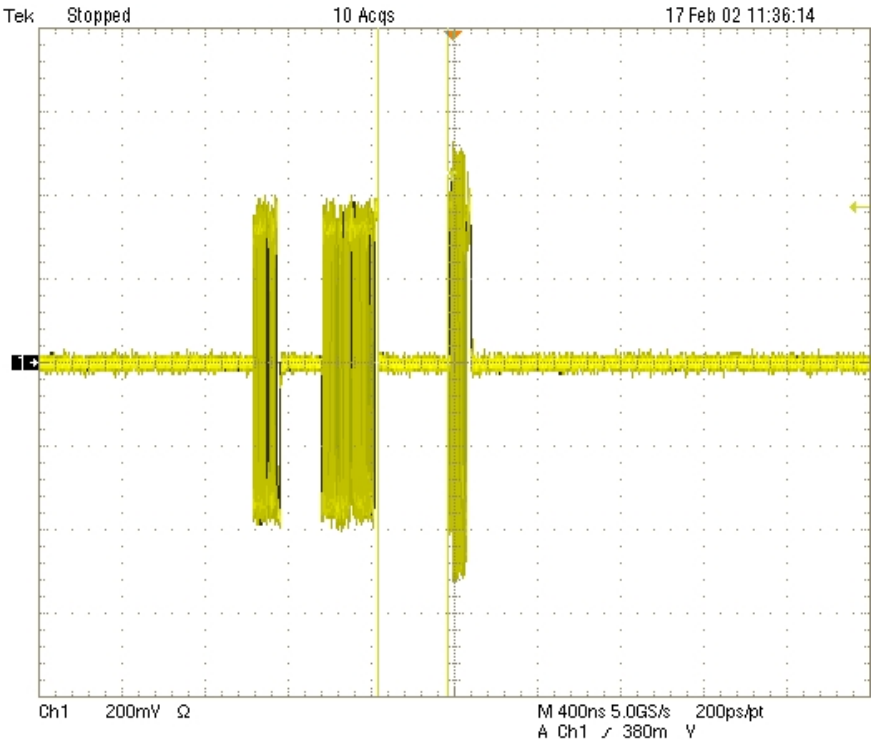


Figure 11: Host and Device Packets

9. From the application menu, select Results> Summary. Click any of the test result buttons to get the details of that test.

10. The result contains EL_21 sync field length (number of bits) of the third packet (from device) on the oscilloscope and it should be of 32 bits. Refer to the following figure. Note that the Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero).

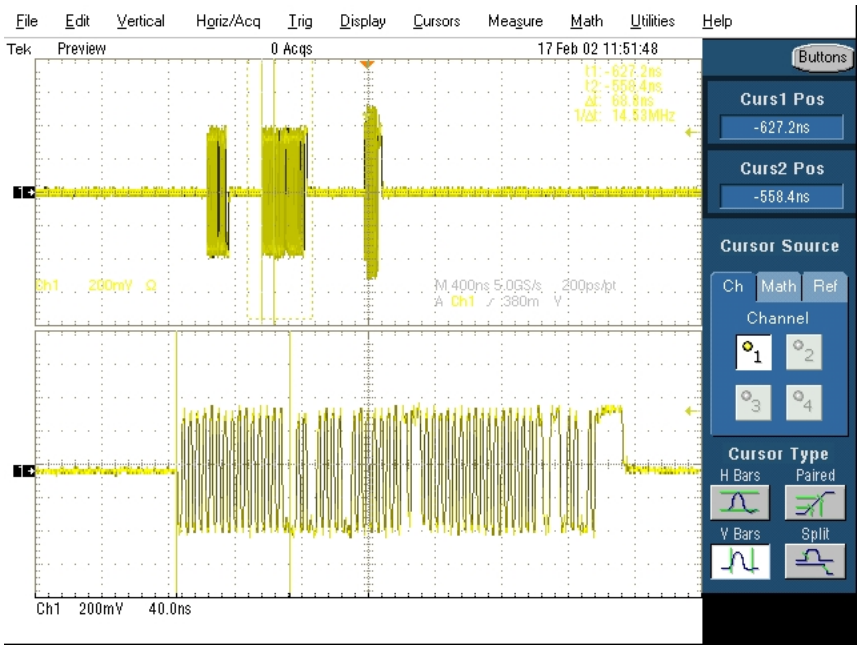


Figure 12: Sync Field – Device Packet

11. The results consist of EL_25 EOP (End of Packet) width (number of bits) of the third packet on the oscilloscope.

    **Note:** EOP could appear as a negative going pulse, or a positive going pulse on differential measurements. The following figure illustrates the appearance of a negative going EOP.

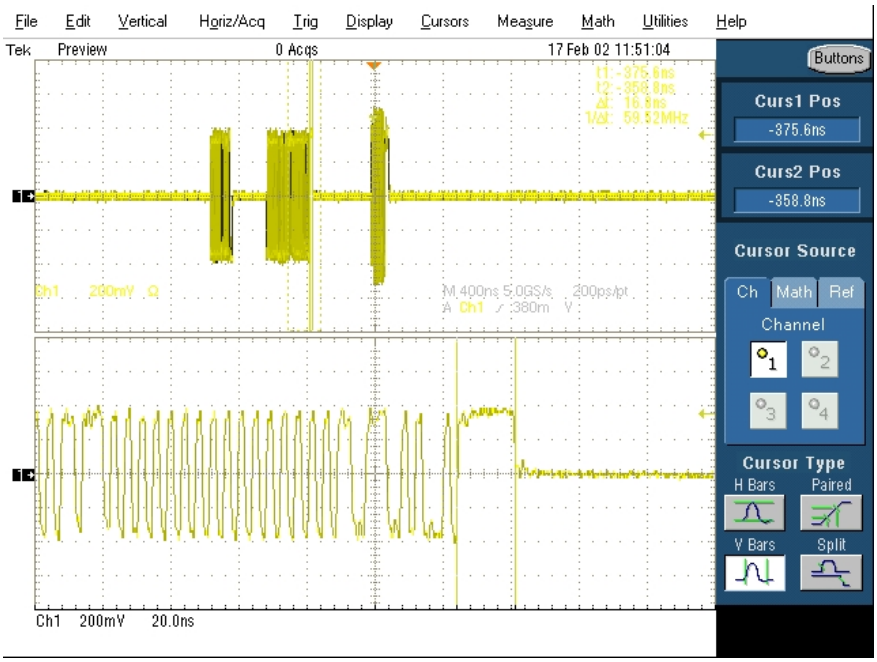


Figure 13: EOP in Device's Packet

12. The results consist of EL_22 inter-packet gap between the second (from host) and the third (from device in response to the host's) packets are shown on the oscilloscope. The second (of lower amplitude) is from the host and the third (of higher amplitude) is a device's response.

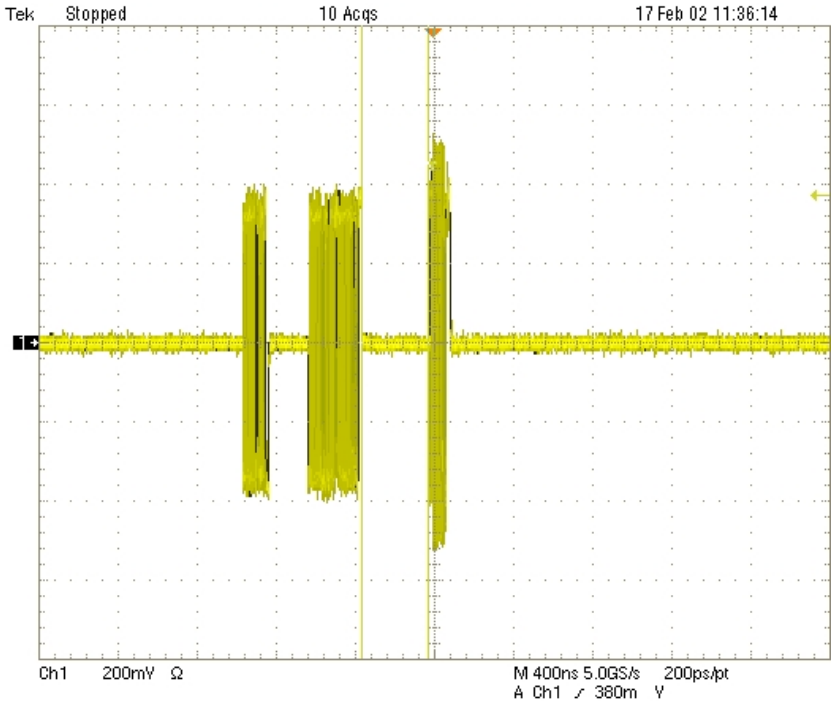


Figure 14: Device Inter-packet Gap

13. Select Packet Parameter measurement from the High-Speed tab and configure for device EL_22 and run the measurements.
14. Ensure that the oscilloscope is armed. In the HS Electrical Test Tool application- Device Test menu, click Step once. This is the second step of the two-step Single Step Set Feature command.

15. The oscilloscope capture should appear as follows:

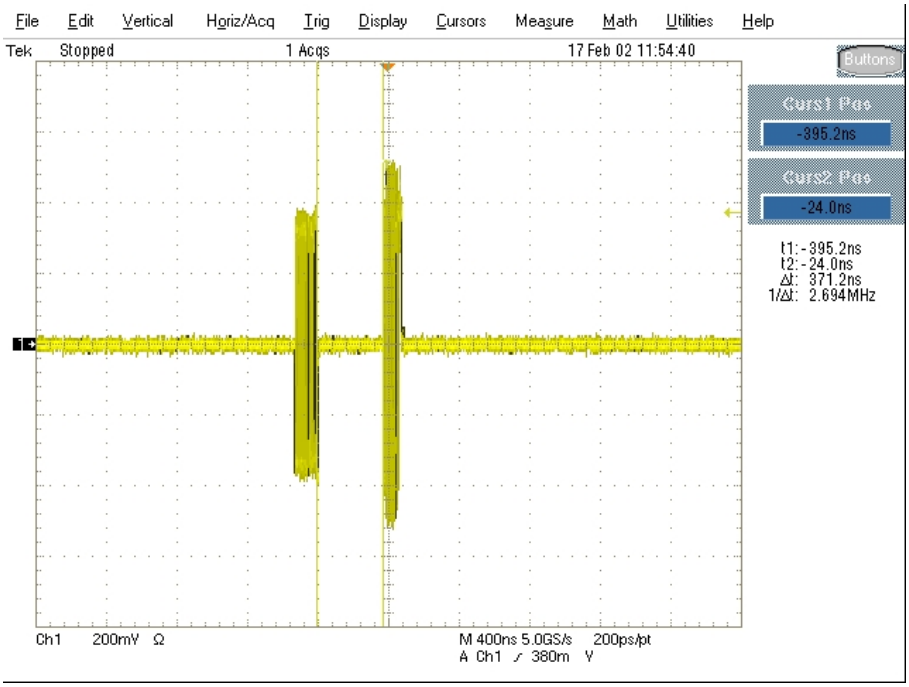


Figure 15: Single Step Set Feature – Second Step

16. The results consist of EL_22 inter-packet gap between the first (from host) and the second (from device in respond to the host's) packets shown on the oscilloscope. The first (of lower amplitude) is from the host and the second (of higher amplitude) is a device's response.
17. Detach the differential probe from the Device High-Speed Signal Quality test fixture.

## 4.6 Device CHIRP Timing (EL_28, EL_29, EL_31)

1. Connect J34 of the Device SQ segment of the test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J31. Connect Channel 2 to D- and Channel 3 to D+. Connect the probe grounds.
3. Launch the TDSUSB software application on the oscilloscopes. For more details, refer to Starting the application.
4. In the applications menu bar select, File> Recall default.
5. Within the USB2.0 compliance test application, select the High Speed tab.
6. Click the Chirp button on the application and select the Device option EL_28, EL_29, EL_31. Click Run.

7. Connect the upstream facing port of the device under test into the TEST port of the test fixture.
8. Click Enumerate Bus and capture the CHIRP handshake as in the following figure. The results can be viewed on the results panel.

   **Note:** Instead of enumerating the device, an alternative method to generate the chirp signal, is to disconnect and reconnect the unit under test (device) to the port.


Figure 16: Device Chirp (Speed Detection)

9. The EL_28 checks the devices CHIRP-K latency in response to the reset from the host port. The time should be between 2.5 µs and 6.0 ms.

   **Note:** The test specification rev 1.0 contains an error regarding EL_28 at the time this test procedure was written. It states that the measurement time must be 2.5 µs to 3.0 ms, which is incorrect. The specification requires the CHIRP-K latency to be between 2.5 µs and 6.0 ms.

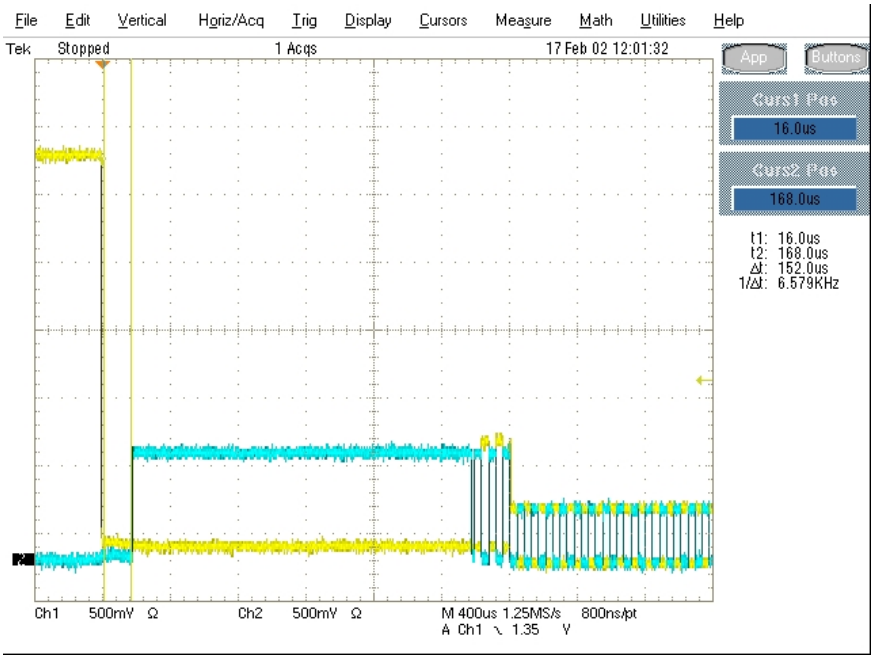


Figure 17: Device Chirp-K Latency

10. The EL_29 checks the device's CHIRP-K duration. The assertion time should be between 1.0 ms and 7.0 ms.

11. Following the host assertion of Chirp K-J-K-J-K-J, the device must respond by turning on its high-speed terminations. This is evident by a drop of amplitude of the alternate Chirp-K and Chirp-J sequence from the 800 mV nominal to the 400 mV nominal. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the device turns on the high-speed terminations. It should be less than or equal to 500 µs. This is EL_31.

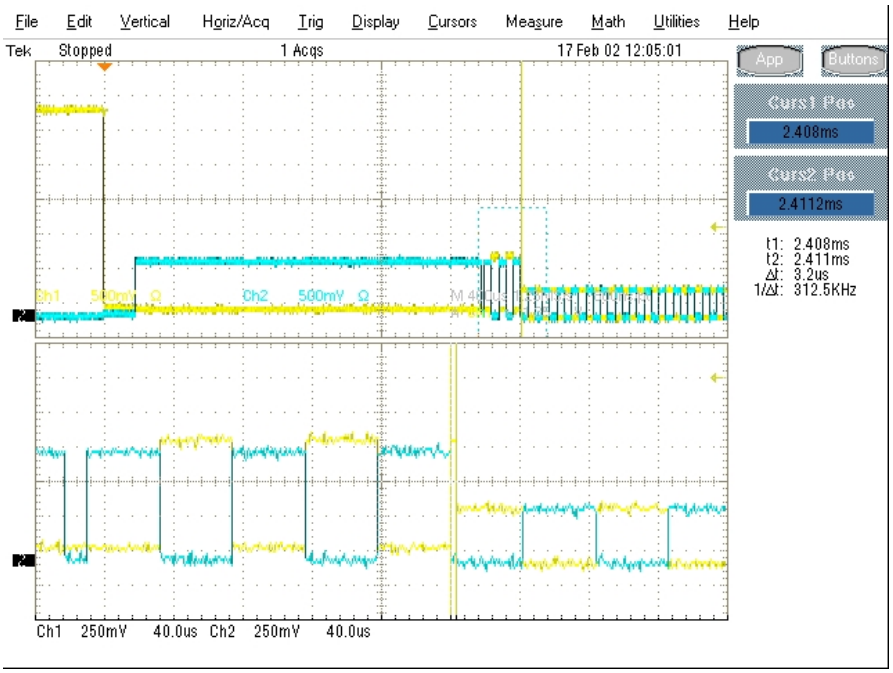


Figure 18: Time From Start of Last J in Chirp K-J-K-J-K-J To Device Turns on HS Termination

12. In addition to turning on its high-speed terminations, the device must also disconnect the D+ pull-up resistor in response to the host's assertion of Chirp K-J-K-J-K-J. The evidence is a slight drop of the D+ level during the Chirp-K from the host. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the D+ pull-up resistor is disconnected. Verify that this is less than or equal to 500 µs. Record the measurement in EL_31.

## 4.7 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

1. Plug the Init port of the test fixture of High Speed Signal Quality test section into a high-speed capable port of the test bed computer.
2. Connect the device under test into the Test port of the test fixture. Click Enumerate Bus to enumerate the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect Channel 2 and Channel 3 FET probes to the test fixture at J31. Connect Channel 2 to D- and Channel 3 to D+. Connect the probe grounds.
4. Select the High Speed measurement tab> More button> Suspend measurement.

5. Set the input Signal Direction and run the measurements.
6. On the HS Electrical Test Tool application - Device Test menu, select SUSPEND from the Device Command dropdown menu. Click EXECUTE once to place the device into suspend. The captured suspend transition should appear as in the following figure.

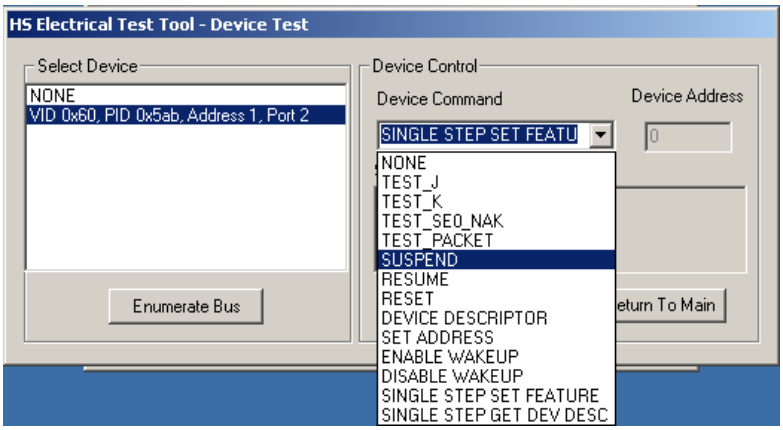


Figure 19: Device Suspend

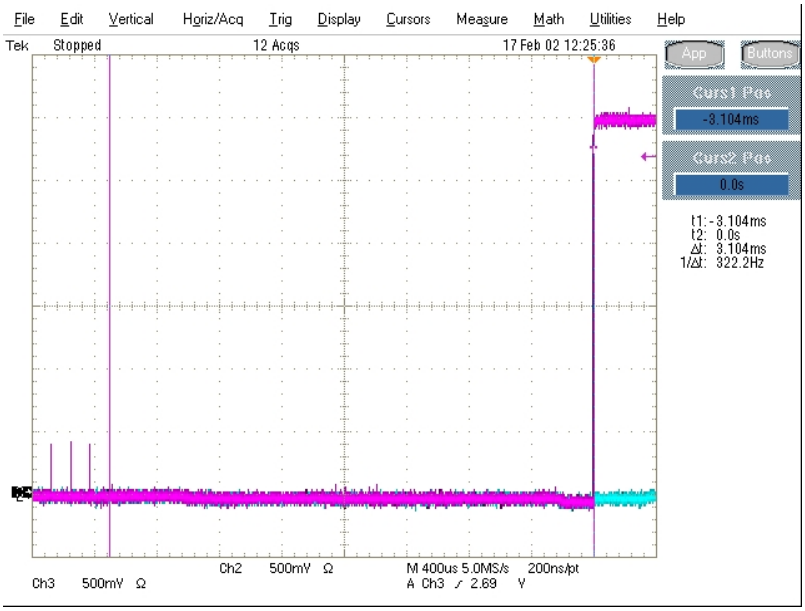


Figure 20: Device Respond to Suspend from High-speed

7. The result contains EL_38, which is the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. The time should be between 3.000 ms and 3.125 ms.

The following steps verify the Resume response of the device under test:

1. Select the High Speed measurement tab> More button> Resume measurement.
2. Set the input Signal Direction and run the measurements.
3. On the HS Electrical Test Tool application - Device Test menu, select RESUME from the Device Command dropdown menu. Click EXECUTE once to resume the device from suspend. The captured resume transition should appear as in the following figure.

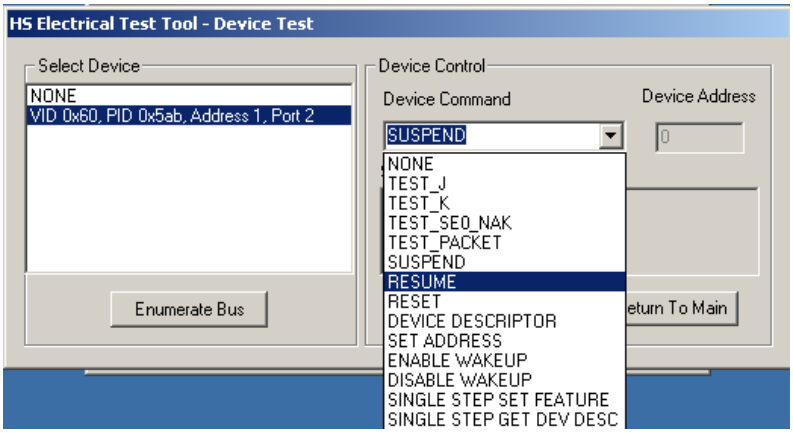


Figure 21: Device Resume

4. The result consists of the time between the falling edge of D+ and the First SOF. This should not exceed 3.0 ms. The device should resume the HS operation, which is indicated by the presence of HS SOF packets (with 400 mV nominal amplitudes) following the K State driven by the host controller. See the following figure. This is EL_40.


Figure 22: Device Resume to High-speed

The following steps verify that the device resumes back to back to high-speed operation after being reset from high-speed operation.

1. Select the High-Speed measurement tab> More button> Reset High Speed measurement.
2. On the HS Electrical Test Tool application - Device Test menu, select RESET from the Device Command dropdown menu. Click EXECUTE once to reset the device operating in high-speed. The captured reset response should appear as in the following figure.

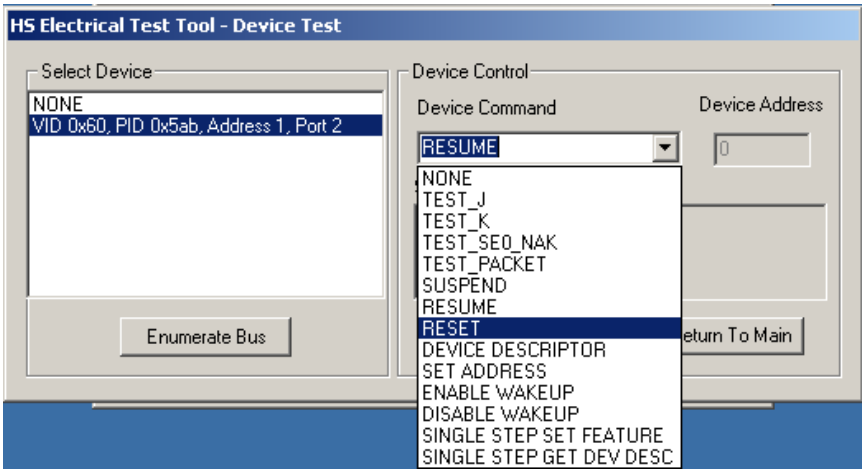


Figure 23: Device Reset

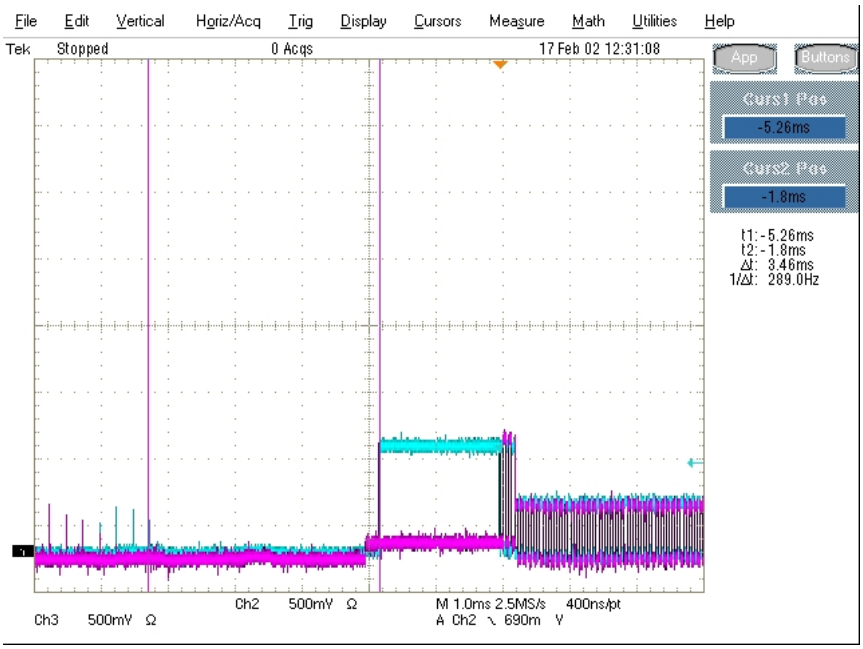


Figure 24: Device Chirp-K in Response to Reset from High-speed

3. The results contain the time between the beginning of the last SOF before the reset and the start of the device chirp-K. The device should transmit a chirp handshake following the reset. It should be between 3.1 ms and 6 ms. This is EL_27.

The following steps verify the device's chirp response after being reset from suspend:

1. Select the High-Speed measurement tab> More button> Reset from Suspend measurement.
2. On the HS Electrical Test Tool application - Device Test menu, select SUSPEND from the Device Command dropdown menu. Click EXECUTE once to place the device into suspend.

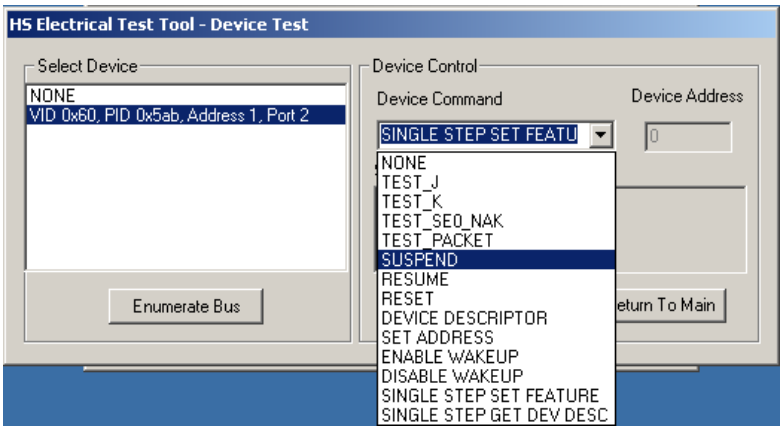


Figure 25: Device Suspend

3. On the HS Electrical Test Tool application - Device Test menu, select RESET from the Device Command dropdown menu. Click EXECUTE once to reset the device in suspend. The captured reset from suspend transition should appear as in the following figure.

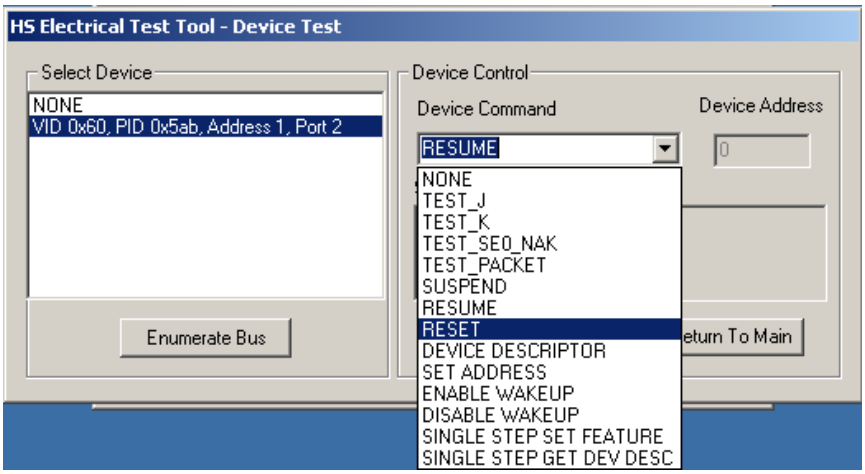


Figure 26: Device Reset

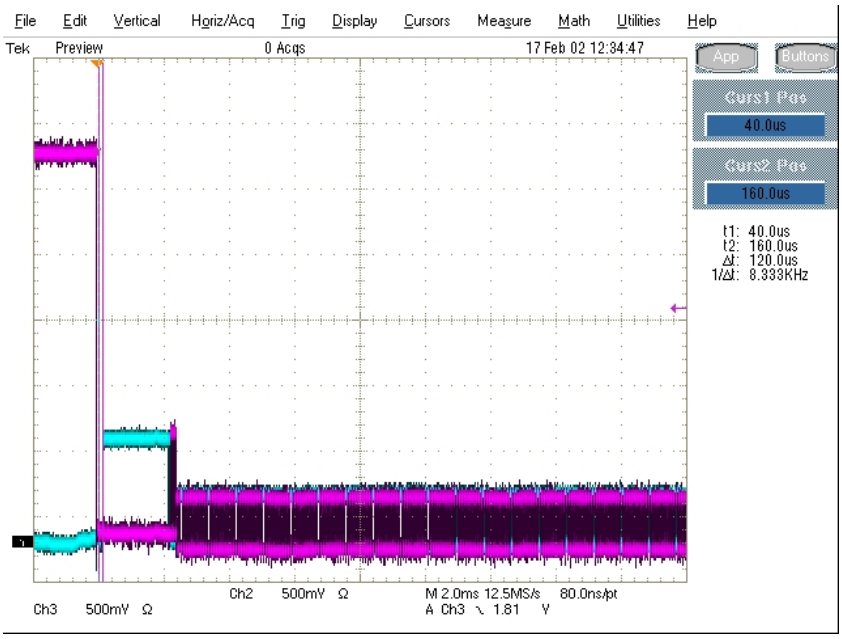


Figure 27: Device Reset from Suspend

4. The device responds to the reset with the Chirp-K. The results contain the time between the falling edge of the D+ and the start of the device chirp-K. It should be between 2.5 µs and 6.0 ms. This is EL_28.

## 4.8 Device Test J/K, SE0_NAK (EL_8, EL_9)

1. Attach the USB cable to the power connector of the Device High-speed Signal Quality section of the test fixture.
2. Verify that the red Power LED is lit, and the red Test LED is off.
3. Connect the Test port of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Click Enumerate Bus to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
4. On the HS Electrical Test Tool application - Device Test menu, select TEST_J from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_J test mode.

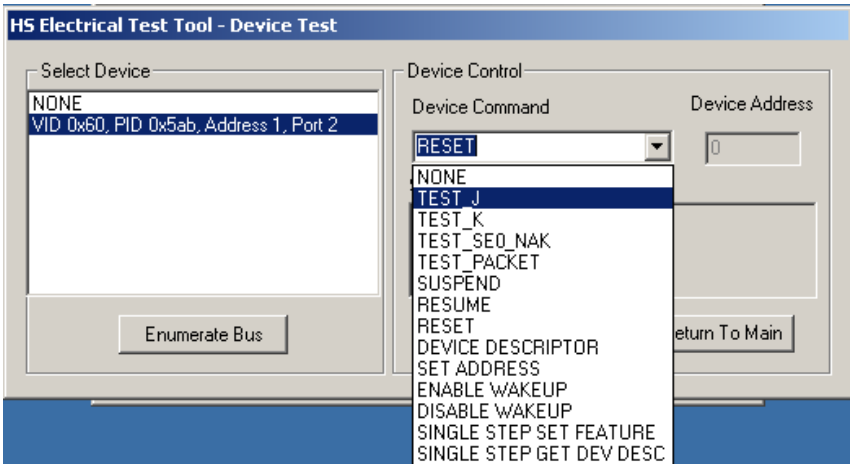


Figure 28: Device TEST_J

5. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
6. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.
7. Return the Test switch to the NORMAL position. Cycle the device power. Click Enumerate Bus once to force enumerate the device. This restores the device to normal operation.
8. On the HS Electrical Test Tool application - Device Test menu, select TEST_K from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_K test mode.
9. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
10. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.
11. Return the Test switch to the NORMAL position. Cycle the device power. Click Enumerate Bus once to force enumeration of the device. This restores the device to normal operation.

12. On the HS Electrical Test Tool application - Device Test menu, select TEST_SE0_NAK from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_SE0_NAK test mode.
13. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.
14. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9. Return the Test switch to the NORMAL position.
15. Remove the Device High Speed Signal Quality test fixture. Cycle the device power to prepare it for subsequent tests.

## 4.9 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

This section tests the sensitivity of the receivers on a device under test. A Tektronix DTG 5000 series instrument with DTGM21, AWG700 series, or DG2040 Data Generator emulates the In command from the hub port to device address 1.

1. Attach the USB cable to the designated power supply port to the Device Receiver test fixture J35 and verify that the red Power LED is lit. Leave the TEST switch at the INIT position. The red test LED should be off and the red INIT LED should be on.
2. Connect the Init port of the fixture to a port on the test bed computer. Connect the Test Port of the fixture to the device under test. Click the Enumerate Bus button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect the Tektronix signal generator to the Device REC test section of the fixture using the SMA cables. Two sets of SMA cables are required, each with a 5x attenuators inserted. Connect CH 1 to SMA1, and CH 0 to SMA2, J27 and J24. The DG2040 and the AWG700 series can be equipped with 5x attenuators for higher resolution of the amplitude adjustments.
4. Connect the differential probe to the test fixture at J25. From the TDSUSB application, select Measurement> Select. Click on the High Speed tab and click Receiver Sensitivity.
5. On the signal generator, select the MIN-ADD1.PDA setup file. This generates IN packets (of compliant amplitude) with a 12-bit SYNC field. Refer to the Load File function in signal generators manual if these signals are not already on it.
6. Start the data generator output with the START/STOP button.

7. On the HS Electrical Test Tool application - Device Test menu, select TEST_SE0_NAK from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_SE0_NAK test mode.

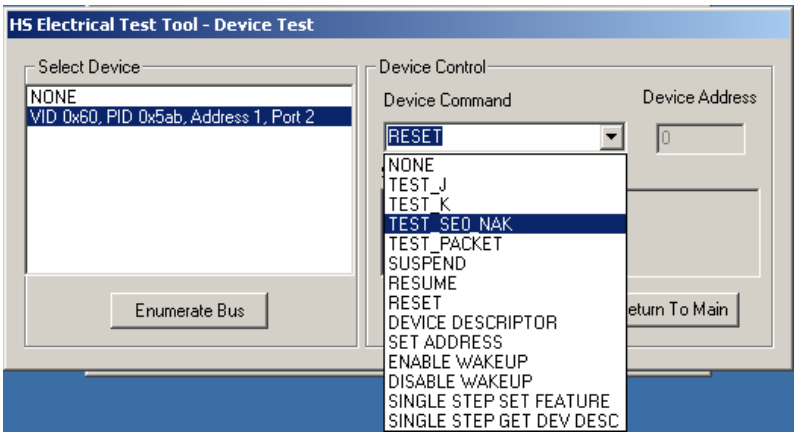


Figure 29: Device TEST_SE0_NAK

8. Place the test fixture Test Switch S6 into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the IN packets from the host controller.
9. Verify that all packets from the data generator are NAK'd by the port under test as in the following figure. Record the Pass/Fail in EL_18.

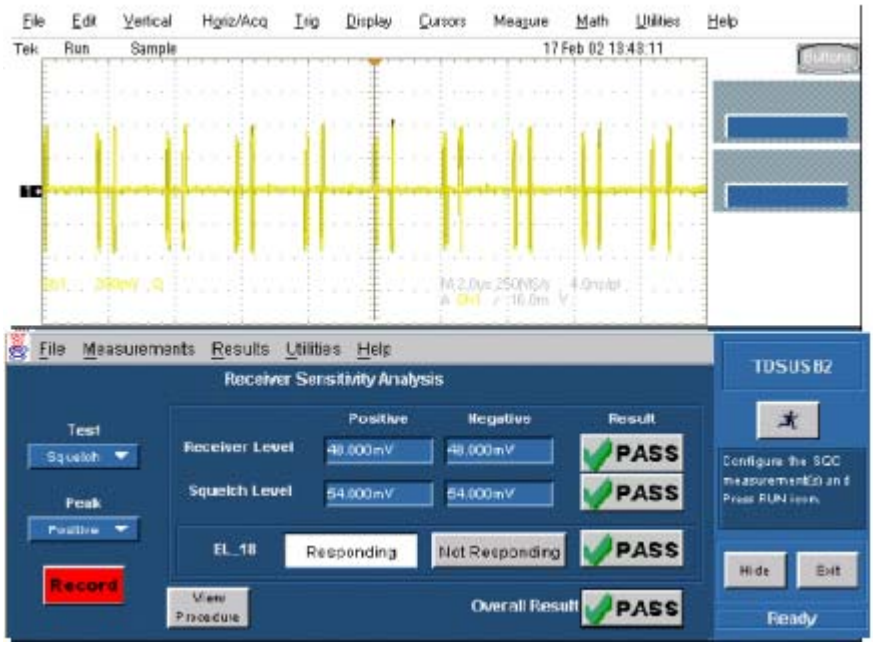


Figure 30: Receiver Respond with NAK to IN from Data Generator

10. On the data generator, load and run IN-ADD1.PDA setup file. Refer to the Load File function in signal generator's manual if these signals are not already on it.
11. Verify that all packets are NAK'd while signaling is at this amplitude.

12. Adjustment of the output level is best done with the keypad in 50 mV while monitoring the actual level on the oscilloscope. Refer to the manual of your signal generator to adjust the output level of each channel.
13. Reduce the amplitude of the data generator packets in 50 mV steps (on the generator before the attenuator) while monitoring the NAK response from the device on the oscilloscope. The adjustment should be made to both channels such that Channel 0 and Channel 1 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begins to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.
14. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Press the record button on the TDSUSB application corresponding to the receiver sensitivity level and record the measurement in EL_17 of appendix A.

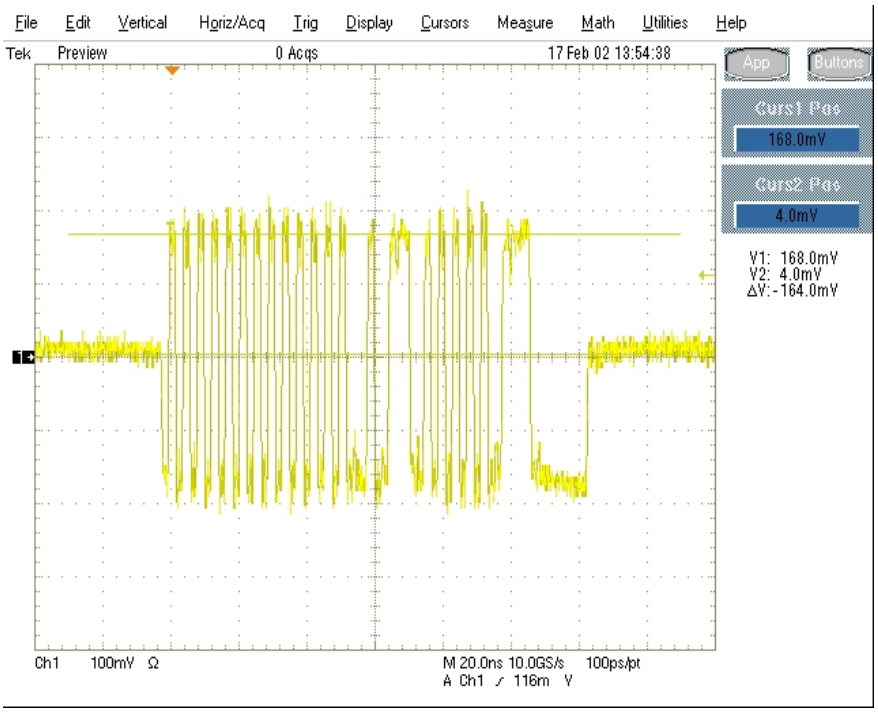


Figure 31: Measuring Differential Voltage Level – Zero to Positive Peak

15. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_17. As long as the receiver continues to NAK the data generator packet above +/- 150 mV, the device is considered to have passed the test. Record PASS/FAIL in EL_17.

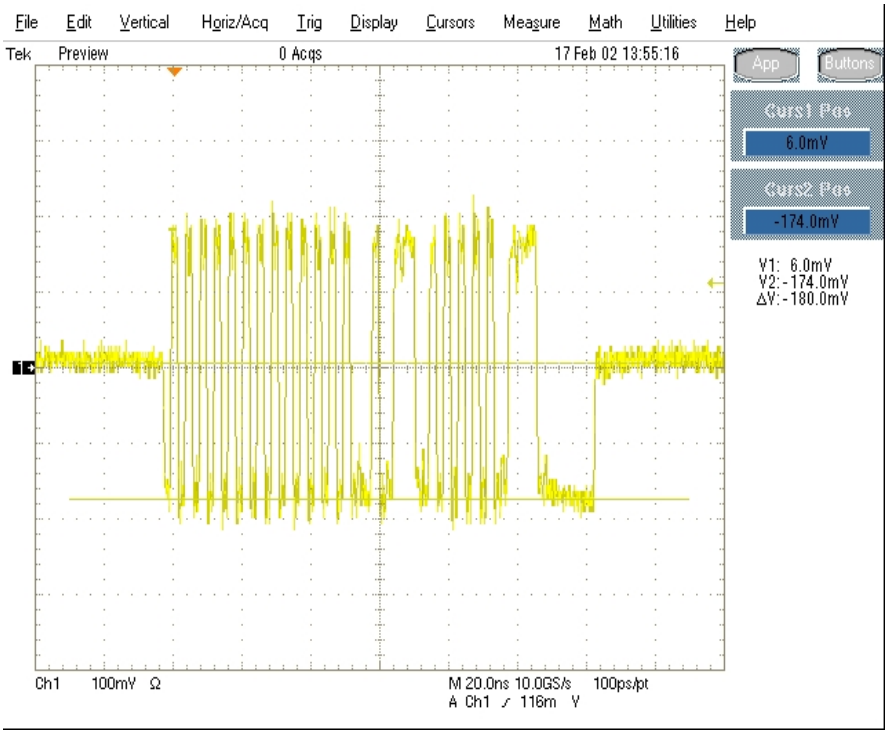


Figure 32: Measuring Differential Voltage Level – Zero to Negative Peak

16. Now further reduce the amplitude of the packet from the data generator in small steps, still maintaining the balance between Channel 0 and Channel 1 until the receiver just cease to respond with NAK. This is the squelch level of the receiver.

17. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The measurement is best made by turning on the Fit To Screen function in the Horizontal menu of the oscilloscope to maintain sufficient sampling rate. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16.

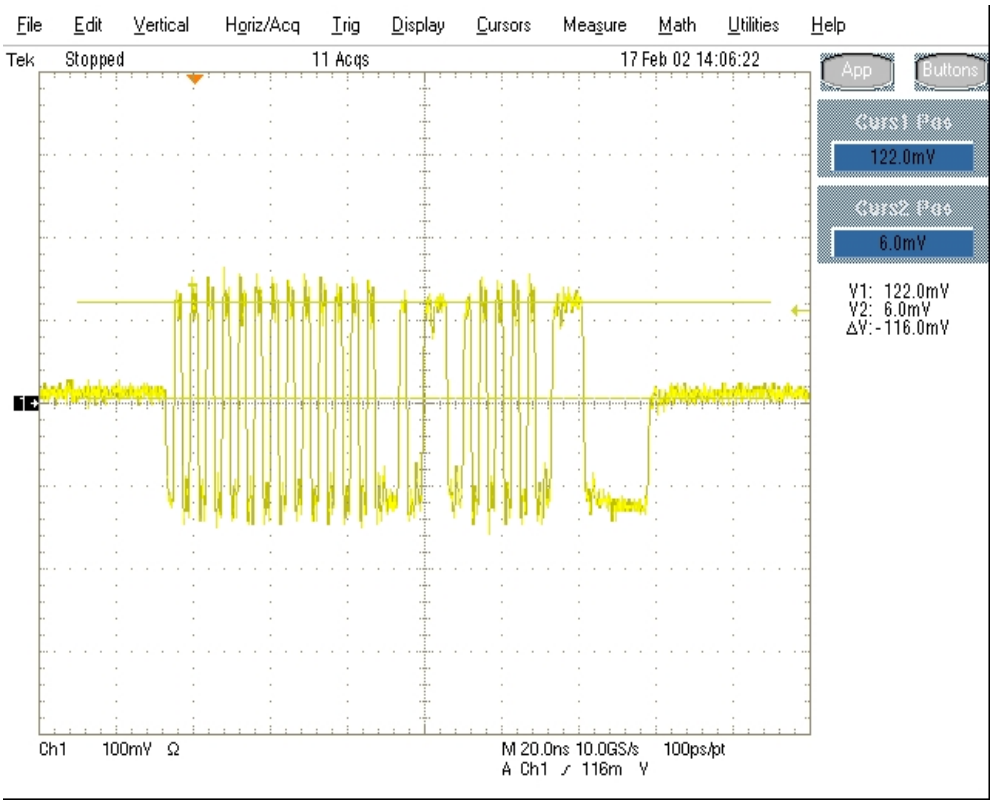


Figure 33: Measuring Differential Voltage Level – Zero to Positive Peak

18. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16. As long as the receiver ceases to NAK the data generator packet below +/- 100 mV it is considered to have passed the test. Record PASS/FAIL in EL_16.

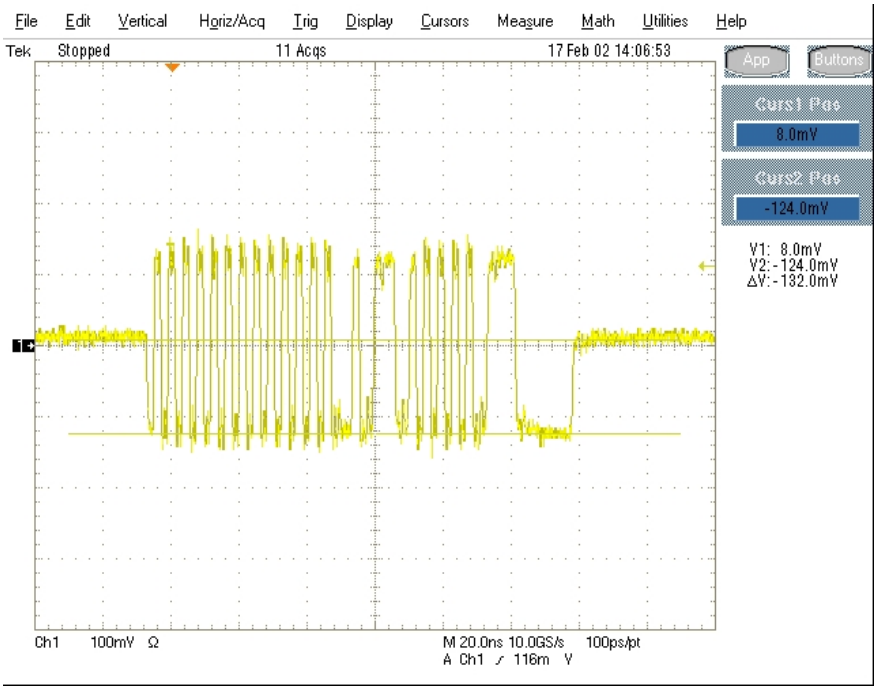


Figure 34: Measuring Differential Voltage Level – Zero to Negative Peak

**Note:** With certain devices, making an accurate zero-to-peak measurement of the In packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the In packet at the test fixture could be considerably higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

# Appendix A

# A.1 Device High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

## A.1.1 Vendor and Product Information

| | Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information |
|---|---|
| Test Date | |
| Vendor Name | |
| Vendor Complete Address | |
| Vendor Phone Number | |
| Vendor Contact, Title | |
| Test ID Number | |
| Product Name | |
| Product Model and Revision | |
| USB Silicon Vendor Name | |
| USB Silicon Model | |
| USB Silicon Part Marking | |
| USB Silicon Stepping | |
| Tested By | |

## A.1.2 Legacy USB Compliance Tests

**Legacy USB Compliance Checklist**

| Legacy Test | Pass/Fail | Comments |
|---|---|---|
| FS SQ | | |
| Inrush | | |
| Interop | | |

P = PASS

F = FAIL

N/A = Not applicable

## A.1.3 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 MBps ± 0.05%.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.11.

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

**Reference documents:** *USB 2.0 Specification, Section 7.1.2.2.*

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

❑ Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

❑ Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

❑ Comments:

## A.1.4 Device Packet Parameters (EL_21, EL_22, EL_25)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

**Reference documents:** *USB 2.0 Specification*, Section 8.2.

**Data Packet SYNC field**

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

**Reference documents:** *USB 2.0 Specification, Section 7.1.18.2.*

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing.

**Reference documents:** *USB 2.0 Specification, Section 7.1.13.2*

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

## A.1.5 Device CHIRP Timing (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.5 µs and no later than 3 ms when being reset from suspend or a full-speed state.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.5.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_29 The chirp handshake generated by a device must be at least 1 ms and not more than 7 ms in duration.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.5.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5 K pull-up resistor and enable its high-speed terminations within 500 µs.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.5.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

## A.1.6 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125 µs after there is a 3 ms idle period on the bus.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.6.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_39 A device must support the Suspend state.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.6.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

**Note:** It is not feasible to measure the device transition back to high-speed operation within two-bit time from the end of the resume signaling. The presence of SOF at nominal 400 mV amplitude following the resume signaling is sufficient for this test.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.7.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_27 Devices must transmit a chirp handshake no sooner than 3.1 ms and no later than 6 ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.5.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_28 Devices must transmit a chirp handshake no sooner than 2.5 µs and no later than 3 ms when being reset from suspend or a full-speed state.

**Reference documents:** *USB 2.0 Specification, Section 7.1.7.5.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

## A.1.7 Device Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

**Reference documents:** *USB 2.0 Specification, Section 7.1.1.3.*

| Test | D+ Voltage (mV) | D- Voltage (mV) |
|---|---|---|
| J | | |
| K | | |

- ❑ Pass
- ❑ Fail
- ❑ N/A

| ❑ Comments: |
|---|

EL_9 When either D+ and D- are not being driven, the output voltage must be 0 V ±10 mV when terminated with precision 45 Ω resistors to ground.

**Reference documents:** *USB 2.0 Specification, Section 7.1.1.3.*

| | Voltage (mV) |
|---|---|
| D+ | |
| D- | |

- ❑ Pass
- ❑ Fail
- ❑ N/A

| |
|---|
| ❑ Comments: |

## A.1.8 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

**Reference documents:** *USB 2.0 Specification, Section 7.1.*

- ❑ Pass
- ❑ Fail
- ❑ N/A

| |
|---|
| ❑ Comments: |

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

**Note:** A waiver may be granted if the receiver does not indicate Squelch at +/-50 mV of 150 mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

**Reference documents:** *USB 2.0 Specification, Section 7.1.*

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments:

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100 mV differential amplitude.

**Note:** A waiver may be granted if the receiver indicates Squelch at ± 50 mV of 100 mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

**Reference documents:** *USB 2.0 Specification, Section 7.1.*

- ❑ Pass
- ❑ Fail
- ❑ N/A
- ❑ Comments: