C-Band Polarimetry using a full digital correlator

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Abstract- **In the context of the Galactic Emission Mapping collaboration, a new receiver at 5GHz is being developed to characterize the galactic foreground to the Cosmic Microwave Background Radiation.. This is a 5GHz heterodyne polarimeter with a high gain IF chain using the latest RF technology working at 600MHz central frequency that feeds a four channel digital correlator. This paper describes the preamplifier/band-pass filter, the digitally controlled amplifier, the frequency converter to zero-IF and a briefly description of the digital correlator. Design options and constraints are presented with some simulations and experimental results of a circuit prototype.**

INTRODUCTION

The Cosmic Microwave Background Radiation (CMBR), with its small temperature fluctuations (50~80 µK) [6] and its small polarization variations (1~10 µK) [7] is the best cosmological probe of the early Universe, allowing a reconstitution of the cosmic history with great precision. However, CMBR is partially obscured by radiation emitted by our galaxy, the Milky Way, and we need detailed maps of the galactic foreground emissions to properly extract the information from CMBR observations. The GEM (Galactic Emission Mapping) collaboration [3, 4, 5] aims at mapping the sky with high sensitivity and absolute calibration at low frequencies both in Brazil and Portugal. For the Northern Sky Hemisphere, a GEM team will proceed towards a survey of the polarized galactic emission at 5GHz with a 9 meter parabolic antenna installed in central Portugal. Although the radiation from the galaxy is considerably stronger than the CMBR at 5GHz, this project still requires a high sensitivity radiometer/polarimeter, with an equivalent noise temperature around 10K. For this purpose a heterodyne radiometer/polarimeter is being developed, using cryogenically cooled PHEMT preamplifiers and 600MHz IF (intermediate frequency) followed by an all-digital correlator built using an FPGA (field programmable gate array).

The present article details the IF section of the receiver and a little information about the digital correlator. The cryogenically cooled front-ends will be published elsewhere.

RECEIVER OVERVIEW

The receiver has a general classical heterodyne topology, the back-end being fully implemented in the digital domain (Figure 1). In radiometry the bandwidth should be as large as possible to permit the best instrument resolution. This is however limited by the available bandwidth free of interference and preferably under protection of the international frequency allocations for the RA (radio-astronomy) service. In our case we want a minimum bandwidth of 200MHz around 5GHz. However, the center frequency had to be changed to 4.9GHz (using the same 200MHz bandwidth) in order to be aligned with the band segment allocated to RA for which we can apply for protection to the Portuguese radio spectrum administration (ANACOM). The radiometer/polarimeter receiver is a double conversion super-heterodyne receiver with zero-IF. The front-end will use cryogenically cooled PHEMT preamplifiers followed by image rejection filter and diode mixers along with a local oscillator. All this equipment will be located at the back end of the antenna feed inside a temperature shield. The IF chain is composed of a preamplifier-filter and a large gain IF amplifier followed by a converter to zero-IF that provides the base-band signals for the correlator. The Base-band signals are digitized and fed to an FPGA where the actual correlation process happens, all done entirely in the digital domain. Signal digitization is performed at 200Ms/s (Mega Samples per Second) with 8 bits of resolution. For this application the required resolution at the ADC is quite low, since the number of samples that are integrated while acquiring a pixel is extremely high (8ns per sample over a few ms of temporal resolution results in a 1:100000 ratio where amplitude and phase resolution came essentially from the integrated signal statistics rather than ADC resolution). Therefore the market availability of 8 bit ADCs dictated this choice. The correlated samples from which the Stokes Parameters (I, Q, V and U) are calculated will determine the polarization gathered by the antenna. These parameters are integrated in the FPGA and the results sent to a PC. To avoid mechanical moving parts a small form factor industrial PC104 is used.

The expected overall system temperature is about 10K corresponding to a total power (over 200MHz of bandwidth) of about -105.6dBm therefore the receiver would need a total gain of about 104dB on the RF and IF altogether to provide the necessary signal level for digitalization. The gain budget

analysis for the system is shown on Table I, corresponding to the block diagram shown on Figure 1.

Antenna	LNA	Passive Filter	Mixer	IF Pre Amplifier	IF Amplifier	Converter	ADC
Input (dBm)	26	-4	-7	31	56	2	Output(dBm)
-105,6	-79,6	-83,6	-90,6	-59,6	-3,6	-1,6	-2

Table 1. Power budget for the complete radiometer / polarimeter.
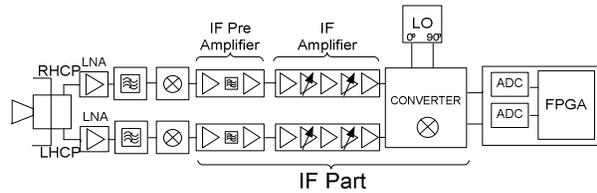
Fig. 1. Overall block diagram.

THE CIRCUIT DESIGN

IF Pre amplifier

The signals coming from the front-end block (located at the feed point) enter the IF unit of the receiver directly to the IF preamplifier and filter module. This module presents a gain of 31 dB with a moderately low noise figure. The design was targeted for gain and proper IF bandwidth shaping purposes but other considerations were taken into account, such as gain variation with temperature and frequency.

The gain stability required relates directly to the kind of data that is going to be extracted from the received signals. In order to observe sub-miliKelvin of antenna temperature, we need to ensure that gain variations would preferably be in a different time scale and smaller than the measured variations. The variation of gain with environmental temperature needs to be minimized at all cost. Therefore amplifiers with minimum gain variation with temperature were selected. Encapsulated MMIC (monolithic microwave integrated circuits) were attractive choices and their possible use was investigated. As shown in Figure 1 this module has two amplifier stages with a band-pass filter between them. The amplifiers used were ERA3 from Minicircuits due to their small temperature drift in the frequency band of interest (500MHz to 700MHz). The manufacturer claims a gain increase with temperature of 0.12 dB from -45 to 85ºC, which corresponds to 0.0009dB/ºC. The filter section is a Butterworth type with 200MHz bandwidth centered at 600MHz. It is implemented in a T configuration with lumped L and C elements. To allow calibration the filter uses trimmer capacitors and fixed inductors. The design of the filter as well all the other parts was computer aided, using the ADS (Advanced Design System) software [3]. A fine adjustment was made in the final design by trial end error, in order to achieve the desired bandwidth and response flatness with commercially available component values. Very wideband MMIC's do not exhibit a constant gain over frequency, higher frequencies presenting the lowest gain. In order to reduce this effect we inserted a slope compensation network, which is a simple RLC network, next to the filter that reduces the gain at lower frequencies by loading the circuit more heavily at lower frequencies. On the modeling we used ERA3

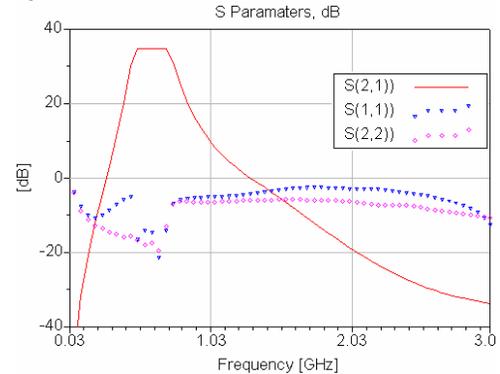and ERA2, both from Minicircuits, and the results are shown in Figure 2.

Fig. 2. IF preamplifier simulation on ADS2005.

The layout uses microstrip lines, and the frequencies involved suggested the usual RF PCB design techniques with 0805 or 0603 size SMD components. The PCB board is packaged in an aluminum milled box specially designed for this type of application to serve both as shielding and thermal mass. The tests were made using an HP 8753E Network Analyzer and results are in Figure 3.
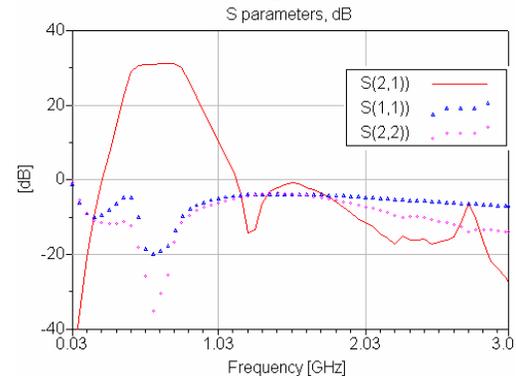

Fig. 3. IF preamplifier measurement results as measured on a HP8753E network analyzer.

IF Amplifier

This stage is the main IF amplifier and will provide most of the gain required. It is composed of five MMIC stages and two digitally controlled attenuators. Considering the values expressed in Table I we would require about 56dB of gain, however, by design, we should operate near the middle of gain control settings which is about 15dB below the maximum gain (for a total gain control of 30dB). In this way a total gain of 71dB would be necessary. Controlling the amount of signal at the input of the ADCs is easily accomplished by the MMIC digital RF attenuators DAT-15R5-PP Digital step attenuators from Minicircuits. Each of these has an attenuation of 15,5dB and is controlled by 5 bits with a 0,5dB step. The variation of gain with frequency and temperature was also taken into account, and in this case we would benefit from a very flat band from 100MHz to 1GHz allowing us to have a perfect flatness between 500MHz and 700MHz. The MMIC's chosen were one ERA3 (21dB) and four ERA2 (15,5dB). The expected decrease in gain of the MMIC amplifiers at higher frequencies was again corrected by inserting slope compensation networks, like we did for the IF preamplifier. This time we inserted two RLC networks for

the entire module. The attenuator was modeled using simple resistive circuits, which proved to be accurate enough for our needs. Simulation results can be seen in Figure 4, after obtaining S parameters for the ERA3 and ERA2 from the manufacturer.
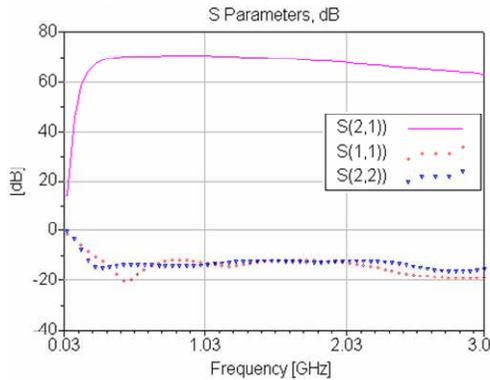

Fig. 4. IF amplifier simulation on ADS2005.

As for the IF preamplifier microstrip lines were used, and the frequencies involved suggested the usual RF PCB design techniques with 0805 or 0603 size SMD components. Packaging was also approximately the same. The test results, obtained with an HP 8753E Network Analyzer are shown on Figure 5.
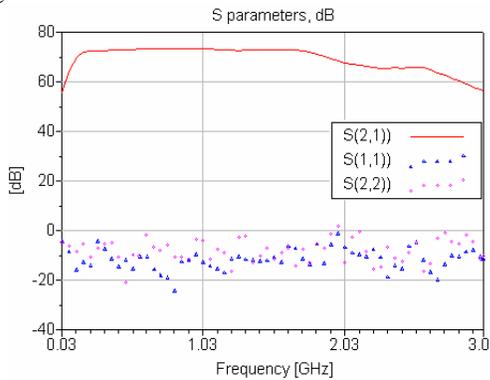

Fig. 5. IF preamplifier results measured on a HP8753E network analyzer.

Converter

The signal from each arm of the IF needs to be converted down to a band of frequencies that allows the signals to be processed in the digital domain. Since we need to preserve 200MHz bandwidth we have two options: i) converting down to 0 to 200MHz and acquire at 400Ms/s (or slightly higher , in order to account for filter roll off and aliasing issues); ii) converting to zero IF, e. g., to -100MHz to +100MHz acquiring at 200Ms/s (or slightly higher, for the same reasons as above) but in order to preserve the total 200MHz bandwidth a complex signal conversion is required with base-band I and Q signals produced for each arm of the receiver (RHCP – Right Hand Circular Polarization – and LHCP – Right Hand Circular Polarization). By using the second option, the complex conversion to a zero-IF we end up with 4 channels to be digitized but at half the sampling rate that would be required otherwise. This is extremely convenient in order to relax as much as possible the requirements for both the ADC and FPGA. The signals from the two arms of the radiometer are split into its phase (I) and quadrature (Q) components. The converter produces the I and Q outputs by multiplying the IF signal with two versions of the local oscillator with a phase difference of 90º. This operation will be applied to both RHCP and LHCP arms, so the implementation uses two identical circuits

The 600MHz IF signal is separated into two channels, using a power splitter ADE-2-9 from Minicircuits to feed a pair of ADEX-10 mixers. The local oscillator (LO) already outputs the correct driving level for the mixers, 7dBm, and the correct phase relation, 0 and 90º of phase difference. The I and Q signals obtained will be low pass filtered to eliminate unwanted frequencies, then amplified and finally low-pass filtered prior to digitization. A diagram of the converter is shown on Figure 6.
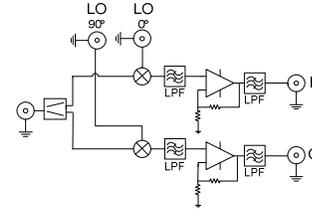

Fig. 6. Zero-IF converter block diagram

The filters that follow the mixers are 7th order Butterwoth low-pass filter with 100MHz cut-off frequency. The output filters are 3rd order Butterworth low-pass with 120MHz cut-off frequency. This last filtering prior to the digital acquisition of signals will eliminate any wideband noise and spurious signals that might be presented at this point ensuring that only the signals of interest are presented to the ADCs. Both filters were implemented using lumped L and C elements. The amplifier uses the OPA657, an OPAMP (operational amplifier from Burr-Brown) in a non-inverting configuration. The layout follows the usual techniques for RF instrumentation using both PCB layout and external metallic shielding. Further care was necessary to externally ensure phase balance both in the RF and LO signal path, in order to guarantee perfect orthogonal output signals in all circumstances. Fine phase trimming was provided with a variable capacitor to allow a precise calibration. The circuit employs microstrip layout design and is constructed on a FR4 epoxy substrate. For the tests we used an RF signal of 600 to 700MHz with -7dBm and an LO signal at 600MHz with 7dBm. The output signal, varying from DC to 100MHz was measured with a spectrum analyzer and presented in Figure 7.
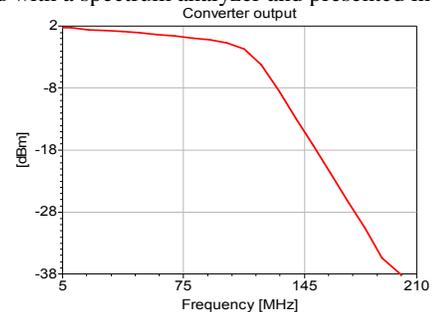

Fig. 7. Converter results as measured on a HP8563A spectrum analyzer.

Local Oscillator

This circuit provides the LO signal to the converter. Since we want to do a zero-IF conversion, the required oscillator frequency is 600MHz, the exact central frequency of the IF

pass-band. We decided to use the encapsulated oscillator ROS615 from Minicircuits which is a VCO (voltage controlled oscillator) that tunes from 580 to 615 MHz. It is operated at the fixed frequency of 600.0MHz. We have both the possibility to tune the frequency using a potentiometer, varying the voltage from 0V to 5V or we may use a PLL synthesizer chip LMX2326 from National Semiconductors. As for the moment no frequency stability better than 1MHz is required, so the LO operates with analog frequency control.

The oscillator signal needs to be split into four equal signals. For simplicity we accomplished this with simple resistive dividers in T attenuator configurations allowing for normalization of the gain and attenuation required, thus providing four identical signals close to 7dBm. Since the signal from the VCO was considerably low (about 0dBm) we needed to amplify it before we split the signal. In order to have isolation between the output ports of this unit it is desirable to have one amplifier per output. Taking these requirements into account we arrive to the design presented on the diagram of Figure 8.

We used an ERA1 (from Minicircuits) MMIC amplifier to raise the power of the VCO to about 10dBm. The resistive divider then lowers each output power to about -4dBm. For this reason another ERA1 amplifier is needed to raise output power again to 7dBm, the power required to drive the converter block.
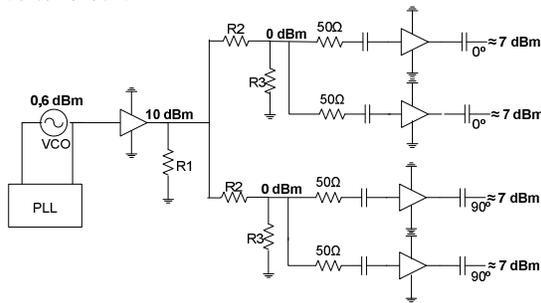

Fig. 8. Local oscillator module block diagram.

The same layout considerations and RF common practices apply for the local oscillator module. This block was also implemented on FR4 substrate using microstrip design and SMD components.

Digital correlator

This circuit is composed by four ADCs and one Altera Cyclone II FPGA. The chosen ADCs accept a 0,5 V peak-to-peak signal and the amplitude signals stay between half of the range and the maximum allowed of the ADCs input signal through the help of digital control attenuators. Since their best performance occurs for differential signals, a differential amplifier was inserted to transform the single ended signal in a differential one. The digital signals have already been interleaved, internally to the ADCs, so each ADC will present two times eight bits data outputs at each cycle corresponding to sample *n-1* and sample *n*. allowing a slower clock but more massive parallelization. The speed of the FPGA is then half of the sample rate that is 100MHz while the ADCs run at 200MHz.

The polarization of the radiation gathered by the radiometer is best described calculating its Stokes parameters.

$$\text{Stokes U} \rightarrow RL = \Re e\left(E_{rcp}E_{lcp}^*\right) \tag{1}$$

$$\text{Stokes Q} \rightarrow LR = \Re e\left(E_{rcp,-\frac{\pi}{2}}E_{lcp}^*\right) \tag{2}$$

$$\text{Stokes I} \rightarrow RR + LL = \left\langle E_{rcp}E_{rcp}^*\right\rangle + \left\langle E_{lcp}E_{lcp}^*\right\rangle \tag{3}$$

To obtain these parameters the digital data (samples) from ADC are correlated and integrated, in parallel, inside the FPGA. After processing and integrating several samples the data rate is slow enough to be transferred to a computer. This computer, a PC104 module (AMD LX800 500MHz from Kontron), interfaces the FPGA is by the ISA bus. This PC is responsible to format the data store it locally and make it available on the network via Ethernet IP using SFTP (secure file transfer protocol).

All the configuration of the FPGA is being developed using VHDL language on Quartus II v6.1 web edition software.

The four layer PCB layout of FPGA obeys no specific standard form. High speed digital design considerations were applied during this design.

CONCLUSIONS

To accomplish the polarimetric measurements at 5GHz for the Galactic Emission Mapping in the North Hemisphere we develop a novel instrument with all polarimetric measurements being performed in the digital domain. In order to achieve this objective, a heterodyne radiometer/polarimeter is being developed and a new intermediate frequency chain with high performance had to be designed along with a new digital correlator implemented in an FPGA developed in VHDL language. The entire IF system and the digital correlator was implemented using standard SMD components and classical approaches to high frequencies and microstrip design, but using commercial RF MMIC devices. Therefore, a high performance IF strip attended by a digital correlator, suitable for a radio-astronomy application, and in particular for the GEM (at Portugal) experiment, was designed, constructed and tested successfully.

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